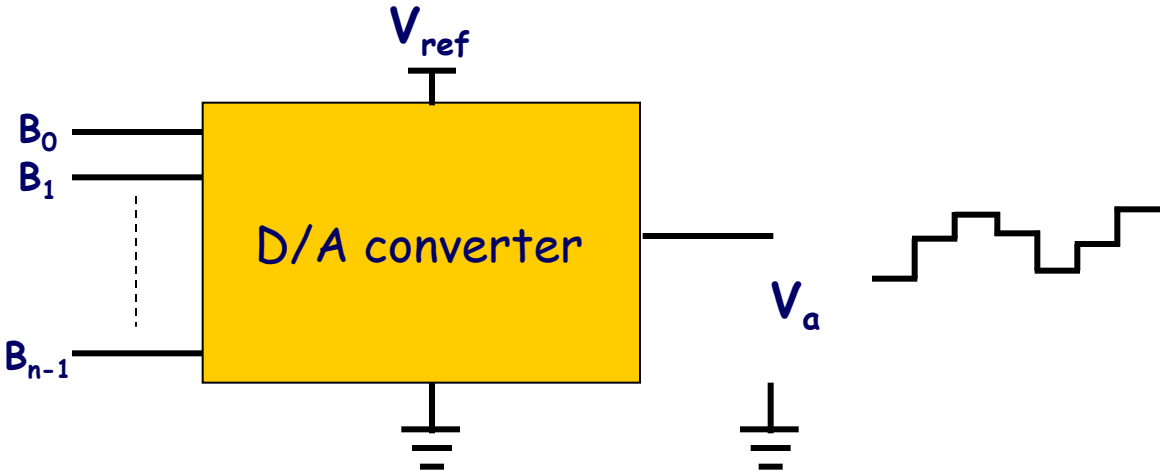
UNIVERSITÀ DEGLI STUDI DI PAVIA

Dept. of Electrical, Computer and Biomedical Engineering

Programming a binary weighted resistor digital to analog converter

Digital to analog converter

- A digital to analog converter (DAC) converts an n-bit digital word into an analog voltage



- Generally, the analog level at the DAC output is sent to a sample and hold circuit

- The staircase-like waveform is then fed to a low pass filter, completing the reconstruction of the analog signal

Digital to analog converter

- The output voltage at the DAC output, V_a, is obtained by assigning to each bit of the input digital word a suitable weight, depending on the bit position in the word

$$V_a = V_{ref} \cdot \left(\frac{B_{n-1}}{2^1} + \frac{B_{n-2}}{2^2} + \ldots + \frac{B_0}{2^n} \right) =$$

$$= \frac{V_{ref}}{2^n} \cdot \left(B_{n-1} 2^{n-1} + B_{n-2} 2^{n-2} + \ldots + B_0 2^0 \right), \quad B_i = 0,1$$

- The maximum value for V_a, $V_{a,max}$, is not V_{ref} but

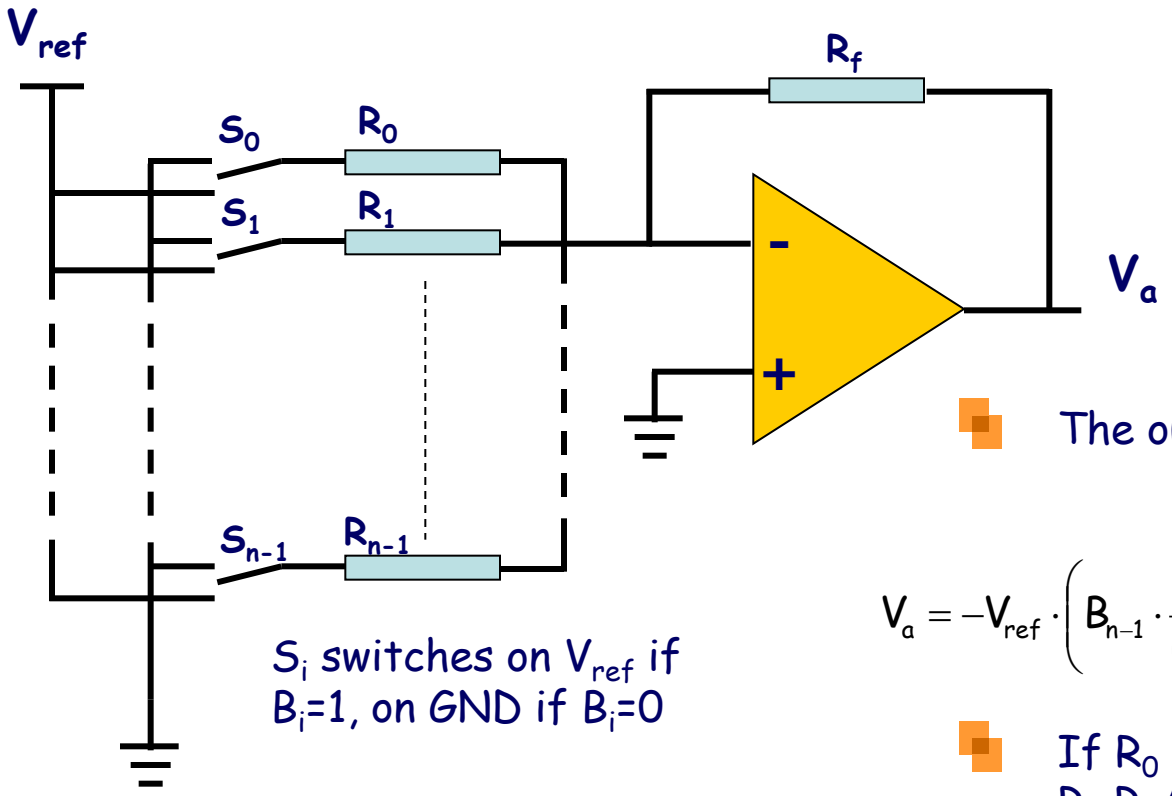
$$V_{a,max} = \frac{V_{ref}}{2^n} \cdot \left(2^{n-1} + 2^{n-2} + \ldots + 2^0 \right) = V_{ref} \frac{2^n - 1}{2^n} = V_{ref} - \frac{V_{ref}}{2^n}$$

where $V_{ref}/2^n$ is the analog value corresponding to the least significant bit (LSB)

Purpose of the experiment

- Implementing a system allowing the user to
  - program an 8-bit DAC through 8 of the 24 digital ports available on the SC2075 platform
  - compute the expected theoretical value of the voltage at the DAC output based on the digital word set at the input
  - acquire the analog voltage at the converter output
- The system should include
  - a binary weighted resistor DAC, assembled on the breadboard
  - a virtual instrument implemented in the LabView programming environment serving as an interface between the acquisition system and the user

Binary weighted resistor DAC



S_i switches on V_{ref} if B_i=1, on GND if B_i=0

- The output sample is given by

$$V_a = -V_{ref} \cdot \left(B_{n-1} \cdot \frac{R_f}{R_{n-1}} + B_{n-2} \cdot \frac{R_f}{R_{n-2}} + \ldots + B_0 \cdot \frac{R_f}{R_0} \right), \quad B_i = 0,1$$

- If R_0 is the LSB resistance and $R_i = R_0/2^i$, one gets

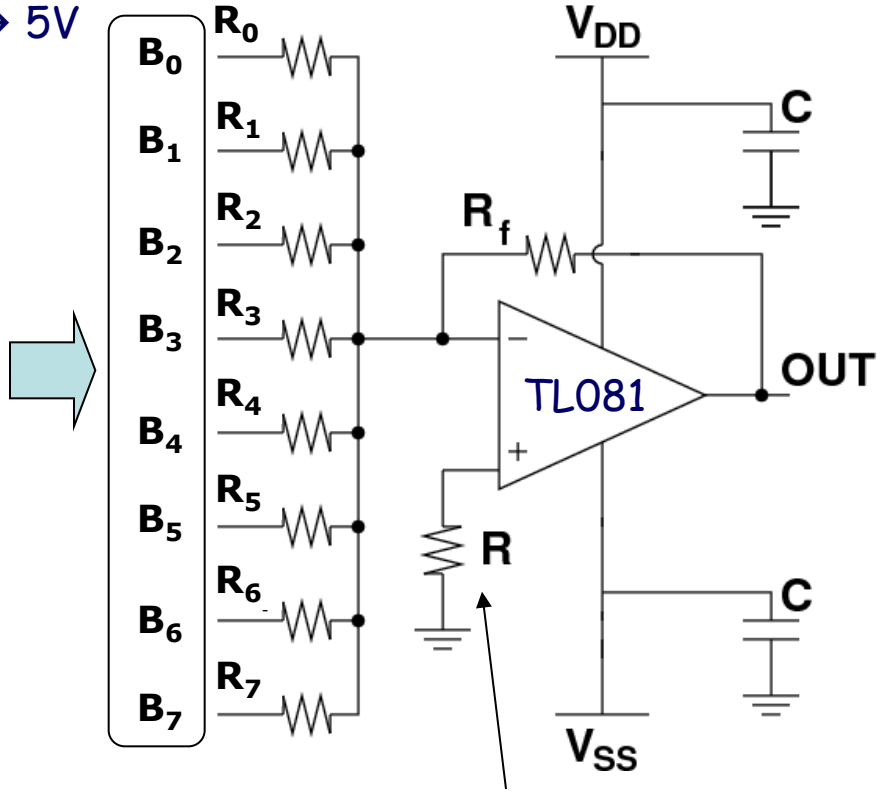
$$V_a = -\frac{R_F}{R_0} \cdot V_{ref} \cdot \left(B_{n-1} \cdot 2^{n-1} + B_{n-2} \cdot 2^{n-2} + \ldots + B_0 \cdot 2^0 \right), \quad V_{a,max} = -\frac{R_F}{R_0} \cdot V_{ref} (2^n - 1)$$

Binary weighted resistor DAC

B_i=0 → 0V

B_i=1 → 5V

from the digital ports of the SC2075 platform



compensating resistance for the op amp input bias currents

R_0 = 511kΩ
R_1 = 243kΩ
R_2 = 130kΩ
R_3 =61.9kΩ
R_4 =33.2kΩ
R_5 =16.2kΩ
R_6 = 8.2 kΩ
R_7 =3.92kΩ
R_f=2 kΩ
R=2 kΩ
C=100 nF
V_{DD}=15 V
V_{SS}=-15 V

TL081 JFET input OpAmp

National Semiconductor

December 1995

TL081 Wide Bandwidth JFET Input Operational Amplifier

General Description

The TL081 is a low cost high speed JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The TL081 is pin compatible with the standard LM741 and uses the same offset voltage adjustment circuitry. This feature allows designers to immediately upgrade the overall performance of existing LM741 designs.

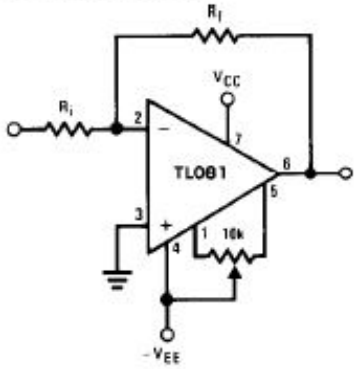
The TL081 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices has low noise and offset voltage drift, but for applications where these requirements are critical, the LF356 is recommended. If maximum supply current is important, however, the TL081C is the better choice.

Features

■ Internally trimmed offset voltage	15 mV
■ Low input bias current	50 pA
■ Low input noise voltage	25 nV/$\sqrt{Hz}$
■ Low input noise current	0.01 pA/$\sqrt{Hz}$
■ Wide gain bandwidth	4 MHz
■ High slew rate	13 V/μs
■ Low supply current	1.8 mA
■ High input impedance	$10^{12}\Omega$
■ Low total harmonic distortion A_V = 10, R_L = 10k, V_O = 20 Vp-p, BW = 20 Hz–20 kHz	<0.02%
■ Low 1/f noise corner	50 Hz
■ Fast settling time to 0.01%	2 μs

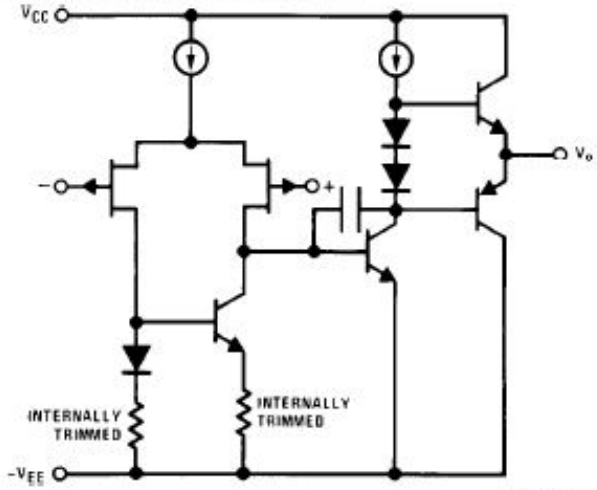
TL081 JFET input OpAmp

Typical Connection



TL/H/8358–1

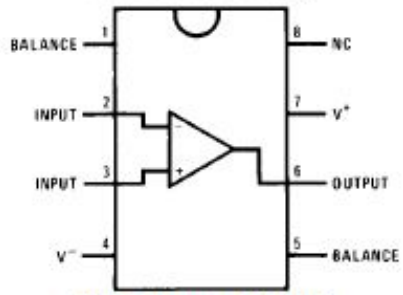
Simplified Schematic



TL/H/8358–2

Connection Diagram

Dual-In-Line Package



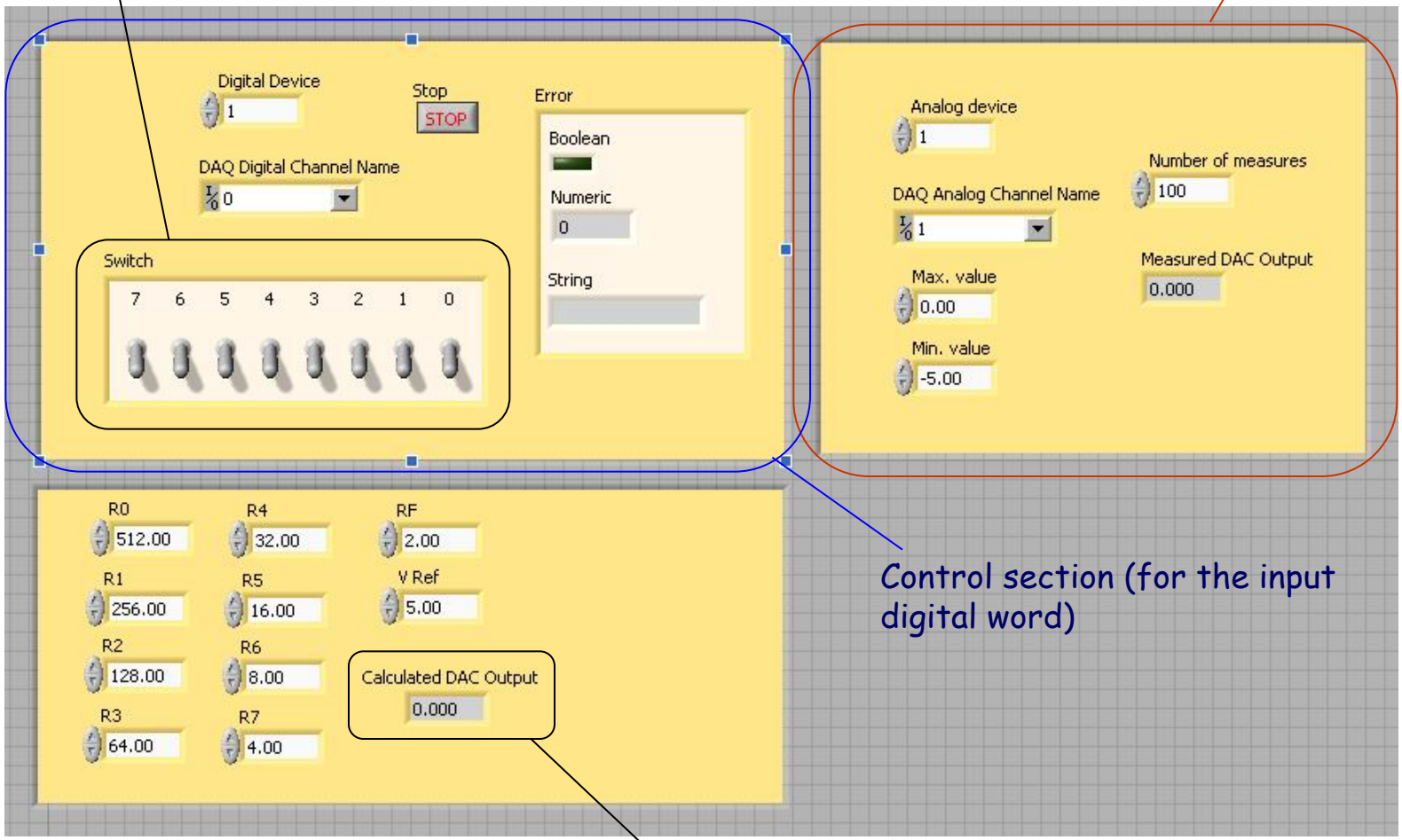
TL/H/8358–4

Order Number TL081CP
See NS Package Number N08E

Front panel

Control to set the input digital word (cluster of Boolean controls)

Acquisition section (for the DAC analog output)

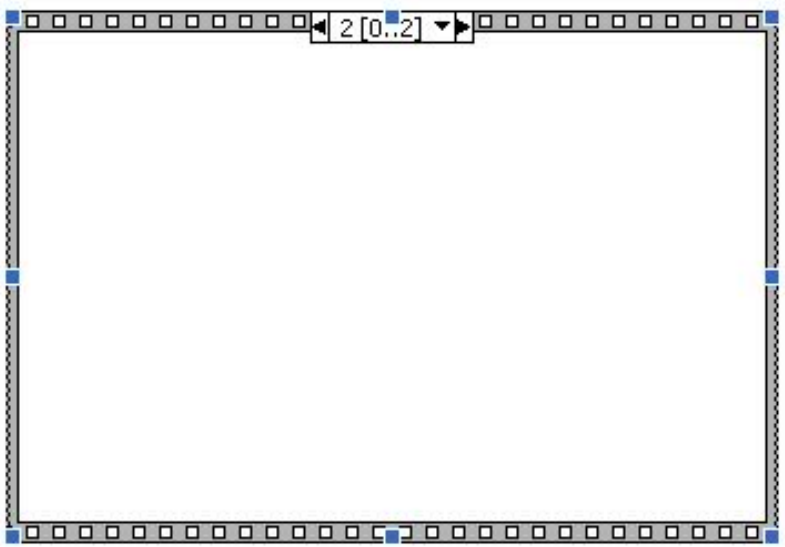


Control section (for the input digital word)

Theoretical value of V_a

Sequence structure

As far as the block diagram is concerned, the LabVIEW VI can be implemented by means of a sequence structure including 3 frames (to add a frame, right click on the frame of the structure and select "Add Frame After"). The sequence structure makes it possible to execute a set of instructions according to a user defined time sequence (first the instructions included in frame 0 are executed, then those included in frame 1, etc.)



The only purpose of using this structure is that of introducing a clear time separation between the three tasks of the program:

- **DAC programming** (frame #0)
- **calculation of the theoretical value of the analog voltage at the DAC output** (frame #1)
- **acquisition of the real voltage sample at the DAC output** (frame #2)

DAC programming (frame #0)

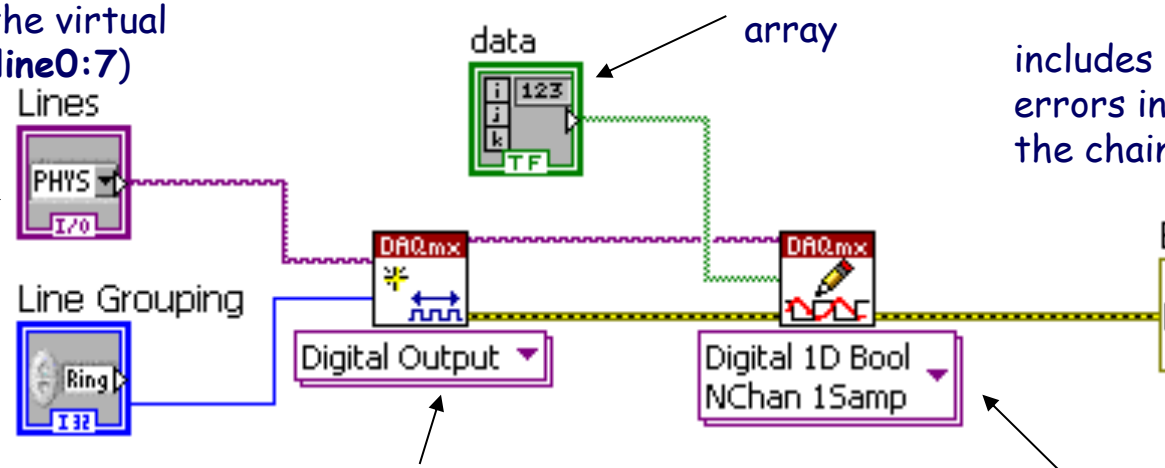
- DAQmx Create Channel.vi is used to configure the digital channel of the data acquisition board (DAQ, on the PC)
- DAQmx Write.vi is used to set the value at the digital output channels configured by the previous function

specifies the name of the digital lines or the ID number of the ports used to create the virtual channel (**Dev1/port0/line0:7**)

Boolean control array

includes information on possible errors in one of the blocks in the chain

grouping of the digital lines in one or more virtual channels (**one channel for each line**)



`Measurement I/O -> DAQmx Data Acquisition -> DAQmx Create Channel.vi`

`Measurement I/O -> DAQmx Data Acquisition -> DAQmx Write.vi`

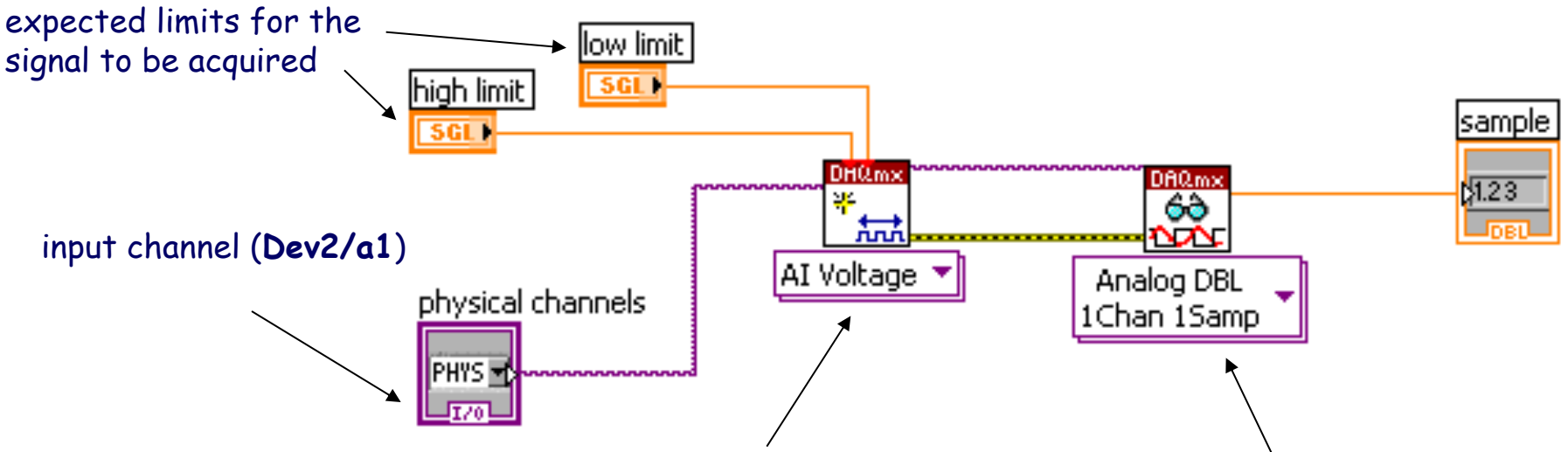
Calculation of the theoretical value of V_a (frame #1)

- Frame #1 of the sequence structure will include all the instructions needed to calculate the theoretical value of the DAC analog output based on the digital word set at the DAC input. To do this, use the relationship

$$V_a = -V_{ref} \cdot \left(B_7 \cdot \frac{R_f}{R_7} + B_6 \cdot \frac{R_f}{R_6} + \ldots + B_0 \cdot \frac{R_f}{R_0} \right), \; B_i = 0,1$$

Acquisition of the DAC output voltage (frame #2)

- DAQmx Create Channel.vi provides the acquisition board with information about the type and range of the signals to be acquired and about the input channel
- DAQmx Read.vi samples the signal from the specified channel and yield the measured value

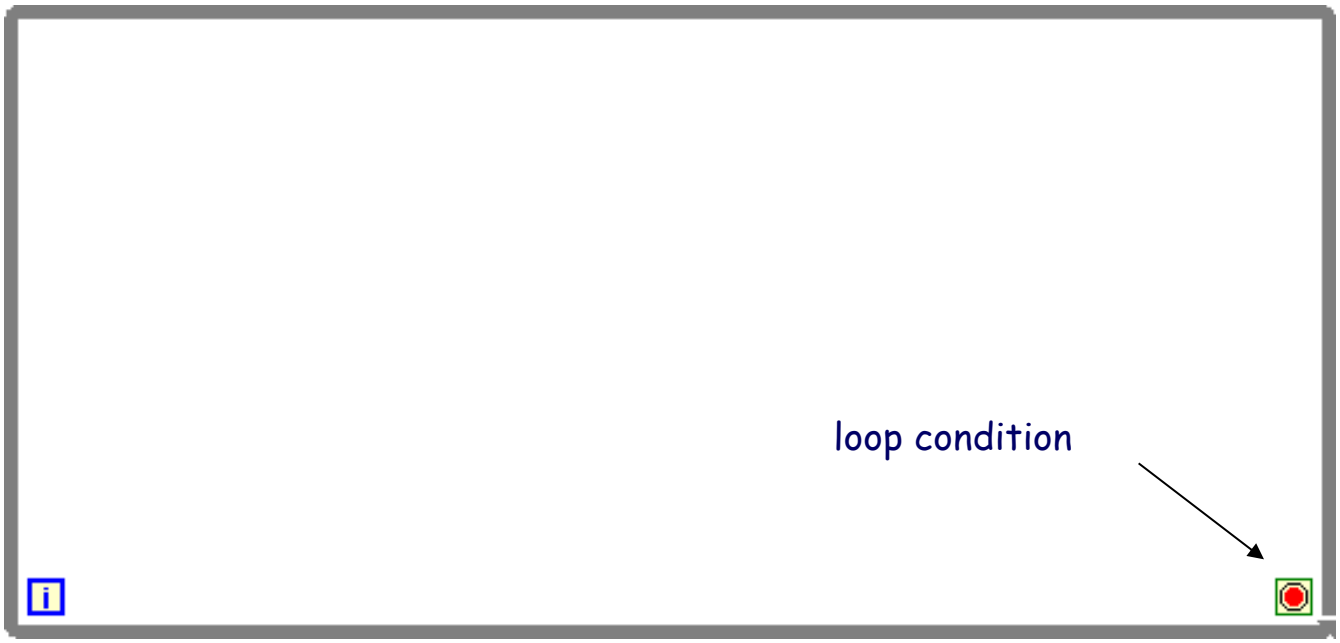


`Measurement I/O -> DAQmx Data Acquisition -> DAQmx Create Channel.vi`

`Measurement I/O -> DAQmx Data Acquisition -> DAQmx Read.vi`

While loop

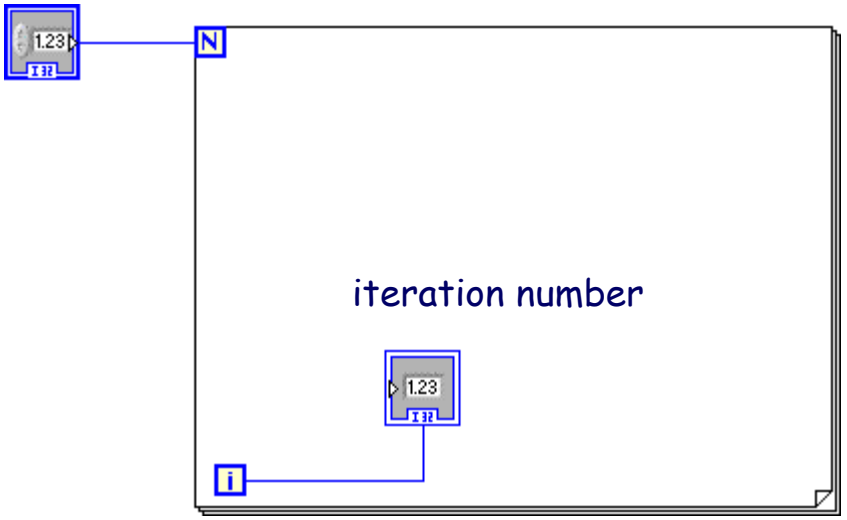
- Needed for continuous acquisition of the signal coming from the conditioning circuit (you can find it in the Structures menu from the Functions palette) – a "stop" button should be included in the virtual instrument to stop the acquisition



For cycle

- We can use a for cycle to reduce the effects of zero average disturbances, therefore improving the measurement accuracy

number of cycles



- Instead of representing (in the graph or in the numeric indicator) each individual acquired sample of the signal, we can represent the average value of N samples – the speed at which the measurement result is represented on the graph will decrease by a factor of N

Suggestions and improvements

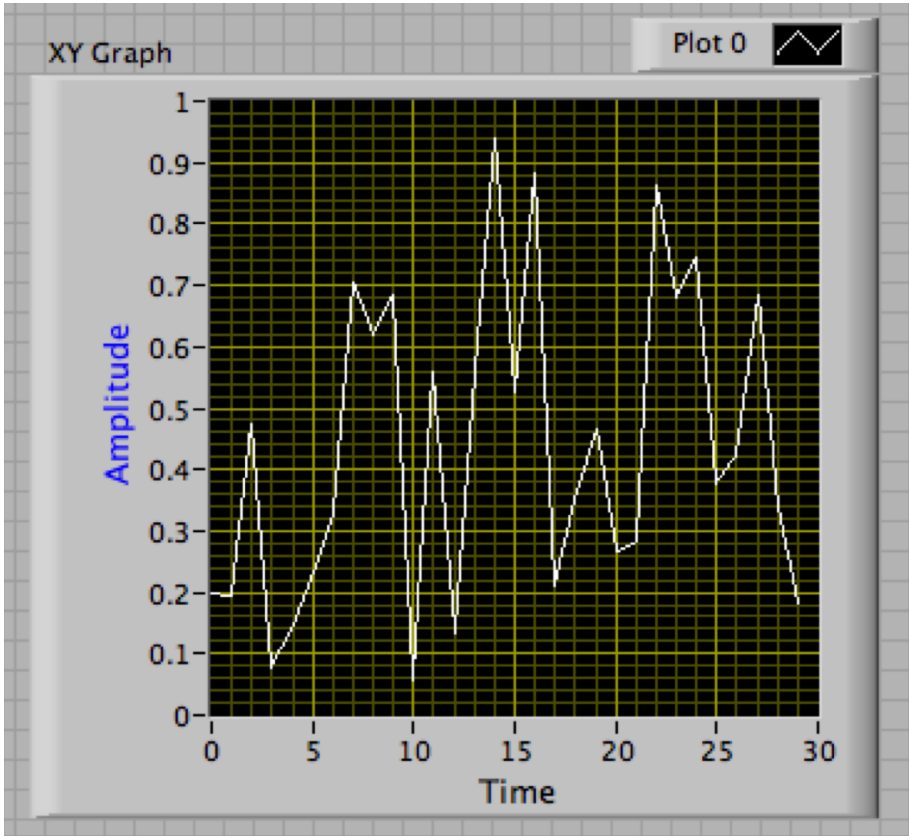
- It might be useful and interesting to compare the theoretical data with the data acquired by the VI and the data measured with a digital voltmeter. What are the reasons for the (unavoidable) differences among the three sets of data?

- Modify the VI in such a way that it can graphically display the input-output characteristic of the DAC (both the theoretical and the measured one) on the front-panel and it can write the relevant data to a file in the form of a numerical table

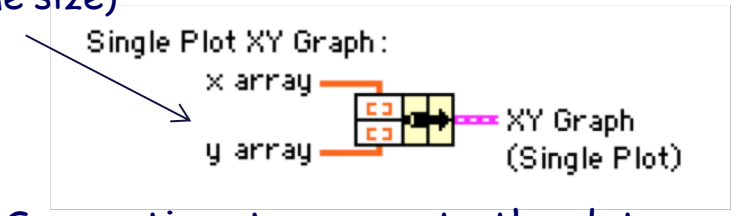
- Modify the VI in such a way that it can graphically display the differential non linearity (DNL) and the integral non-linearity (INL) of the DAC

Graphical representation of the I/O characteristic and of DNL e INL

- XY graph (Modern-> Graph ->XY Graph o Classic ->Classic Graph ->XY Graph)
- A Bundle function is required (Programming-> Cluster, Class & Variant-> Bundle) to group the independent (X) and dependent (Y) variables in a single array

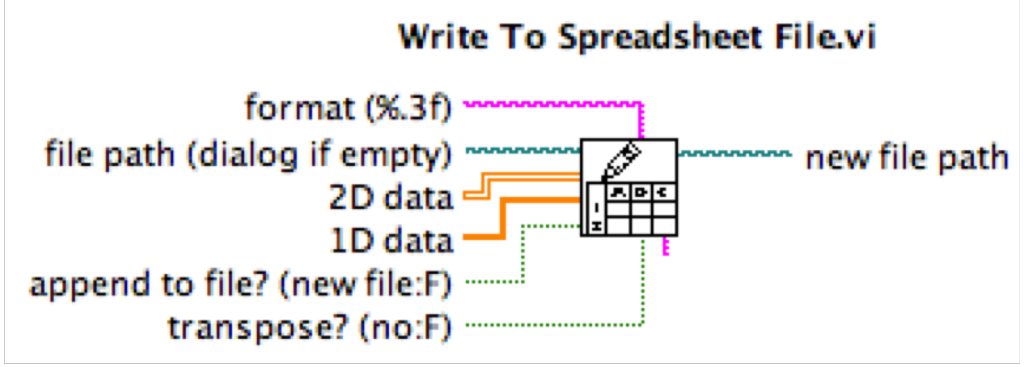


Input data in the form of vectors (same size)



Suggestion: to generate the data vectors one could use tunnels in "indexed" modes in a for structure

Writing a file

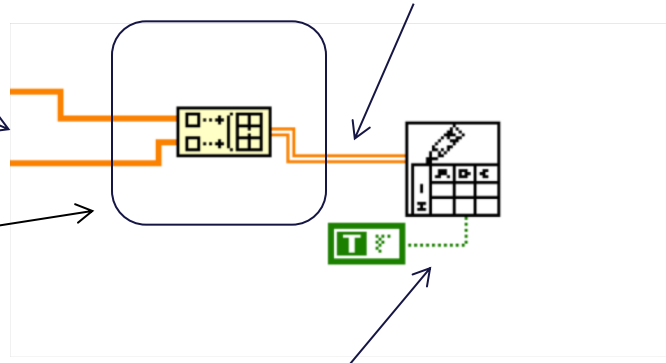


Programming-> File I/O->
Write To Spreadsheet File.vi

output: 1 2D array (2 column data table)

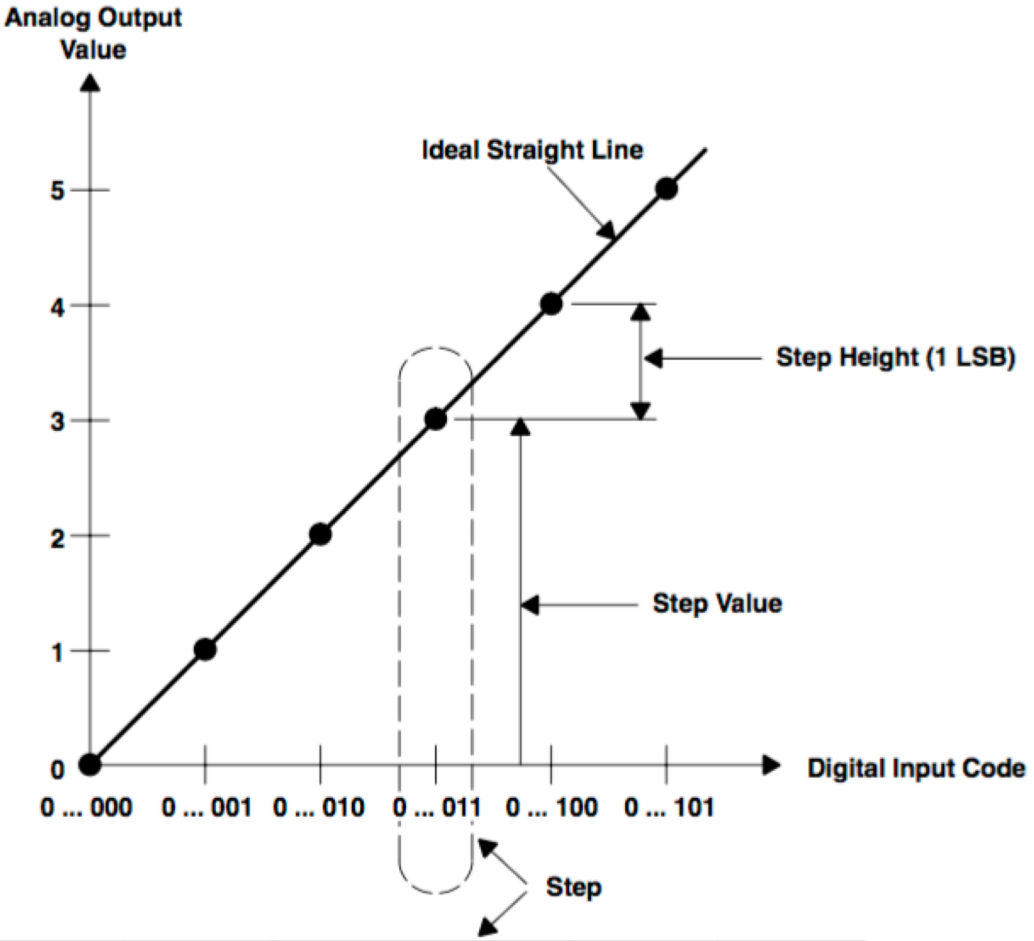
input: 2 1D arrays

Programming-> Array-> Build Array



2D array transpose? yes

Input-output characteristic

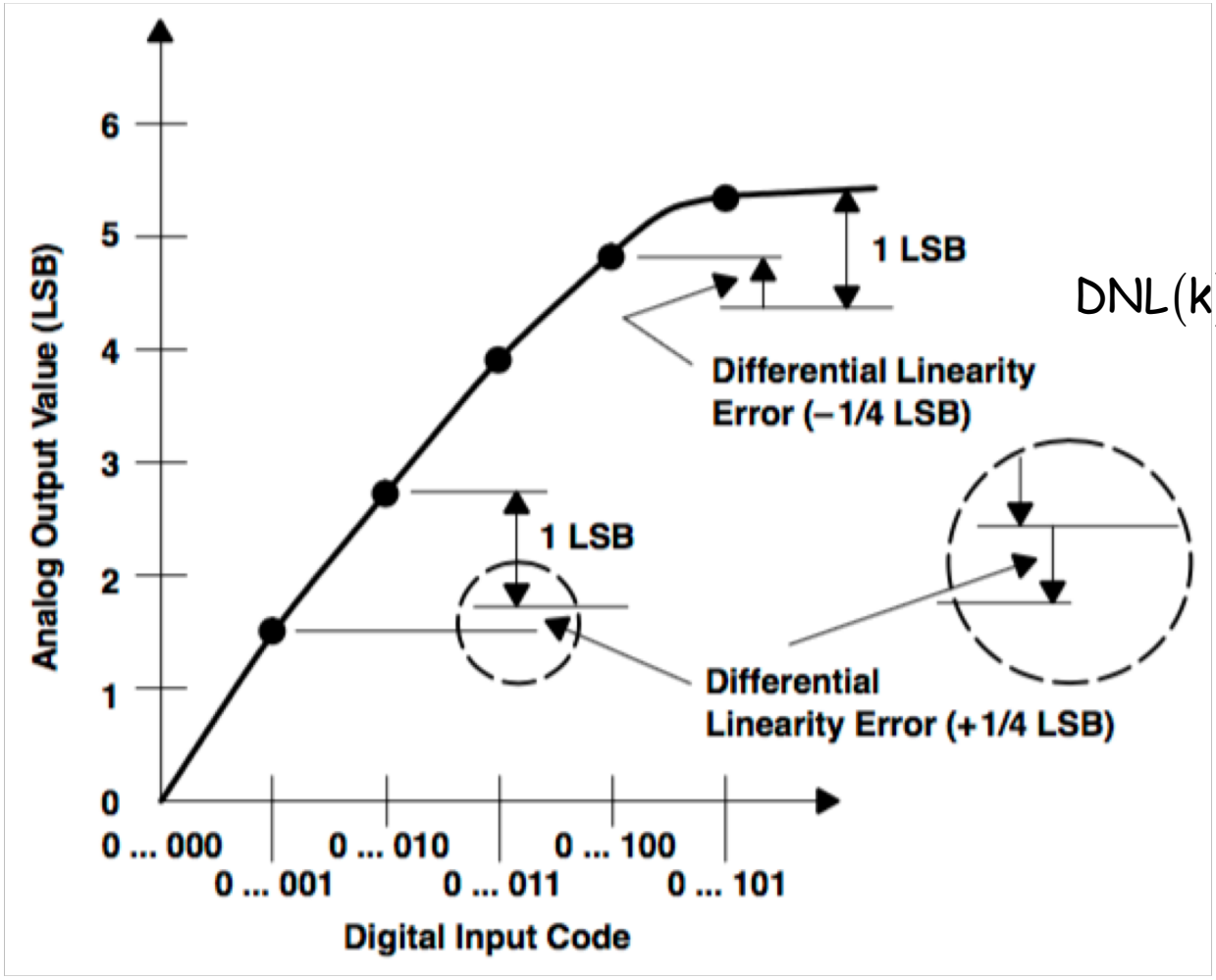


CONVERSION CODE

Digital Input Code	0 ... 000	0 ... 001	0 ... 010	0 ... 011	0 ... 100	0 ... 101
Analog Output Value	0	1	2	3	4	5

Elements of Transfer Diagram for an Ideal Linear DAC

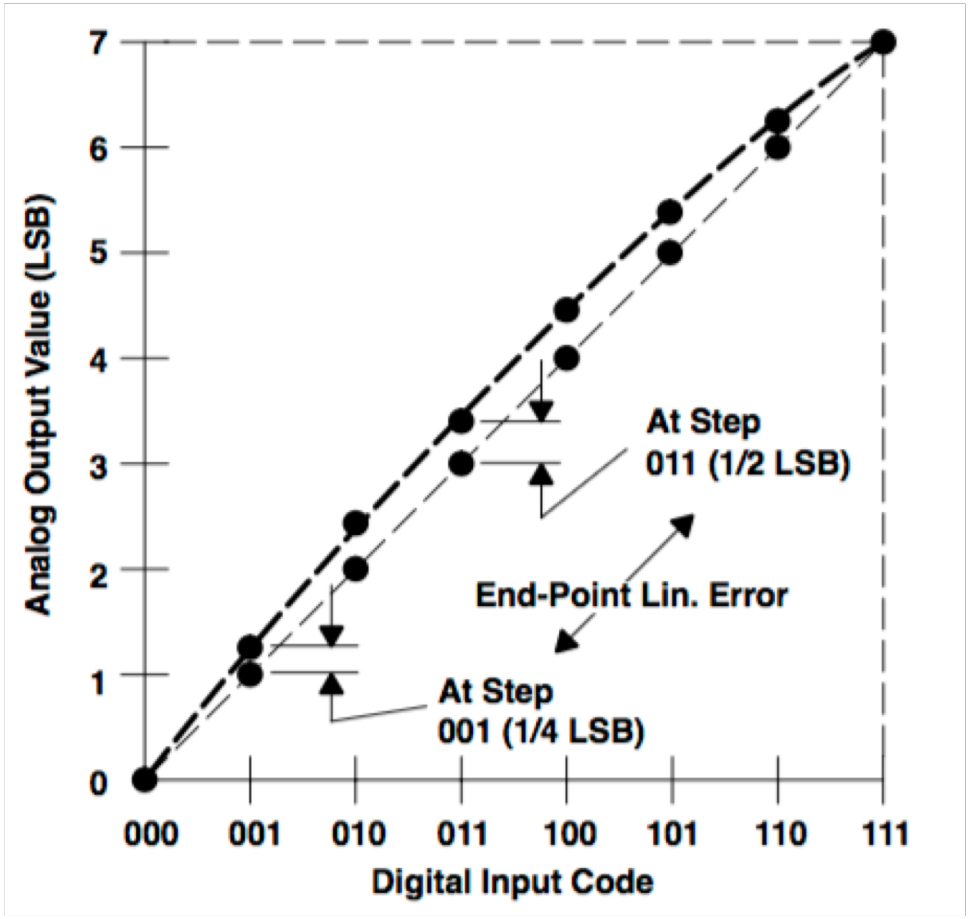
Differential non-linearity



$$DNL(k)=\frac{V_{out}(k+1)-V_{out}(k)}{LSB}-1,\ k\in\left[1,\ 2^n-1\right]$$

$$LSB=\frac{V_{REF}}{2^n}$$

Integral non-linearity



$$INL(k)=\frac{V_{out}(k)-k\cdot LSB}{LSB},\ k\in[0,\ 2^n-1]=$$
$$=\frac{V_{out}(k)}{LSB}-k$$

$$LSB=\frac{V_{out}(2^n-1)-V_{out}(0)}{2^n-1}$$