Integrated Circuit Packaging and Thermal Design

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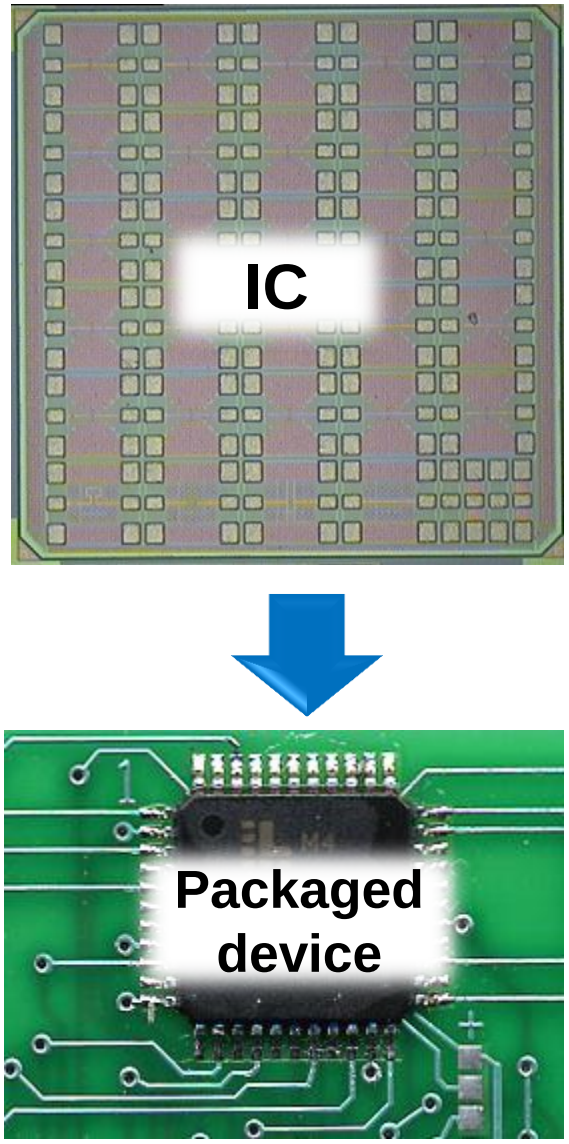
Introduction to IC Technologies

Packaging

- Die attach
- Wire bonding
- Packaging materials *
- Package types (TQFP, MLF,COB)
- Thermal design *



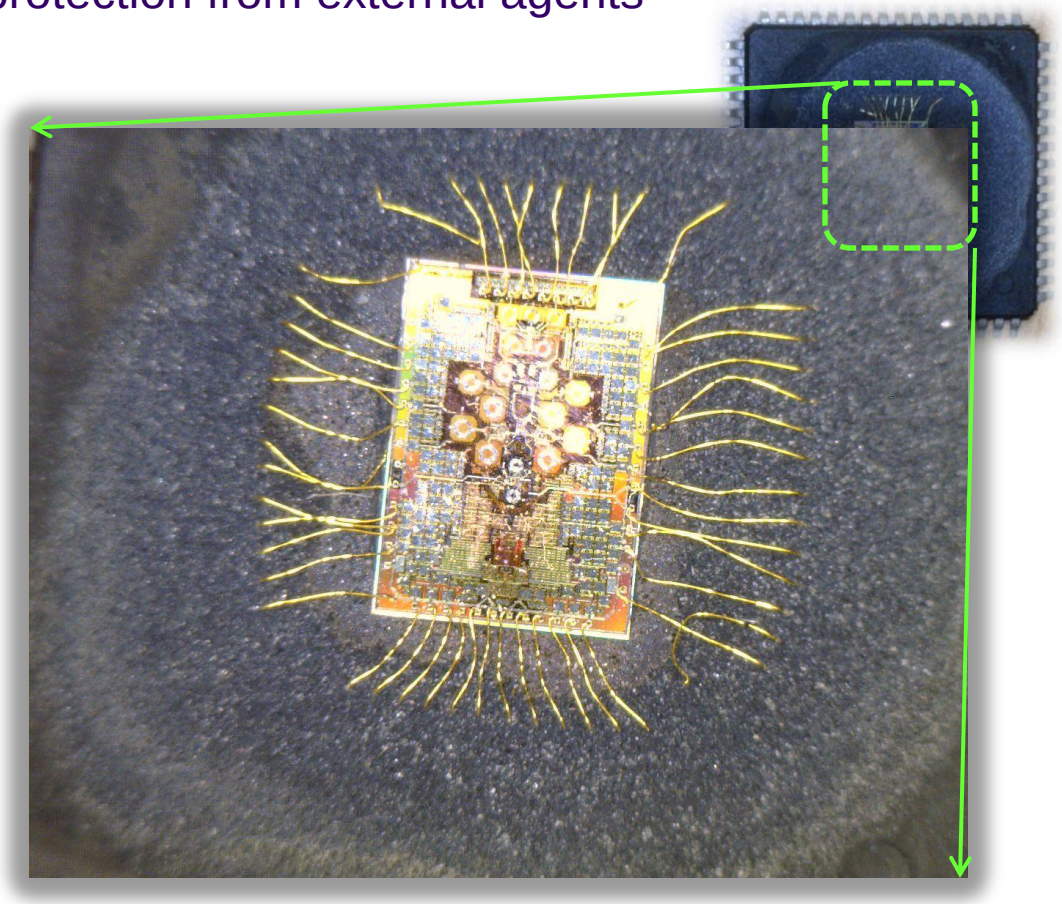
Refer to:

G. Torelli e S. Donati, *"Tecnologie e Materiali per l'Elettronica"*, Ed. CUSL

Packaging

Packaging is used to:

- Provide electrical connection between IC pads and PCB lines
- Mechanical and chemical protection from external agents
- Easier handling
- Thermal dissipation



PACKAGING PHASES

Die attach

Wire bonding

Sealing

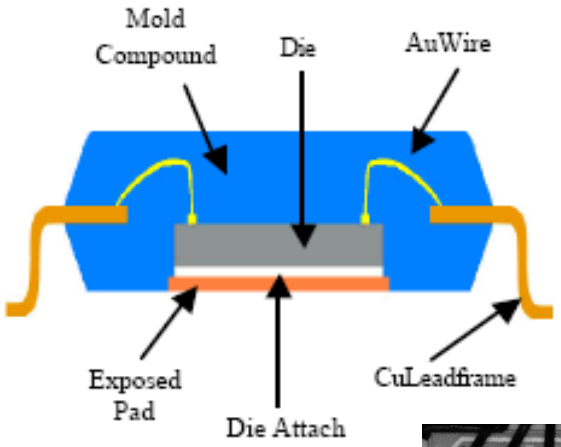
Die attach

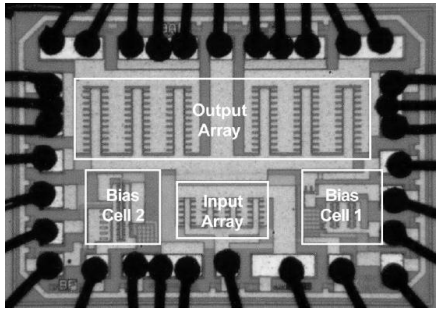
- **Eutectic solder**: wafer is back-plated with Au and package has an Au internal paddle. Eutectic Au/Si is formed at 400°C.

- **Sn/Pb solder**: wafer is back-plated and a tin/lead solution is deposed on the package paddle. Soldering is carried out at 200-350°C.

- **Conductive epoxy**: adhesive epoxy loaded with conductive materials (e.g. Au) is dispensed on the lead-frame. Soldering is carried out by means of epoxy polymerization at 125-175°C.

Wire Bonding





Manual bonding machine

Wire materials:

Au, Al

Typical bonding wire diameter ~ 30μm

Electrical parameters:

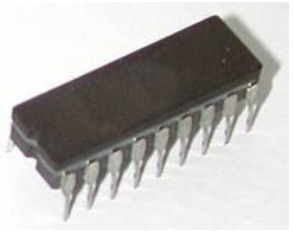
- Self Inductance ~ 1nH / mm
- DC resistance ~ 30mΩ / mm
- Capacitance ~ 100fF / mm

Packaging Materials

COST

- Metal packages: (kovar)
  - Used for high power and high reliability devices
  - Excellent thermal dissipation
  - EM shield
  - High cost

- Ceramic packages: (alumina)
  - E.g. glass-seal (“frit-seal”)
  - Good thermal dissipation
  - Intermediate cost



- Plastic packages: (epoxy)
  - Mechanic stress due to different thermal coefficients
  - Low thermal conductivity
  - Low cost

Plastic Materials

- Definition: **polymers** (long chains of atoms bonded to one another) These chains are made up of many repeating molecular units, derived from monomers through a process called *polymerization*.

- Polymerization processes: polyaddition, direct polymerization and polycondensation

- Excellent isolation properties: strong bonds between monomers provide a high electric stiffness ($\bar{E}_{MAX}$)

- Mechanical properties can be improved using additives such as glass fibers

For plastic and ceramic materials, refer to:

Dispense di G. Torelli e S. Donati, *"Tecnologie e Materiali per l'Elettronica"*, Ed. CUSL

Plastic Materials

- **Thermoplastic materials**: teflon (PTFE), polystyrene, polycarbonates
  - Melt reversibly at high temperatures
  - Typically quite flexible
- **Thermosetting plastics**: epoxy resin, silicon resin, polyester, …
  - Harden irreversibly after it is cured

- Applications:
  - Capacitors dielectric material (polystyrene, polyester resin, polycarbonates)
  - Printed circuit board (epoxy, teflon)
  - Isolation (teflon)
  - Packages (epoxy)

Relevant Parameters

• Thermal conductivity [W/°C cm]	0.1 - 0.3
• Thermal capacity [J/°C cm^3]	40 – 160
• Resistivity [GΩ cm]	>1
• Dielectric strength E_R [kV/mm]	10 - 100
• Loss tangent Tan δ (= – Im[ε] / Re[ε])	10^{-4}-10^{-2}

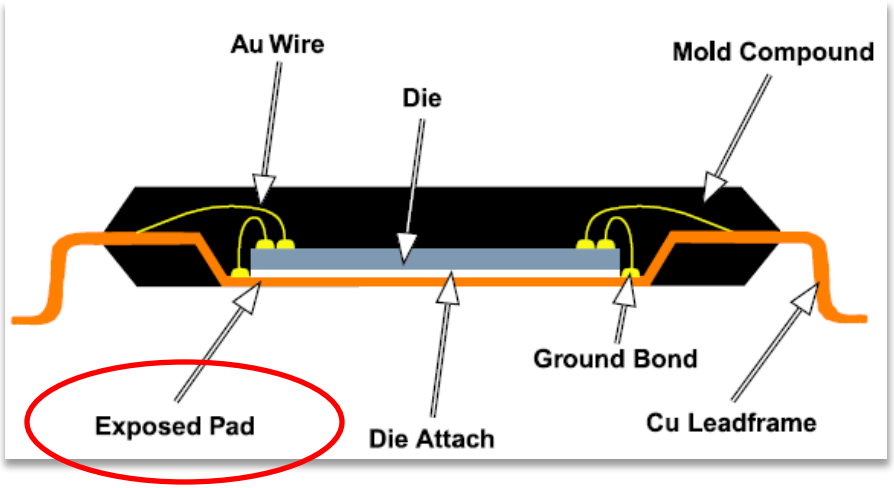
Ceramic Materials

- Ceramic materials are compounds obtained from various materials reduced in fine particles, as a result of a *firing* (sinterization) process
- Features:
  - Hardness, stiffness
  - Immunity to humidity and corrosion
  - Good isolating and resistive materials can be synthesized

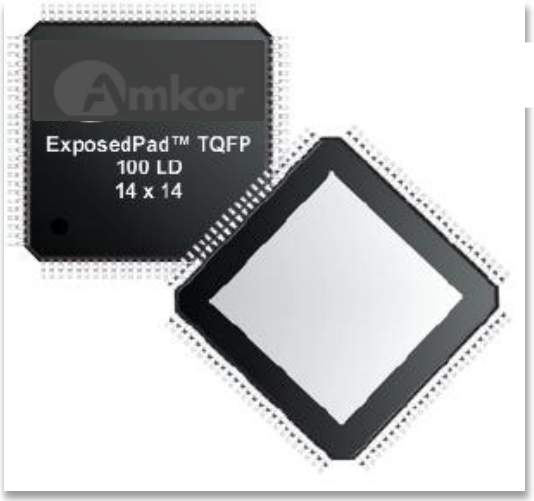
Production Process

- Grinding
  - Compound materials are reduced to fine particles (Ø~1mm)
- Compact formation
  - Usually through mechanical pressure
- Firing
  - Liquid phase: sintering is carried out above the melting point of at least one component;
  - Solid phase: grain diffusion; better mechanical properties and reduced aging effects

Exposed-Pad TQFP

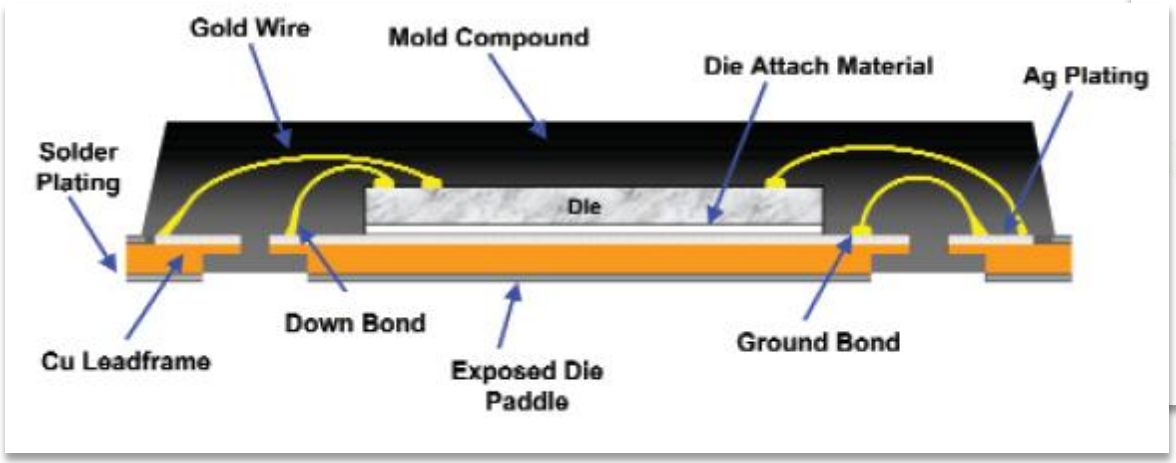


Exposed Pad Thin Quad Flat Package (TQFP)



- The Exposed Pad can increase heat dissipation by as much as 110% over a standard TQFP.
- The Exposed Pad can be connected to ground, reducing “ground” inductance for high frequency applications.
- Used in high performing products such as telecom, disk drives, pagers, wireless, CATV/RF modules, radio and other similar applications.

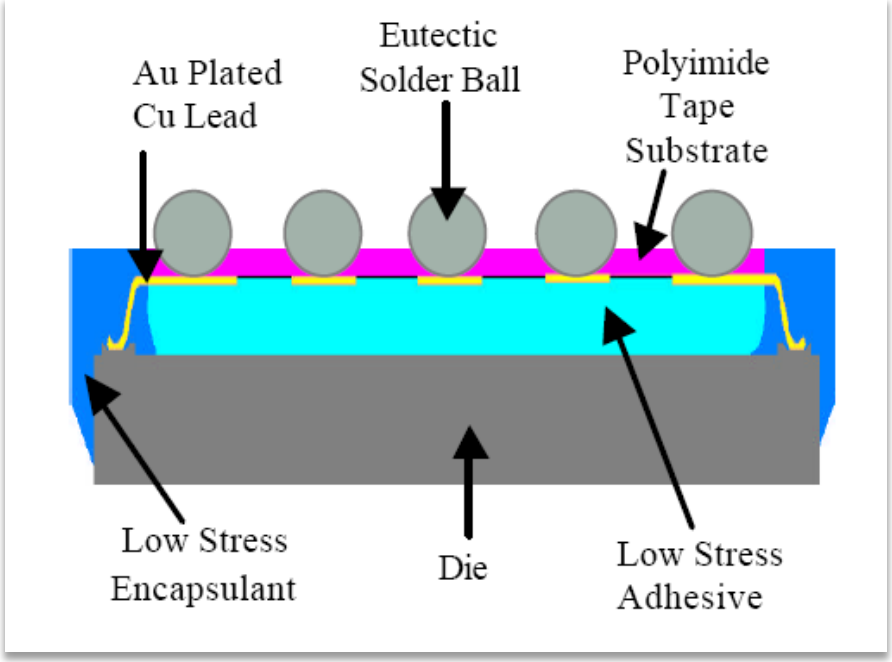
Exposed Pad Micro-Lead Frame



- Plastic encapsulated package with a copper leadframe substrate
- reduced lead size strongly reduces the parasitic inductances and capacitances
- An ideal choice for handheld portable applications such as cell phones and PDAs or any other application where size, weight and package performance are required issues.

Chip-Scale Packages

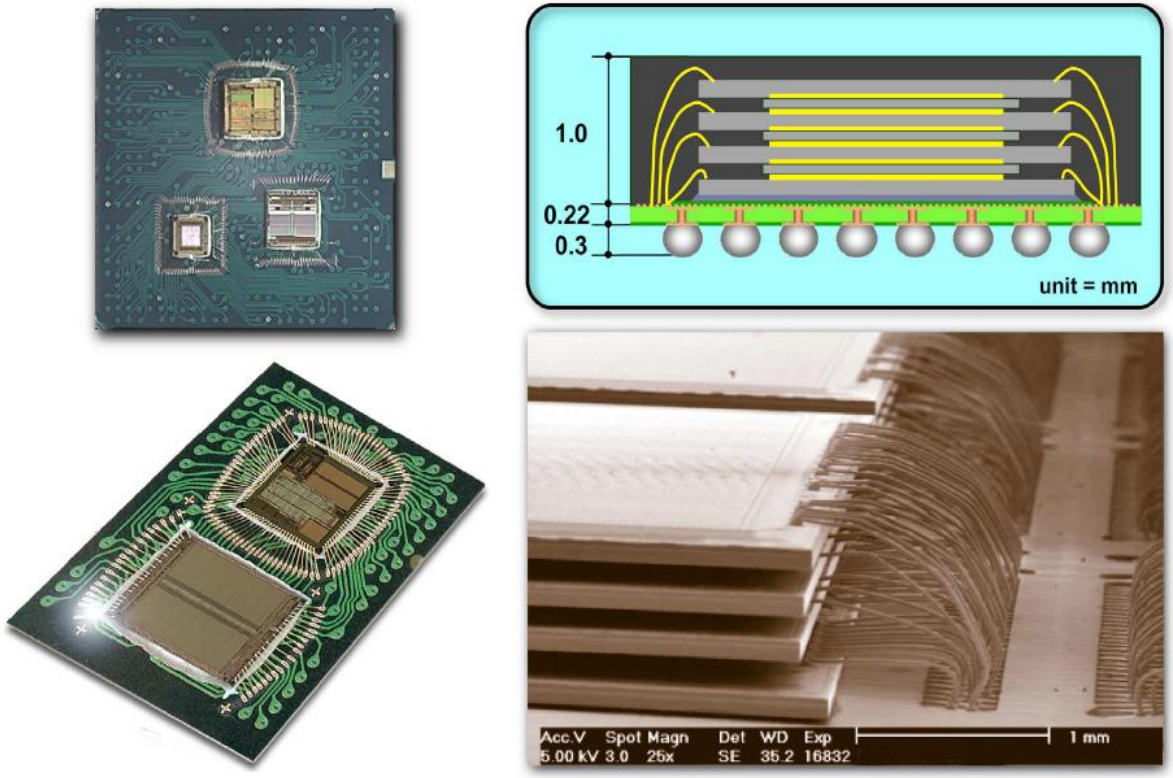
Ball Grid Array



A true Chip Scale Package. Used for ICs with large pin count (e.g. memory, analog, ASICs, RF devices and simple PLDs requiring a small package size).

System-in-Package (SiP) Example

Multichip and Stacked Dice



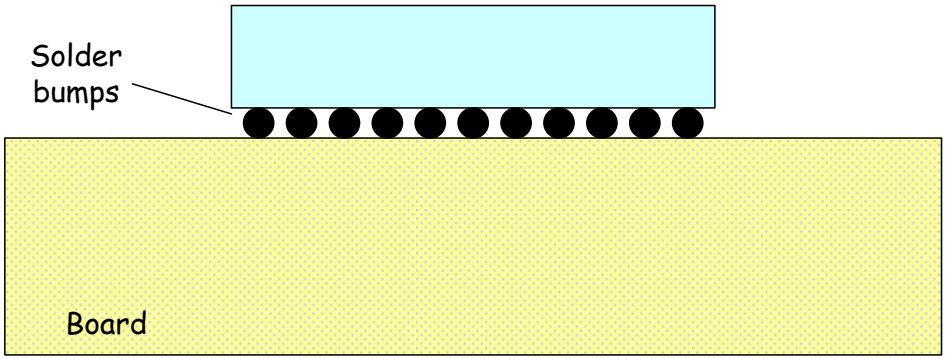
Multichip Module

Stacked Dice

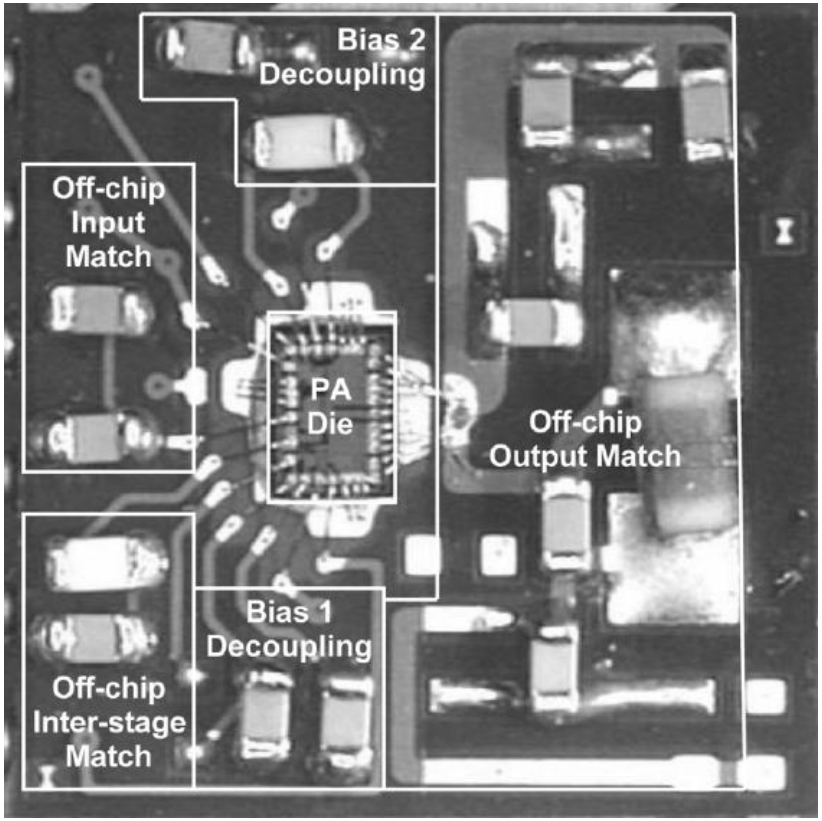
B. Murari, “Bridging the Gap Between the Digital and Real World: the Expanding Role of Analog Interface Technologies”, International Solid-State Circuits Conference 2003, *San Francisco, February 10, 2003*

Chip-on-Board

Flip-chip



Chip-to-PCB wirebond

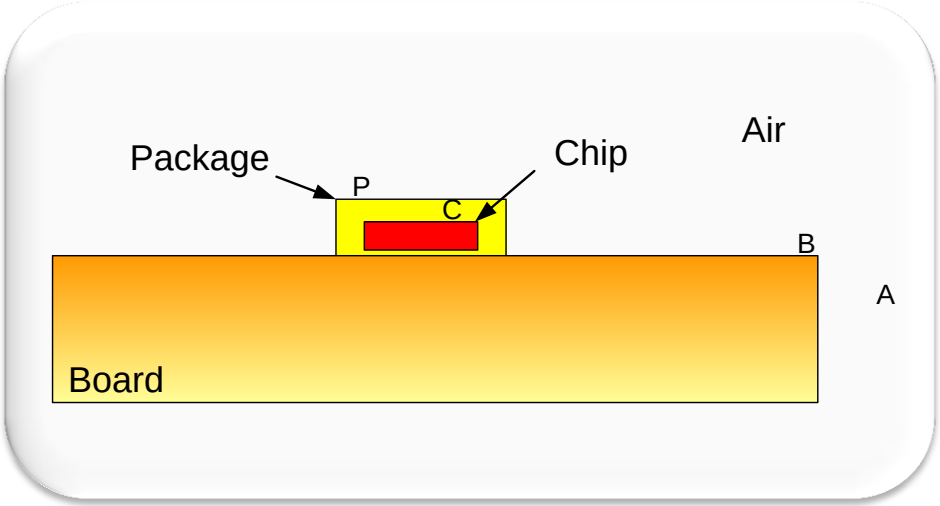


- Eliminate package parasitics
- Minimize size
- High speed / power applications

Thermal Design

- Temperature range:
  - Commercial 0°C< T < 70°C
  - Industrial -40°C < T < 85°C
  - Military range -55°C < T < 125°C

- Thermal exchange mechanisms:
  - Conduction
  - Convection
  - Radiation



Electrical-Thermal Equivalent

Dissipated Power ⟺ Electrical Current

Temperature ⟺ Electrical Potential (Voltage)

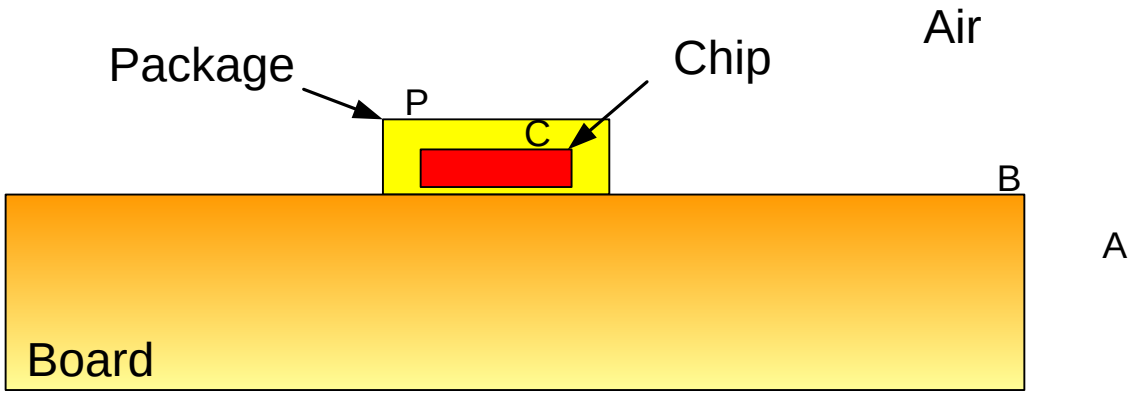
Equivalent Thermal Resistance ⟺ Electrical Resistance

$$R_{TH} = \frac{\Delta T}{P} \qquad R = \frac{\Delta V}{I}$$

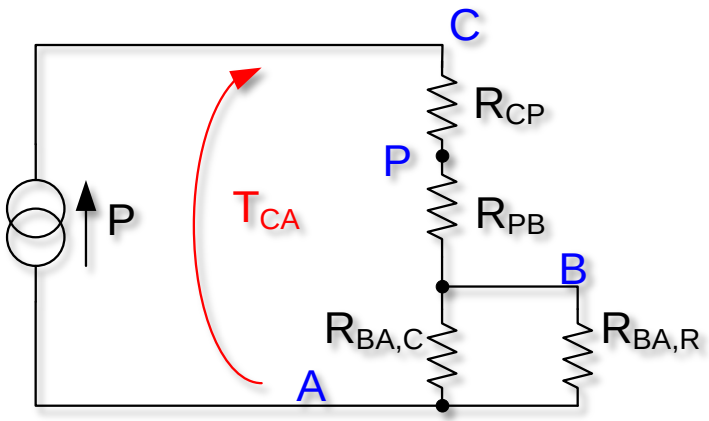
Fourier Law $\Phi = -K\nabla T$ ⟺ $J = \sigma E = -\sigma \nabla V$

K thermal conductivity [W/°Ccm] ⟺ σ el. conductivity [S/cm]

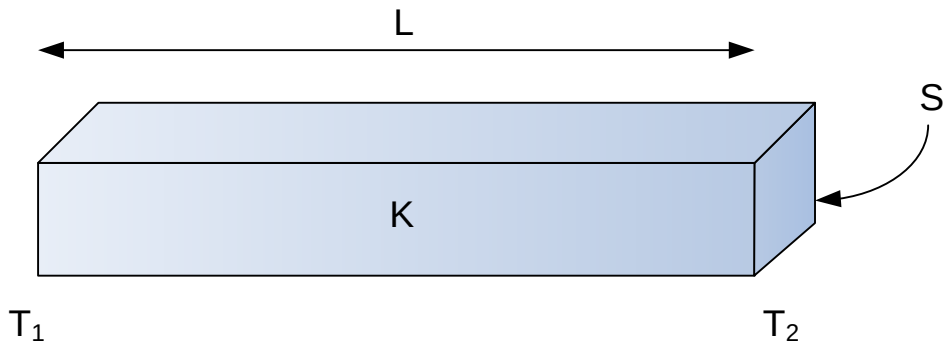
Thermal Modeling



Thermal Equivalent Circuit



Thermal Conduction



$$R_{TH} = \frac{1}{K}\frac{L}{S}$$

During transients *thermal capacitance* must be taken into account:

$$C_{TH} = \rho c L S$$

During transients thermal capacitance must be taken into account:

$$\frac{\partial T}{\partial t} = \frac{K}{\rho c}\frac{\partial^2 T}{\partial x^2} = \alpha \frac{\partial^2 T}{\partial x^2}$$

(Free) Thermal Convection

- The **Nusselt number (N_{NU})** measures the enhancement of heat transfer from a surface that occurs in a 'real' situation, compared to the heat transferred if just conduction occurred.

$$N_{NU} = \frac{hL}{K}$$

Convection heat transfer coeff.

Effective thermal conductivity

Characteristic length (Volume/Surface)

Th. Conductivity

Convection thermal resistance:

$$R_{TH,CONV} = \frac{1}{hS}$$

Empirical expression:

$$h = 0.4\left(\frac{\Delta T}{L}\right)^{1/4} \left[mW/°Ccm^2\right]$$

where ΔT is in °C and L in cm.

Thermal Radiation

- *Thermal radiation* is electromagnetic radiation emitted from the surface of an object which is due to the object's temperature. The total amount of radiation, of all frequencies, **goes up very fast as the temperature rises**:

$$P = \varepsilon \sigma S T^4$$

ε	emissivity (<1)
σ	Stefan-Boltzmann constant = 5.67 10^{-8} W/m^{2}K^4
S	surface area

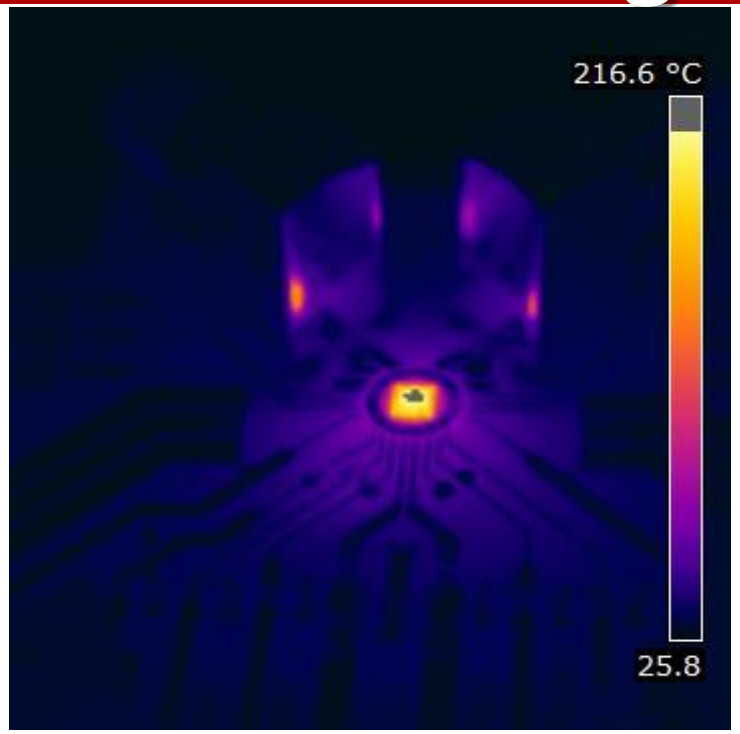
Power radiated toward ambient:

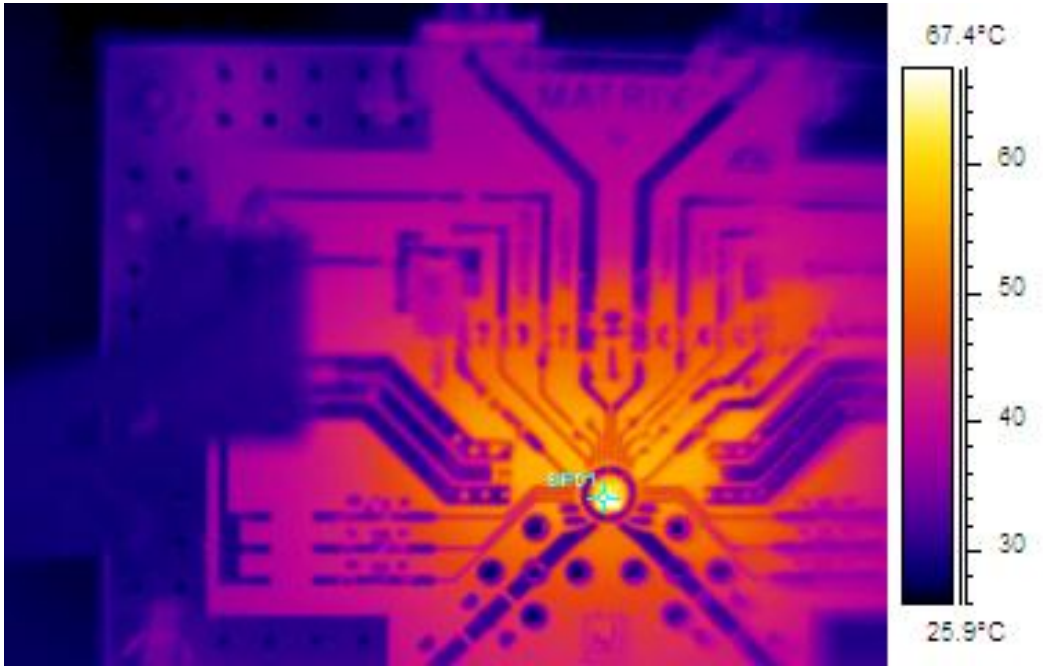
$$\Delta P \approx 4\sigma S T_a^3 \Delta T$$

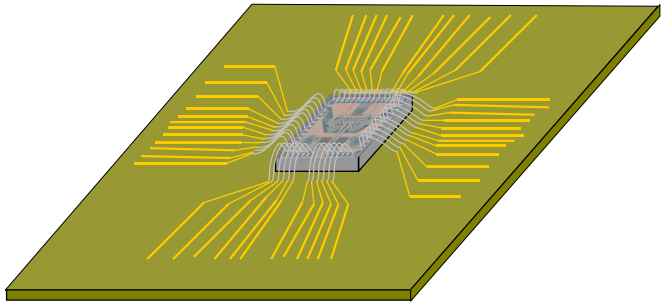
Radiated Thermal Resistance:

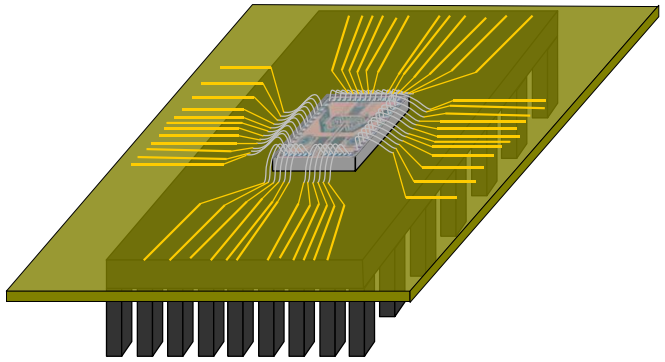
$$R_{TH,R} \approx \frac{1}{4\sigma S T_a^3}$$

Thermal Diagram









Homework

10 devices over an 8cm x 12.5cm printed circuit board.

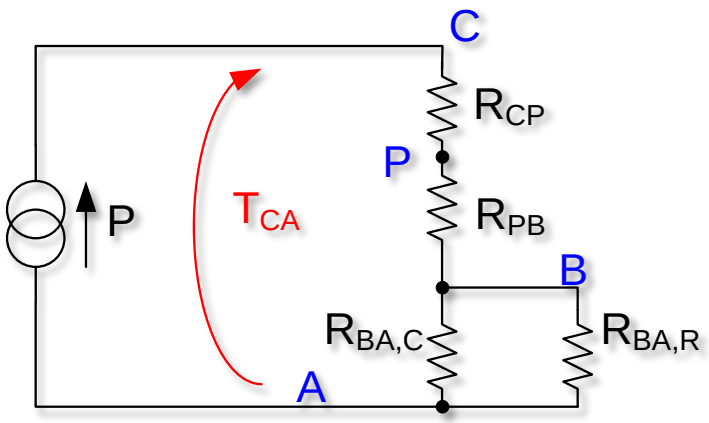
R_{CP}=20°C/W

R_{PB}=3°C/W

Maximum ambient temperature: 40°C

Maximum operating temperature of each device: 85°C

Find the maximum power dissipated by each element.



References

- References:
  - www.amkor.com

- Reading Material:
  - Dispense di G. Torelli. Introduzione alla tecnologia dei circuiti integrati su silicio. 2006. (IC Technologies)
  - Dispense di G. Torelli e S. Donati, *"Tecnologie e Materiali per l'Elettronica"*, Ed. CUSL
  - Dispense del corso *Microfabrication Technology*, UCB http://organics.eecs.berkeley.edu/~viveks/ee143/