AA 2012/2013

Lezioni di Tecnologie e Materiali per l'Elettronica

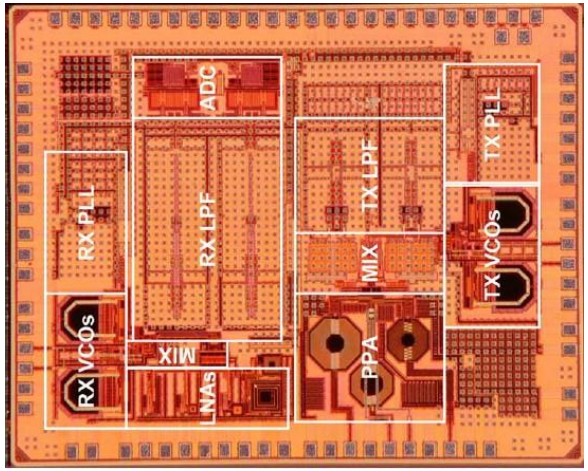
Danilo Manstretta

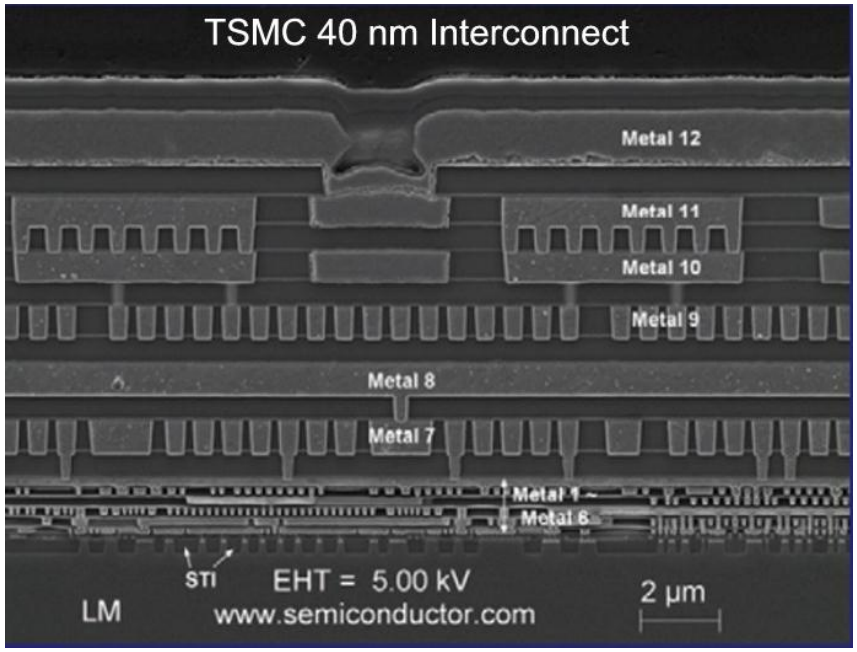
danilo.manstretta@unipv.it

microlab.unipv.it

Università degli Studi di Pavia

Outline





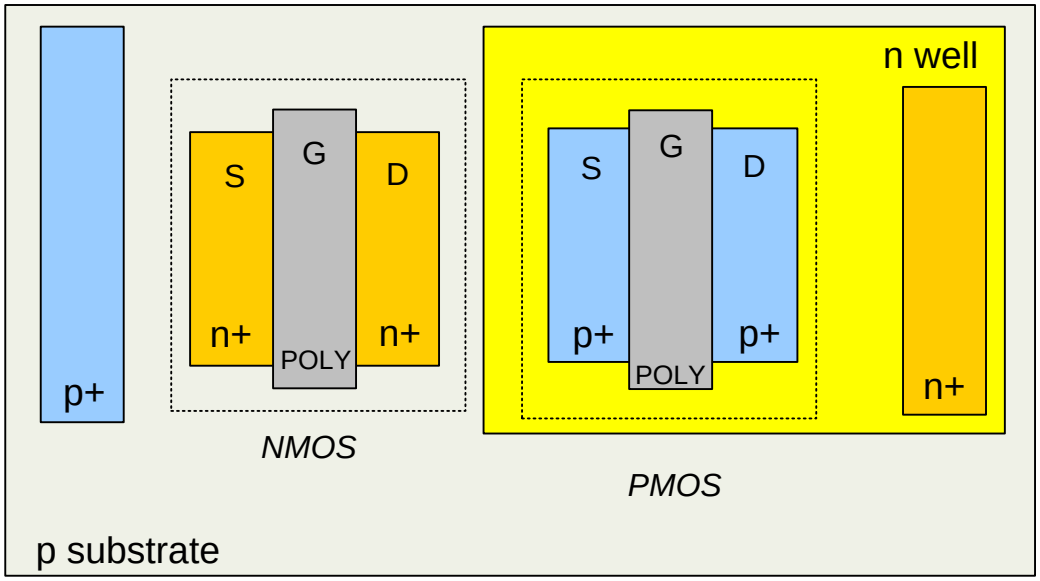
- **Passive components**
  - Resistors
  - Capacitors
  - Inductors
- **Printed circuits technologies**
  - Materials and fabrication steps
  - Assembling
- **Monolithic IC technologies**
  - Fabrication steps (thermal oxidation, thermal diffusion, …)
  - IC technologies (CMOS, BiCMOS)
  - Packaging and Thermal Design

HOW A MOS TRANSISTOR IS BORN

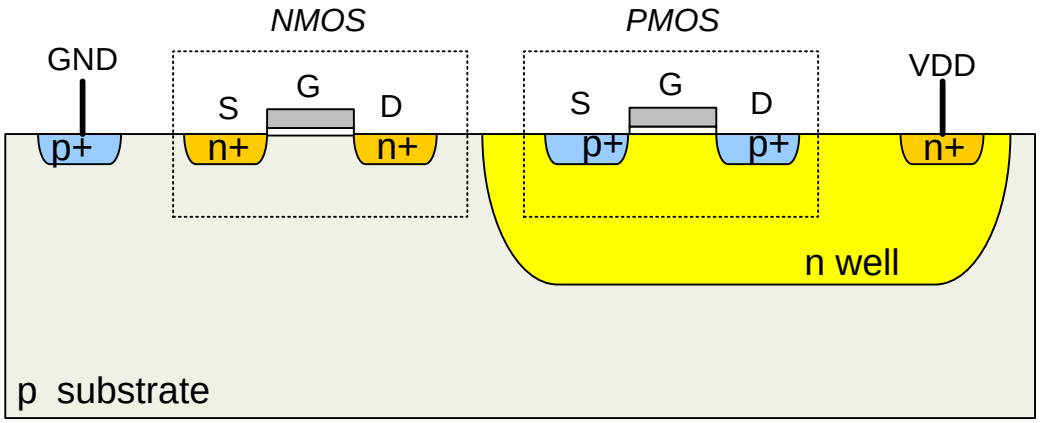
CMOS PROCESS FLOW

CMOS Technologies

TOP VIEW



CROSS SECTION



MOSFET Operation

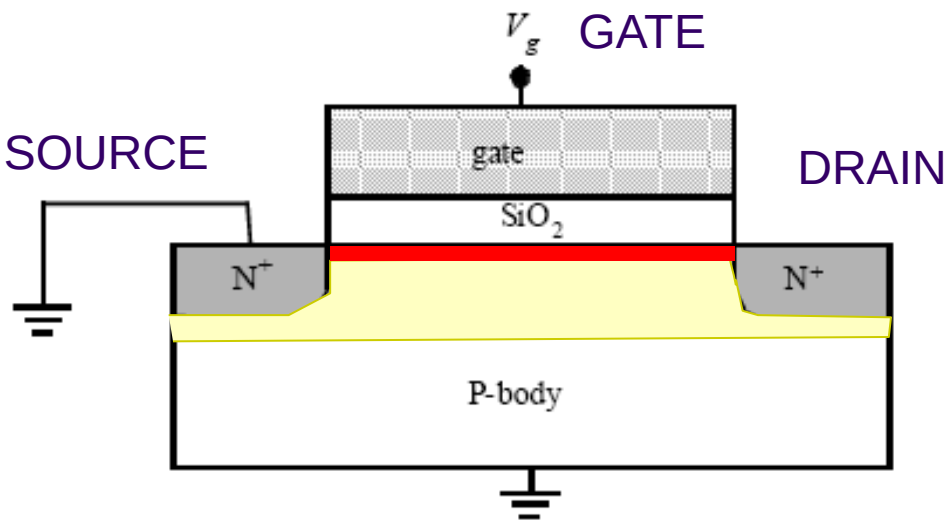
$$I_D = \frac{W}{L}\mu_n C_{ox}\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

$$\phi_B = \frac{KT}{q}\ln\left(\frac{N_A}{n_i}\right)$$

$$V_{TH} = V_{FB} + 2\phi_B + \frac{\sqrt{4qN_A\varepsilon_S\phi_B}}{C_{ox}}$$

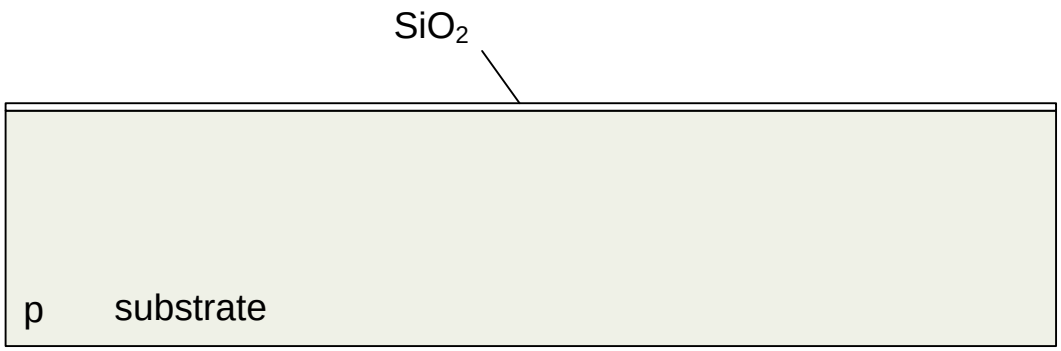
$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$C_{gs}\Big|_{Vds=0} = C_{ox}WL$$

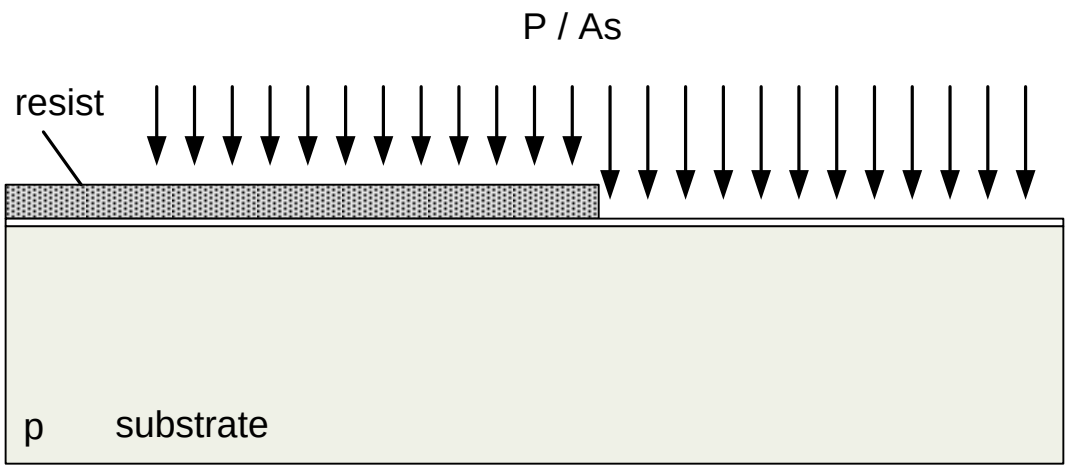


n_i=1.45 10^{10} cm^{-3} at 300K

CMOS Process Flow (1)

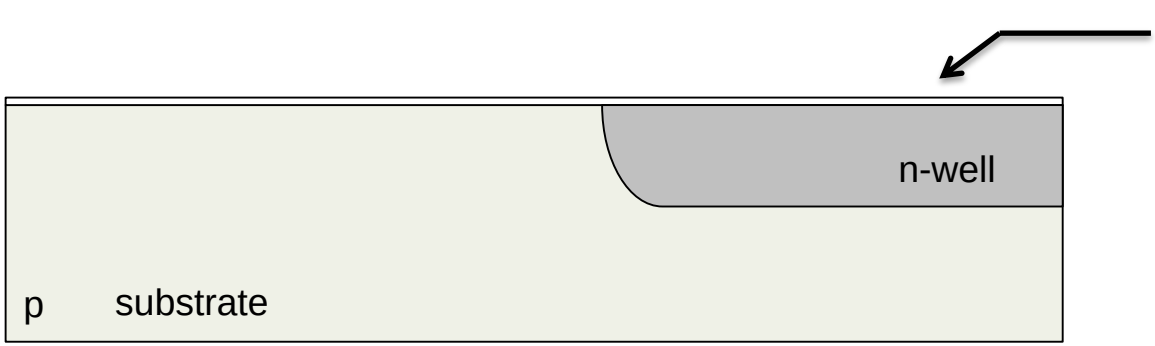


a) Oxidation



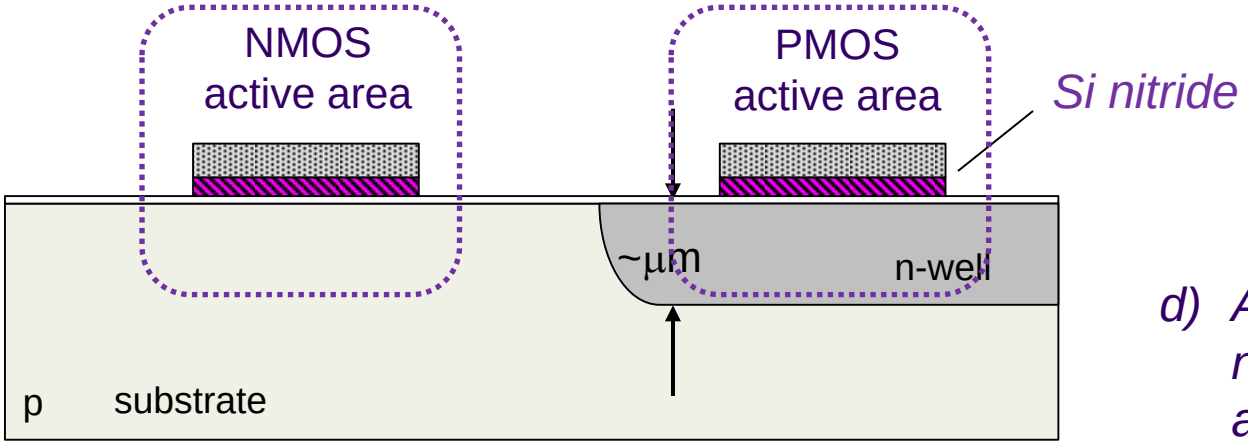
b) N-well implant

CMOS Process Flow (2)



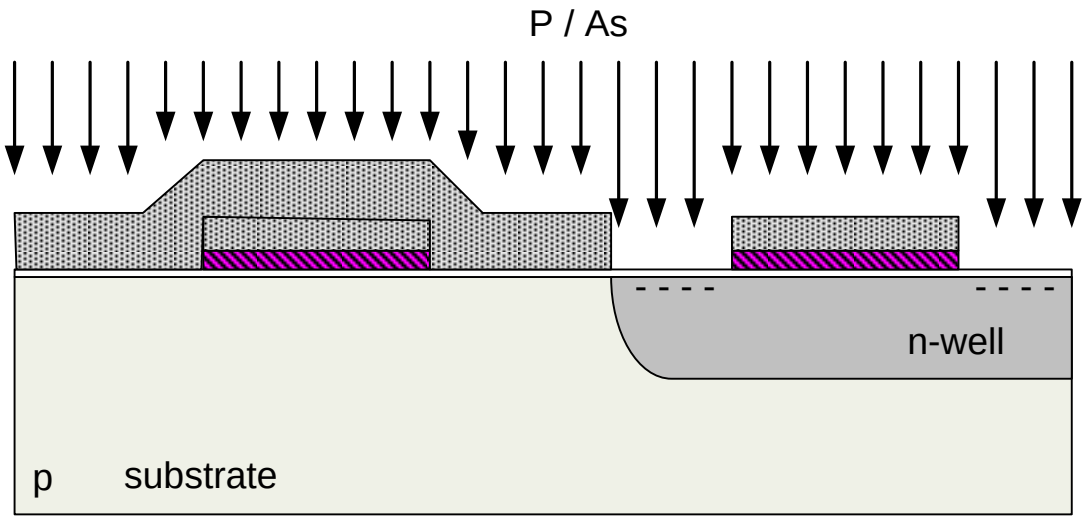
c) N-well diffusion (drive-in)

***The "active areas"** areas are the substrate regions where active devices are implemented. Active areas are surrounded by **isolation regions.** Si nitride is deposed over active areas to protect it from doping and oxidation carried out over "isolation" regions.*

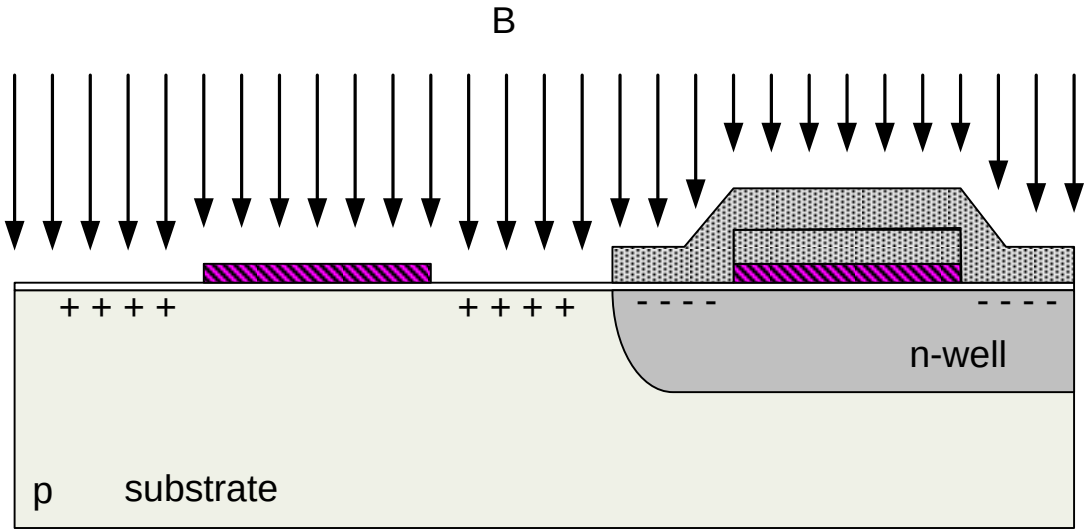


d) Active area definition: Si nitride "shield" deposition and etching

CMOS Process Flow (3)

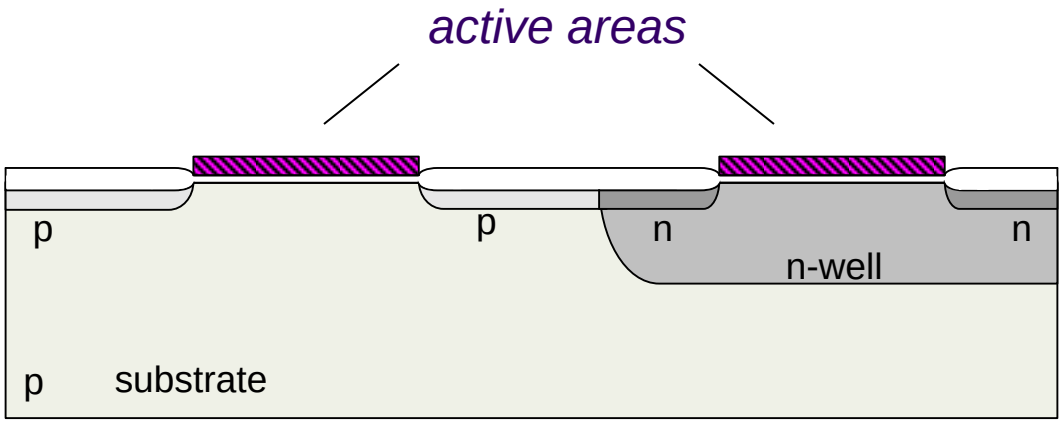


e) Field n-type implant on n-wells



f) Field p-type implant on substrate

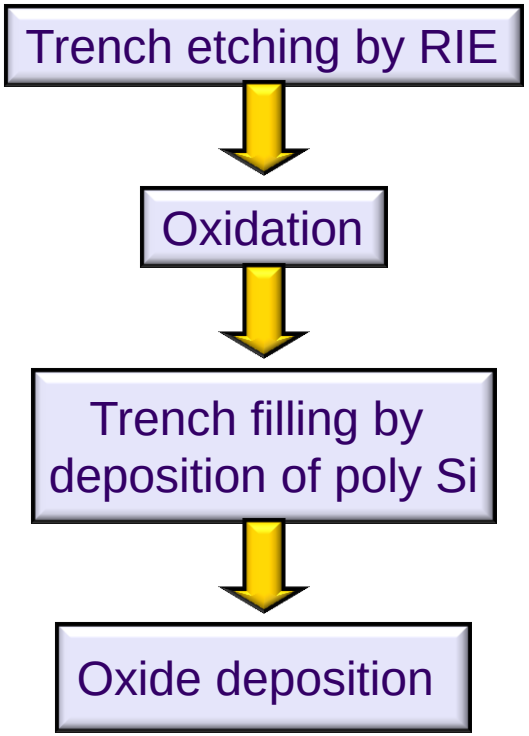
CMOS Process Flow (4)

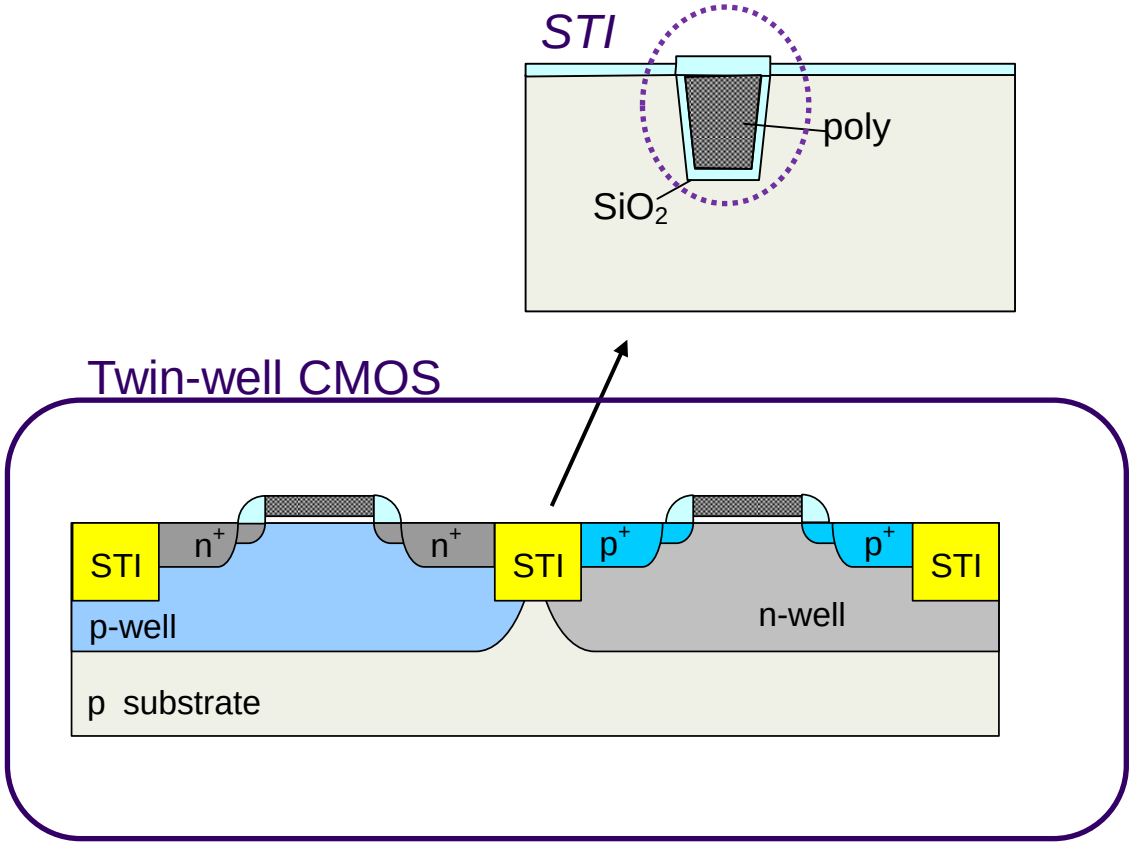


A thick oxide layer is formed over isolation regions

g) Field oxidation and diffusion

Shallow Trench Isolation (STI)

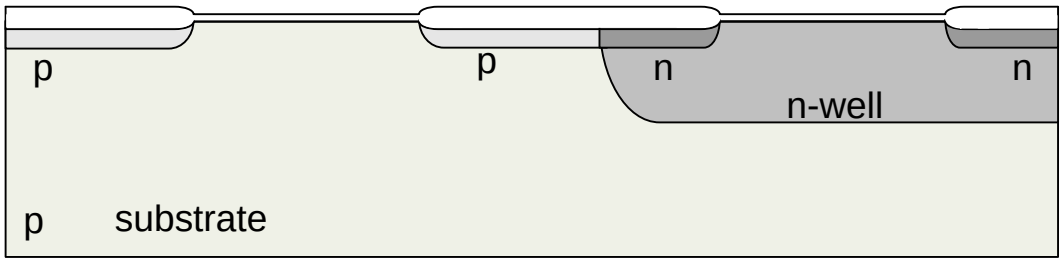




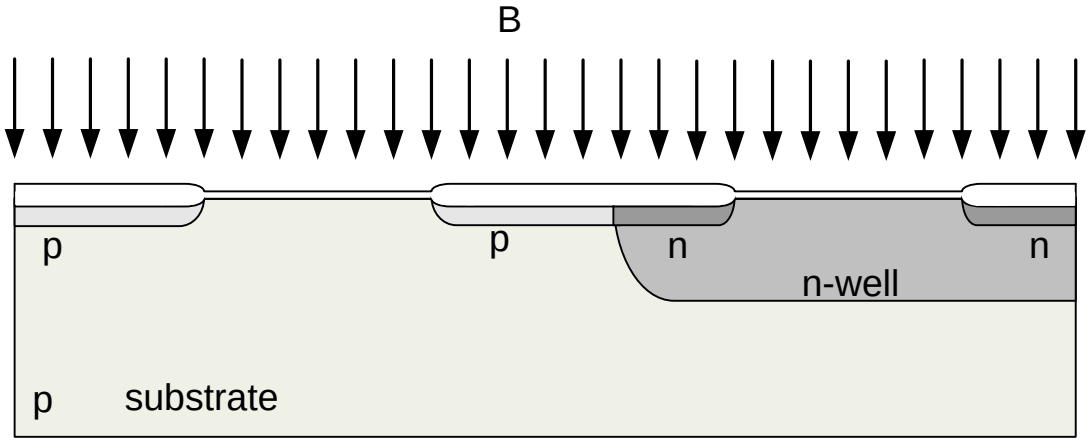
Shallow (e.g. 0.35μm depth) trench isolation in a twin-well process allows tighter well spacing.

CMOS Process Flow (5)

Creation of active devices (e.g. MOS transistors)

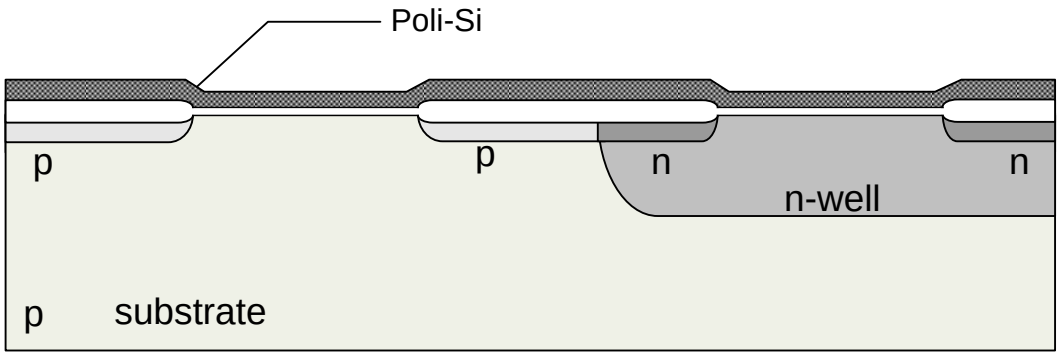


h) Gate (dry) oxidation

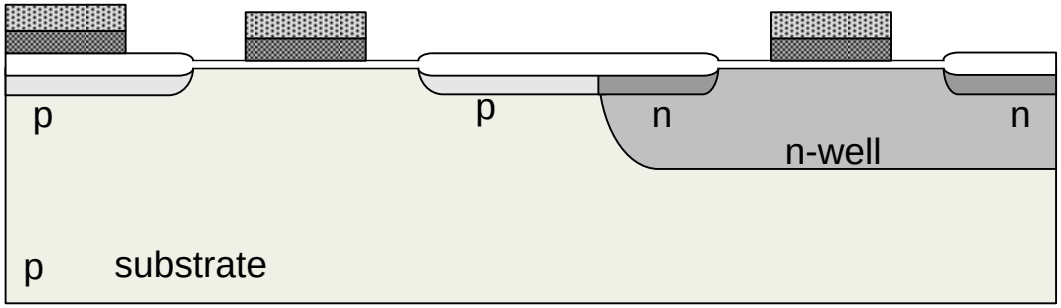


i) (Selective) Threshold adjustment implants

CMOS Process Flow (6)



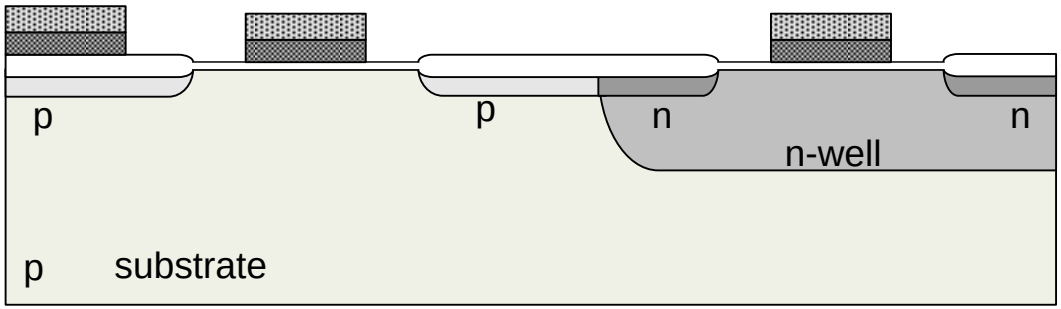
j) Poly deposition and <u>doping</u>



k) Poly etching: S/D definition

→ SELF - ALIGNMENT

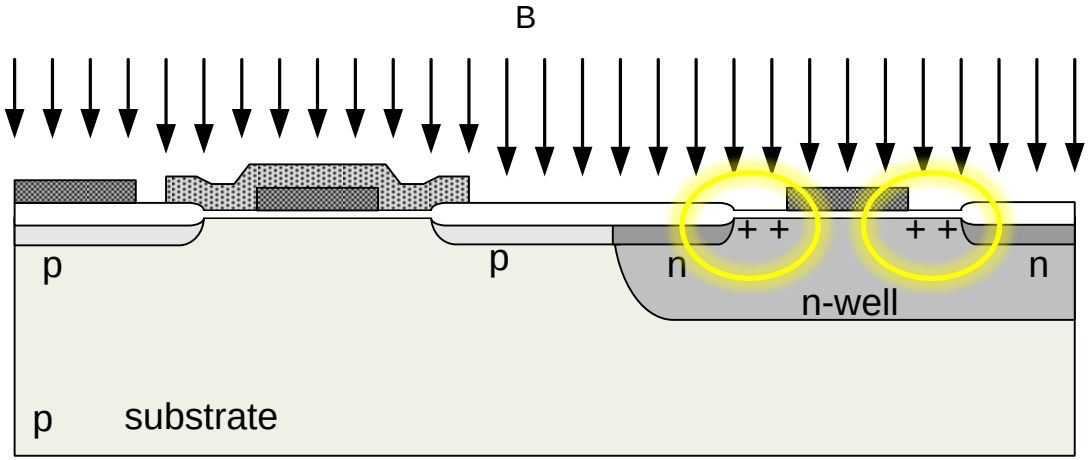
CMOS Process Flow (7)



k) Poly etching: S/D definition (SELF - ALIGNMENT)

Self-alignment

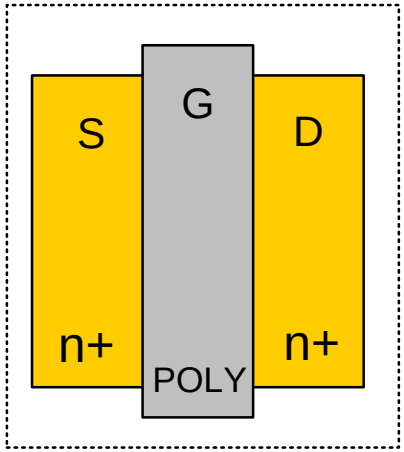
poly-Si GATE is used as a mask to define the SOURCE/DRAIN regions



l) Source/drain pMOS implant

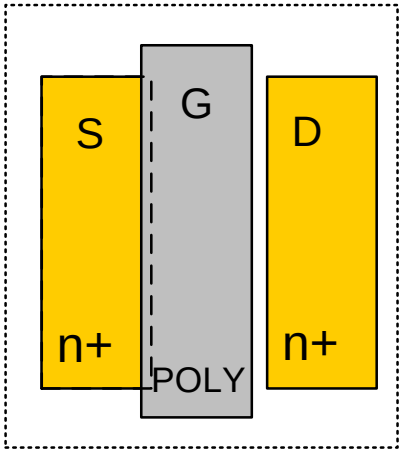
Source/Drain Self-Alignment

1. Perfect Alignment



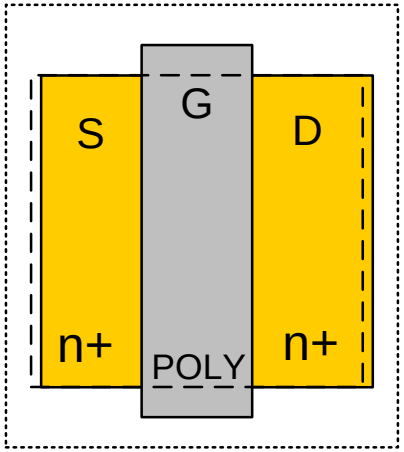
NMOS

2. Misalignment (no self-alignment)



NMOS

3. Misalignment (self-alignment)



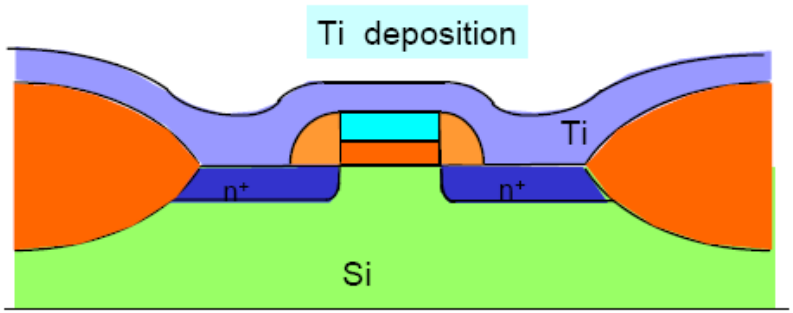
NMOS

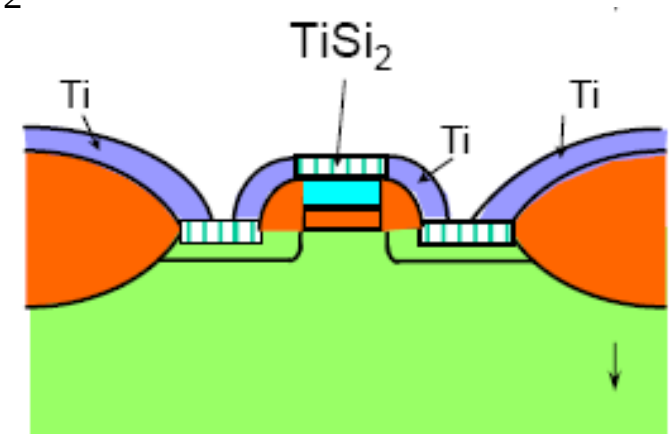
In case of mask alignment error, if source, drain and gate are drawn independently, the device may non work at all (case 2.).

If source/drain are implanted/diffused using the gate as a mask, self-alignment occurs and any mask misalignment has minimal influence

Self-aligned silicide (salicide)

$$Ti + 2Si \rightarrow TiSi_2$$



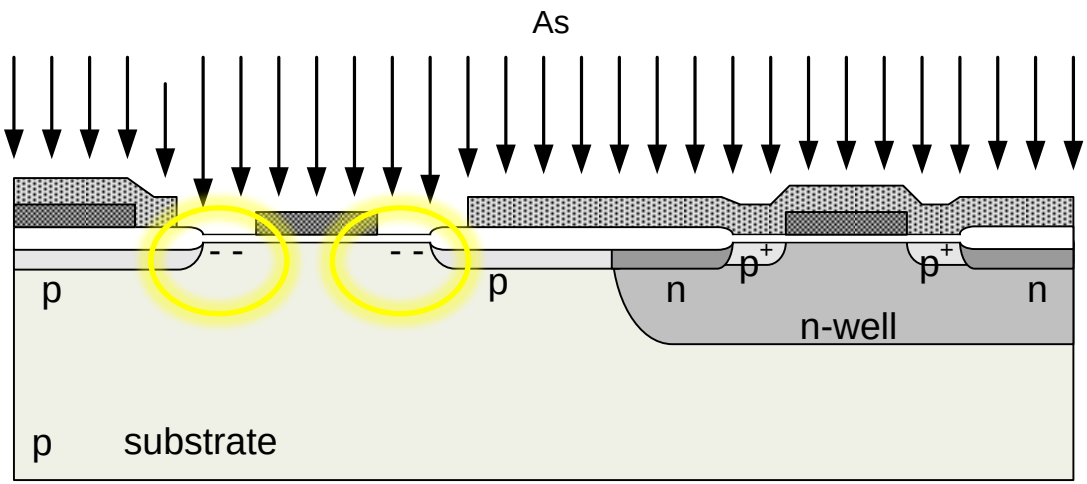


Ti reacts with Si to form Ti-silicide.

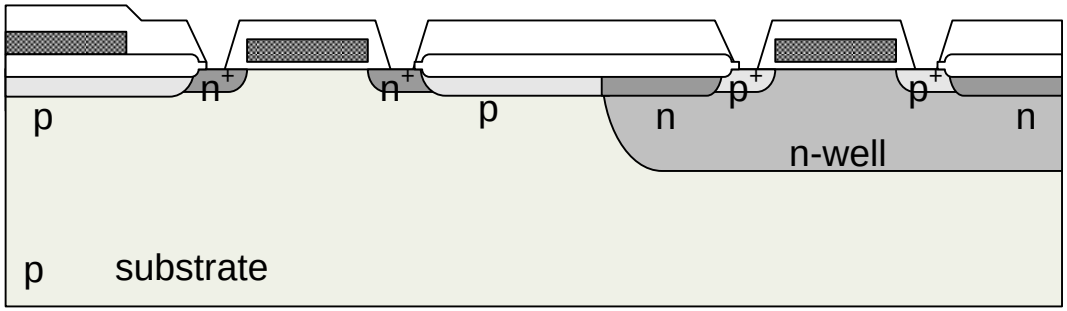
Ti then removed by selective chemical etching.

- Poly with silicide ($TiSi_2$) has much lower sheet resistance
  - P+poly Rsh with silicide 10Ω/sq
  - P+poly Rsh without silicide 400Ω/sq
- The same is true for substrate and Si diffused regions
  - P+diff.with silicide 10Ω/sq
  - P+diff.without silicide 150Ω/sq

CMOS Process Flow (8)

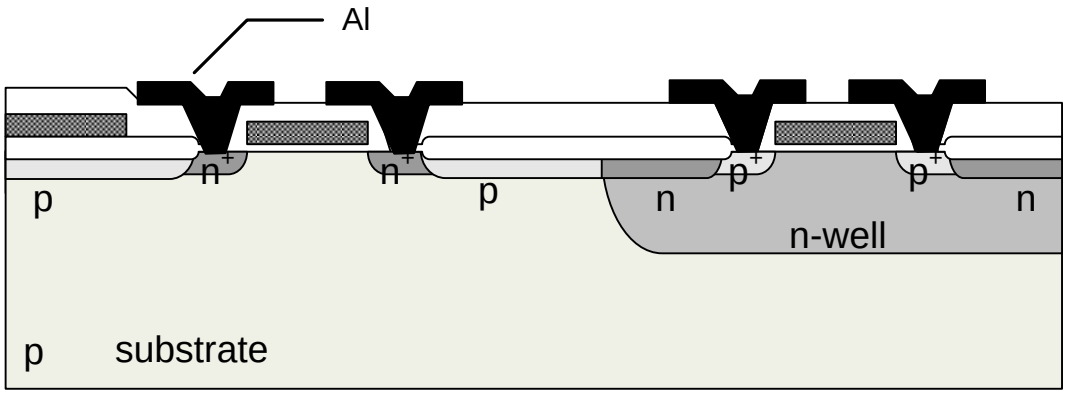


m) Source/drain nMOS implant

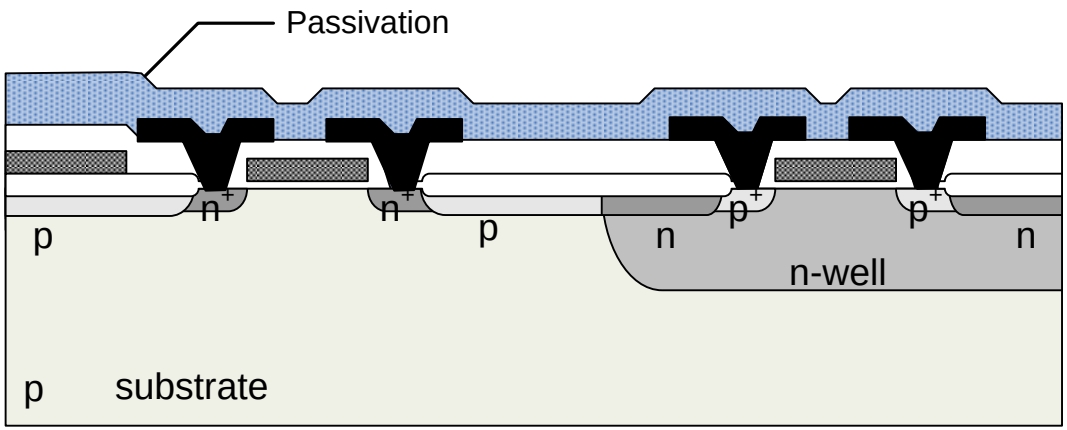


n) Inter-layer oxide <u>deposition</u> and via opening

CMOS Process Flow (9)

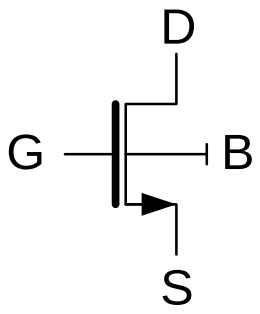


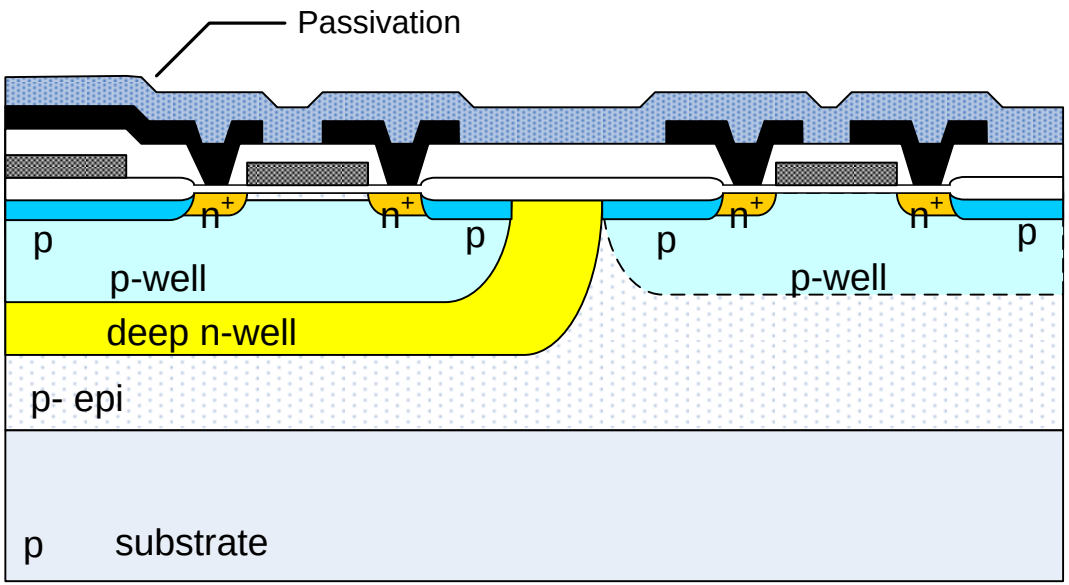
o) Al deposition



p) Passivation and <u>pad opening</u>

Triple-well Process



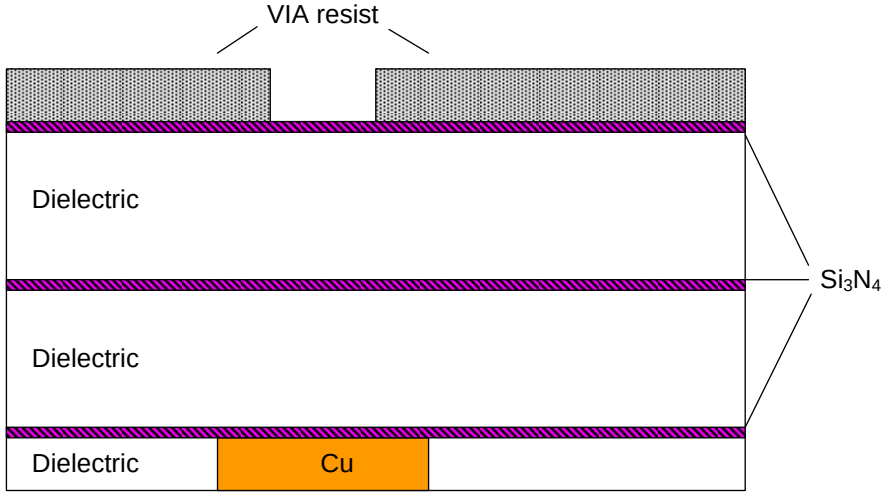


A triple-well process allows to define a different bulk terminal for NMOS devices built in different p-wells.

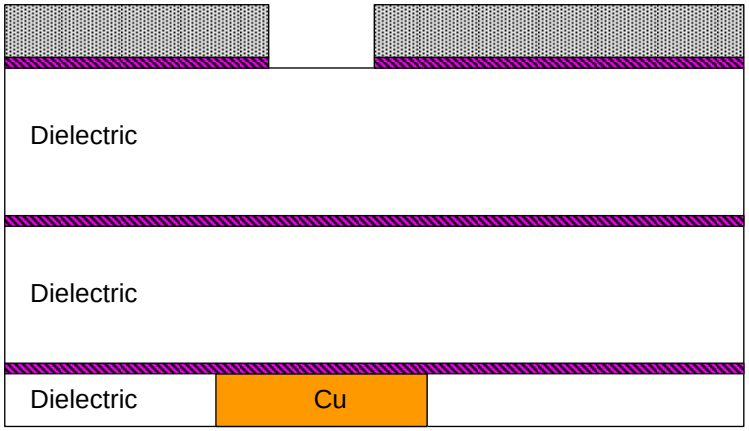
Advantages:

- Improved isolation
- Bulk node can be biased at voltages above GND (reduced bulk effect)

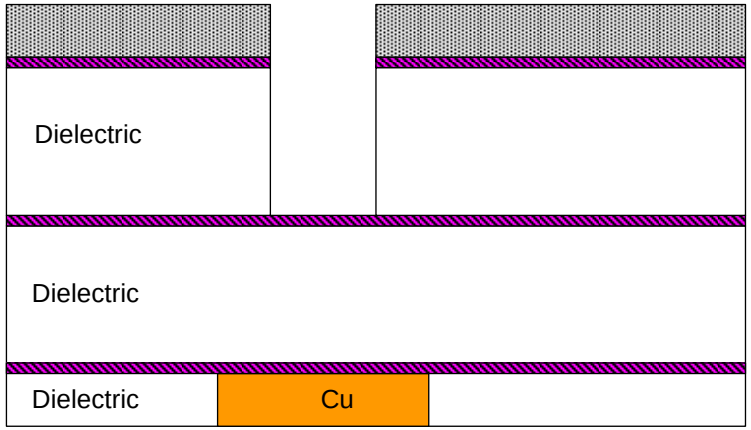
Dual Damascene Process



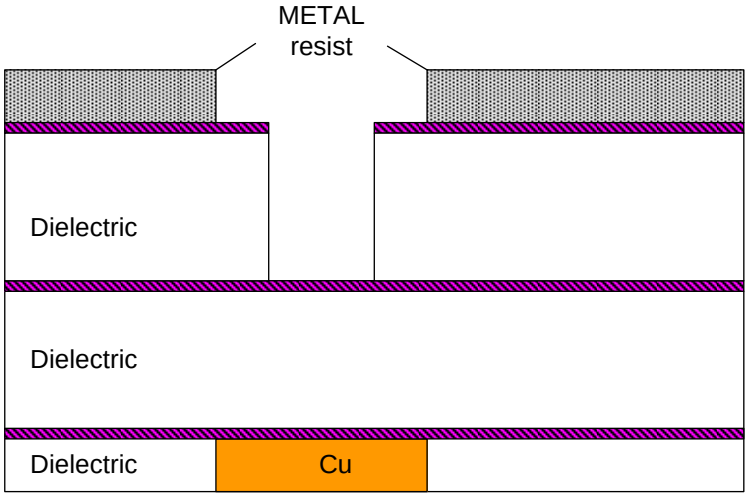
a) VIA resist deposition and definition



b) Etch stop definition

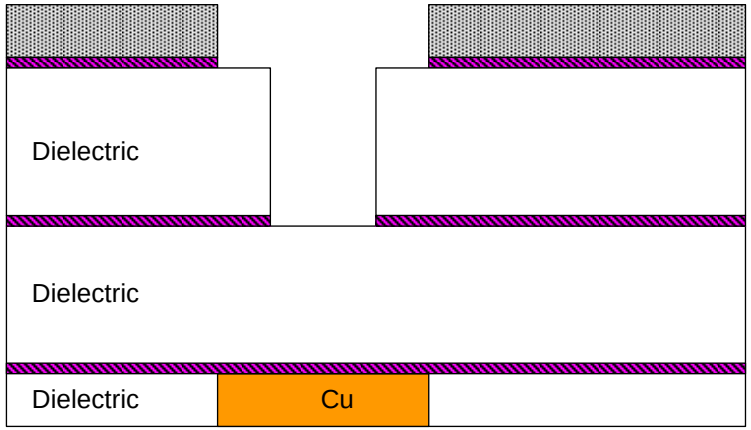


c) Dielectric etching

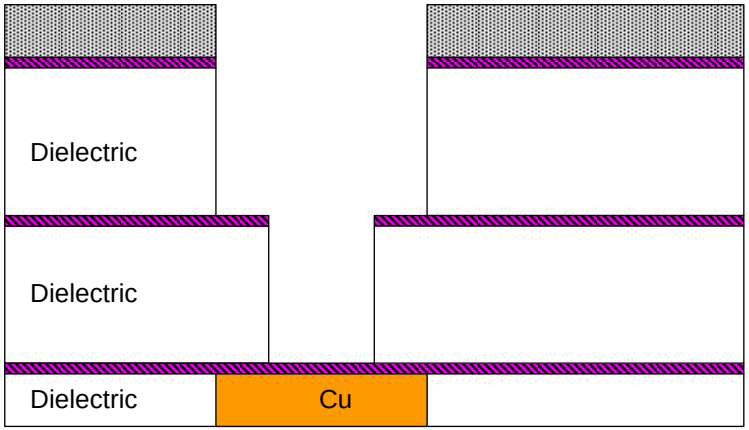


d) METAL resist deposition and definition

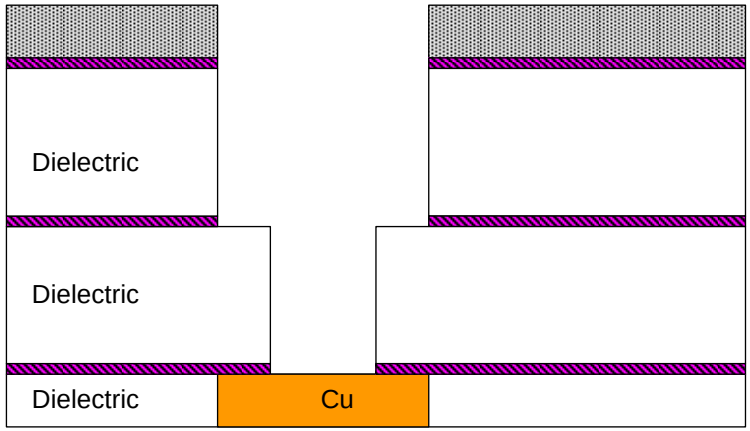
Dual Damascene Process (2)



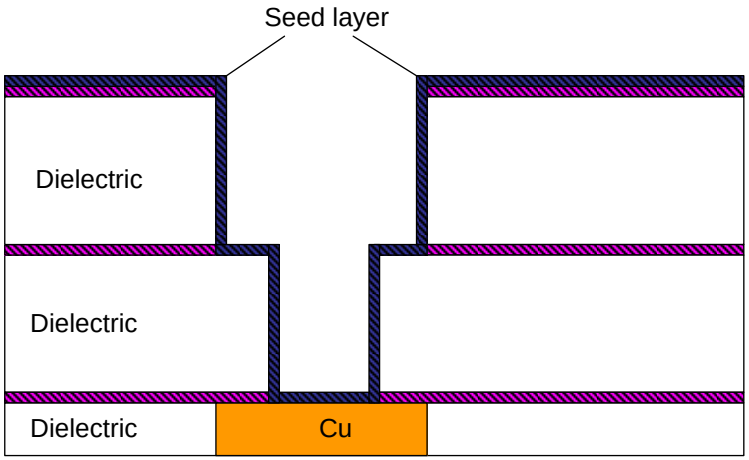
e) Etch stop definition



f) Dielectric etching

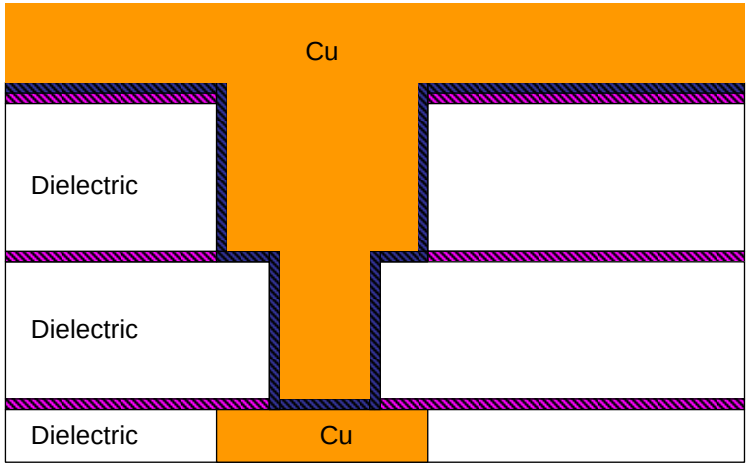


g) Etch stop definition

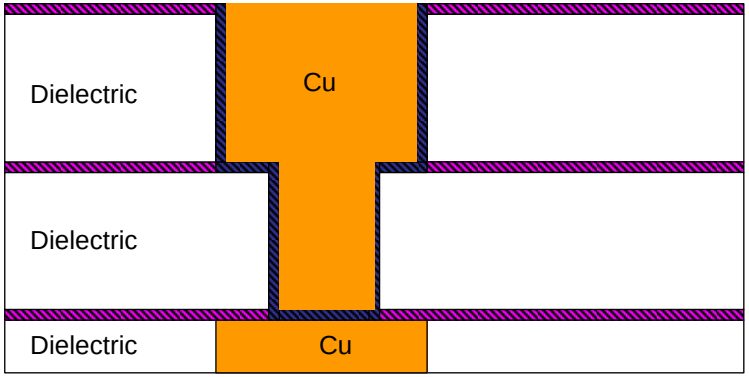


h) Seed layer deposition

Dual Damascene Process (3)



i)



j)

a) VIA resist deposition and definition

b) Etch stop definition

c) Dielectric etching

d) METAL resist deposition and definition

e) Etch stop definition

f) Dielectric etching

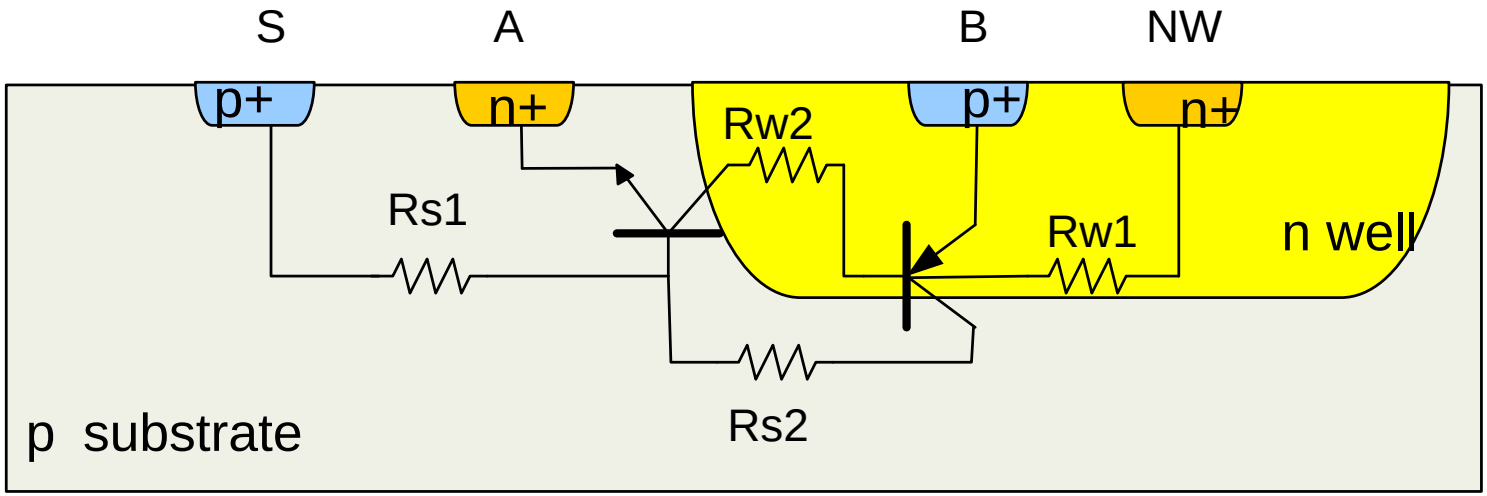
g) Etch stop definition

h) Seed layer deposition

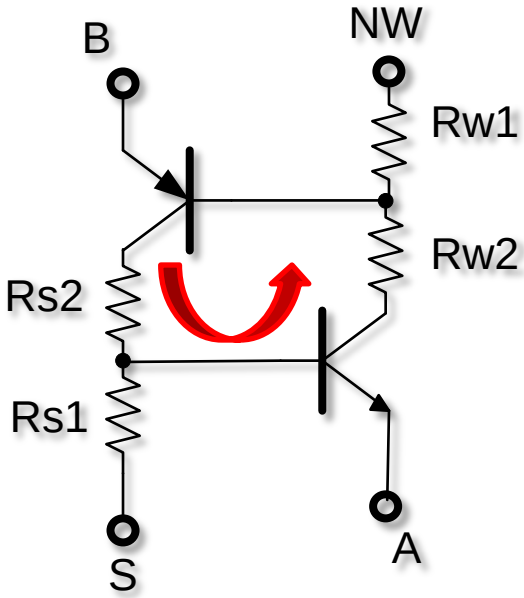
i) Cu deposition

j) CMP

Latch-up



Positive feedback loop!



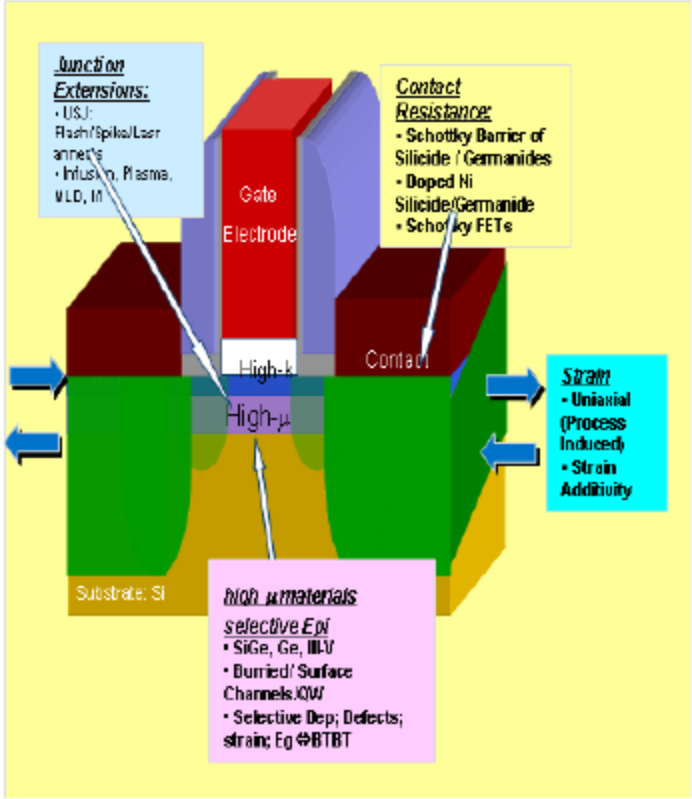
Latch-up prevention:

Rs1, Rw1 as small as possible

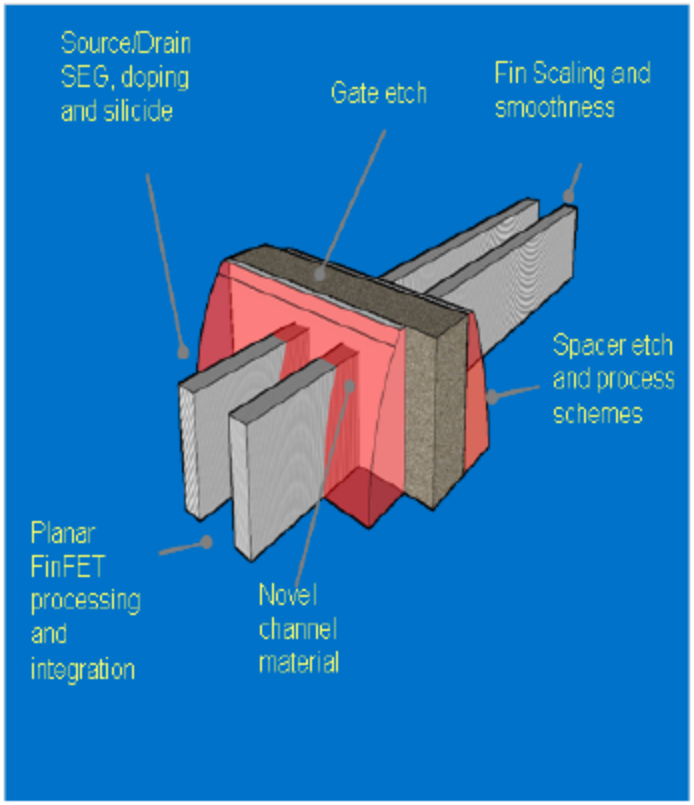
- Low substrate resistivity (high doping)
- Bulk contact close to active devices

The MOS of the Future

Planar



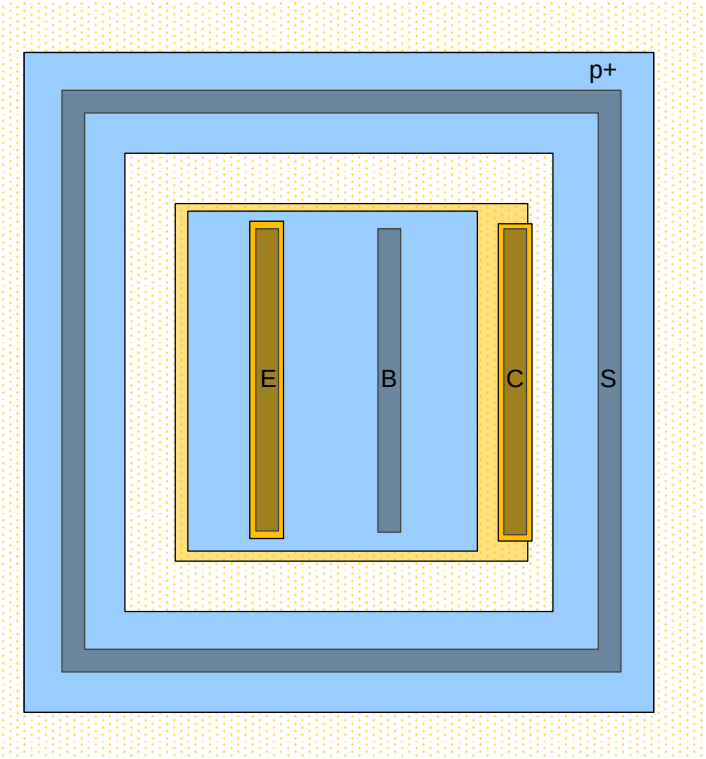
Non-Planar



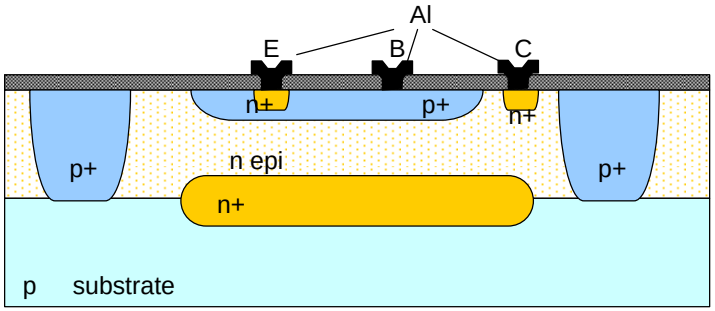
Bipolar Technologies

Standard Buried Collector

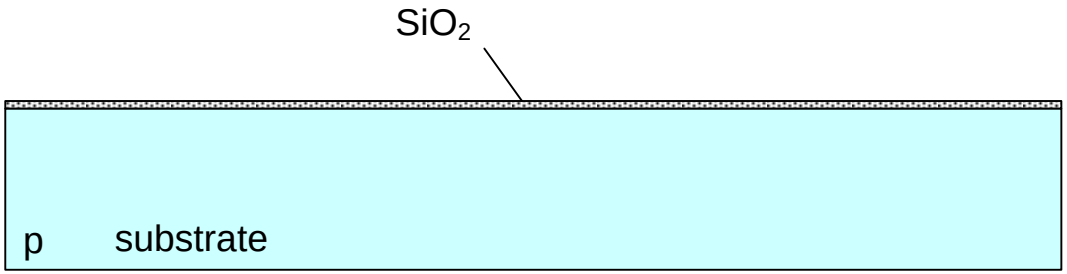
TOP VIEW



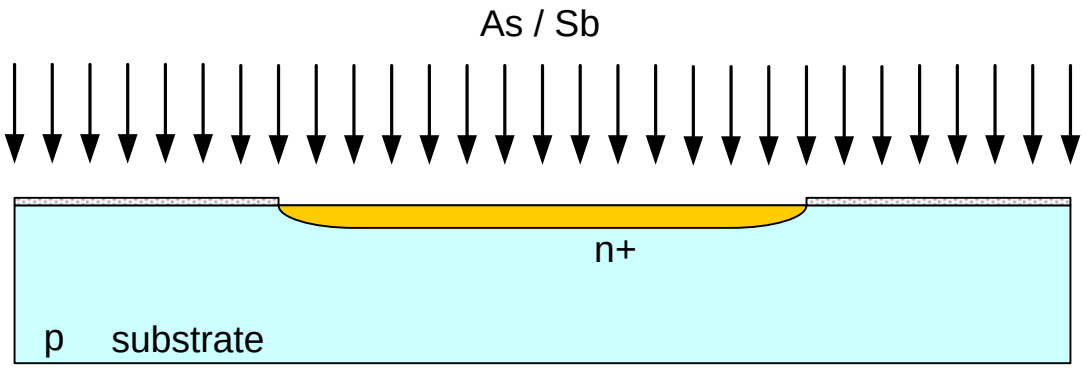
CROSS SECTION



Bipolar Process Flow



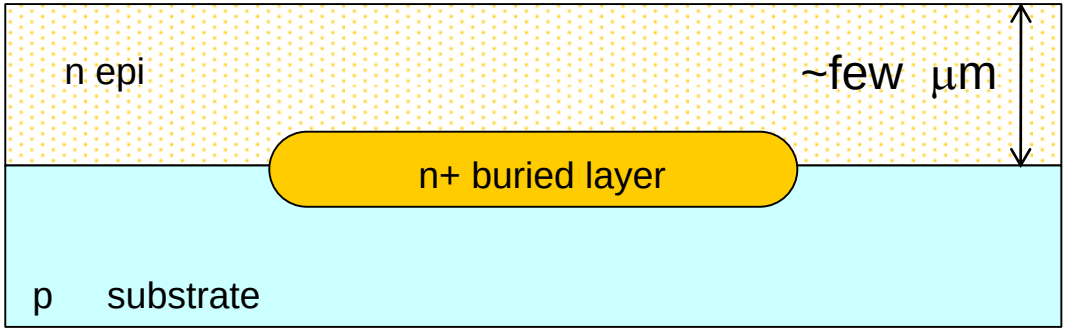
a) Thermal oxidation



b) Buried layer deposition

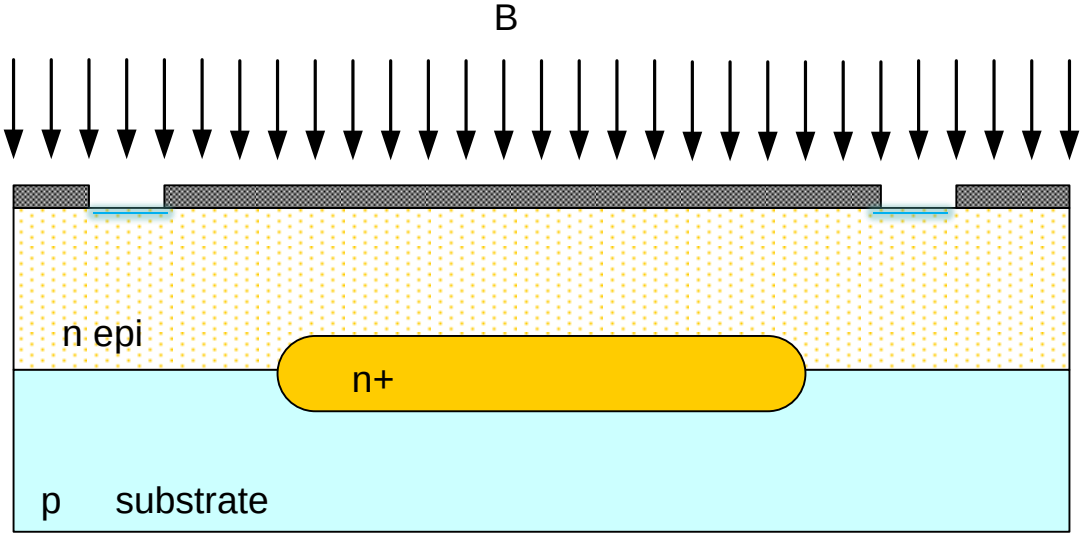
The buried layer is used to provide a low impedance path for the collector current from the active collector area to the collector contact.

Bipolar Process Flow (2)



c) N-epi growth

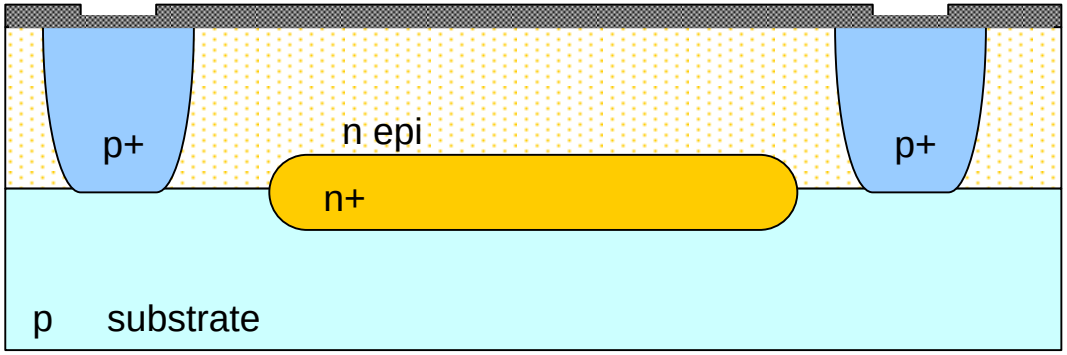
The epitaxial layer thickness and resistivity vary: large thickness (~10μm) and resistivity (>10Ωcm)) are required for high voltage/power applications



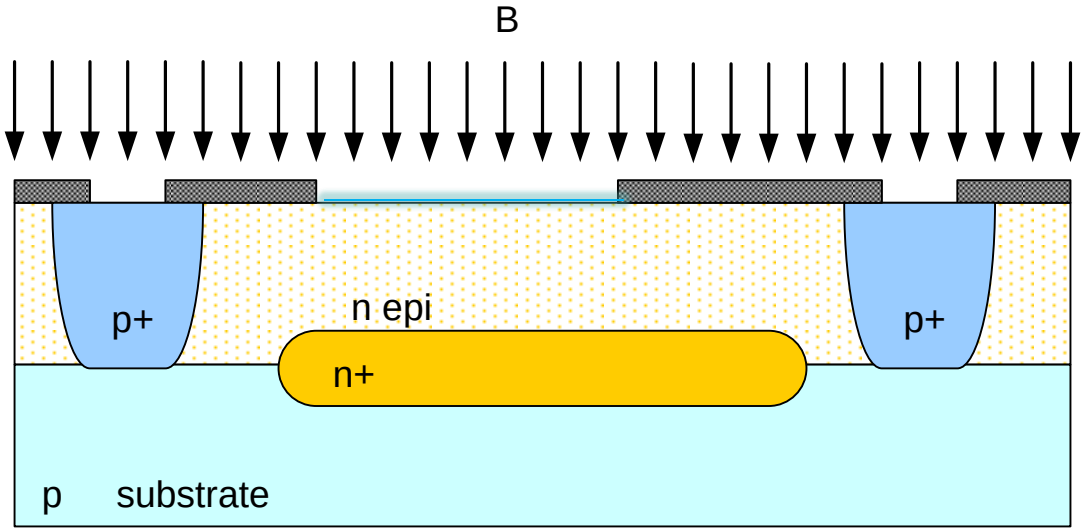
d) P-well *isolation* definition

Bipolar Process Flow (3)

Isolation diffusions require long time (hours) and high temperatures (1200°C)

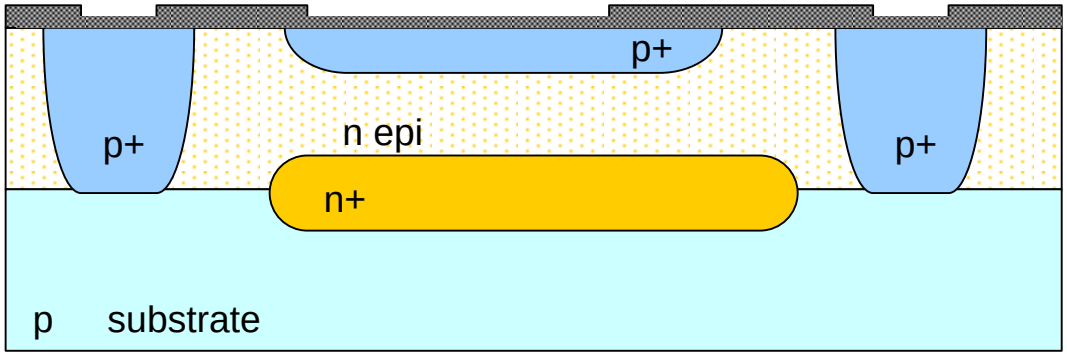


e) Isolation diffusion

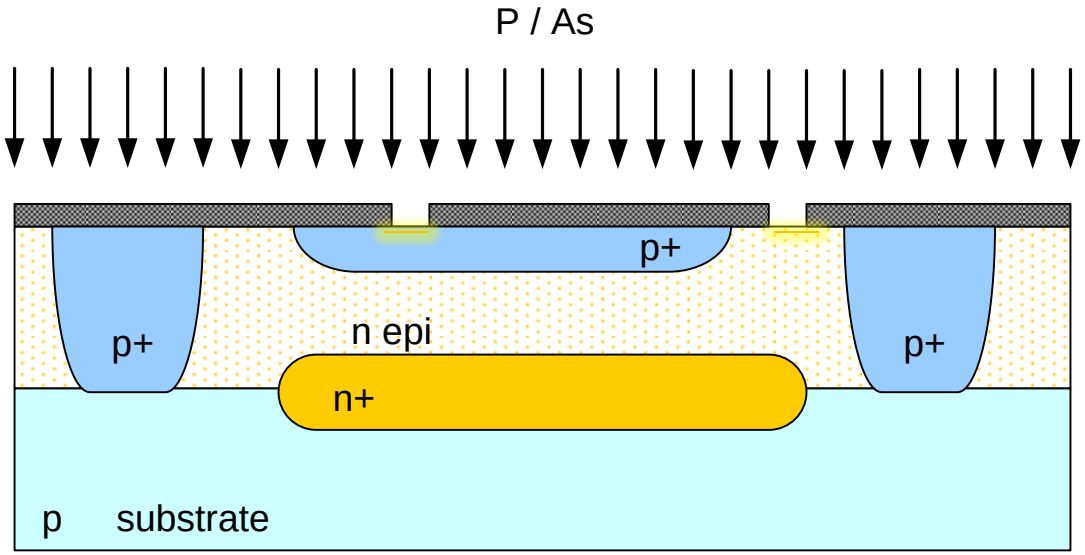


f) base region definition and implant

Bipolar Process Flow (4)

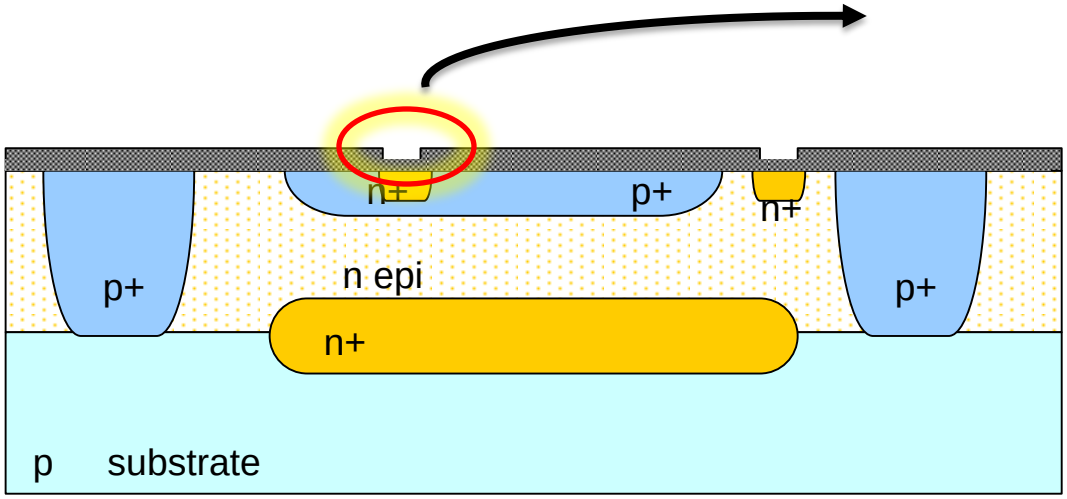


g) Base diffusion (drive-in)



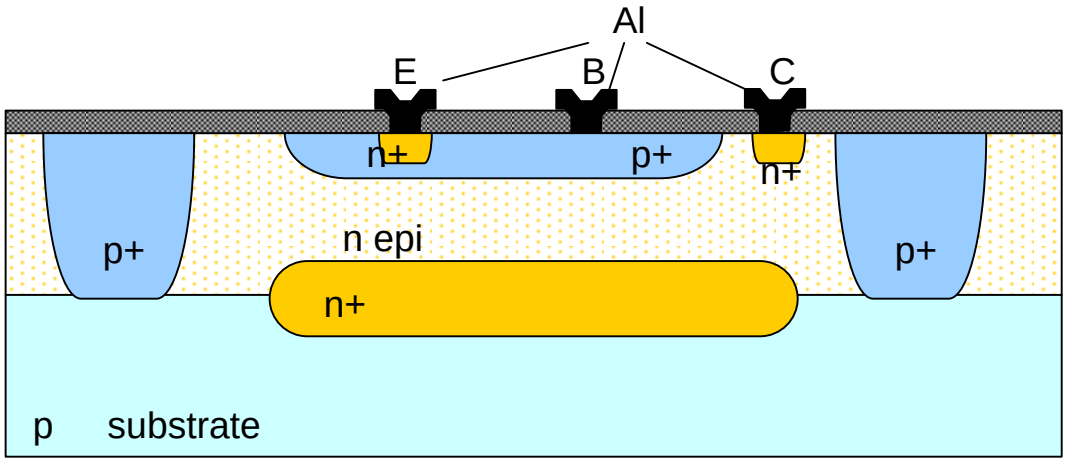
h) Emitter/collector definition and implant

Bipolar Process Flow (5)



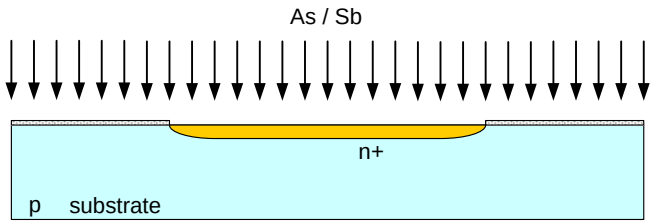
The transistor base width depends on the difference of the base and emitter diffusion depths. Transistor's f_T is inversely proportional to base width.

i) Emitter/collector diffusion (drive-in)

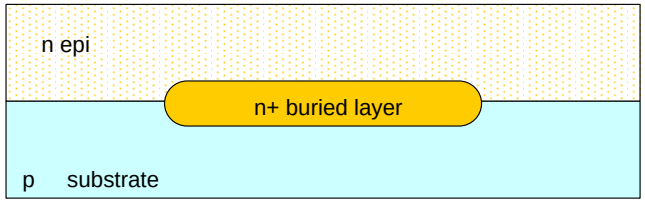


j) Contact opening and metal deposition

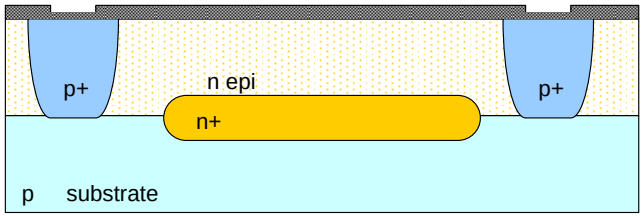
Bipolar Process Flow - Summary



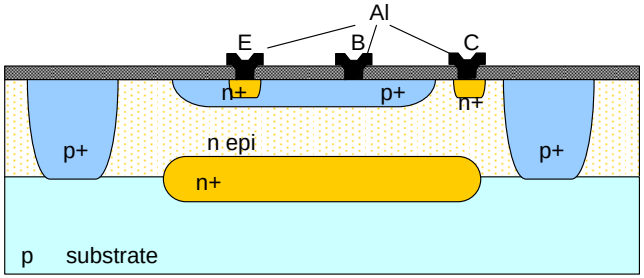
b)



c)



d)



j)

a) Thermal oxidation

b) Buried layer deposition

c) N-epi growth

d) P-well isolation definition

e) Isolation diffusion

f) Base definition and implant

g) Base diffusion (drive-in)

h) Emitter/collector definition and implant

i) Emitter/collector diffusion (drive-in)

j) Contact opening and metal deposition

References

- Reading Material:
  - Dispense di G. Torelli. Introduzione alla tecnologia dei circuiti integrati su silicio. 2006. (IC Technologies)
  - Dispense del corso *Microfabrication Technology*, UCB http://organics.eecs.berkeley.edu/~viveks/ee143/