AA 2012/2013

Lezioni di Tecnologie e Materiali per l'Elettronica

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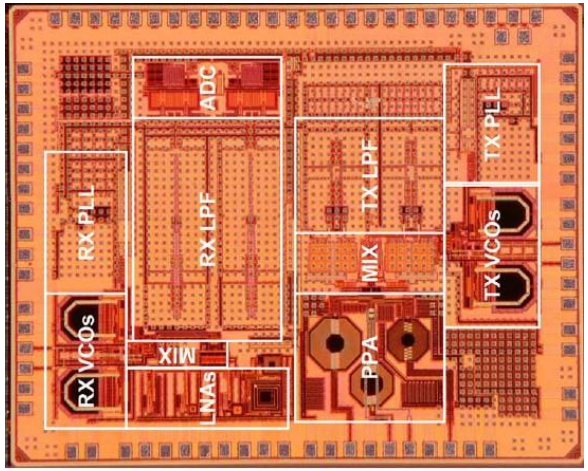
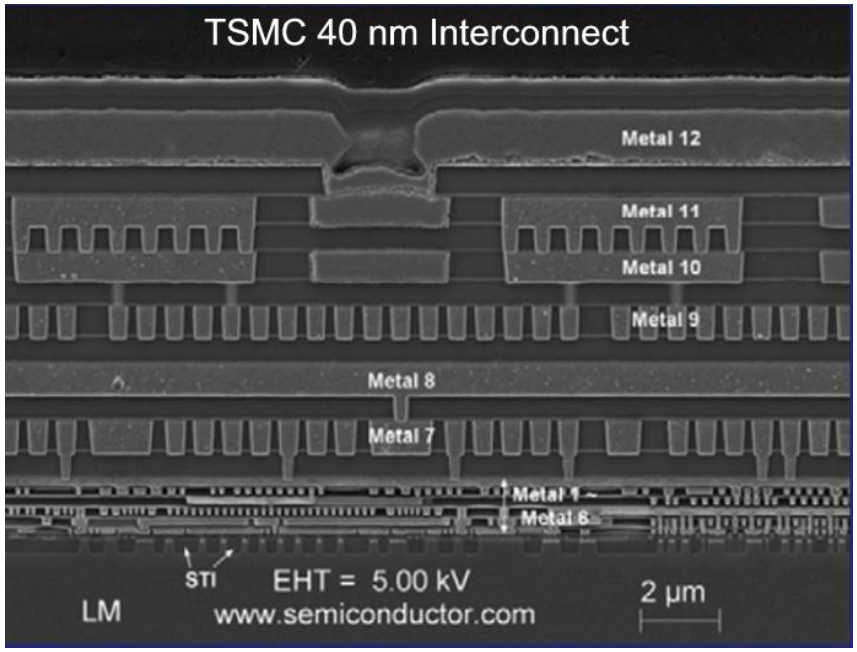
Outline



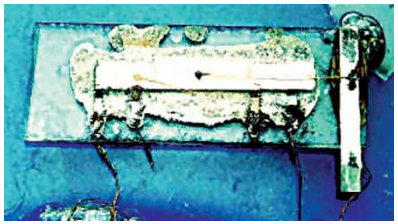


- **Passive components**
  - Resistors
  - Capacitors
  - Inductors
- **Printed circuits technologies**
  - Materials and fabrication steps
  - Assembling
- **Monolithic IC technologies**
  - Fabrication steps (thermal oxidation, thermal diffusion, …)
  - IC technologies (CMOS, BiCMOS)
  - Packaging and Thermal Design

Semiconductor Technologies

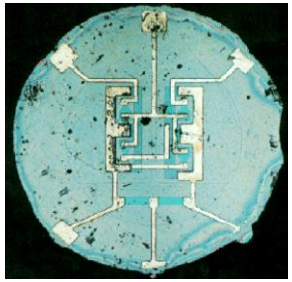
- Point-contact Ge transistor, 1948

J. Bardeen, W. Brattain, W. Shockley (Bell Labs)



- Integrated Circuit, 1958

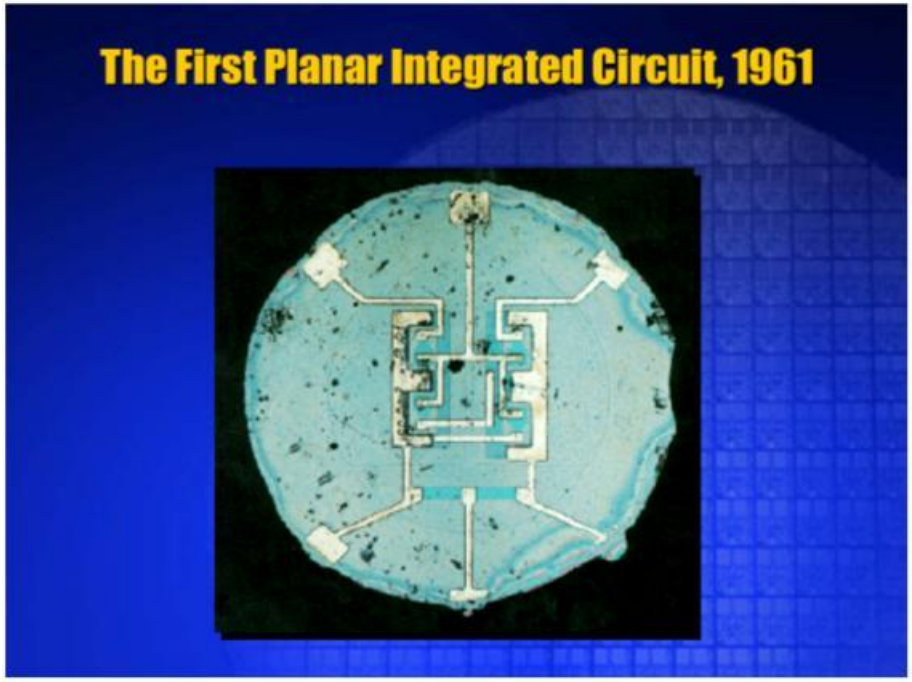
J. Kilby (Texas Instruments)



- Silicon Integrated Circuit, 1961

R. Noyce (Fairchild Semiconductor)

Planar IC Technologies

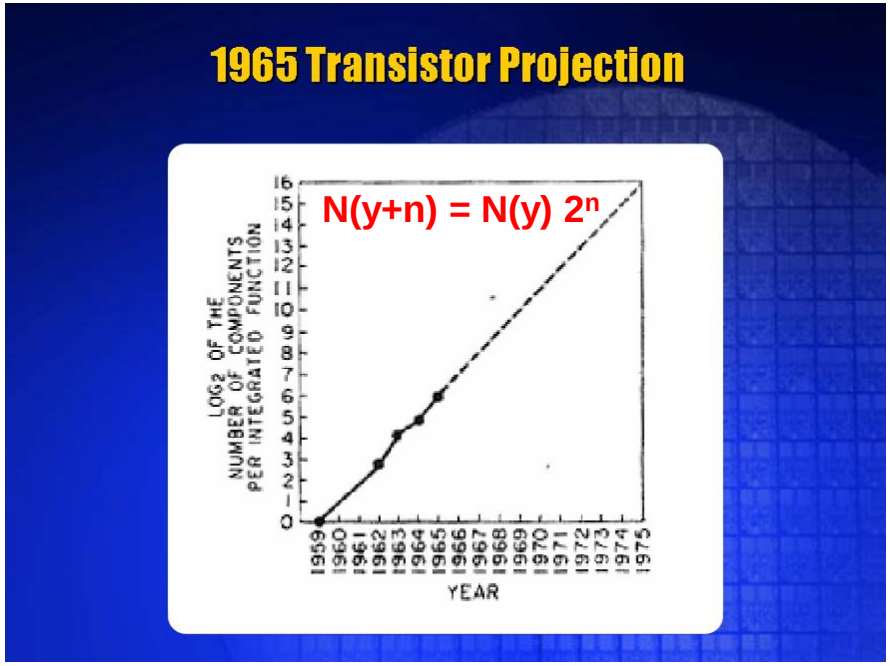


Jack Kilby and Texas Instruments received U.S. patent #3,138,743 for miniaturized electronic circuits.

Robert Noyce and the Fairchild Semiconductor Corporation received U.S. patent #2,981,877 for a silicon based integrated circuit.

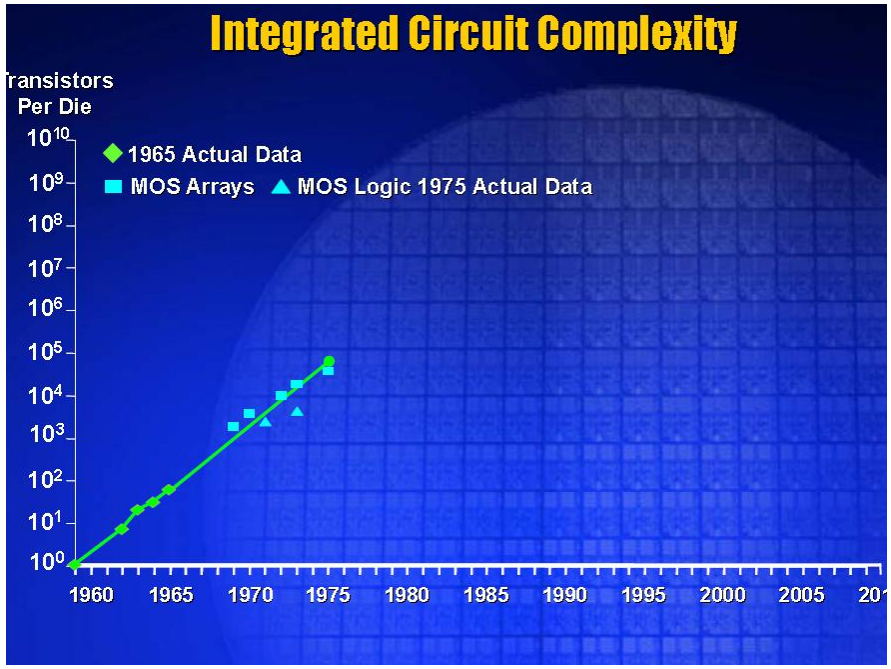
Moore Law (1965)

G. Moore prediction, 1965



Annual doubling

Actual data

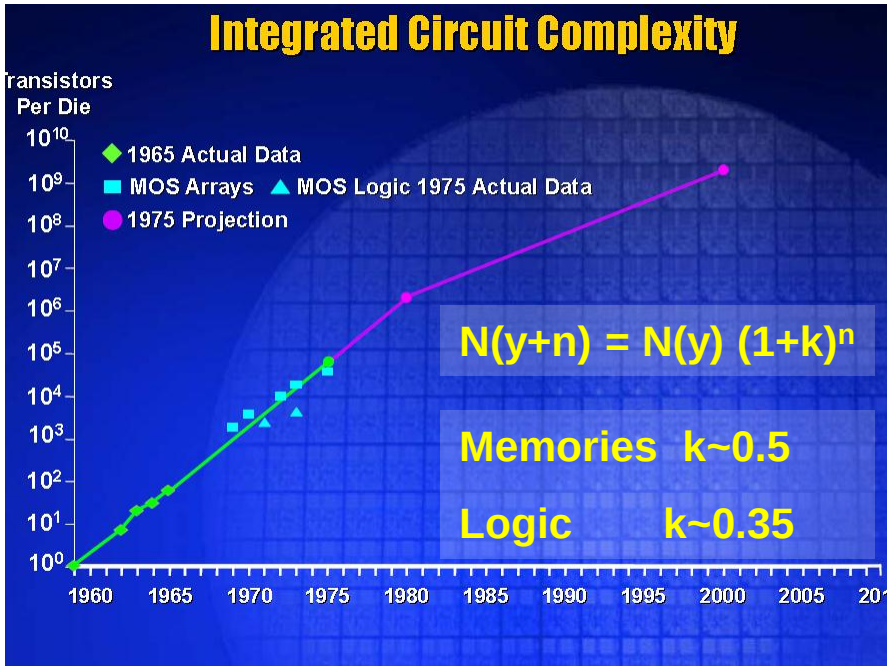


Complexity (measured as number of transistors) of the most complex ICs

G. Moore, Plenary talk, ISSCC 2003

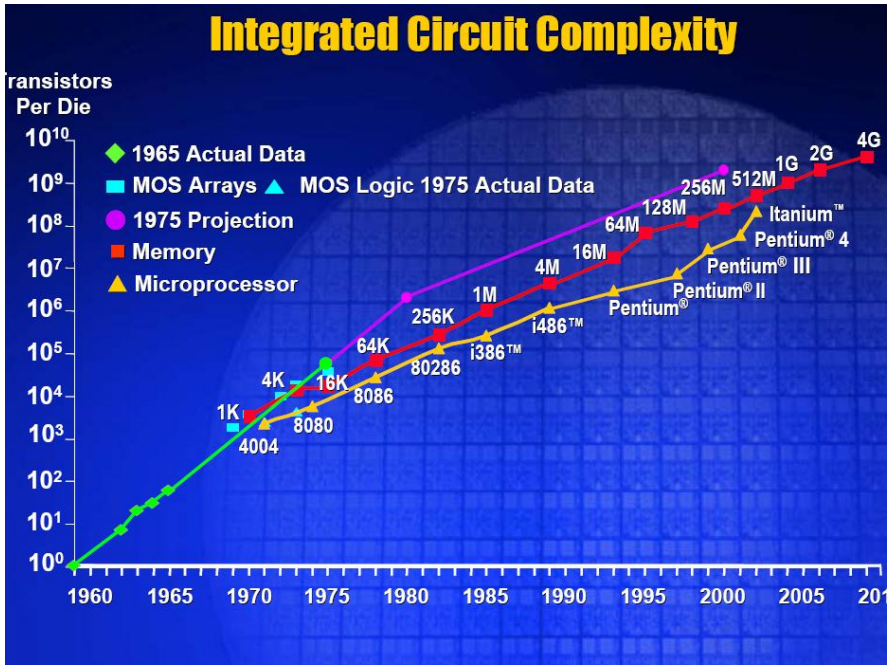
Moore Law (1975)

G. Moore prediction, 1975



Two-year doubling

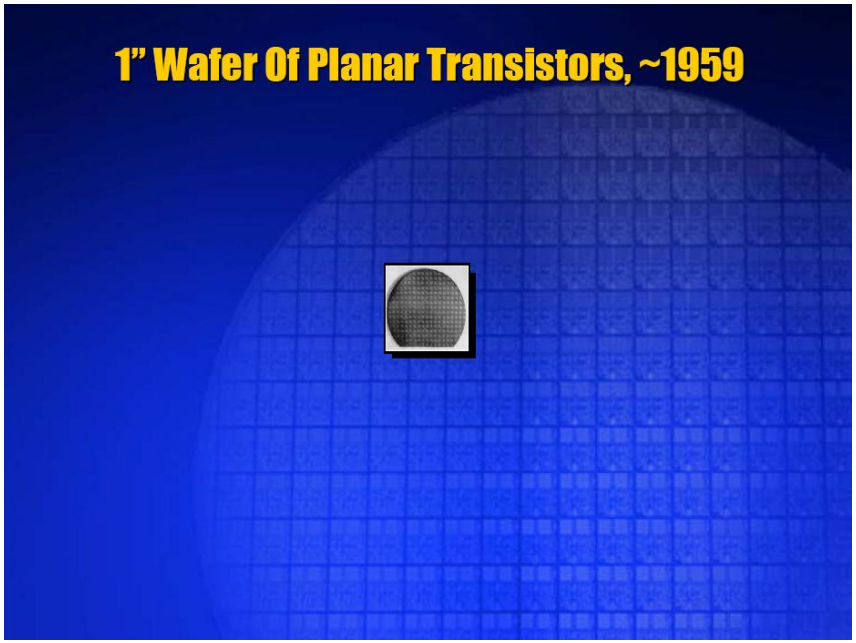
Actual data

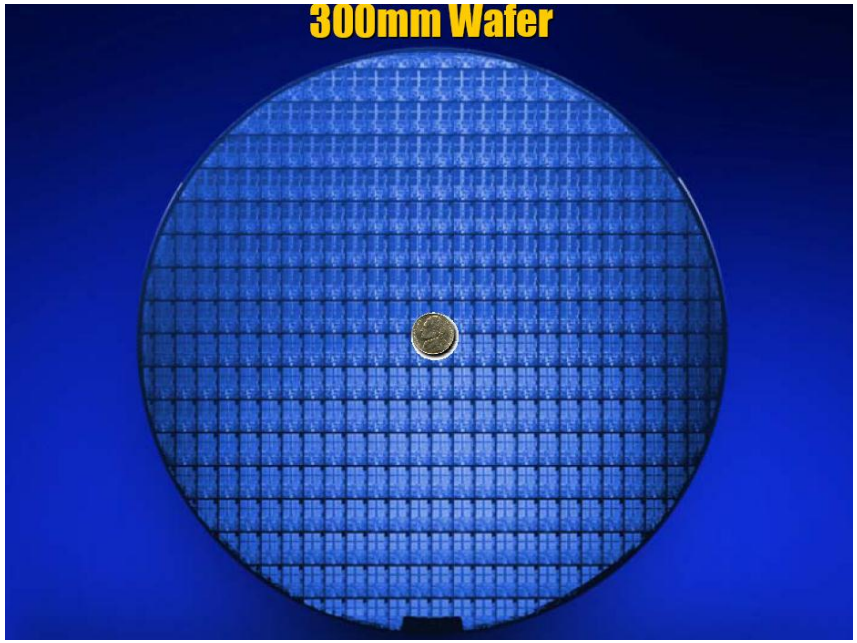


Complexity (measured as number of transistors) of the most complex ICs

G. Moore, Plenary talk, ISSCC 2003

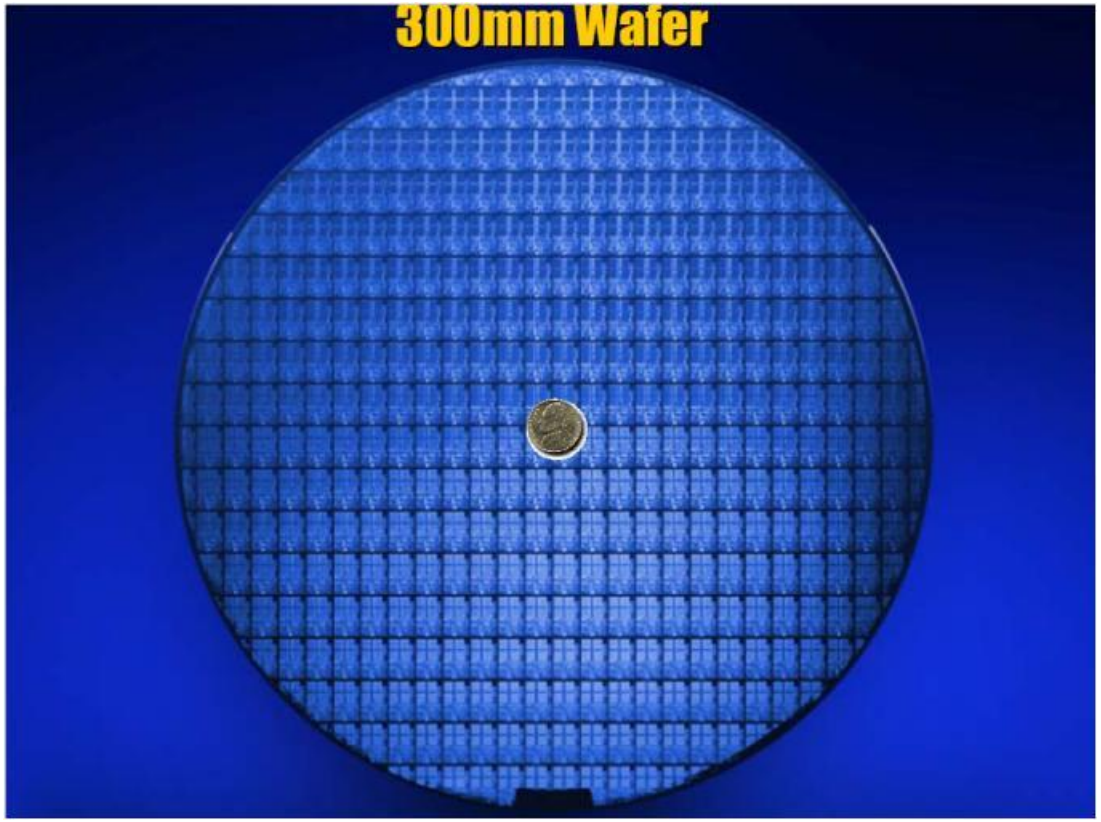
Wafer Size





How many transistors can we process together?

Batch Processing



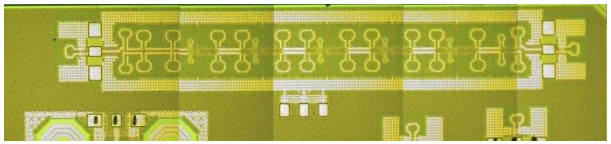
- 12 inches wafer ~ 700cm^2
- 50 wafer shuttle contains ~ 35000 dice

Introduction to IC Technologies

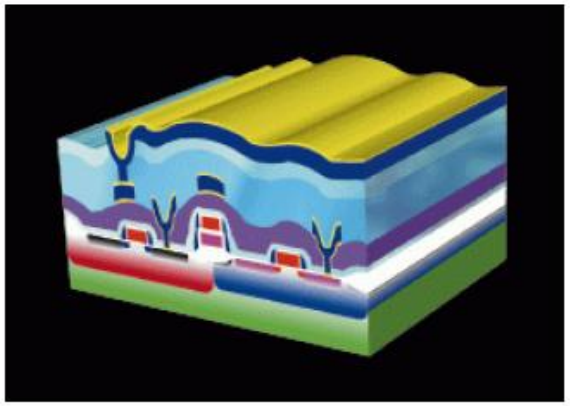
- Semiconductor materials
- Wafer fabrication process
- Production steps:
  - Thermal oxidation
  - Thermal diffusion
  - Ion implantation
  - Thin film deposition
  - Epitaxial growth
  - Lithography
- MOS transistors
- Bipolar transistors

Integrated Circuit
(Physical layout)

Integrated Circuit
(Die photograph)

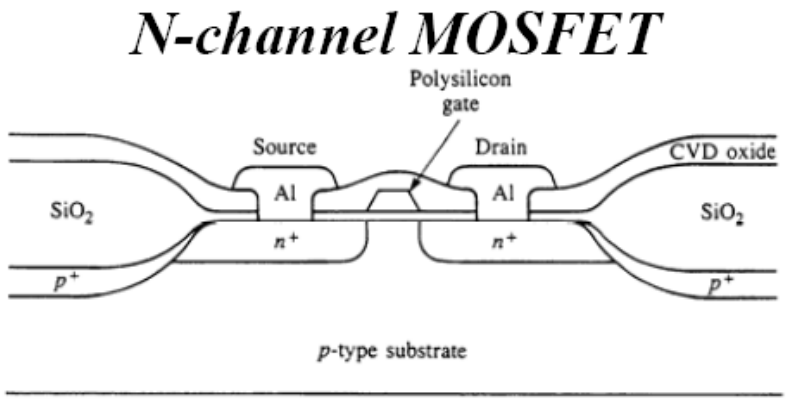


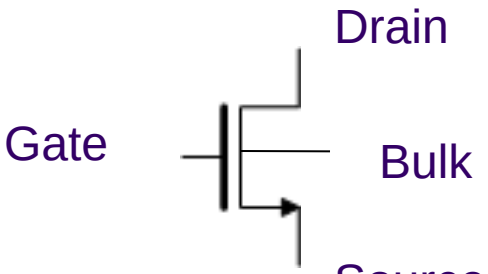
Processing
Steps



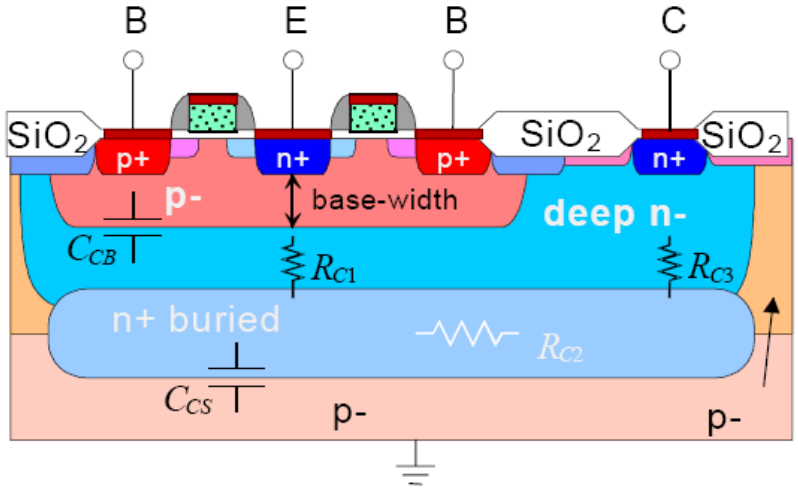
Active Devices

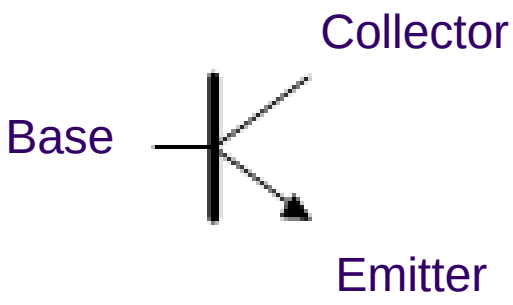
CMOS Technology





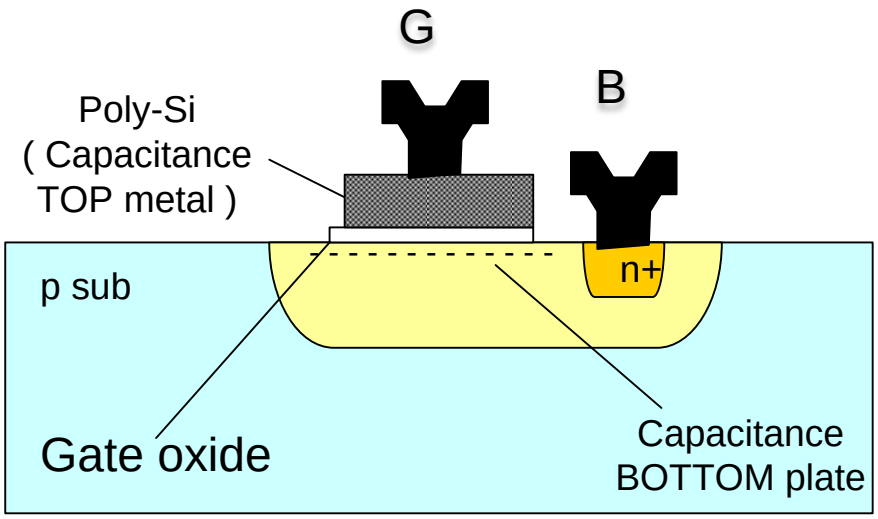
Bipolar Technology



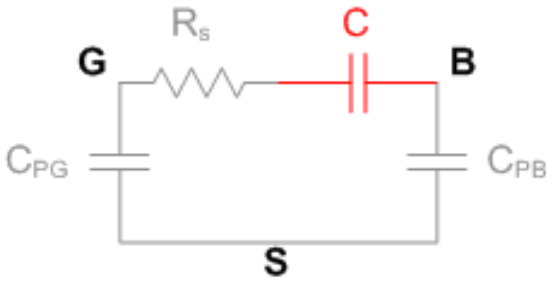


MOS Capacitance

Physical Layout
(Cross section)



Equivalent Circuit

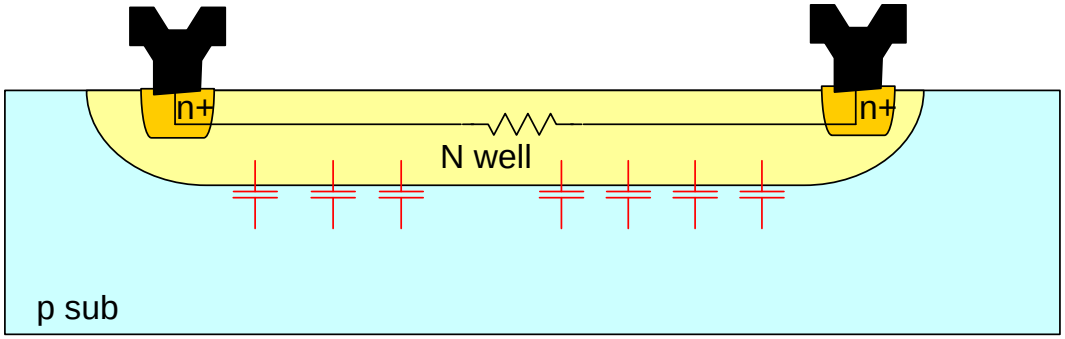


$$C = C_{ox} WL$$

Resistors

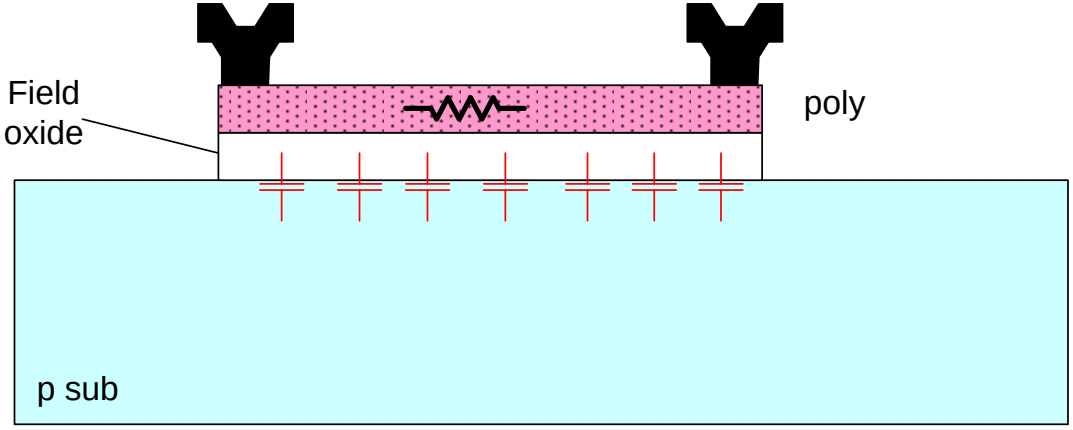
Well resistors

- ~200Ω/sq sheet resistance
- High parasitic capacitance
- Non-linear resistance

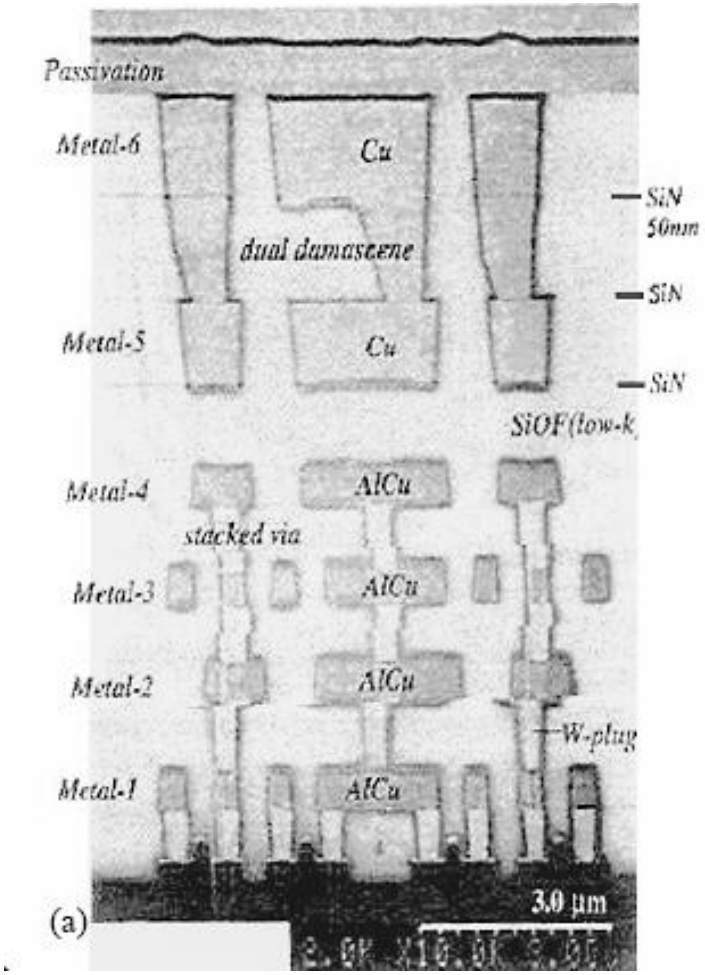


Poly resistors

- ~200Ω/sq sheet resistance
- Linear resistance



Technology Cross-Section



- Metal stack in a recent CMOS technology
- Cu and Al interconnect
- Inter-layer VIA holes

$$\varepsilon_{ox} = 3.45 \cdot 10^{-11} F/m$$

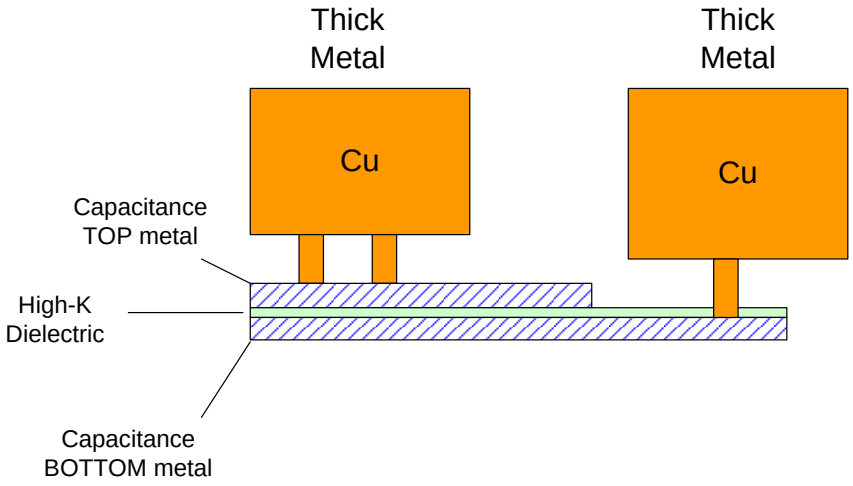
$$\varepsilon_{o} = 8.85 \cdot 10^{-12} F/m$$

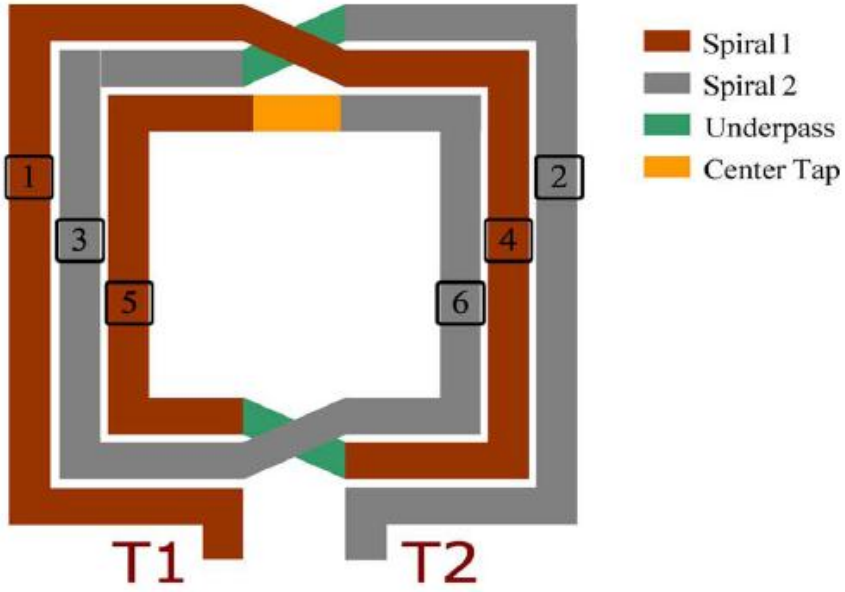
$$\varepsilon_{Si} = 1.04 \cdot 10^{-10} F/m$$

$$\sigma_{Cu} = 5.7 \cdot 10^{7} S/m$$

$$\mu \approx 5 \cdot 10^{10} \mu m^2/Vs$$

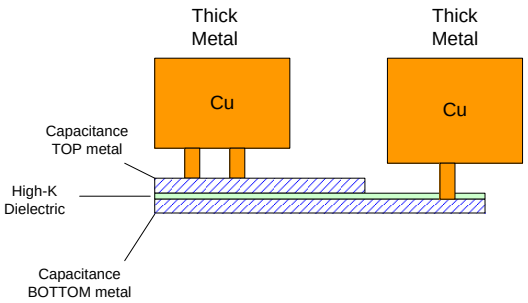
Passive Devices



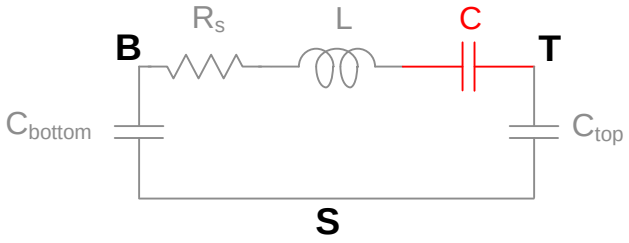


- Metal-Insulator-Metal (MiM) capacitor (C_u~2-5fF/μm^2)
- Center-Tapped Inductor inductance < ~15nH)

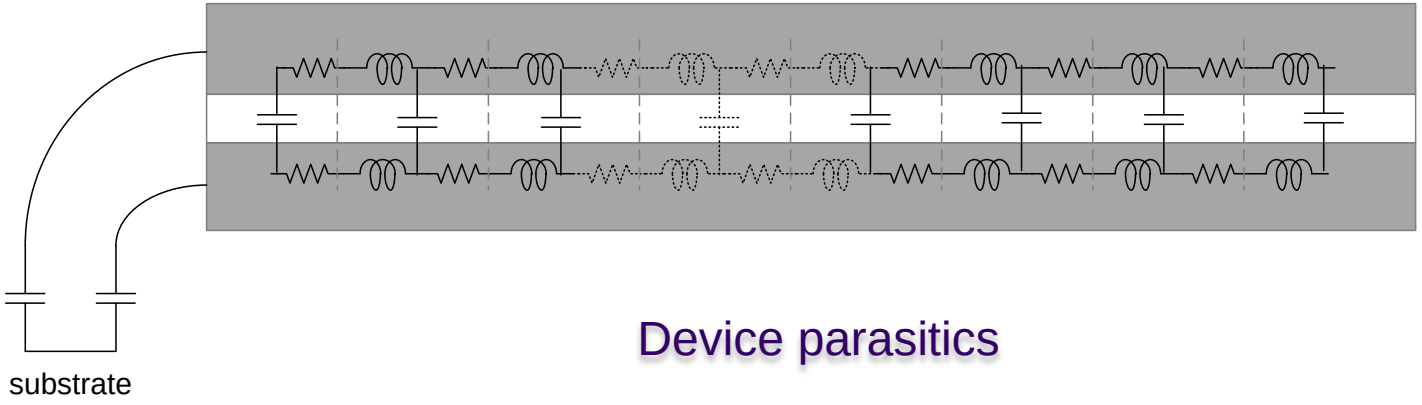
MiM Capacitors



MiM capacitor
Physical layout
(cross section)



Equivalent circuit

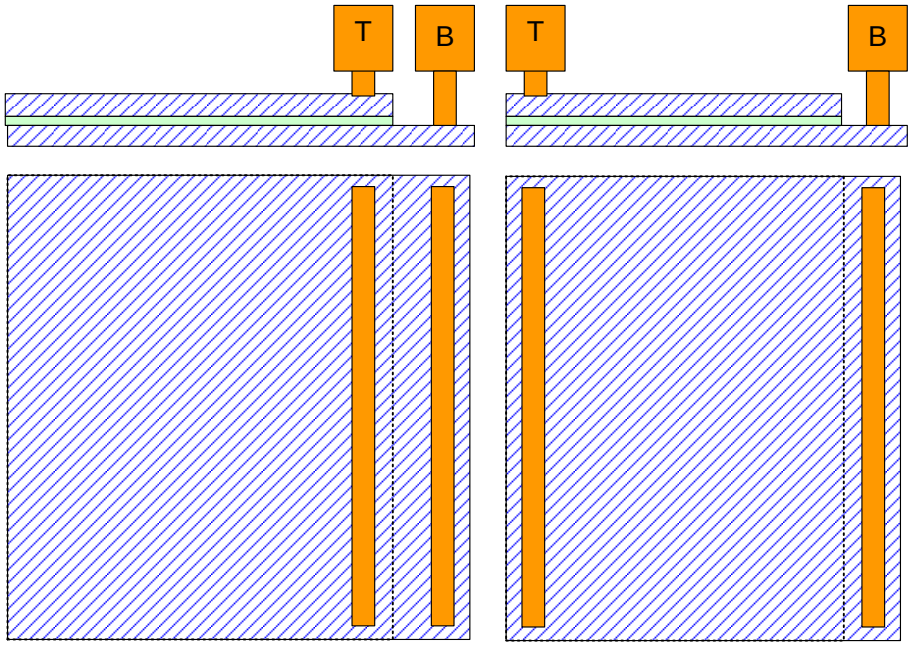


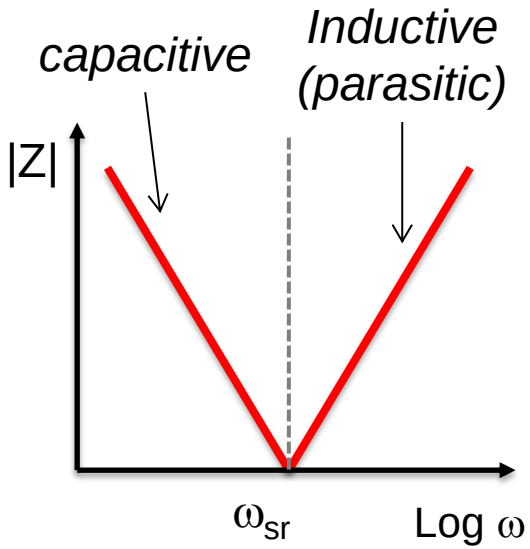
Device parasitics

MiM Caps: Self-Resonance

CROSS SECTION

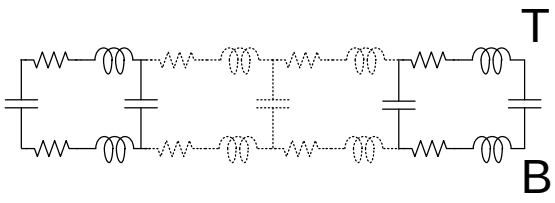
TOP VIEW

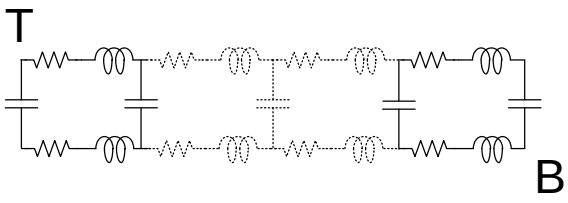




HIGHER SELF-RESONANCE FREQUENCY

LOWER SELF-RESONANCE FREQUENCY





MOSFET Operation

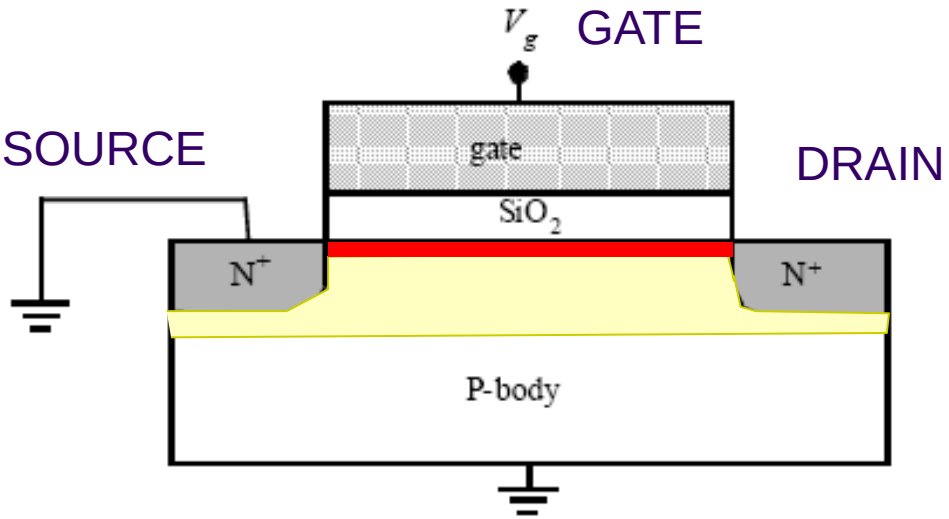
$$I_D = \frac{W}{L}\mu_n C_{ox}\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}}{2}\right]$$

$$\phi_B = \frac{KT}{q}\ln\left(\frac{N_A}{n_i}\right)$$

$$V_{TH} = V_{FB} + 2\phi_B + \frac{\sqrt{4qN_A\varepsilon_S\phi_B}}{C_{ox}}$$

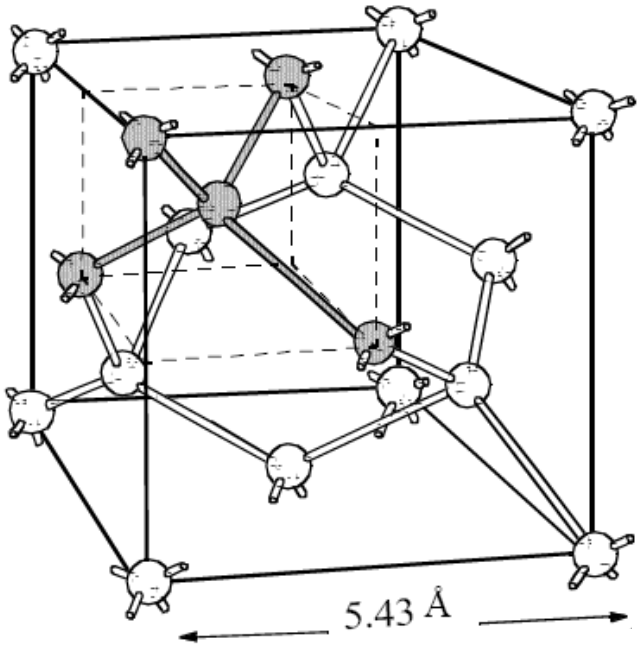
$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$C_{gs}\Big|_{Vds=0} = C_{ox}WL$$

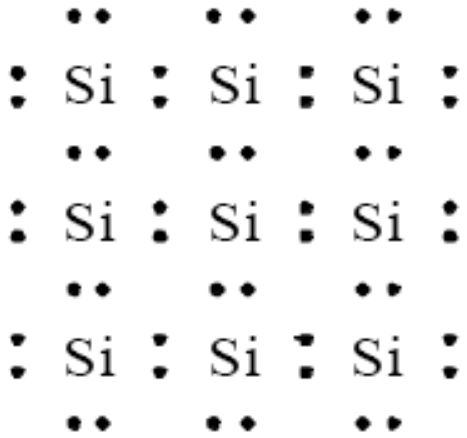


n_i=1.45 10^{10} cm^{-3} at 300K

Monolithic Silicon



Silicon



Properties at 300K

- R_a 1,18Å
- ε_r 11,7 (SiO_2 ε_r 3,9)
- E_g 1,12eV
- T_f 1412°C
- σ_{TH} 1,5 W/Kcm

Si Atomic density: $5 \cdot 10^{22}$ cm^{-3}

Mobility and Conductivity

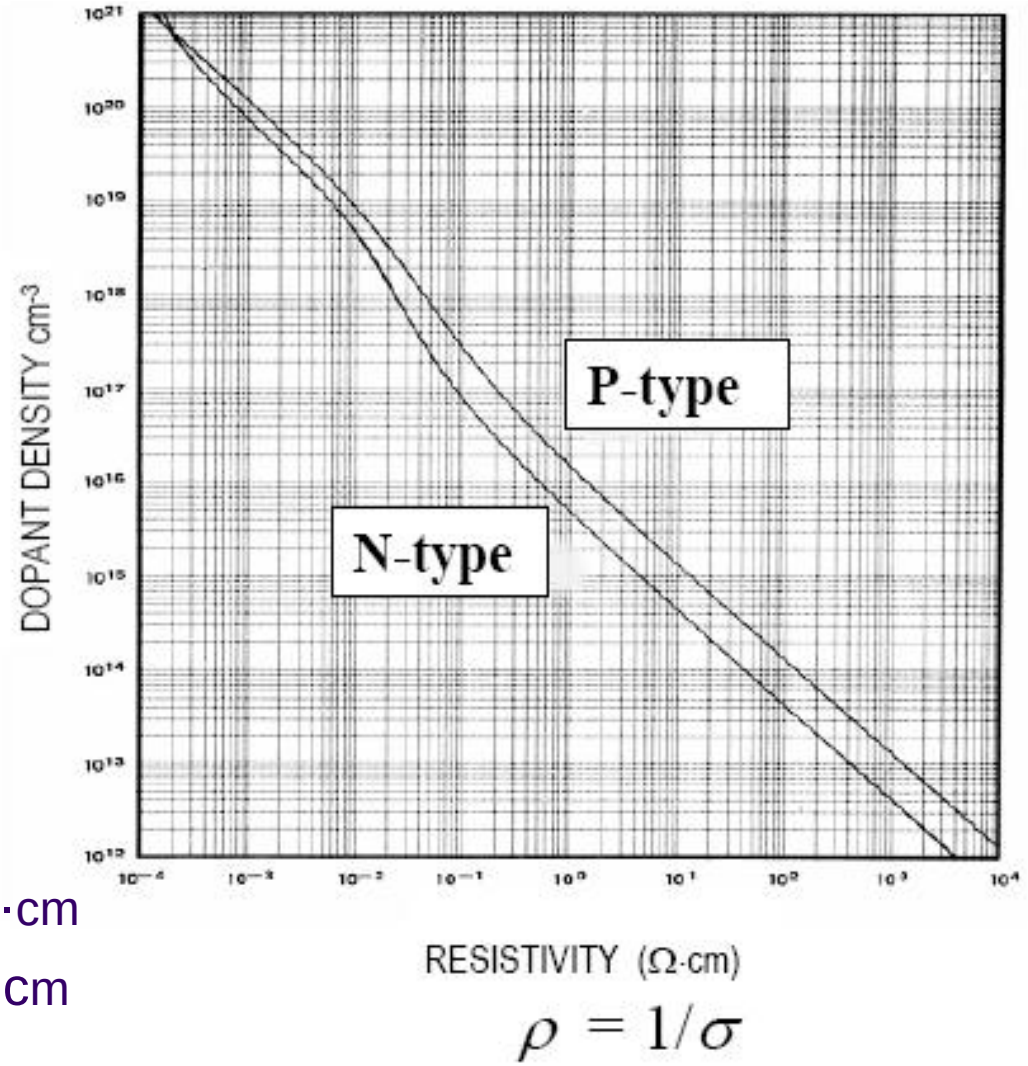
Generic Si:

$$J_{drift} = \sigma E = \left(qn\mu_n + qp\mu_p\right)E$$

N-type Si:

$$n = N_D \qquad p = \frac{n_i^2}{N_D}$$

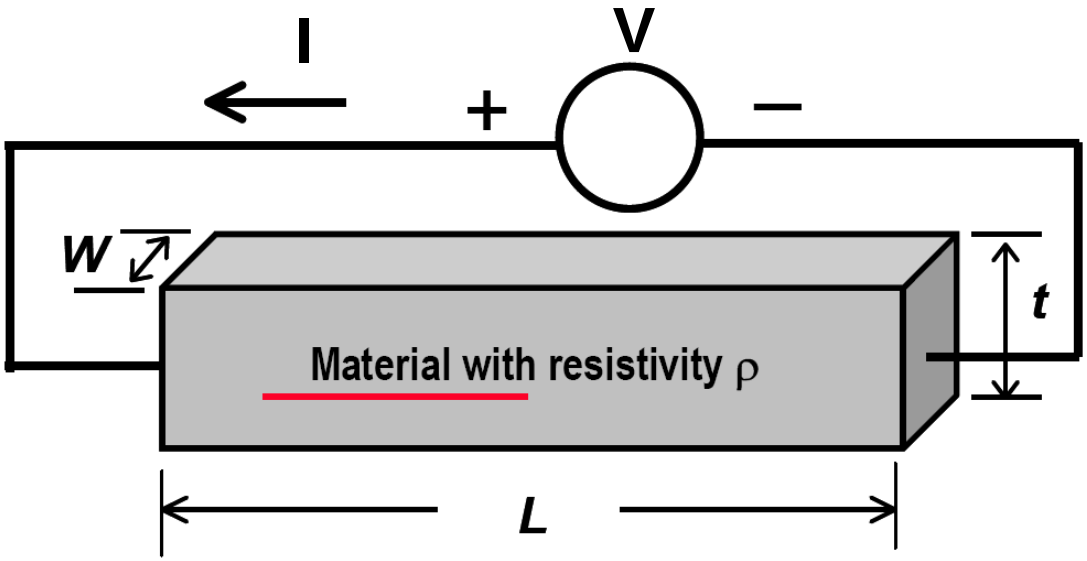
$$J_{drift} = \sigma E = \left(qN_D\mu_n\right)E$$



P-type

- Na=10^{14} cm^{-3} ρ=150 Ω·cm
- Na=10^{19} cm^{-3} ρ=9m Ω·cm

Sheet Resistance



$$R = \rho \frac{L}{Wt} = R_{\square} \frac{L}{W}$$

$R_{\square}=\rho/t$

Scaling and Time Delay

$$C_{gs}\Big|_{Vds=0} = C_{ox}WL$$

$$R = \rho\frac{L}{Wt} = R_{\square}\frac{L}{W}$$

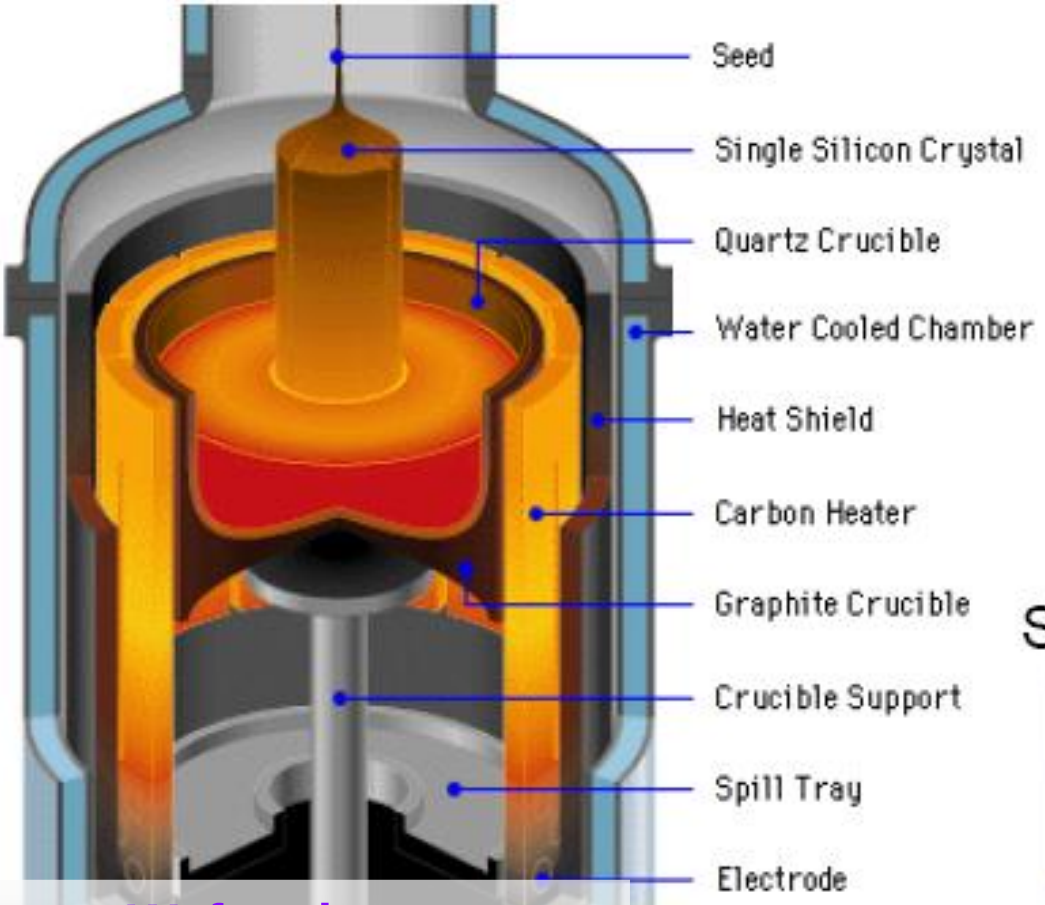
$$\Rightarrow \quad \tau = R_{\square}\frac{L}{W}C_{ox}WL = R_{\square}C_{ox}L^2$$

- Scaling of device size leads to shorter time delay and higher (maximum) operating frequency!

HOW INTEGRATED CIRCUITS ARE MADE

IC PROCESS FLOW

Si Wafer Fabrication



Crystal Ingots

Shaping and Polishing

Wafer size

Diameter 8-12 inches

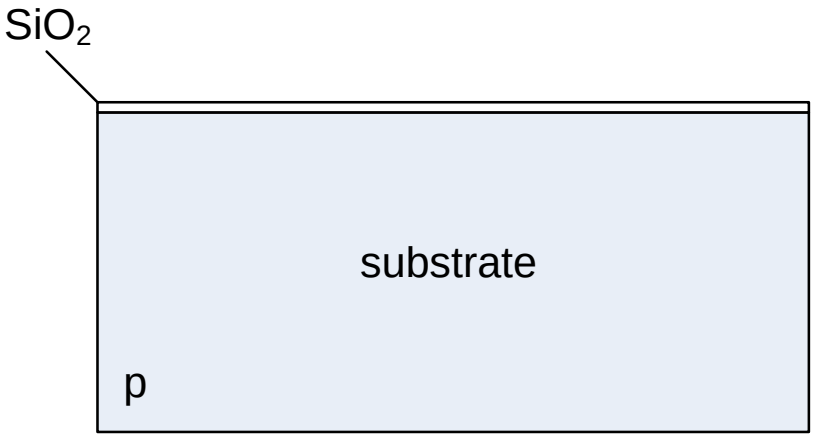
Thickness 300μm-1.2mm

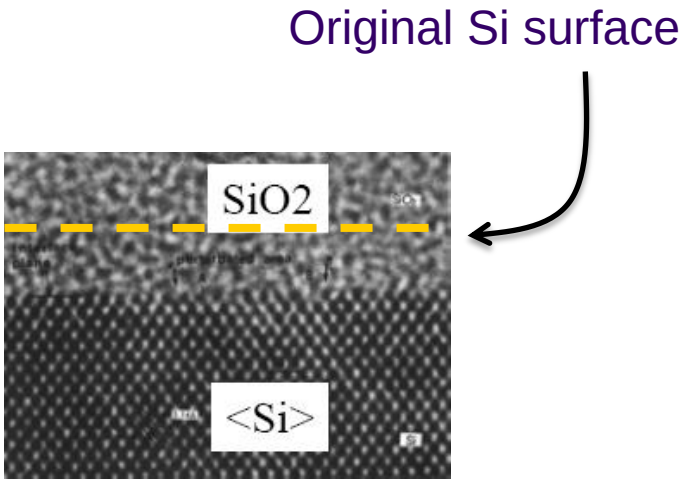
Si Wafer Fabrication

- During wafer production a controlled amount of impurity (dopant) is inserted together with silicon
- Typically p-type impurity (e.g. Boron) for CMOS processes

Thermal Oxidation

- Creates a thin silicon di-oxide (SiO_2) dielectric layer of excellent quality
- Thermally grown SiO_2 is used as:
  - Gate oxide in MOS transistors (~25Å in 90nm CMOS)
  - Isolation between substrate and metal layers (field oxide)
  - Mask for doping diffusion

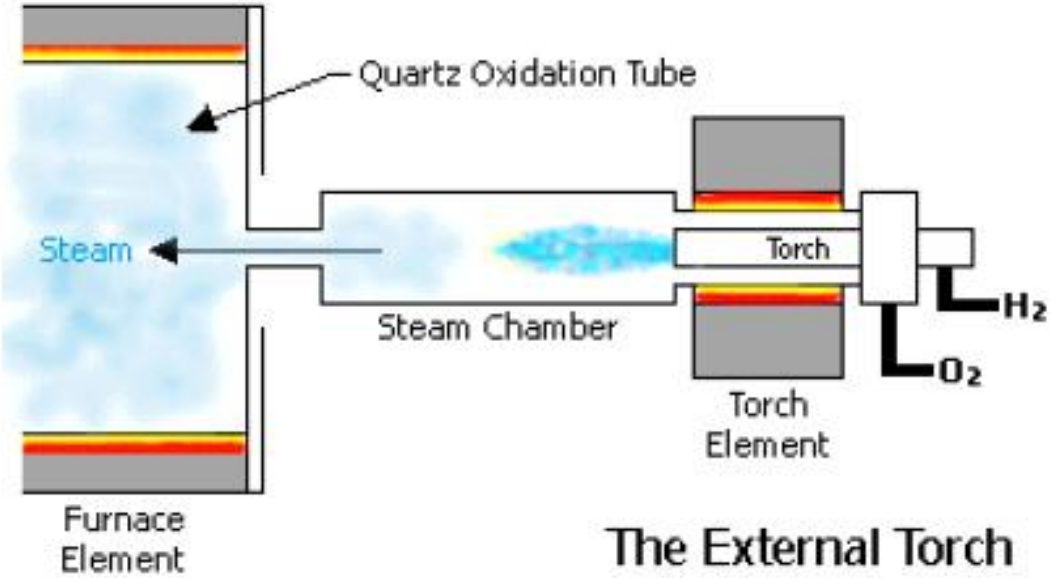




Thermal Oxidation Setup

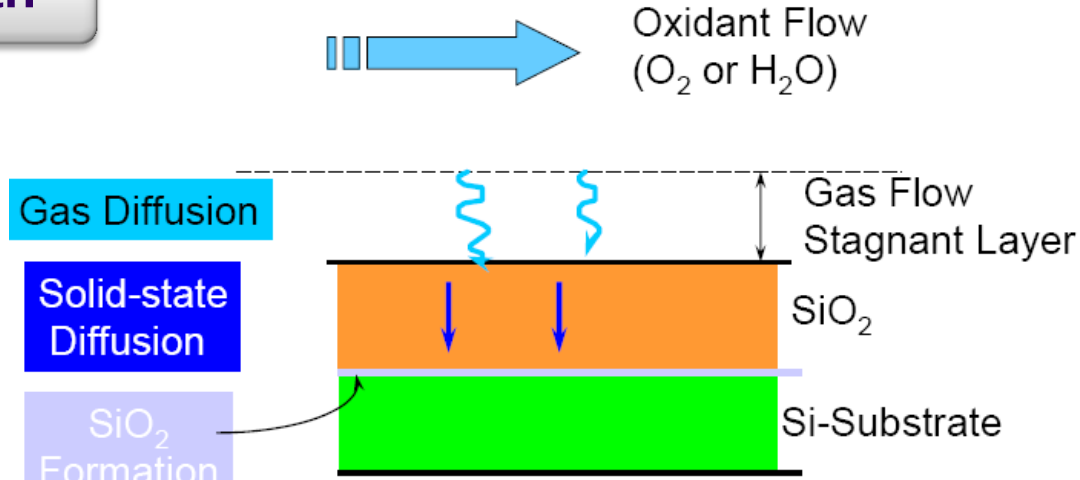
Wet oxidation

Steam generation for wet oxidation



The External Torch

Oxide growth



Arrhenius Law

Like may other chemical reactions, thermal oxidation is governed by Arrhenius law. Reaction speed varies exponentially with temperature:

$$C = C_0 e^{-\frac{E_A}{KT}}$$

K = 1.38 10^{-23} J/K

= 8.6 10^{-5} eV/K

E_A = 1.18 eV (dry oxidation:O_2)

E_A = 0.79 eV (wet oxidation: H_2O)

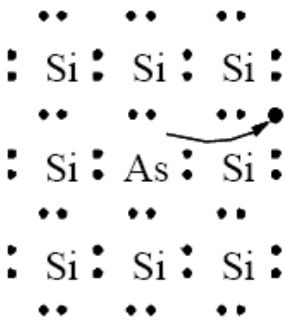
Temperature dependence of reaction speed. Example:

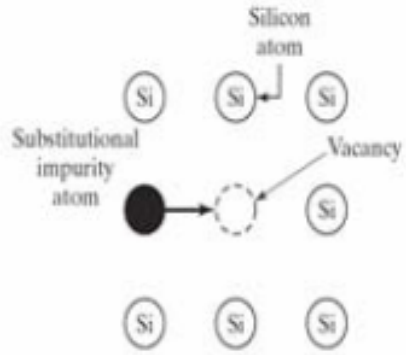
- *speed at 1100°C* *0.1 μm per hour*
- *speed at 100°C* *1.5 10^{-12} μm per hour*

Need for a very accurate temperature control!

Thermal Diffusion

- Introduces a controlled amount of impurities (dopant) in the area directly below the surface (n/p-well for contact, isolation, etc.)
- Impurities *substitute* Si atoms
  - N-type (donor atoms): As, P, Sb
  - P-type (acceptor atoms): B
- Misfit Factor = $R_{A,sub} / R_{A,Si}$



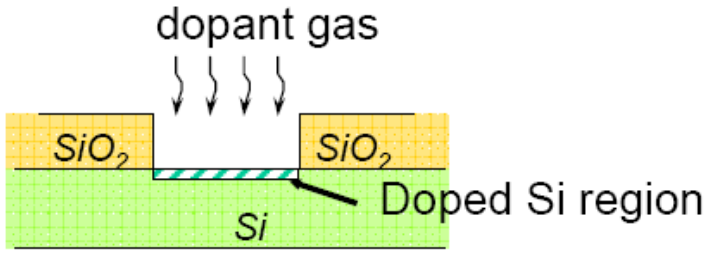


Dopant Diffusion Steps

- Predeposition

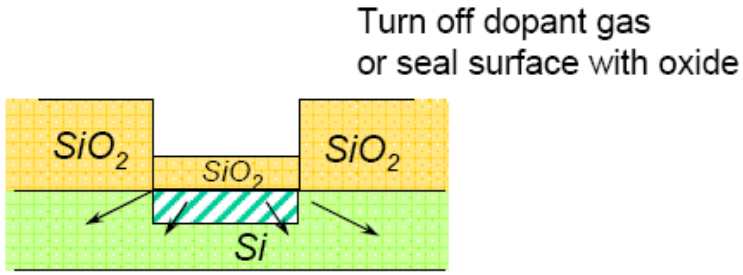
  Dopant gas: PH_3, AsH_3, B_2H_6

  Doping elements are introduced in a shallow region beneath the surface



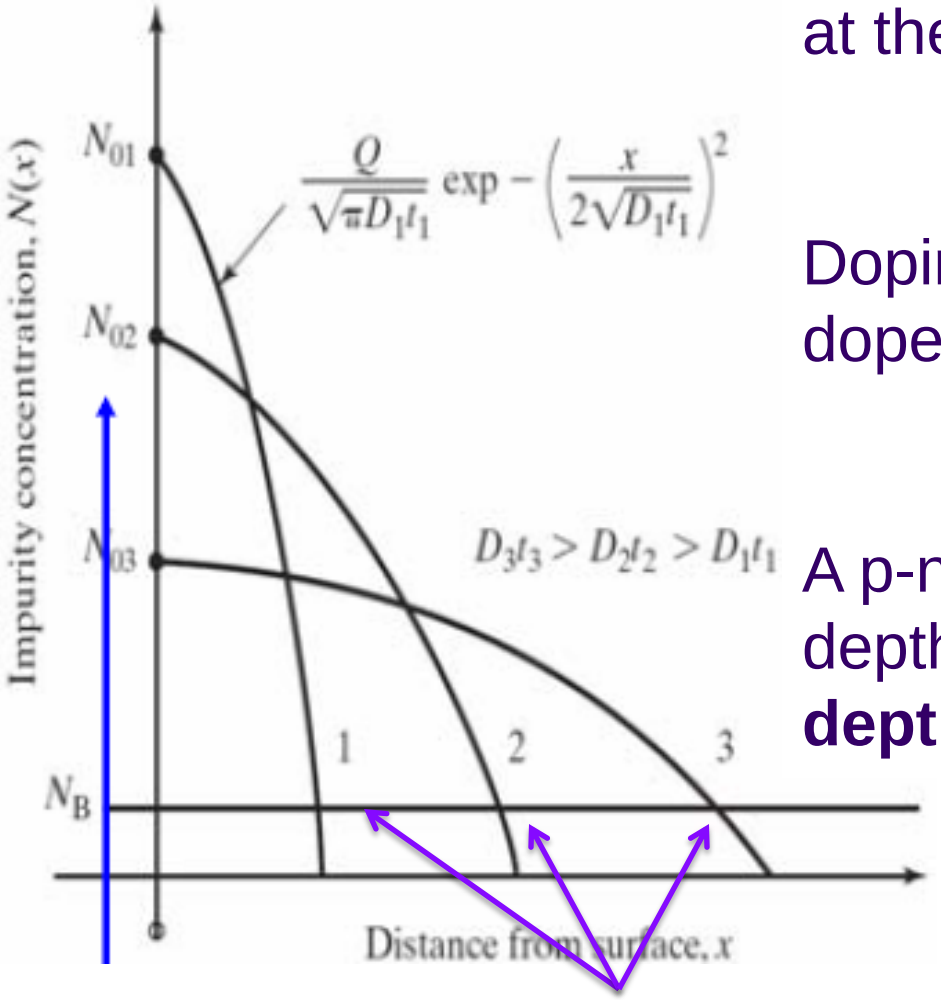
- Drive-in

  Doping elements diffuse inside the substrate.



- Thermal diffusion setup is similar to thermal oxidation setup.
- The process is controlled by the reaction temperature.

Dopant Profiles: Drive-in



Peak doping concentration is **always** at the Si surface

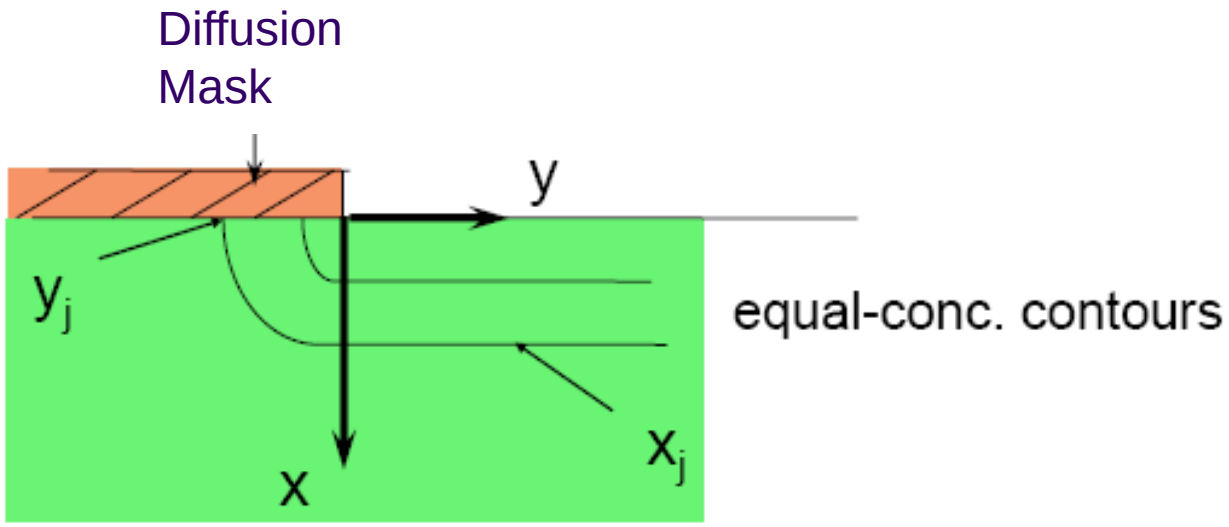
Doping is carried out on an already doped Si substrate

A p-n junction is formed at a certain depth below the surface: **junction depth**

JUNCTION DEPTH

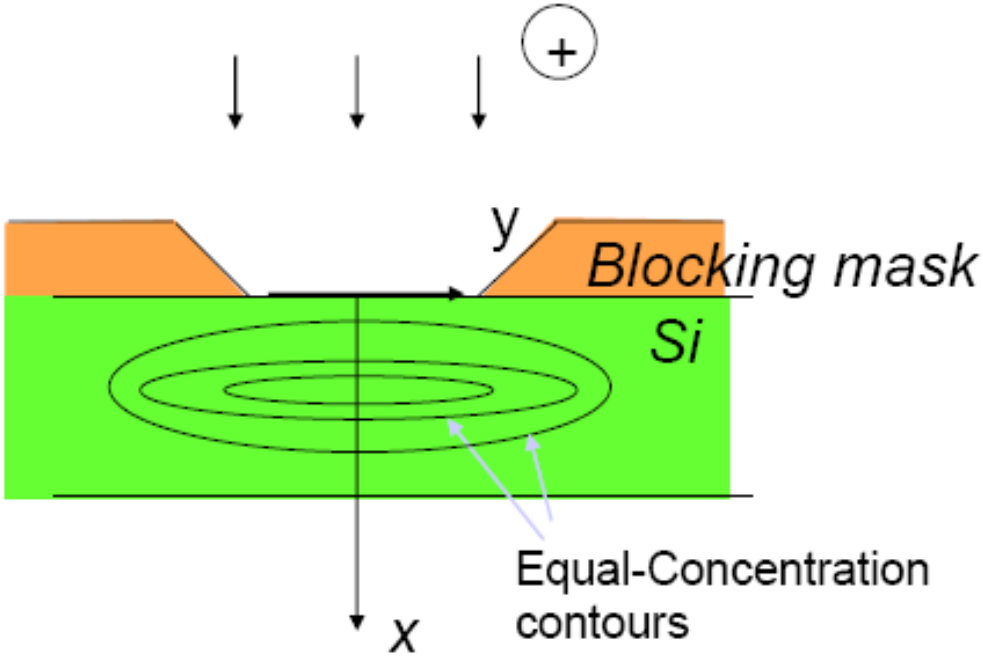
Doping profiles limited precision

- Further thermal cycles alter the dopant profiles
- Diffusion takes place in two dimensions: *lateral diffusion* limits planar selectivity as a function of doping depth



Ion Implantation

- Introduces a well controlled amount of dopant in the substrate
- Can be a substitute for thermal diffusion or just for predeposition
- Must be followed by a thermal cycle (annealing) to repair damages

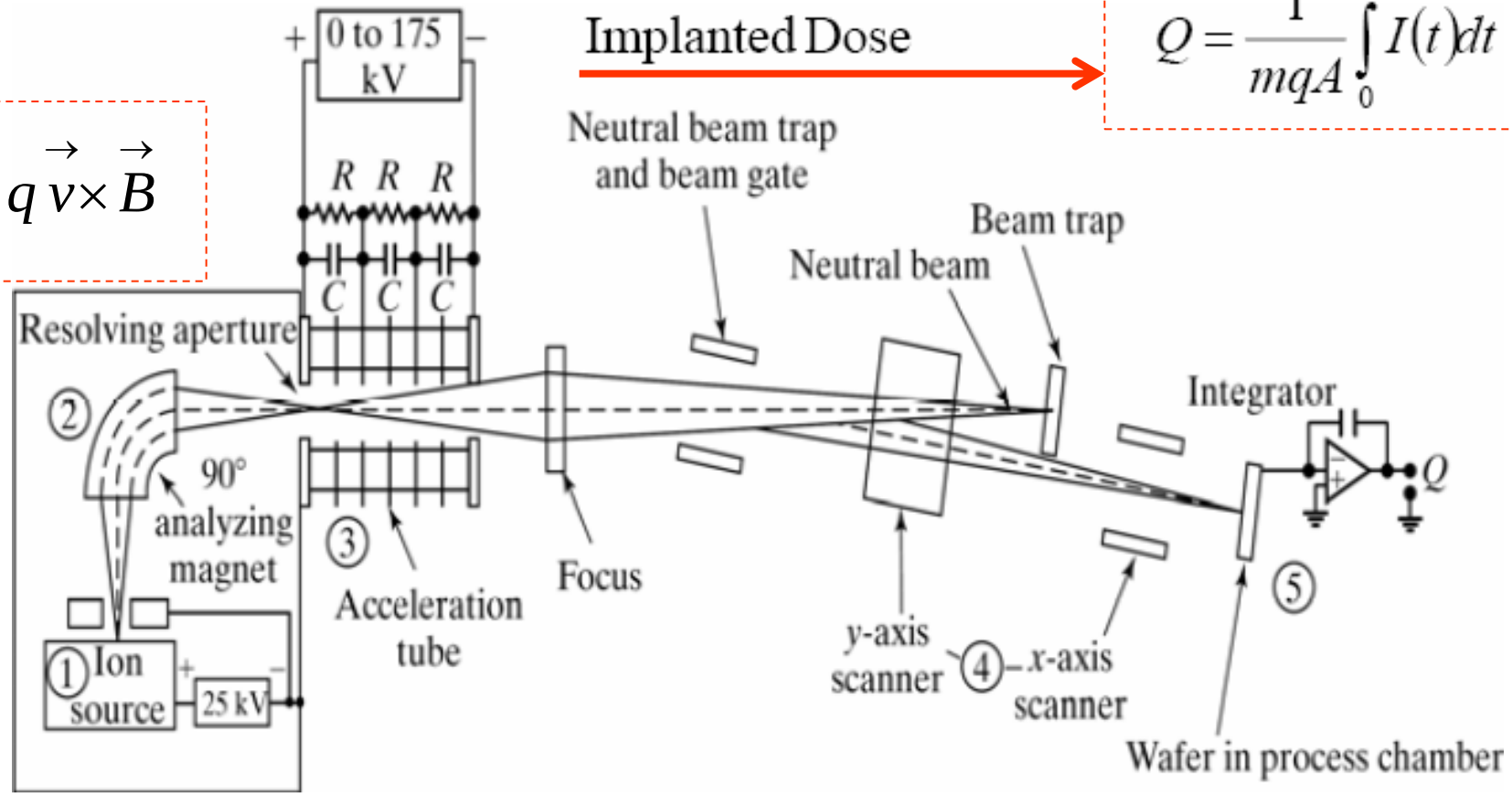


Ion Implantation

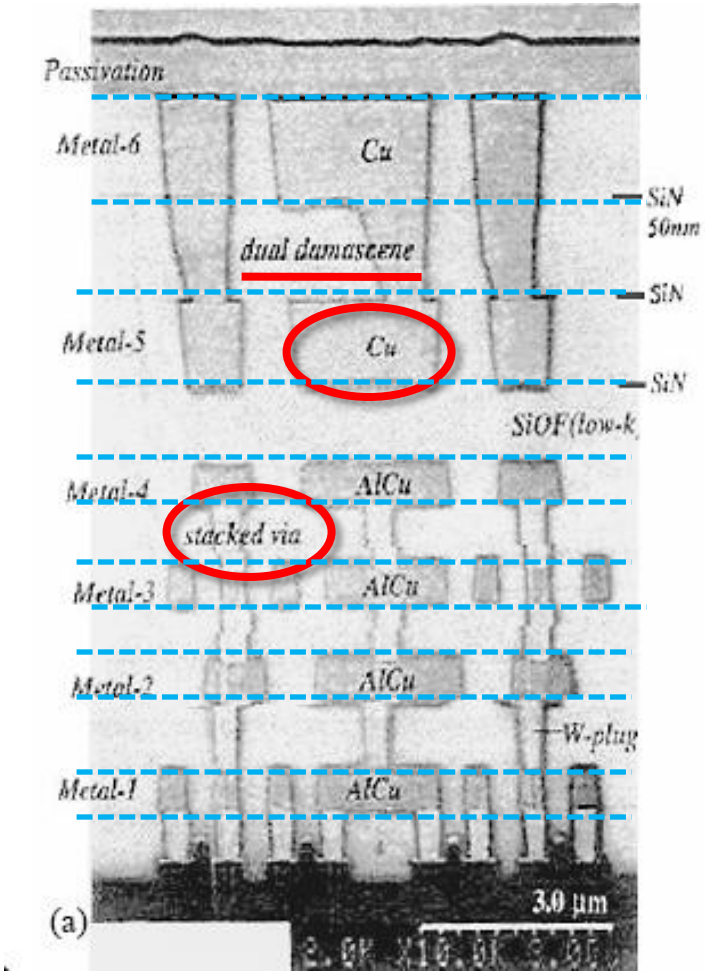
$$\vec{F} = q\,\vec{v} \times \vec{B}$$

Implanted Dose

$$Q = \frac{1}{mqA}\int_0^T I(t)dt$$



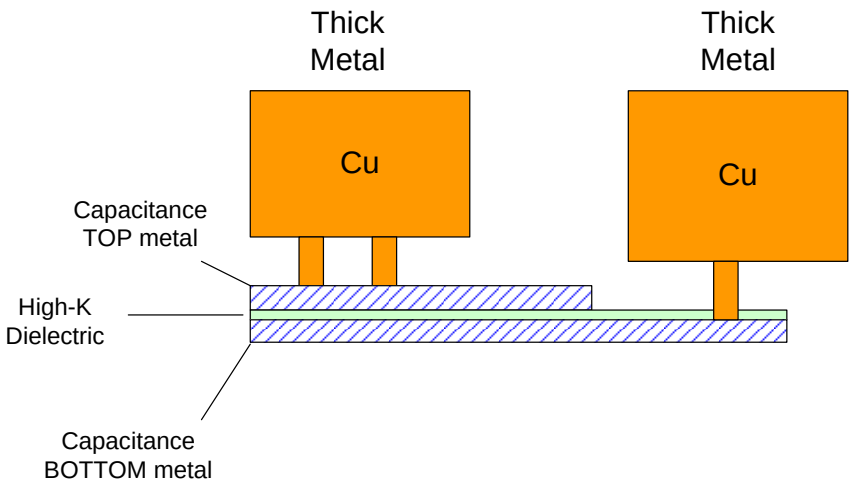
Technology Cross-Section



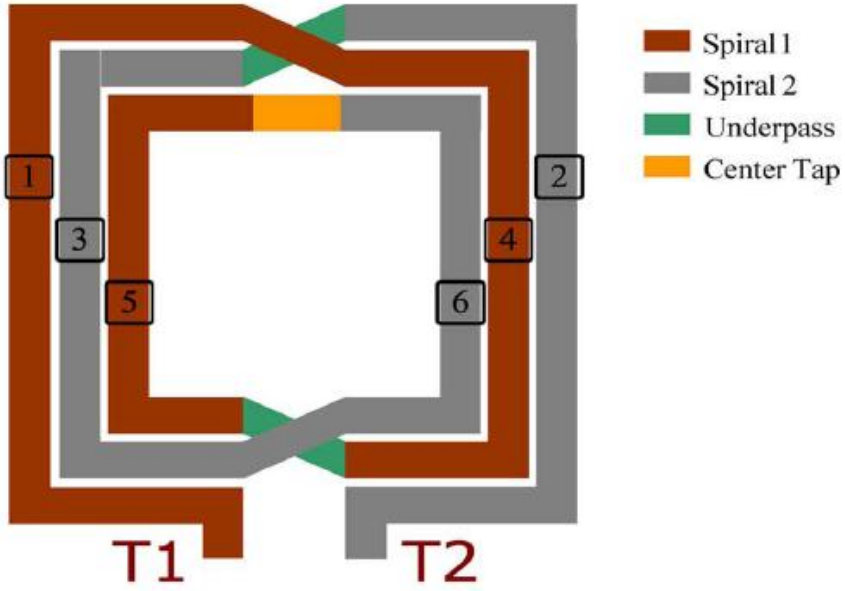
- Metal layers stack in a recent CMOS technology
- Cu and Al interconnect
- Inter-layer VIA holes

Passive Devices

- Metal-Insulator-Metal (MiM) capacitor

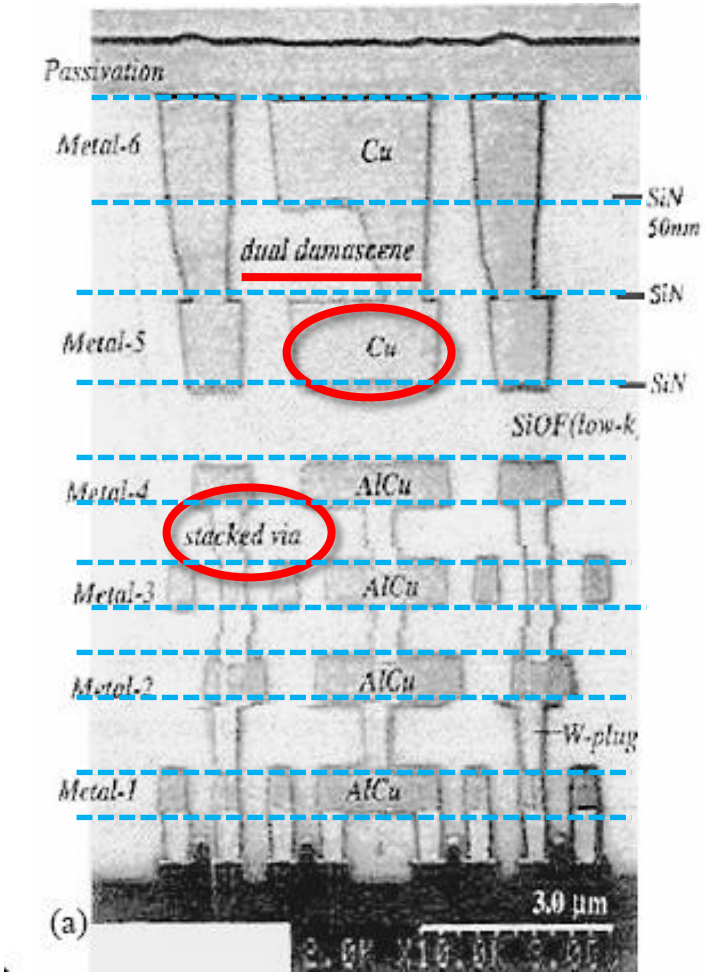


- Center-Tapped Inductor

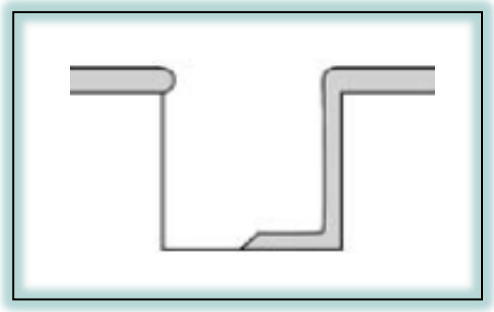


Thin Film Deposition

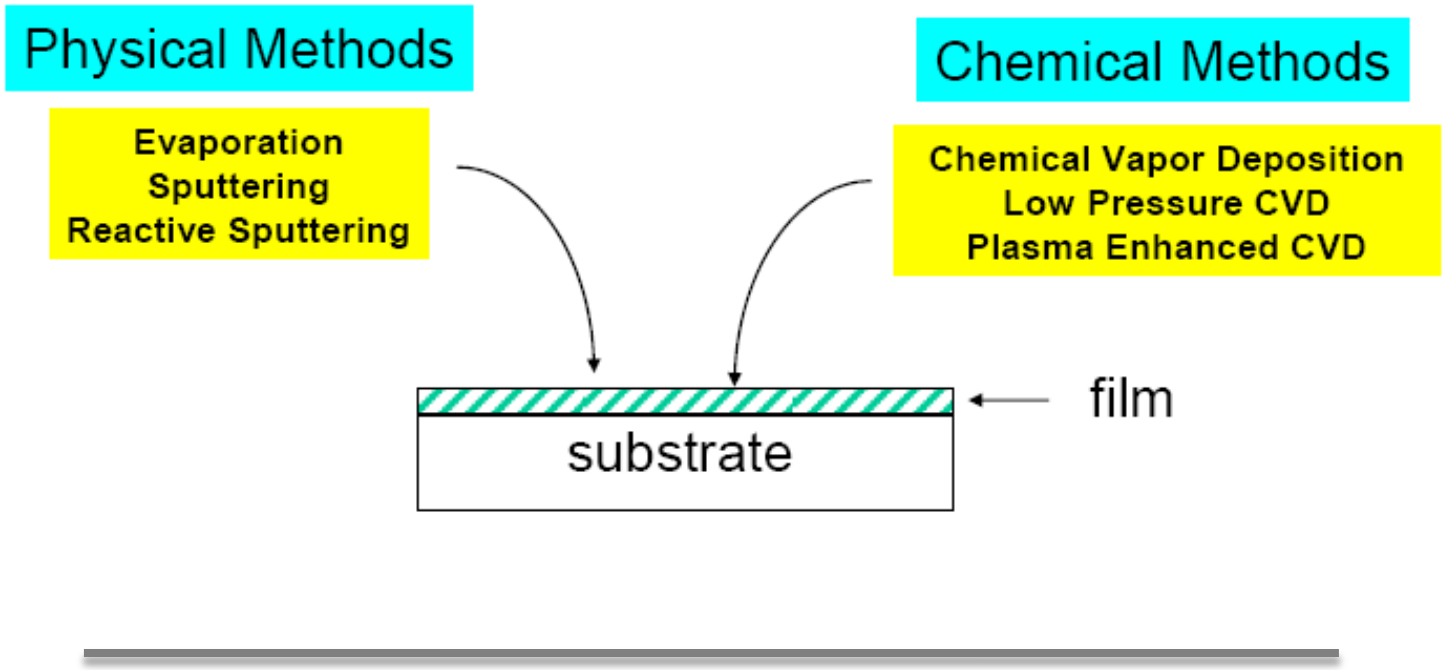
METAL LAYERS STACK



- Important parameters:
  - Uniformity: constant layer thickness
  - Processing temperature
  - Cost per wafer
  - Step coverage



Thin Film Deposition



Conductive layers: Al, Cu, poly-Si, W, other metals

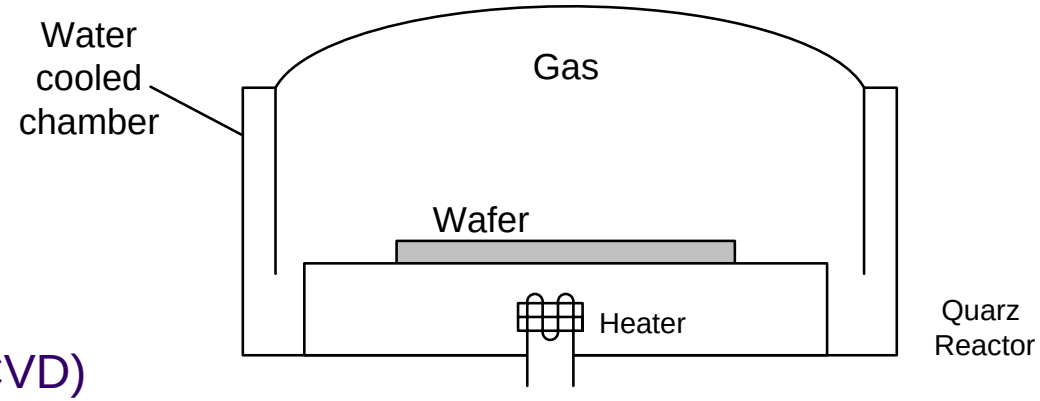
Dielectric layers: SiO_2, silicon nitride (Si_3N_4)

Chemical Vapor Deposition (CVD)

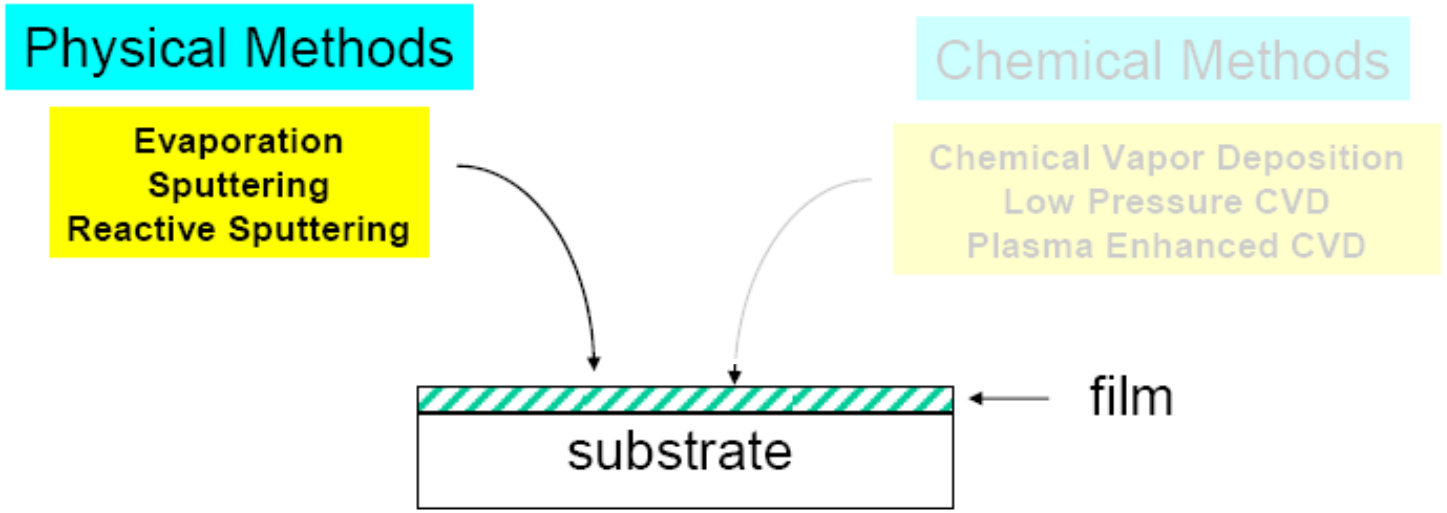
1. The chemical reaction of one or more gas compounds creates the desired material in gas (vapor) form.
2. A thin film of material is formed through deposition from vapor state.
3. Substrate heating enhances the chemical reaction, accelerating the deposition process (Temperatures up to 1000°C)
4. Alternatively plasma can be used to enhance reaction (plasma enhanced CVD) at moderate temperatures (up to 400°C)

There are three main types:

- Atmospheric-pressure CVD
- Low-pressure CVD (LPCVD)
- Plasma enhanced CVD (PECVD)

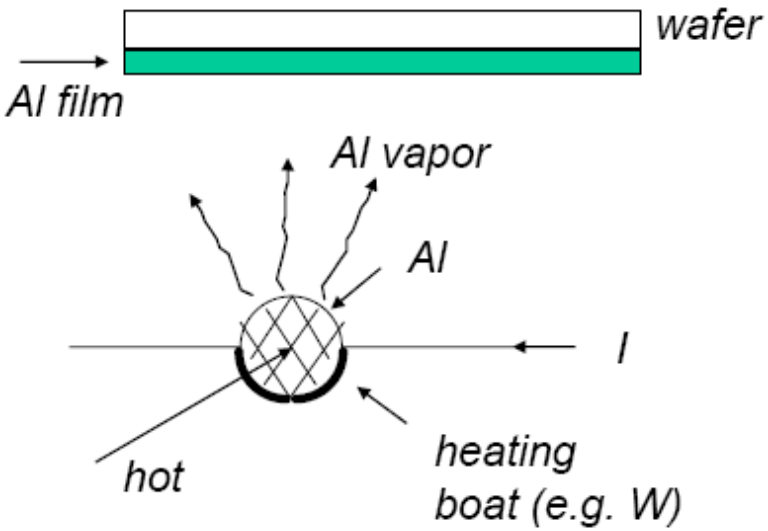


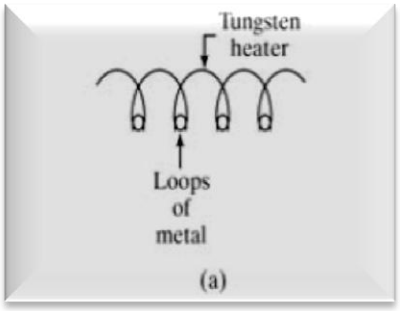
Physical Vapor Deposition (PVD)

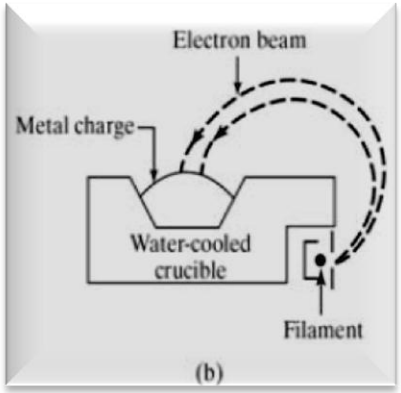


1. The atoms of the material to be deposed reach high kinetic energy in a *vacuum* chamber
2. Thanks to vacuum condition, atoms reach the substrate (target) with few or no collisions
3. A thin layer with *crystalline structure* is formed

PVD: Evaporation



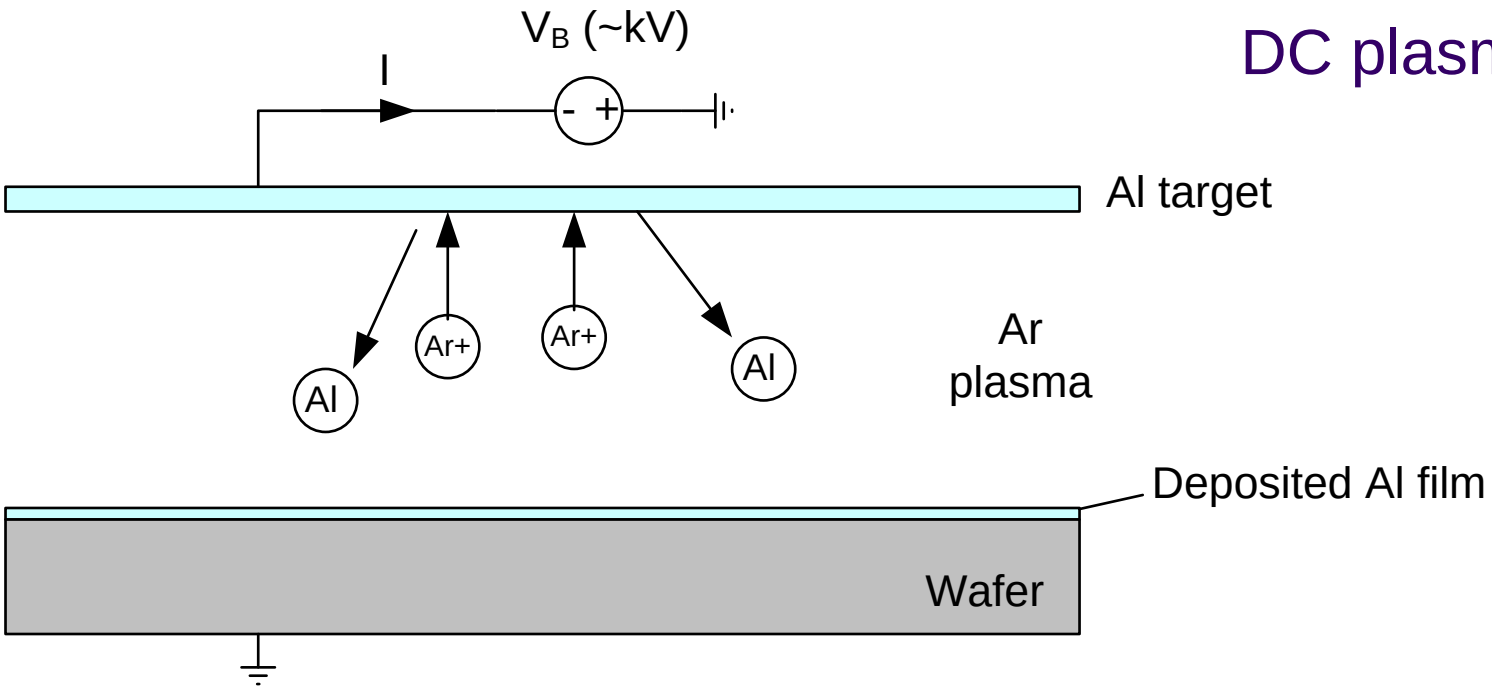




Joule heating **Filament** **Electron beam**

- The desired material is vaporized through heating in a vacuum chamber
  - Joule heating, electron beam, pulsed laser beam, filament evaporation (current), flash evaporation

PVD: Sputtering



DC plasma

- Plasma is a low pressure gas where a high energy electric field is used to drive ionization creating a large number of ions and free electrons
- Fine particles of the desired material are ejected from a solid target by applying *plasma* excitation

Vapor Phase Epitaxy (VPE) *

- It is a type of CVD where the deposed layer (epitaxial layer) has *crystalline structure*
- High temperature (1000 -1250°C) is required
- Dopant is added in the reaction chamber during deposition

$$SiCl_4 + 2H_2 \rightarrow Si + 4HCl$$

* Crescita epitassiale

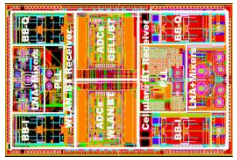
Expitaxial Layer

- ☺ Uniform doping concentration
- ☺ Abrupt doping concentration step
- ☺ Higher mobility compared to doping through overcompensation

- ☹ Autodoping: impurities in the reactor atmosphere alter doping in the epitaxial layer
- ☹ Outdiffusion: impurities in the Si wafer diffuse into the epitaxial layer
- ☹ Buried layers alter the shapes in the epitaxial layer

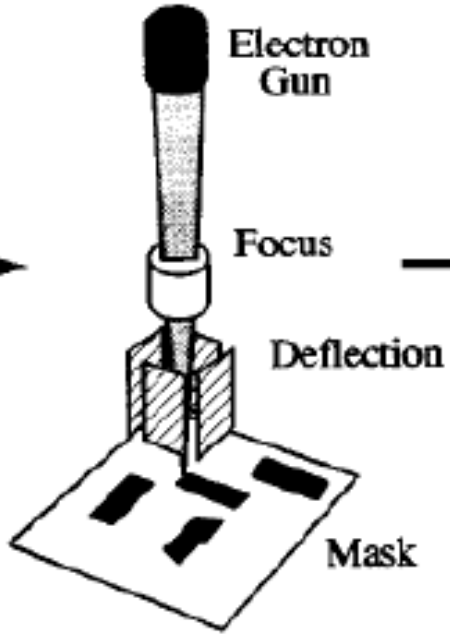
Lithographic Process

Design



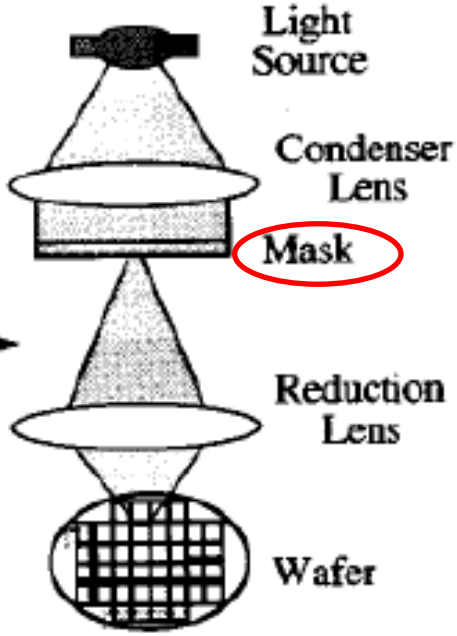
CAD System
- Layout
- Simulation
- Design Rule Checking

Mask



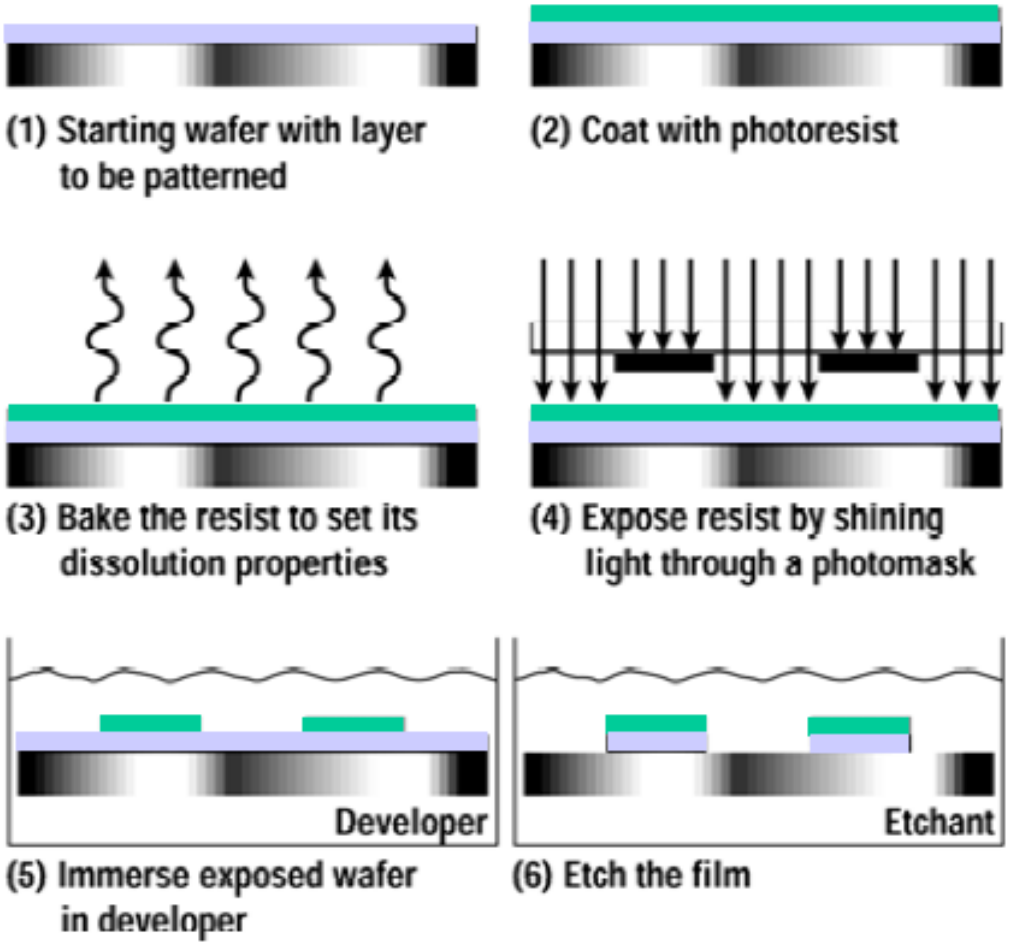
Mask Making

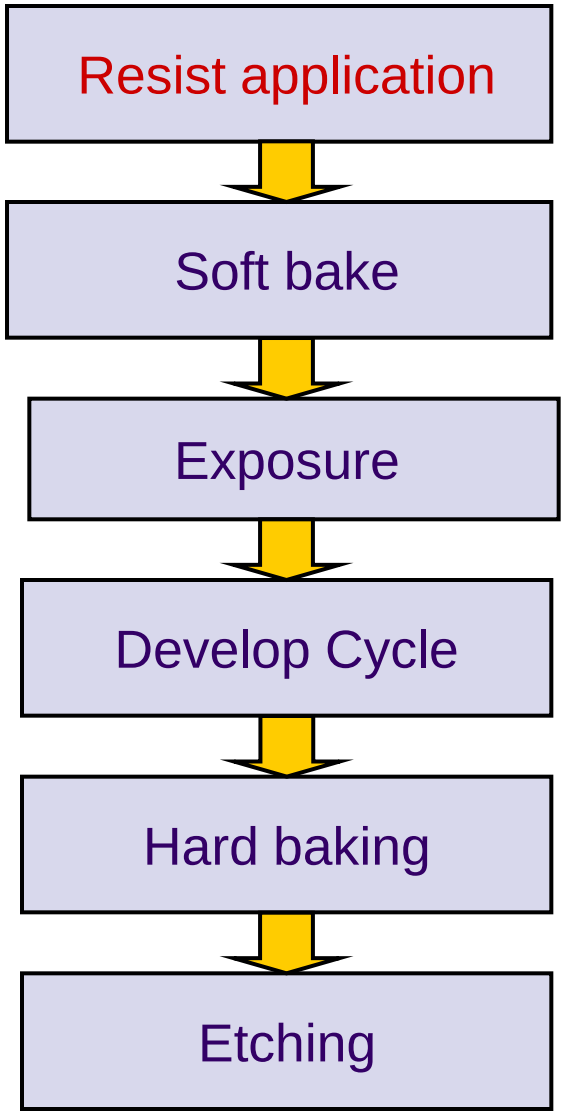
Wafer



Wafer Exposure

Lithographic Process

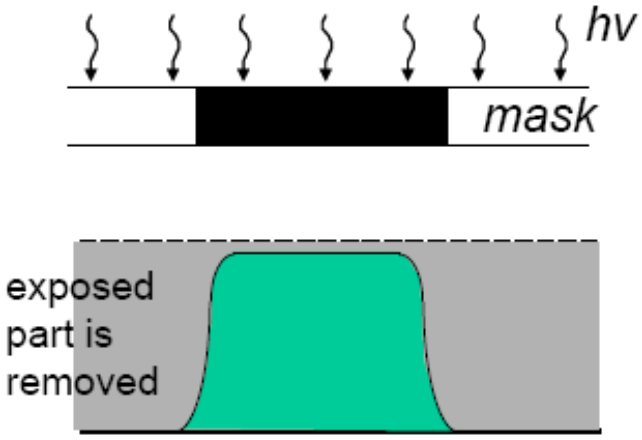


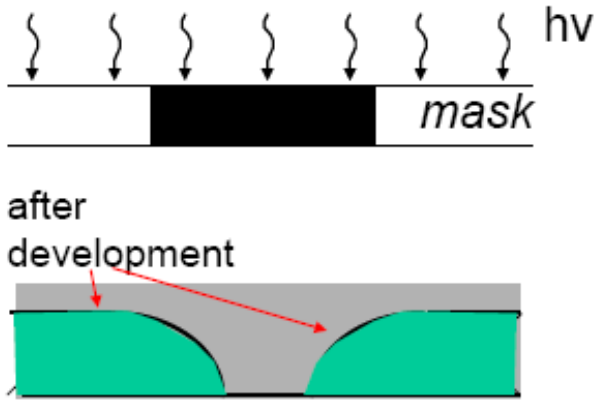


Resists for Lithography

Photo-resists are composite materials made of:

- Organic polymer
- Photoactive compound
- Solvent (eliminated during soft-bake)





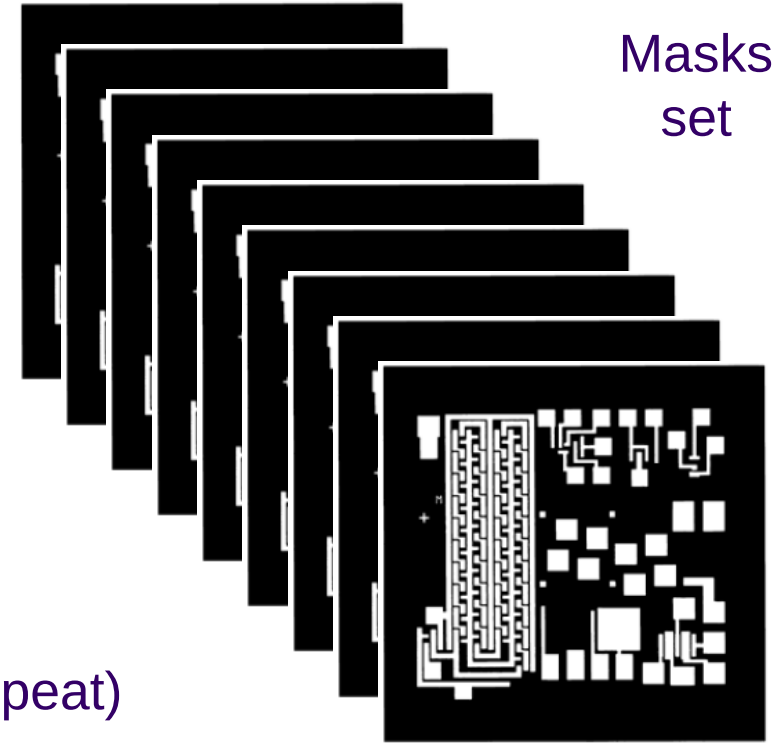
- Positive resist

Higher resolution

- Negative resist

Lower resolution

Photolithographic Masks



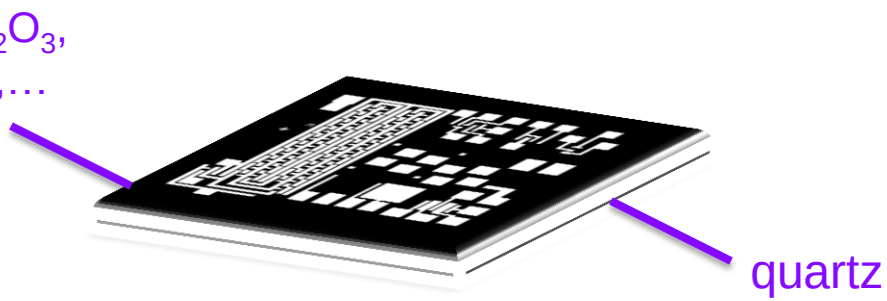
Masks set

Mask making:

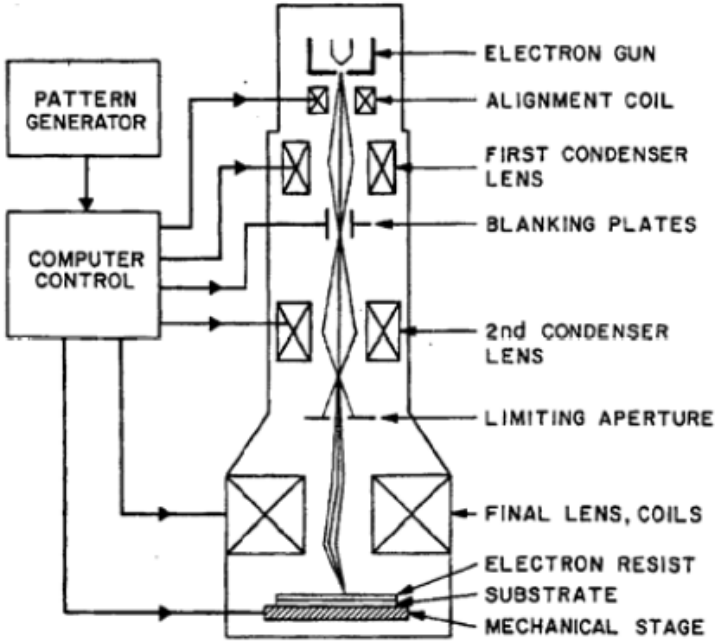
electron beam lithography (step and repeat)

Each mask includes:

- Alignment marks
- Mask making patterns
- Process monitor patterns



Mask Making

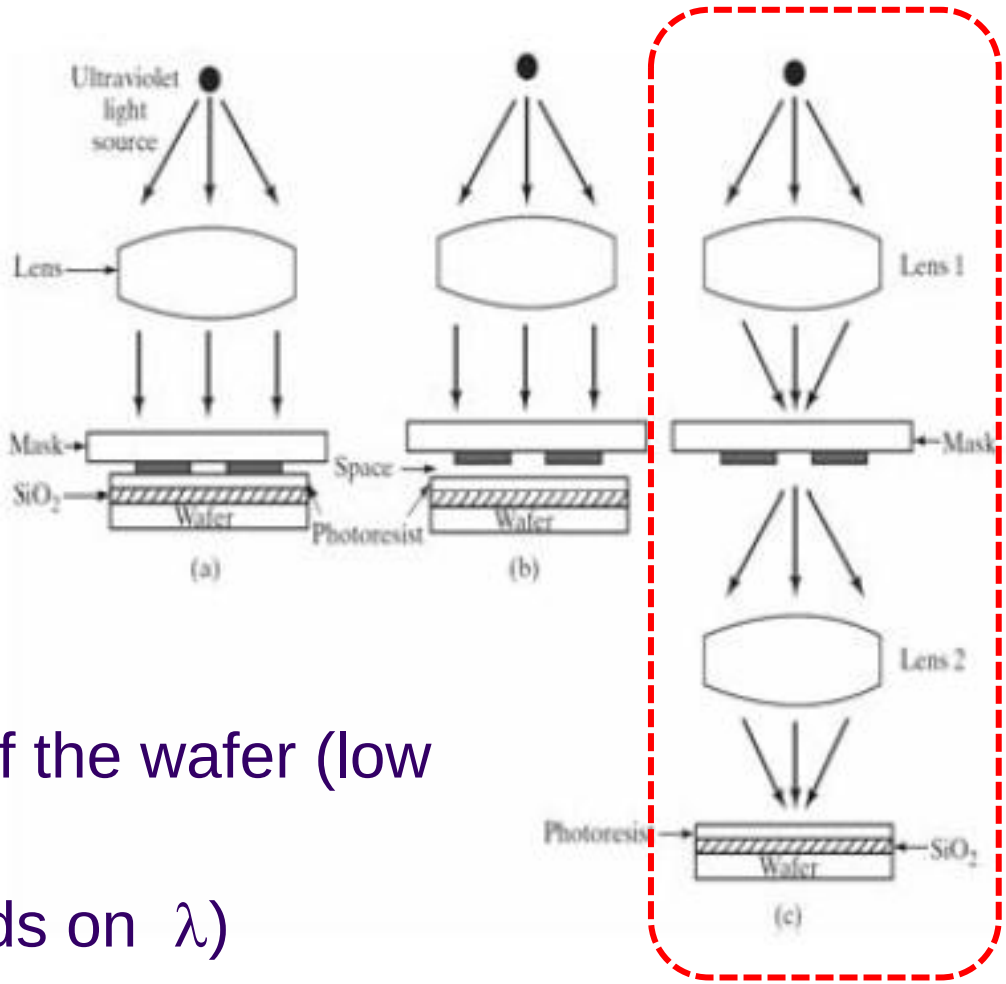


- Electron beam lithography
  - Resist activated directly by directive electron beam, without mask
  - Resolution < 1nm
  - Very low throughput (very high cost)

Printing Techniques

Techniques:

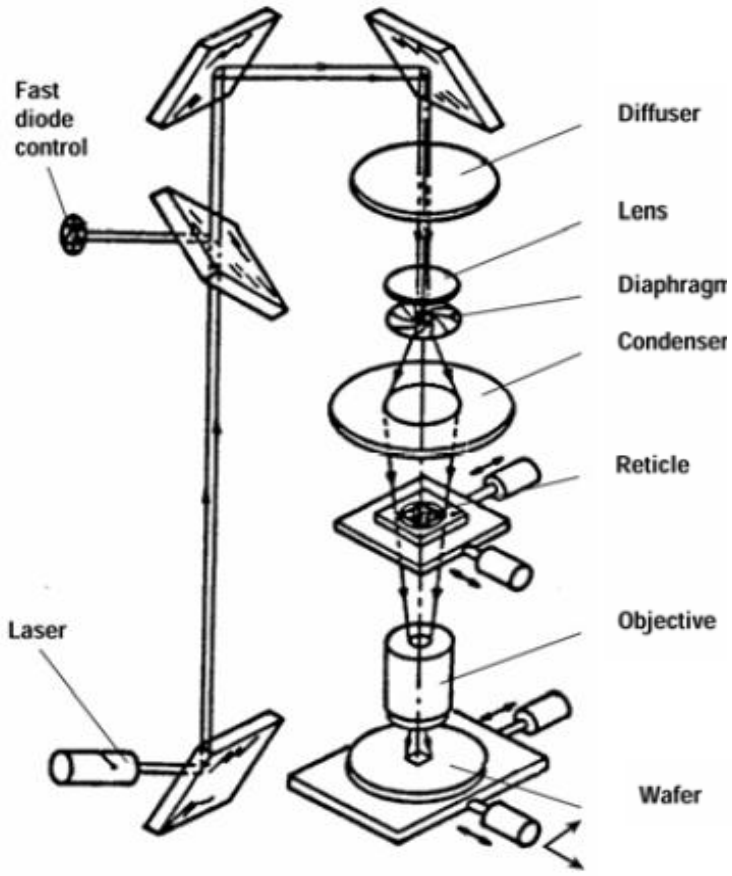
- Contact
- Proximity
- Projection



- Exposure of a portion of the wafer (low throughput)
- High resolution (depends on λ)
- Requires excellent planarity of the wafer for proper focusing

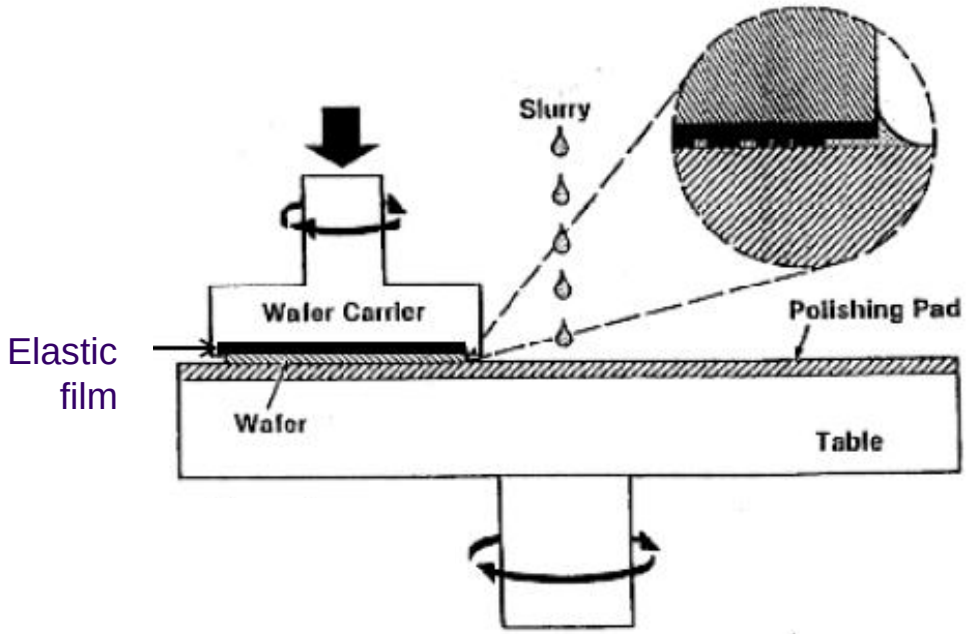
Step and Repeat

WAFER STEPPER



- Exposition carried out on a limited area (field), then wafer is repositioned and exposition is repeated on an adjacent area
- Focus and alignment after each step
  - low throughput
- De-magnification: 4-10:1
  - Excellent chip resolution: better than mask resolution

Chemical Mechanical Polishing - CMP



- Thick dielectric film deposition
- Wafer is polished using abrasives and etching agents
- Enhanced local and long range planarity

References

- Reading Material:
  - Dispense di G. Torelli. Introduzione alla tecnologia dei circuiti integrati su silicio. 2006. (IC Technologies)
  - Dispense del corso *Microfabrication Technology*, UCB http://organics.eecs.berkeley.edu/~viveks/ee143/