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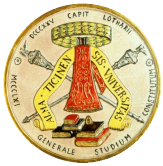
DIPARTIMENTO DI ELETTRONICA



DOTTORATO DI RICERCA IN MICROELETTRONICA

XXII CICLO

Design and Modeling Techniques for bulk CMOS mm-Wave Wideband Front – Ends

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“A process cannot be understood by stopping it. Understanding must move with the flow of the process, must join it and flow with it.”

The First Law of Mentat, quoted by Paul Atreides to Reverend Mother Gaius Helen Mohiam

Frank Herbert, from the book “Dune” (1965)

Acknowledgments

Here I am, at the end of these three years, writing these few lines to thank all the people who supported me in this period.

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To all the people I forgot…

Index

Introduction

Exploiting wireless communications has been one of the main target in the last few years. In this scenario, the cellular phone market represented the main target for semiconductor industry. The availability of newer and larger bandwidth in the frequency spectrum opened to the possibility of higher bitrates communications, thanks to the lower costs made possible by integrating more and more functionalities leveraging the continuing scaling of CMOS technologies.

However, in order to extract the maximum performance from CMOS technology, which is usually targeted to digital circuits, new design techniques need to be devised to deal with the realities of these technologies: lossy substrates, low-Q

passives, long interconnect parasitics, and high-frequency coupling issues.

This is getting even worse if we consider very high frequency operation, such as the mm-Wave range; that is, the range of frequencies between 30 and 300 GHz. At first glance, availability of mainstream products operating at these frequencies could seem improbable at least.

Nevertheless, in the last few years there has been an increasingly interest in going to higher frequencies; there is an obvious bandwidth advantage in exploring higher (or wider) frequency ranges, enabling the possibility of higher data-rates communications.

For this reason, the Federal Communication Committee granted unlicensed bands around 60 GHz and 77 GHz for several wireless applications.

An intense research activity is currently underway. One of the more important topic is represented by the design and modeling of passive components working at these frequencies. High quality passive components are the key to provide good circuit performances, reducing overall losses; on the other hand, an accurate modeling of all the effects involved is mandatory in order to provide a good agreement between simulations and real circuit performances, reducing time-to-market. Moreover, new circuit topologies leveraging the aforementioned capabilities can overcome some of the

intrinsic disadvantages of CMOS technologies, such relatively high parasitics, leading to a fully integrated System-On-Chip with both RF and baseband processing on the same die, key to obtaining cheap products.

In this Ph. D thesis design of passive components for mm-Waves applications will be addressed, with a particular focus on transmission lines. Accurate modeling approaches will be provided, targeted to reproduce the correct behavior of all the involved components. All this concepts will be applied to a receiver front-end targeted to 60 GHz operation, resulting in state of the art performances and in an optimum correspondence between simulations and measurements, opening for future improvements such as more complicate structure, for example phased arrays.

In **Chapter 1** a general overview of mm-Wave systems and applications will be discussed. Advantages of higher frequency operations will be investigated, along with mm-Wave channel propagation characteristics and the main challenges in mm-Wave CMOS design.

In **Chapter 2** the design and optimization of integrated transmission lines will be addressed. Integrated transmission lines are becoming attractive in CMOS design at mm-Wave frequencies due to the small wavelength involved. However, very critical design rules have to be fulfilled, and the lossy CMOS substrate can lead to very poor performance. All these

issues will be investigated, leading to the creation of shielded structures and obtaining performances comparable with more expensive technologies, thus enabling high quality mm-Wave passive components on cheap CMOS substrates.

In **Chapter 3** an efficient simulation method for the analysis of periodic structures (in particular transmission lines) will be presented. This method leverage the possibilities of general purpose electro-magnetic commercial softwares, enabling a fast and accurate analysis of periodic structures, such as periodic shielded transmission lines or transmission lines with dummies. With this approach, it will be possible to easily take into account the effects of metal dummies on the behavior of transmission lines and use them as an advantage.

In **Chapter 4** modeling of mm-Wave passive components will be investigated. One of the main issue in creating models is to provide equivalent circuits valid both in the time and frequency domain, in order to be able to perform complicate system simulation that involve both transient response and frequency translation. Starting for a simple and physical model of an integrated spiral inductor, modeling of more complex structures (such as coupled inductors, low value inductors and transmission lines) will be addresses. The modeling approach will then be applied to some real test cases, providing an insight into layout and co-simulation in order to correctly predict the real circuit behavior.

In **Chapter 5** a wideband LNA will be presented. In order to satisfy the requirements for high bitrates communications, a very large bandwidth (around 9 GHz) has to be covered. In order to fulfill this requirement with a reasonable power consumption, new techniques have to be adopted, and modeling is a critical issue in order to provide simulations representative of the real circuit behavior. The proposed LNA reaches this goal, with an optimum agreement between measurements and simulations. A mm-Wave wideband receiver has then been implemented, reaching state of the art performances. The proposed modeling techniques reveal to be valid and reliable, thus simplifying the design and reducing time-to-market.

1

mm-Wave systems and applications

During the last decades we experienced a continuous growth in wireless communications. Starting from GSM mobile phones in the first 1990s, dedicated to voice communications, a continuing demand for different wireless communications have pushed standards to achieve better performances, in order to enable applications such as Bluetooth [1.1], dedicated to provide various services such as low-power, low data-rate transmission to exchange information between mobile terminals and gadgets such as mobile phones headsets.

New standards have appeared, as Wi-Fi [1.2], enabling higher data-rates over short-range distances. These applications have been supported by low-cost silicon technologies, which

provided cheap and low-power products. However, this trend has been slower in respect to the continuous growing of personal data, supported by cheaper and cheaper storage solutions; recent developments [1.3] pushed wireless data-rates in the range of 300 Mb/s, which are still lower than their cable counterpart (1 Gb/s).

One promising solution seems to be represented by the 7 GHz of unlicensed spectrum around 60 GHz [1.4]. Until now, applications in these frequency range have been restricted to relatively expensive and power-hungry technologies (such as GaAs, SiGe etc.) but recent developments in CMOS technologies suggested the possibility to use cheaper and low-power technologies to do the job. However, since mm-wave frequencies are about one order of magnitude higher than anything has been integrated on CMOS substrates, many design challenges arise, in particular in active and passive components modeling. Thus, as it will been shown in this work, it is necessary to develop appropriate design strategies (i.e. using both lumped and distributed components, full wave analysis, precise parasitic extraction of active components) to achieve a good alignment between expected and real world performances.

There are other benefit in using higher frequencies; for example, it is possible to exploit smaller wavelengths to improve the resolution of imaging systems; other applications are represented by short-range, low-cost radar, particularly

targeted to automotive applications, such as anti-collision systems. All the above applications will be discussed in this chapter, along with main design challenges and opportunities.

1.1 mm-Waves Channel Propagation

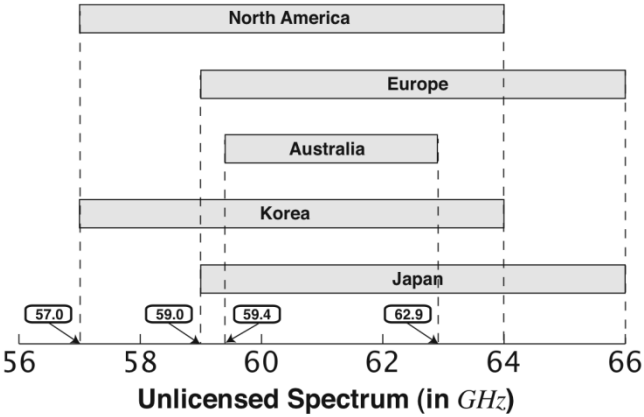


Fig 1.1 60 Ghz frequency spectrum available in different world regions.

In 2001, the Federal Communications Commission (FCC) set aside a continuous block of 7 GHz of spectrum between 57 and 64 GHz for wireless communications (Fig 1.1) [1.4] in North America; similarly, other frequency bands are available in other regions.

One major advantage in this allocation is that the spectrum is "unlicensed" - in other words, an operator does not have to buy a license before operating equipment in that spectrum.

Such a high bandwidth is an ideal candidate to high bit-rate transmission; in fact, recalling Shannon's theorem [1.5]:

$$C = BW \cdot \log_2(1 + SNR) \tag{1.1}$$

where C is the maximum data rate of a communication channel (i.e. channel capacity), BW is the Bandwidth of the channel, and SNR is the Signal-to-Noise Ratio of the information. This equation describes the tradeoff between channel capacity, signal Bandwidth and SNR; for example, in order to increase the amount of information transmitted, it is possible to increase bandwidth for a fixed SNR. Practically, this is the case of 60 GHz communications. From this point of view, we can compare 60 Ghz communications to other wireless standards in terms of signal bandwidth and Equivalent Isotropically Radiated Power (EIRP) [1.6]:

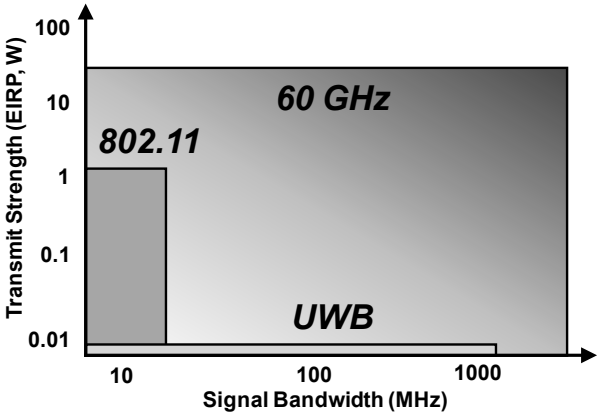


Fig 1.2 Signal Bandwidth and Transmit Strength for different wireless standards

As we can see from the picture, for existing standards we have two different situations: 802.11 (Wi-Fi) relies on a small channel bandwidth (40 MHz) in the ISM (Industrial, Scientific and Medical) band and a relatively high EIRP (160 mW – 22 dBm), while UWB [1.7] is characterized by a large channel bandwidth (520 MHz) and a small EIRP (0.4 mW - -4 dBm), in order to not interfere with existing communication standards. Both 802.11 and UWB rely on complex modulation schemes (Orthogonal Frequency Division Multiplexing, OFDM), implemented in on-chip DSP, which require a lot of power to operate.

On the other hand, 60 GHz spectrum is characterized by a very large channel bandwidth (as we will see, standard proposal allocate around 2.5 GHz per channel) due to the lack of existing applications in these frequency bands and a very high EIRP (8 W – 39 dBm). The main reason behind this high transmit power is due to signal propagation characteristics at these frequency; recalling Friis transmission equation [1.8]:

$$P_r - P_t = G_r + G_t - \alpha + FSPL \qquad (1.2)$$

where P_r and P_t are the received and transmitted power (dBm), respectively, G_r and G_t are the antenna gain (dBi) of the receiving and transmitting antenna, respectively, α is the attenuation coefficient of the propagation medium (dB) and FSPL is the Free-Space Path Loss (dB), which can be expressed as:

$$\mathrm{FSPL} = 20\log_{10}\left(\frac{\lambda}{4\pi \mathrm{D}}\right) \tag{1.3}$$

where λ is the wavelength and D the distance between transmitting and receiving antenna. Since EIRP (dBm) can be expressed as:

$$\mathrm{EIRP} = \mathrm{P_t} + \mathrm{G_t} \tag{1.4}$$

we can rewrite (1.2) as:

$$\mathrm{P_r} = \mathrm{EIRP} + \mathrm{G_r} - \alpha + \mathrm{FSPL} \tag{1.5}$$

As frequency increase, for a fixed antenna area A, antenna gain increases proportionally to the square of frequency [1.8]:

$$\mathrm{G} \propto \frac{\mathrm{A}}{\lambda^2} \tag{1.6}$$

thus, at mm-Wave, it is possible to employ smaller antennas with higher directivity compared to lower frequencies (fig 1.3).

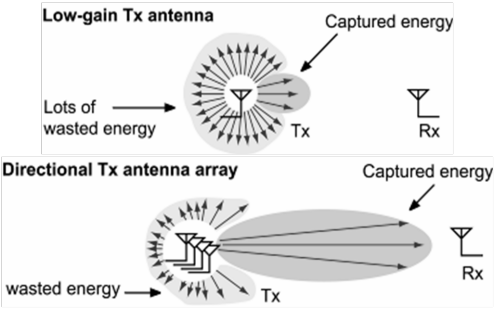


Fig 1.3 High Directivity antenna array

However, at higher frequency, air attenuation increases. In particular, at 60 GHz we have a peak of attenuation (see fig. 1.4) of about 15 dB/Km mainly due to Oxygen resonance. The situation is even worse in the case of rain or other adverse weather conditions; for this reason, long range transmission are difficult to realize; other frequency ranges (such as from 70 to 120 GHz) are more suited due to their lower attenuation. For medium-range transmission, however, this drawback can be seen as an advantage, giving a natural isolation between devices operation in the same frequency range and enabling frequency reuse by spatial isolation.

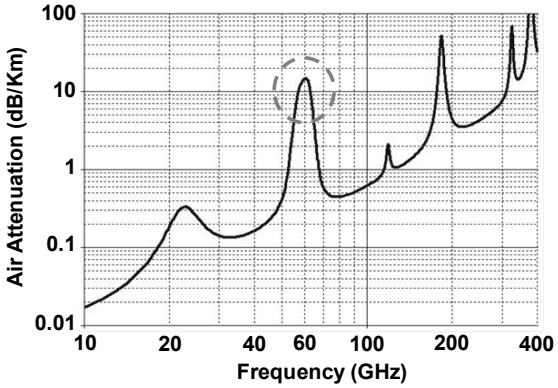


Fig 1.4 Air attenuation versus frequency.

On the contrary, for short range communications (~10 m) air attenuation becomes negligible; in this case FSPL is the main limit. In fact, by doing some easy math, we can conclude that, for a fixed distance D, FSPL at 60 GHz is 28 dB higher than in the case of Wi-Fi communications:

$$\Delta = 20\log_{10}\left(\frac{60}{2.4}\right) \cong 28\ \text{dB} \qquad (1.7)$$

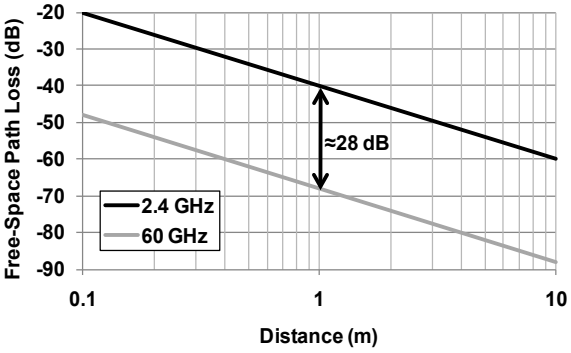


Fig 1.5 Free-Space Path Loss versus distance at 2.4 and 60 GHz.

Figure 1.5 shows FSPL versus distance at the frequency of 2.4 and 60 GHz. In order to compensate this difference in the link budget, we can use an higher power and antennas with higher gain (that is, higher EIRP and higher gain in the receiving antenna). Recalling that EIRPs for 802.11 and 60 GHz communications are 22 and 39 dBm, respectively, we can conclude that 17 dB can be recovered from higher 60 GHz EIRP [1.4]; the remaining 11 dB can easily come from receiving antenna. Moreover, the larger bandwidth can be used to increase data rate and relax complexity, employing less complicate modulation schemes.

Besides air attenuation, many objects may represent a serious obstacle to propagation at these frequencies (see fig. 1.6); moreover, this attenuation is often physically due to reflection. To overcome this problem, a possible solution is represented

by phased arrays [1.9], employing beam steering. By exploring different propagation paths, it is possible to reduce overall losses, exploiting multiple reflection to reach the designed device.

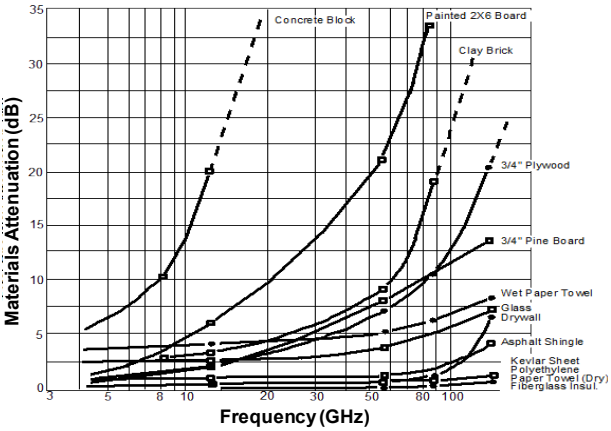


Fig 1.6 Attenuation versus frequency of various materials

Phased arrays can be created by integrating on the same silicon die different instantiations of receivers ad transmitters; recently, on-chip antennas have been proposed, along with complete phased arrays. This approach permits to increase transmitted power and sensitivity, at the cost of higher power consumption and occupied area. However, mainly due to substrate losses, integrate antennas suffer from low gain [1.10]; a possible solution is to employ external antennas, but this can lead to problems in creating a suitable package and in the interface between on-die circuits and on-package antennas.

1.2 Mm-Waves Applications

All the above considerations lead us to consider many applications in this unlicensed frequency range; large bandwidth can provide high data-rate communications, while small wavelength can be exploited in high resolution imagining and radar systems.

1.2.1 W-PAN and Wireless HDMI

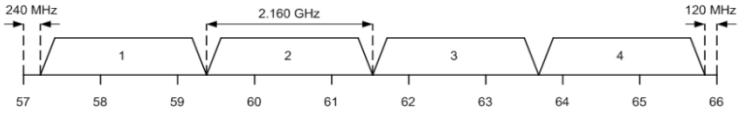


Fig 1.7 ECMA [1.11] standard proposal operation band frequencies

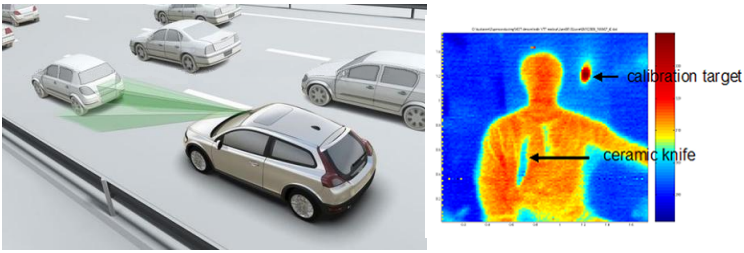
Industry group ECMA International recently announced a worldwide standard for the radio frequency (RF) technology that makes 60 GHz “multi-gigabit” data transfer possible. The specifications for this application [1.11], which involves chips capable of sending RF signals in the 60 GHz range, are expected to be published as an ISO standard in 2009.

The 57-66 GHz band is divided into 4 channel, each with a bandwidth of 2.160 GHz. Each channel is targeted to a data-rate able to sustain Full HD video (1080P) at 30 frames per second. The intention is to replace the HDMI cable between different devices, for example Full HD TVs and players. Alternatively, these 4 channels can be grouped in order to

sustain higher data rates, to reach the full 8.64 GHz bandwidth.

In this work, a Low Noise Amplifier (LNA) along with a full receiver targeted to this application, will be presented in Chapter 4.

1.2.2 Automotive Radars and Imaging



a) b)

Fig 1.8 Automotive anti-collision radar (a) and imaging applications (b)

The key development of automotive radars has been the dramatic reduction in area, cost and power for such a system. Until now, only luxury automobiles were equipped with mm – wave radars (with compound semiconductor technologies), but this situation is going to change soon: it's a matter of time before CMOS technology become industry standard for also this field of applications. Figure 1.8a shows a possible future road environment with driving assist features such as an anti-collision radar.

Promising technologies are radars at 24 and 77 GHz [1.12]. Radar is an all–weather sensor with approximately 5 cm resolution that operates in real time. The scanning RF signal, usually a pulse–shaped signal, is transmitted toward the target of interest. Information regarding shape, distance and speed of the target is embedded in the arrival time and shape of the reflected pulse. The FCC has allocated the 22 – 29 GHz band for short range automotive radar applications and the 76 – 77 GHz band for long range (100m) automatic cruise control automotive radar application [1.12].

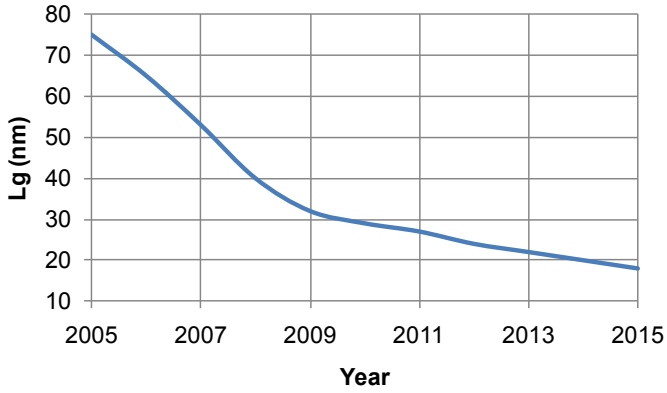
Another application is represented by passive mm-Wave imaging systems [1.13] that produce a picture of a scene by detecting thermally generated mm-Wave radiation (fig. 1.8b), usually in the range of 77 GHz. Systems using mm-Waves offer advantages over equivalent instruments detecting infrared and visible light because the mm-Wave radiation can penetrate low visibility and obscuring conditions (caused for example by clothing, walls, clouds, fog, dust smoke and sandstorms). Thus mm-Wave imaging systems could be used in a range of important applications such as medical diagnostics (such as skin cancer detection) [1.14], mapping of hotspots in bushfires and covert and/or overt surveillance for intruders, contraband and weapons.

1.3 Silicon CMOS: design challenges and opportunities

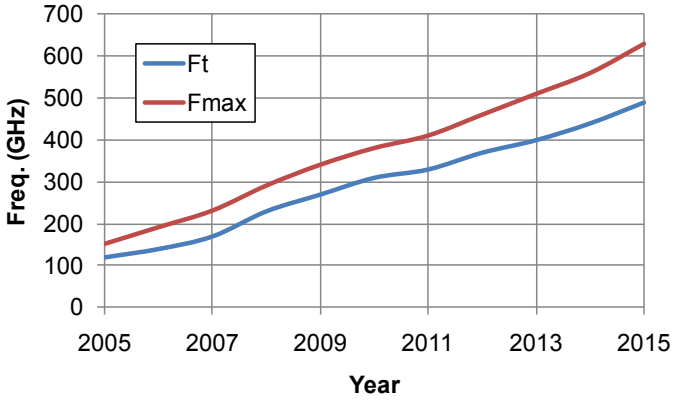
There are already products available in the mm-Wave frequency range. However, almost all this high frequencies applications are relatively expensive, employing technologies such as: GaAs, MESFETs, PHEMT, InP, HEMT, GaAs MHEMT, GaAs HBT, InP HBT. While these technologies offer good performances at high frequencies of operation, they are very expensive and have low manufacturing yields.

As for RF applications in the low GHz regime, the real breakthrough in mass market application will be represented by the use of lower–cost and higher–yield silicon technologies. This process will benefit from silicon steady scaling, mainly driven by the digital aim to reduce the cost per function. Transistors became small enough, and consequently fast enough, to operate at frequencies as high as 60 GHz. Now mm-Wave silicon circuits have been widely demonstrated starting with the 90 nm technology node [1.15, 1.16]. Despite many dire predictions about CMOS scaling, the scaling has continued down to the 32 nm technology node and it's still going on (fig. 1.8a). Moreover, integration of mm-Wave analog circuits with baseband processing on the same die will further lower packaging costs and power consumption.

However, it is necessary to employ new design methodologies to increase the operating frequency by a factor of 10 (in order to operate in the 60 GHz range), since the process Ft and Fmax [1.17] have only doubled in the last few technology steps (figure 1.8b) [1.18].



a)



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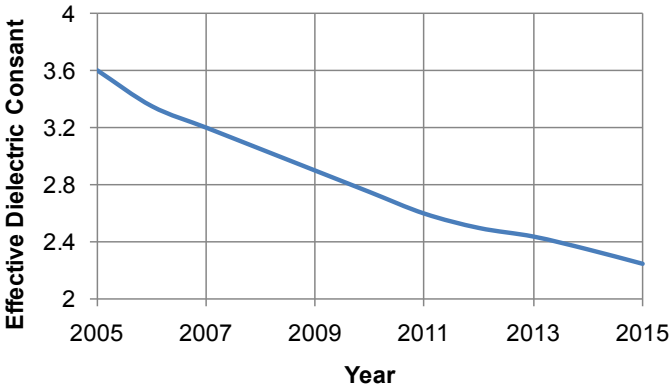

c)

Fig 1.9 Gate length L_g (a), process F_t and F_{max} [1.17] (b), and Effective Dielectric Constant (c) scaling with years.

These new design methodologies include careful modeling of both active components, employing full-wave simulations for distributed analysis and characterization of basic building blocks by means of extensive measurements. Both lumped and distributed elements components should be employed where necessary, and designers have to become familiar with standard RF and microwave design techniques, in order to exploit the “best of both worlds”.

Moreover, passive components such as inductors and transmission lines are getting even worse with scaling, since there is a strong trend in lowering metal and oxide thicknesses, due to materials and processes constraints. In order to not increase back-ends parasitics, the effective dielectric constant of oxide layer is lowered (see fig. 1.8c);

however, this strategy not only do not counterbalance the increased metal losses, but leads to higher substrate losses, due to the reduced distance between metal layers and bulk substrates. Thus, as it will be shown in Chapter 2, it is necessary to employ new structures in order to reduce (or even suppress) substrate losses. Besides, there's no inherent area advantage in using scaled technology nodes: in a common high frequency analog circuit, active area is very small compared with passives area, which only scales with frequency of operation.

Anyhow at the end of this paragraph it should be pointed out that when working with ultra-scaled devices we have to consider some inherent drawbacks: with technology scaling the intrinsic gain of transistors is getting lower and lower ($g_m/g_0 \approx 7$ with 65nm technology) and extremely low supply voltages mean severe limitations in the achievable voltage swing. Despite this, there is still motivation to continue to use newer scaled technology since smaller transistors will provide good performances, lowering power levels and enabling integration of more and more functions on the same silicon die. Moreover, analog performance will benefit from the introduction of new and more performing materials in transistor building, such as Metal Gates in 32 nm IBM technology [1.19].

1.4 Conclusions

What makes mm-Wave attractive is the possibility of high data-rate communication, targeted to short distance communication. A silicon CMOS implementation would be the ideal choice, due to the higher level of integration offered with a high yield, with lower costs and power dissipation in respect of less cheaper technologies.

Some solutions are already available; in particular, in this work a complete receiver for 60 GHz application will be shown; the main goal is the realization of a complete beam forming CMOS integrated phased array. Many challenges have to be overcome, both from system and design point of view. Moreover, the issues of packaging and the antenna integration problem is an open field of research for mm – wave designers.

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2

Integrated transmission lines design and optimization

In mm-wave on-chip applications, integrated transmission lines are mandatory to interconnect different blocks of the RF chip (e.g. LNAs, local oscillators, mixers, PAs). They are also attractive to implement on-chip functions such as matching sections, filters, baluns, which would require inductive components with very small values, typically in the range of 30-300 pH. Though in this scenario spiral inductors could result in small area occupation, being typically limited to one-turn structures, their value can be predicted with less accuracy. When many inductors connect to the same active device, not only the distribution net adds significant contribution to each spiral impedance but also mutual effects,

hard to be accurately predicted, become a significant source of error, especially when dealing with low inductors' values. All of these issues will be addressed in the next chapter.

Short-circuited line sections can effectively replace inductors at these frequencies, bringing some practical advantages. Line characterization can be performed on prototypes of arbitrary length, from which unit-length parameters can be easily obtained, in order to synthesize the required inductance value. This reduces the sensitivity to measurements uncertainties. Moreover, lines can be easily integrated in RFICs, since their cross-section is fixed, allowing standardized connections to active devices, while only their length is changed (and re-tuned) to achieve the required inductance.

Among the possible geometries, Coplanar Waveguide (CPW) lines have been widely adopted, thanks to some interesting features. In fact, compared to Microstrip (MS) lines, they offer more degrees of freedom (e.g. signal line width, line gap) to synthesize the target characteristic impedance, while allowing the optimization of other line parameters such as attenuation and phase velocity. Moreover, the two lateral ground conductors almost completely shield the signal line from other lines and inductors, allowing a compact integration of many inductive components on a small area without unwanted couplings.

Many papers have been published in recent years reporting various CPW lines topologies on different Silicon processes, providing performances comparable to spiral inductors, in terms of quality factor and occupied area.

A rigorous study of all loss sources is mandatory in order to optimize performances of CPW lines, and search new structures with minimum loss.

2.1 Coplanar Wave Guide

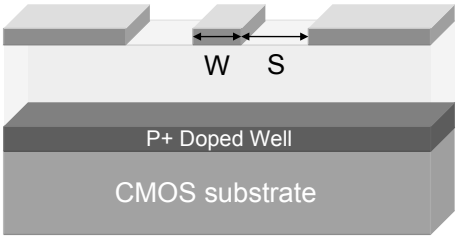

Fig. 2.1 Standard Coplanar Wave Guide transmission line. A P+ doped well is often introduced in order to prevent latch-up.

Figure 2.1 shows the geometry used to obtain a standard CPW. The two ground conductors and the signal line are realized on the top metal layer, which offers the lowest sheet resistance and highest distance from the substrate. Usually, a thin P+ doped well, with a substantially higher conductivity (about two order of magnitude), is created on top of the CMOS substrate, in order to prevent latch-up phenomena.

To achieve the desired characteristic impedance two parameters are available to the designer, i.e. the signal conductor width W and the gap distance S between signal and ground conductors. The design is made more complicate and achievable performances are limited by the need for a specified metal density at each metal level. Dummies in metal levels where signal and ground are drawn can limit realizable impedances, while those at other levels can impair performances.

The two main loss mechanisms in CPW are metal losses and substrate losses. Metal losses are due to the rather low conductivity of the metal used in the CMOS process and to their small thickness. Substrate losses are due to the short distance between metal and substrate and to substrate resistivity; hence, if a doped well is created under the CPW gaps, substrate losses can become dominant. Radiation and dielectric losses in the oxide layers are negligible with respect to substrate and metal losses for a typical CMOS process.

In principle, an optimum performance is expected as a compromise between metal and substrate losses. In fact, increasing the width of the signal conductor decreases metal losses, but larger gaps are needed to keep the impedance value constant, causing a reduction of field confinement in the low-loss oxide region and an increase of substrate losses.

A set of CPWs in a standard 65nm BULK CMOS process from STMicroelectronics (featuring 7 metal Cu layers, plus an Al metal cover layer) have been simulated, using the commercial simulator HFSS from Ansoft.

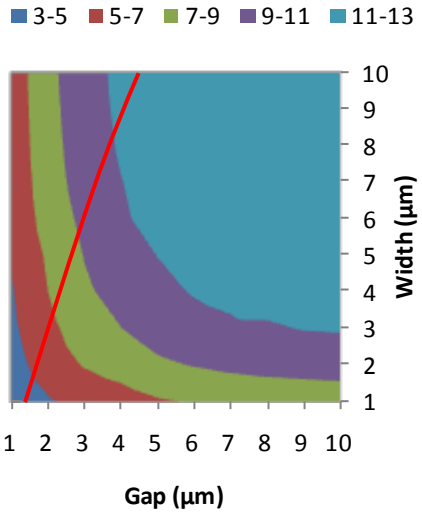

Fig. 2.2 Line quality factor [2.1] as function of W and S @ 60 GHz (substrate without a P+ doped well). Solid line correspond to 50 Ω CPWs.

Figure 2.2 shows line quality factor [2.1]:

$$Q_L = \beta / (2\alpha) \qquad (2.1)$$

at the frequency of 60 GHz, as function of W and S, in the case of a CMOS substrate without a P+ doped well. Solid line represents the locus of W and S that provides a constant 50 Ω impedance. The maximum feasible quality factor is around 12-13, with reasonable width and gap dimensions; larger values

of W and S would require dummies in order to maintain the minimum required density, thus impairing performances.

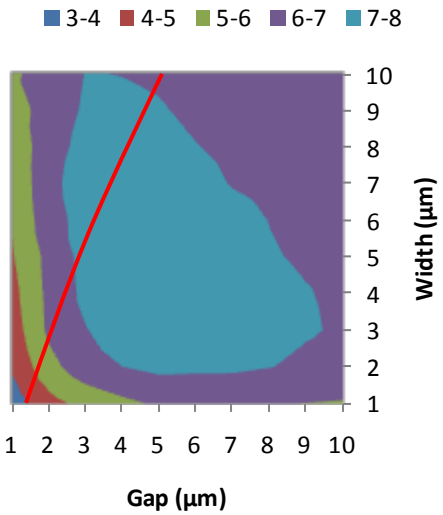

Fig. 2.3 Line quality factor [2.1] as function of W and S @ 60 GHz (substrate without a P+ doped well). Solid line correspond to 50 Ω CPWs.

When a doped well is created, attenuation increases and the optimum conditions to maximize quality factor strongly change (see Figure 2.3).

In fact, there is an optimum combination of W and S which maximizes the quality factor, balancing metal and substrate losses; in this case, however, the maximum quality factor drops to 8, well below the best achievable performance without P+ well.

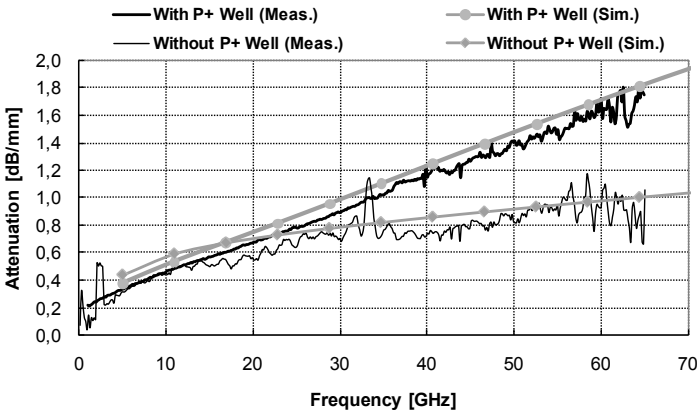

Fig. 2.4 Measured and simulated attenuation of a CPW on a substrate with and without P+ doped well.

Figure 2.4 plots the attenuation of a 50 Ω CPW with a fixed geometry (W = 9.5 μm, S = 4 μm) in the case of a substrate with and without a P+ doped well. Both simulations and measurements show that the P+ doped well gives a substantial contribution to substrate losses, in particular at higher frequencies. In fact, at 60 GHz the total loss is around 1 dB/mm without a P+ well, and increases to 1.7 dB/mm with a P+ well, almost doubling the total attenuation.

2.2 Shielded Transmission Lines

To reduce overall attenuation it is mandatory to reduce substrate losses, especially if a doped well is present; traditionally, this can be done employing a shielded transmission line. The first structure that can be used is a Microstrip (MS) line, whose ground plane totally shield the

ground conductor from the CMOS bulk substrate. The second possibility is to shield the CPW from substrate using a lower metal layer, thus creating the so-called Grounded Coplanar Waveguide (G-CPW) [2.2]. This approach can be effective in minimizing substrate losses; however, due to the characteristics of modern CMOS back-ends, it can lead to higher metal losses.

2.2.1 Microstrip

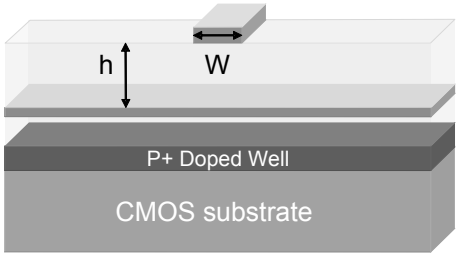

Fig. 2.5 Microstrip transmission line.

In a standard CMOS stackup the distance between metal layers cannot be modified; hence, once metal layers have been chosen, the distance between the bottom ground plane and the signal line (h, see Figure 2.5) is fixed (~4 μm). This is a serious drawback in a microstrip line (Fig. 2.5) design. In fact, once the desired characteristic impedance has been fixed, there is only one signal width which fulfils this requirement and thus, no possibility of optimization. The main advantage of this transmission line is the complete shielding from substrate losses; however, this usually comes at the

price of an increased resistance in the ground plane: in fact, the lowest metal layer is usually thinner (about five times thinner) compared to the higher metal layers, thus causing the current flowing into that ground plane to face a higher resistance, increasing total attenuation.

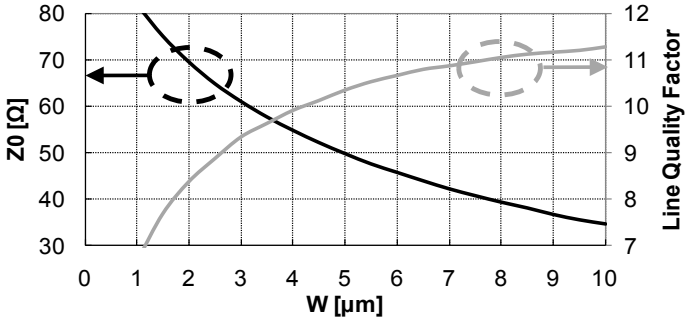

Fig. 2.6 Characteristic Impedance and Line Quality Factor of a microstrip line as function of line width W.

Simulations of a microstrip line for different line widths (Fig. 2.6) show that, with a 50 Ω target impedance, the necessary line width is 5 µm; in this case, line quality factor is slightly higher than 10, and attenuation is 1.2 dB/mm. So, what is gained by suppressing substrate losses is counterbalanced by increased metal losses, due both to reduced signal width and increased ground plane resistance.

2.2.2 Grounded Coplanar Waveguide

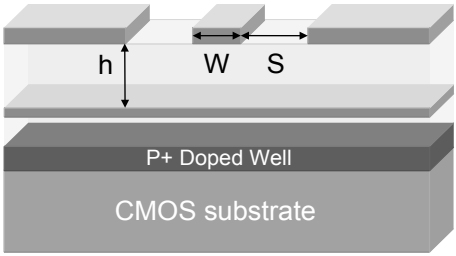

Fig. 2.7 Grounded Coplanar Wave Guide transmission line.

Since a G-CPW (Fig. 2.7) represents a mixture of a standard CPW and a MS [2.2], the ratio between W and h and between S and h strongly influences the EM field distribution [2.3] and the characteristics of the line.

	R (Ω/mm)	*L* (pH/mm)	*G* (mS/mm)	*C* (fF/mm)
CPW (w/out P+ well)	8.87	339	0.97	140
CPW (with P+ well)	9.02	339	4.04	151
G-CPW (M1 Ground)	9.15	229	0.04	187

Table I T-Lines RLGC Parameters at 60 GHz

The effect of adding a ground shield in Metal 1 to a standard CPW (W = 9.5 μm, S = 4 μm) is evidenced in Table I, which reports the RLGC line parameters [2.4] at 60 GHz. Parallel losses are almost completely suppressed (G ~ 0). This is not surprising because parallel losses are related to substrate losses, in particular to the effect of the P+ well.

The second effect is due to the interaction between the signal conductor and the new ground conductor, which results in a lower L and a higher C. This leads to a lower characteristic impedance (~35 Ω); in order to obtain a higher impedance, it is necessary to reduce the width of the signal line or increase the gap. In both cases, metal losses increase.

With a target impedance of 50 Ω, two solutions are possible; the first results in a G-CPW with W and S both equal to 3 μm. This geometry provides a quasi-TEM mode that is a mixture of a standard CPW mode and a MS mode; in fact, simulation shows that about 60% of the total return current flows in the top metal layers, while 40% flows in the lower metal layer. Attenuation is 1.55 dB/mm, mainly due to the reduced width of the signal line; substrate losses are almost suppressed, at a cost of higher metal losses. Line quality factor is 7.6. The second solution correspond to W = 5 μm and S = 10 μm. In this case the G-CPW practically degenerates into a MS; in fact, almost all return current flows in the lossy lower ground plane (~75%) instead of on the top ground planes (~25%). As a result, attenuation is 1.18 dB/mm and quality factor is 9.5, showing that total losses are still higher than a CPW without a P+ doped well.

2.2.3 Optimum substrate shield

A G-CPW is efficient in suppressing substrate losses, however, for a modern technology:

- h cannot be controlled;
- thickness of lower ground plane is very low, therefore its resistance is not negligible;
- the addition of a metal ground shield lowers L and increases C, thus lowering line impedance.

In order to realize an efficient substrate shielding, the optimum solution would be to suppress substrate losses without impairing L and C and without increasing total resistance.

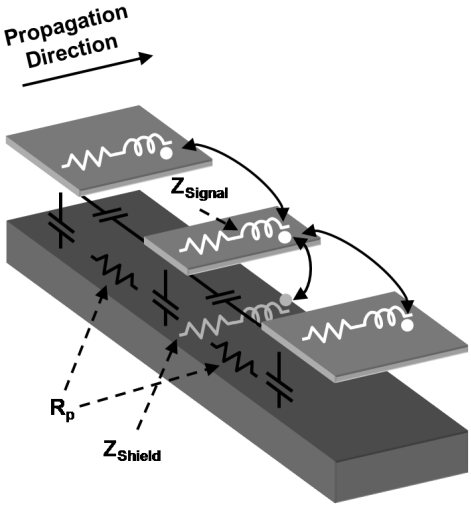

Fig. 2.8 CPW physical model

This is more clear considering a physical lumped element equivalent model for a standard CPW (Fig. 2.8). It has been proven [2.5] that, in order to suppress substrate losses, it is sufficient to lower the resistance R_p; this can be done with a G-CPW. However, this leads to a reduction of total inductance, since the mutual coupling between signal and shield conductors is positive and currents flowing in signal and shield are opposite. Moreover, total capacitance is increased, as total resistance (and thus line losses).

All the above considerations suggest that an efficient shield should increase conductivity in the direction orthogonal to signal propagation (that is, lowering R_p as much as possible), and provide a very high resistance along the propagation direction, in order to hamper as much as possible the return current flow on the shield (that is, providing an high Z_{Shield} without modifying Z_{Signal}). This would cause all ground return current to flow in the higher metal layer, which provides a low series resistance.

This concept has been proved with simulation in Ansoft HFSS, defining a shield with an anisotropic material with a high conductivity in the direction orthogonal to signal propagation (similar to Metal 1 conductivity), and a very low conductivity (~0) in the propagation direction; in this case, line quality factor is equal to 25, almost doubled in respect to CPW without the P+ doped well.

A way to realize such a shield is to employ a periodic shield, such a slotted structure on Metal 1, comprised of metal strips orthogonal to the propagation direction, connected to ground at some distance from the signal line (see fig. 2.9).

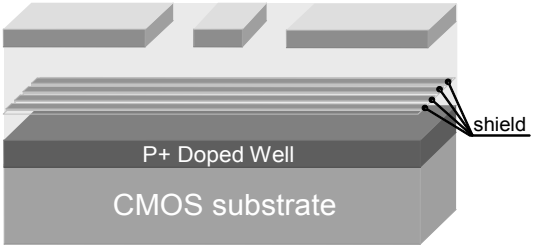

Fig. 2.9 Shielded CPW

The length and separation of the strips must be carefully optimized to enhance the shield efficiency. Since the resulting structure is periodic, its numerical simulation is more complicate than standard CPW analysis. This motivated the introduction of a new and efficient simulation method for periodic transmission line, presented in the following chapter. In this chapter the result of the design of two different kind of periodic lines, employing this simulation method, will be discussed. The first periodic CPW will be targeted to employ slow wave structure to maximize the phase constant in order to reduce the physical length of the transmission line for a given electrical length. The second line, exploiting a periodic shield, will be optimized in order to suppress substrate losses and to maximize the line quality factor. Measurements will be provided, validating the proposed simulation approach.

2.3 Design and Experimental Results

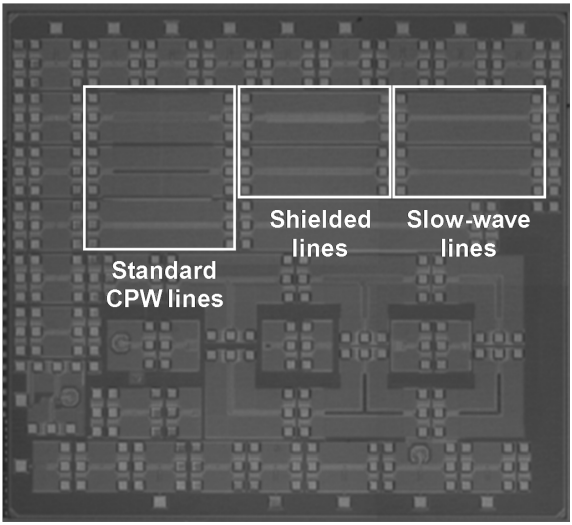

Fig. 2.10 Measured transmission lines chip photomicrograph.

All the lines were fabricated in the 65nm CMOS bulk process from STMicroelectronics (see paragraph 2.1). Figure 2.10 shows the chip photomicrograph. The lines were designed using the method exposed in the following chapter, employing the commercial simulator HFSS from Ansoft, and its "eigenmode" EM simulator engine in particular [2.7]. All the measurements were performed using Cascade Infinity Probes and an Anritsu VNA. Probe tips calibration was performed on a standard alumina substrate, and measurements were de-embedded by the Open-Short method [2.8].

2.3.1 Slow-Wave CPW Lines

Slow-wave CPW's are a result of a smart use of the dense stratification available in modern CMOS processes, to artificially increase the effective dielectric constant of the line. This is achieved, as shown in Figure 2.11, by adding equally spaced floating metal strips underneath the transmission line, to locally increase the line capacitance: as a result, phase velocity of the line is decreased. In addition, these strips help fulfilling the metal density rules mitigating the problem of introducing metal dummies.

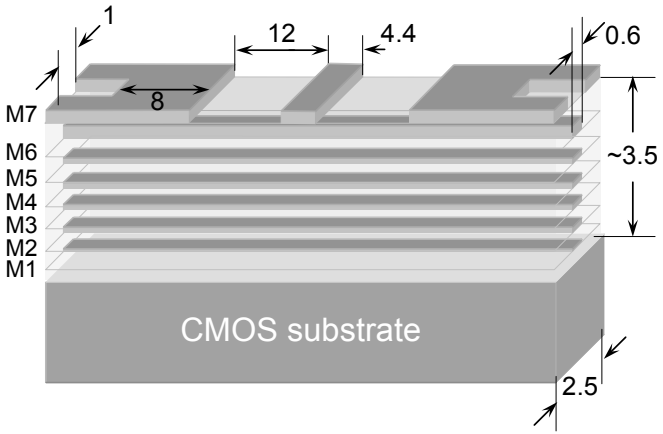

Fig. 2.11 Geometry of the proposed slow-wave CPW transmission line, detail of the cross section. Dimensions in μm (drawing not to scale).

Besides W and S, a slow-wave CPW offers two additional degrees of freedom i.e. the shield's metal strips width w_b and spacing s. These quantities define the period $d = w_b + s$ of the unit cell. W and S control the characteristic impedance, like in

a standard CPW. On the other hand, the values of w_b and s can be optimized in order to maximize shield efficiency and phase constant. These effects, however, are not simple to analyze with common methods. Relying on an accurate and fast simulation method, many simulations have been performed in order to gain more insight into slow-wave CPW design intended for matching networks, where the goal is maximum quality factor Q_L, maintaining a large value of the phase constant β for minimum area occupation. In these simulations, carried out at 60 GHz, fixed values of W = 4.4 μm and S = 12 μm were considered, allowing characteristic impedances close to 50Ω. These values are at the edge of the allowed range for density rules fulfillment, and were not changed even if the obtained characteristic impedance was less than 50Ω, since larger gaps violate design rules, and narrower line widths increase conductor losses too much.

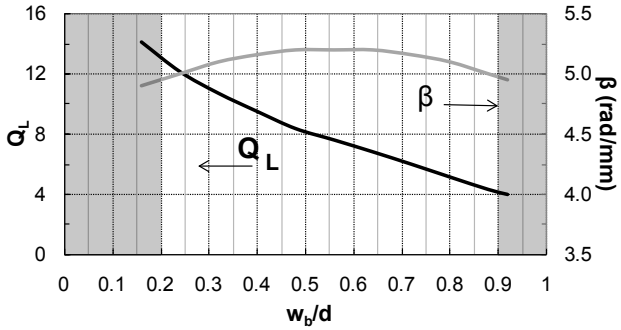

Fig. 2.12 Quality factor and phase constant of the slow-wave CPW transmission line at 60 GHz versus the ratio between strip width and unit cell period w_b/d for d = 2.5 μm. Shadowed regions correspond to geometries forbidden by design rules.

Figure 2.12 shows Q_L and β as a function of the ratio w_b/d for a fixed period d = 2.5 μm. It is evident that reducing w_b yields larger values of Q_L, without affecting β too much. Characteristic impedance varies between 45.6 Ω for w_b/d = 0.16 and 35.7 Ω for w_b/d = 0.92. Because the ratio w_b/d equals the metal density, not all values are possible (shaded regions in Figure 2.12 correspond to metal densities forbidden by design rules), and the smallest feasible value should be used.

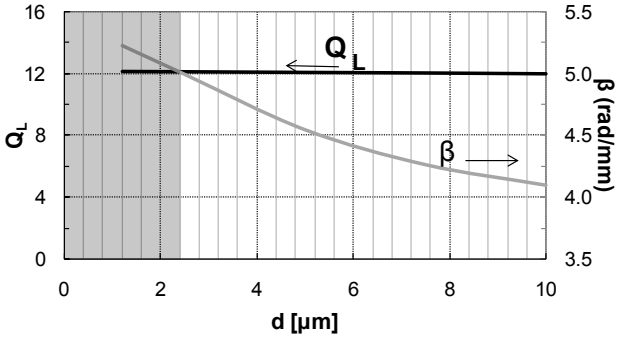

Fig. 2.13 Quality factor and phase constant of the slow-wave CPW transmission line at 60 GHz versus cell period d for w_b/d = 0.24. Shadowed regions correspond to geometries forbidden by design rules.

The effect of changing the unit cell period was also explored. Figure 2.13 shows Q_L and β as a function of d, assuming a fixed ratio w_b/d = 0.24, i.e. a value close to the minimum allowed. In this case β increases for small values of d, while Q_L remains constant. Also in this case design rules set a limit to the minimum periodicity, due to the smallest feasible width of the strips ($w_b \geq 0.5$ μm). The shaded region in the plot corresponds to forbidden line widths.

Characteristic impedance varies between 42.9 Ω for d = 1.2 μm and 51.9 Ω for d = 10 μm.

Based on these simulations, the slow-wave CPW with the dimensions reported in Figure 2.11 was implemented. The resulting characteristic impedance is about 45 Ω. Measurements, performed on prototypes and reported in Figure 2.14, show a very good agreement with simulations.

Note that α and β are almost doubled with respect to the standard CPW line, i.e. slow-wave CPW provide the same quality factor (Q_L at 60 GHz) as standard CPW, but they are suited to implement stubs and matching line sections using only half of the length, leading to a more compact circuit with unaltered performance. As a drawback, slow-wave lines usually require a larger cross-section for the same impedance as standard CPW line. Moreover, they allow increasing the capacitance per unit length, but the inductance is almost the same as for standard CPW lines: the range of feasible characteristic impedances is reduced with respect to standard CPW lines.

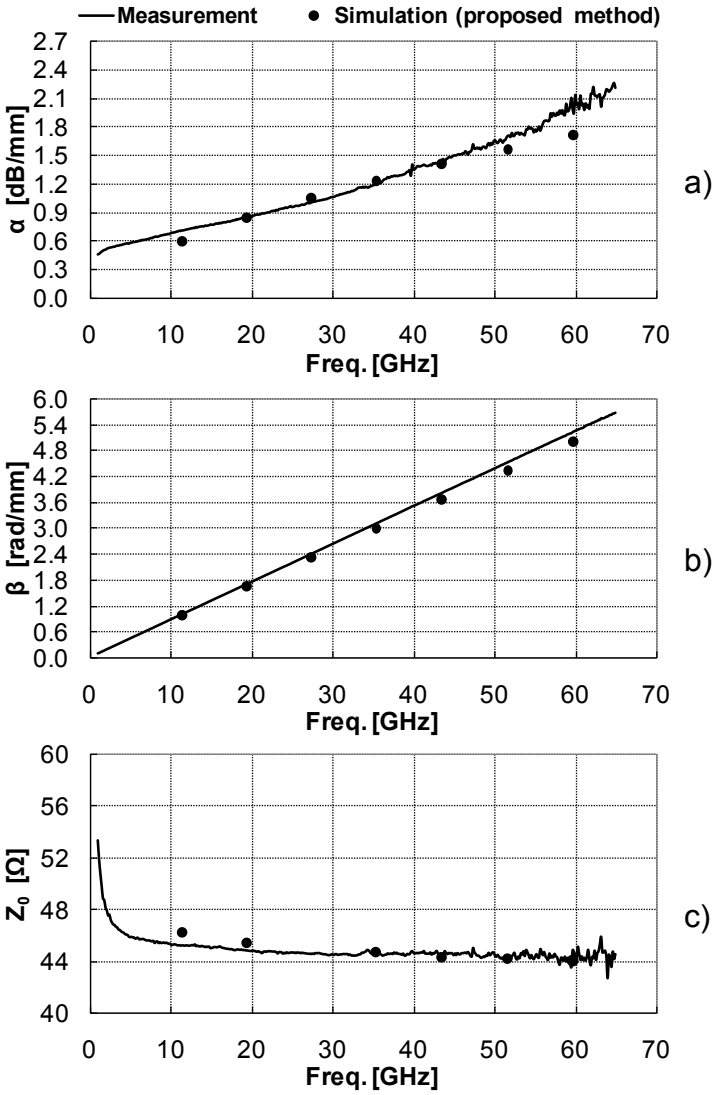

Fig. 2.14 a) Attenuation, b) phase constant, c) characteristic impedance vs. frequency for the slow-wave CPW shown in Figure 2.16; measurement (–) and simulation with the proposed method (●).

2.3.2 Shielded CPW Line

As pointed out in Section 2.1, in a standard CPW the EM field penetrates to some extent in the lossy CMOS substrate, contributing to the total attenuation factor. By simulating a standard CPW with a fictitious loss-free CMOS substrate, is has been found that in the CPW of Figure 2.1 the substrate losses are about 40% of the total. The obvious remedy to reduce substrate losses would be to resort to an additional shielding metal layer, e.g. realized in Metal 1, thus obtaining a G-CPW (see section 2.2.2) [2.9]. Unfortunately, this solution is not practical in our case, due to the small thickness of the oxide layers between Metal 1 and Metal 7 set by the CMOS process. In fact, a 50 Ω G-CPW designed in our process would have a maximum signal-line width W not much different from that of a MS, and a gap distance much larger than W (the structure would resemble more a MS-line than a G-CPW). In such a structure, a significant amount of longitudinal current would flow in the thinner bottom ground plane (Metal 1) rather than on the thicker top grounds (Metal 7), and the increase in metal losses would completely overwhelm the improvement in attenuation obtained by substrate shielding.

With these limitations in mind a different shielding structure was considered, inspired – to some extent – by the patterned ground used in shielded inductors, consisting of an array of thin metal strips realized in Metal 1, as shown in Figure 2.15, and connected to the top ground planes. Actually, this screen

can be seen as an equivalent bottom ground-plane with anisotropic resistivity (very high resistivity in the propagation direction, relatively low resistivity in the orthogonal direction), which prevents the flow of longitudinal currents, still providing a good shielding of the substrate.

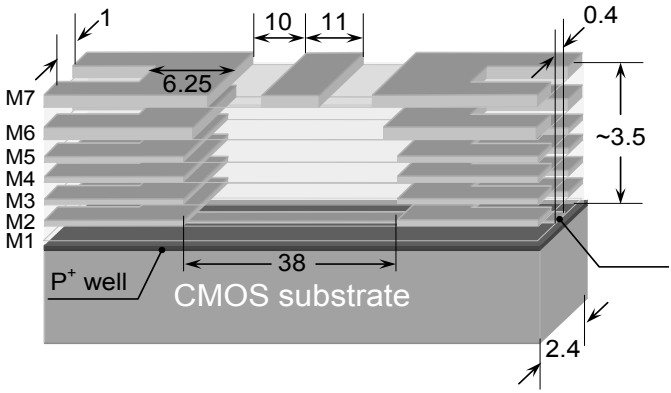

Fig. 2.15 Geometry of the proposed shielded CPW transmission line, detail of the cross section. Dimensions in μm (drawing not to scale).

Metal strips geometry must be carefully optimized to obtain the maximum shielding efficiency, without introducing additional source of losses. As for the slow-wave CPW line, simulations were performed at 60 GHz, to analyze the effects of metal strip width w_b and periodicity d for W = 11μm, S = 10 μm. The results are reported in Figures 2.16, which show Q_L and β as a function of the ratio w_b/d for a fixed d = 2.4 μm and of d for a fixed value of w_b/d = 0.17, respectively.

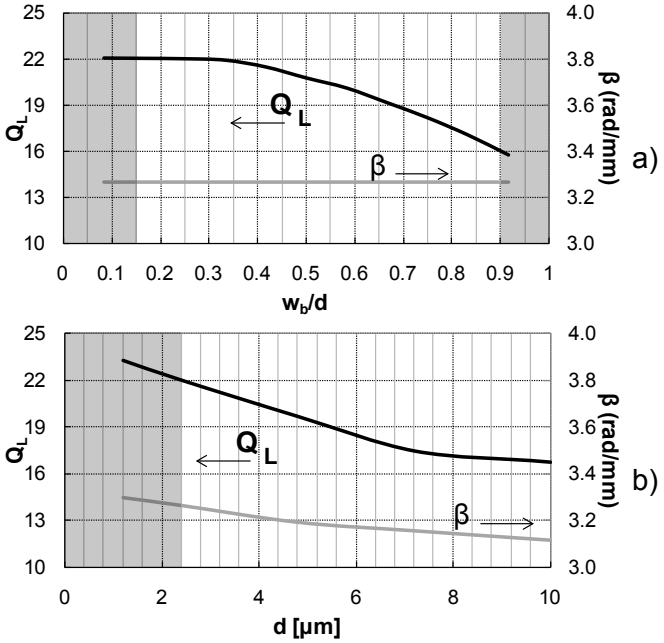

Fig. 2.16 Quality factor and phase constant of the shielded CPW transmission line at 60 GHz: a) versus the ratio between strip width and unit cell period w_b/d for d = 2.4 μm; b) versus period d for w_b/d = 0.17. Shadowed regions correspond to geometries forbidden by design rules.

Again, shaded regions correspond to geometries forbidden by design rules. Plots show that the narrower the strips and the shorter the period, the higher Q_L, β being less sensitive to the shield geometry. Characteristic impedance ranges from 49.3 Ω to 52.5 Ω for the geometries considered in the plots.

According to these considerations, a shielded-CPW (S-CPW) with the geometry shown in Figure 2.15 was realized. After optimization, W = 11 μm, S = 10 μm, w_b = 0.4 μm and d = 2.4 μm were chosen, in order to maximize Q_L, β and to obtain a 50 Ω characteristic impedance. Note that in this case a

characteristic impedance of 50 Ω was obtained, without violating design rules. The strips were connected to the top ground planes and to the other dummy fills by vias displaced by 27 μm from the structure centerline (for simplicity, vias are not shown in the figure). To better validate the effectiveness of the proposed S-CPW line, P+ well was generated under the line in order to verify the shielding efficiency in the case where the substrate produces the worst impairment of attenuation.
Figure 2.17 shows the good agreement between measured and simulated results. For comparison, also simulation results of the S-CPW on a substrate without P+ well are reported, showing only a marginal improvement in attenuation (about 0.02 dB/mm), thus confirming the high shielding efficiency of the proposed structure).

The S-CPW shows an attenuation of 0.65 dB/mm at 60 GHz, i.e. a 30% improvement over standard CPW line. The shield affects also the phase constant of the S-CPW, which is increased by a 25% with respect to CPW. Consequently, the S-CPW features a quality factor Q_L = 22 at 60 GHz, a figure almost doubled with respect to the CPW (Q_L = 12 at 60 GHz). Additional simulations considering the same shielding structure with substrate contacts under the bottom metal bars show that also in this case line performance remains unaltered, confirming that no return currents flow in the lossy substrate.

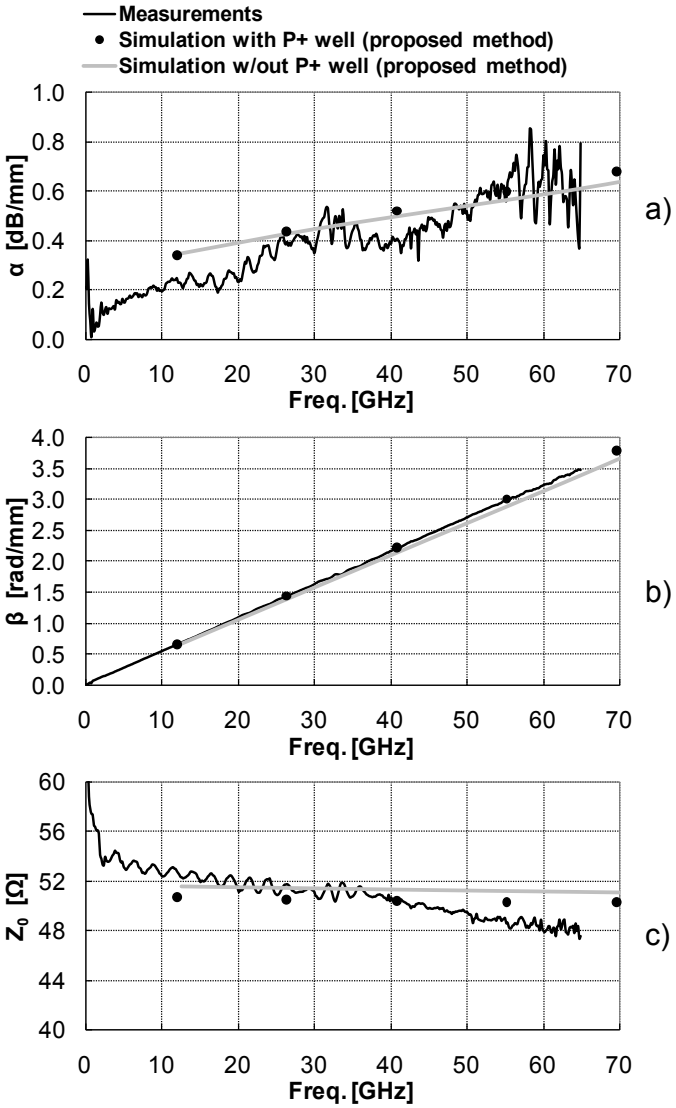

Fig. 2.17 a) Attenuation, b) phase constant, c) characteristic impedance vs. frequency for the shielded CPW shown in Figure 10; measurement (–) and simulation with the proposed method (●).

2.4 Conclusions

In this chapter, a rigorous analysis of integrated transmission lines has been carried out. Leveraging modern 3D E.M. simulators, it has been possible to consider various geometries, optimizing the design in order to reduce transmission line losses. Thanks to this analysis, it has been possible to chose a suitable structure to either optimize the phase constant or the line attenuation. All the exposed concepts have been validated through measurements of fabricated prototypes. Finally, Table II compares performances of the realized CPW lines versus state of the art of integrated transmission lines of the same 50 Ω characteristic impedance. Noteworthy, although implemented in standard bulk CMOS, shielded CPW are comparable with lines realized in SiGe, SOI and high resistivity CMOS substrates [2.10-2.15].

REF	Technology	Line type	α @ 60 GHz [dB/mm]
[2.20]	Intel CMOS 90nm High-Resistivity (HR) Substrate	MS	1.2
[2.20]	Intel CMOS 90nm HR	CPW	0.6
[2.21]	ST CMOS 90nm BULK	G-CPW	1.1
[2.22]	ST CMOS 130nm SOI	CPW	0.65
[2.23]	IBM SiGe 130nm	MS	0.8
[2.24]	ST CMOS 65nm SOI	CPW	0.7
[2.25]	ST SiGe 130nm - thick copper metal option	MS	0.5
This work	ST CMOS 65nm BULK	CPW	1
This work	ST CMOS 65nm BULK	Shielded-CPW	0.65

Table II State of the art of 50 Ω integrated transmission line.

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3

Simulations of periodic transmission lines

Standard transmission lines are usually uniform structures, i.e. their cross-section is constant along the propagation direction. In this case the propagation characteristics of the line can be derived considering its cross-section only, by using a 2D EM analysis method [3.1]. On the other hand, lines realized in ultra-scaled CMOS technologies are usually periodic, rather than uniform, the periodicity being introduced intentionally, as in the slow-wave line shown in Figure 3.1a, or resulting from technological constraints, e.g. when a usually periodic pattern of dummy metals cells is introduced in order to guarantee IC planarity, as shown in Figure 3.1b. In these cases, 2D EM analysis methods cannot be used, or may prove inaccurate

whenever dummy metals cannot be placed far enough from line's conductors.

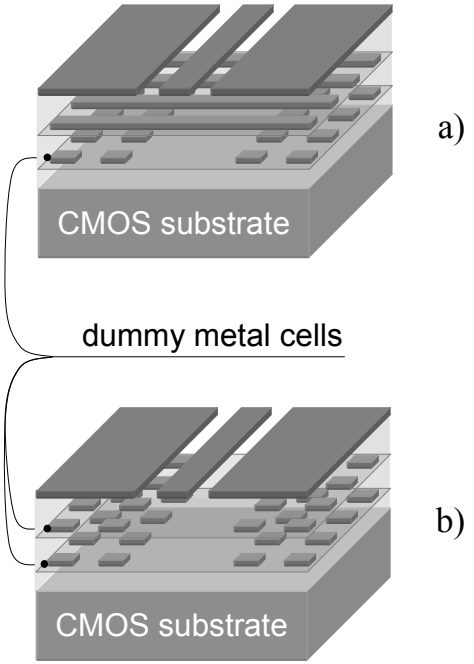

Fig. 3.1 Transmission lines in scaled CMOS: slow-wave CPW (a), and standard CPW (b).

3D EM analysis – leading to the representation of a line section in terms of scattering parameters from which its propagation characteristics are deduced – may require very long simulation times and memory resources, due to the huge number of unknowns resulting from the discretization of a large structure with fine geometrical details. Moreover, a multi-modal representation of the structure and/or sophisticated de-embedding techniques are often needed, since dummy cells

and metal bars represent discontinuities very close to the reference sections of the ports, thus exciting higher-order modes [3.2]. Accuracy can be improved by considering longer line sections or a higher number of propagation modes on the port sections but this has an enormous impact on simulation time.

In this chapter a different approach, based on the periodic nature of the lines, is proposed, in order to speed-up simulation without loss of accuracy.

3.1 Unit Cell Analysis

Propagation characteristics of periodic structures can be studied by considering their "unit cell", enclosed by periodic boundaries defined on surfaces normal to the propagation direction (see Figure 3.2). This approach has been followed to characterize periodically screened coplanar waveguides on semi-insulating GaAs substrate in [3.3], where the unit cell was analyzed according to circuit theory, by simply cascading short sections of CPW with and without metal bars, represented by their ABCD matrices. In this chapter this approach will be extended to the full-wave electromagnetic analysis of the unit cell, in order to consider all the discontinuity effects that cannot be accounted for by a circuit analysis.

3.1.1 Standard Floquet Analysis

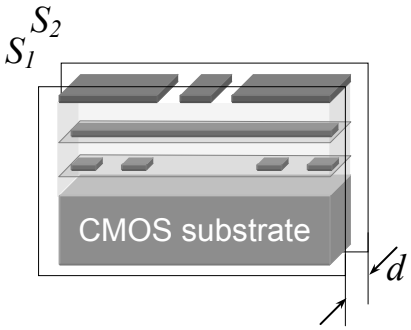

Fig. 3.2 Transmission line characteristics can be obtained from unit cell analysis.

According to Floquet's theorem [3.4], the problem can be formulated in order to find an EM field (Floquet's mode), solution of the Maxwell's equations inside the unit cell, which satisfies the following periodicity condition:

$$\vec{E}_2 = \vec{E}_1 e^{-\gamma d} \qquad \vec{H}_2 = \vec{H}_1 e^{-\gamma d} \tag{3.1}$$

where γ is the complex propagation constant, $\vec{E}_1, \vec{H}_1, \vec{E}_2, \vec{H}_2$ are the electric and magnetic fields on surfaces S_1 and S_2, and d is the length of the unit cell (see Figure 3.2).

The standard procedure for determining Floquet's modes and their propagation constants consists in finding, at a given (angular) frequency ω, a matrix relationship between the discretized fields on S_1 and S_2, and determining the propagation constant as an eigenvalue of that matrix [3.5]

(since we are interested in the quasi-TEM mode of the periodic structure, only the first eigenvalue must be evaluated). Repeating the procedure for different values of ω, the dispersion curve $\gamma = \gamma(\omega)$ of the quasi-TEM mode can be obtained. Unfortunately this procedure cannot be applied in conjunction with commercial EM solvers (e.g. Ansoft HFSS^{TM}), since they usually do not provide the system matrices generated during the solution (FEM matrices, in the case of HFSS). Therefore, specialized solvers must be developed [3.6], [3.7].

3.1.2 Extension to general-purpose E.M. solvers

In order to be able to exploit the flexibility of commercial electromagnetic solvers, HFSS in particular, a different procedure for finding the dispersion curve of the quasi-TEM Floquet's mode of the structure has been adopted. The approach is similar to the one described in [3.7] in the context of a Finite-Difference Frequency-Domain algorithm, and consists in considering an equivalent resonant-cavity model of the periodic cell, obtained by imposing the following periodic boundary conditions on surfaces S_1 and S_2 :

$$\vec{E}_2 = \vec{E}_1 e^{-j\theta} \qquad \vec{H}_2 = \vec{H}_1 e^{-j\theta} \tag{3.2}$$

where θ is a given periodic phase shift. As discussed in [3.7], the complex propagation constant $\gamma = \alpha + j\beta$ of the quasi-TEM

mode of the periodic structure is deduced from the complex resonant frequency $\Omega = \omega_r + j\omega_i$ of the first mode of the cavity obtained by solving a suitable eigenvalue problem. When the periodic structure can be considered lossless, the procedure is straightforward, since in this case γ is imaginary ($\gamma = j\beta$) and Ω is real ($\Omega = \omega_r$), ω_r representing the frequency at which the fields of the quasi-TEM mode satisfy the periodicity condition (3.2). Therefore the value of β at ω_r is simply given by $\beta = \theta/d$. Actually, in the lossless case the two procedures are equivalent, the only difference being how the $\omega - \beta$ diagram is obtained, i.e. finding β for a given ω when using the standard procedure, or finding ω for a given $\beta = \theta/d$ when using the equivalent resonant-cavity model. When losses cannot be ignored, as in the case of CMOS transmission lines, the eigensolution inside the equivalent resonant-cavity model is in terms of damped quasi-sinusoidal fields, and therefore the eigenvalue Ω is complex. Its real part has the same meaning as in the lossless case (and thus the $\omega - \beta$ diagram is obtained in the same way as before), whereas the imaginary part accounts for the damping which, according to the theory of resonant cavities, can be expressed in terms of the well-known "quality factor" [3.8]

$$Q = \frac{\omega_r}{2\omega_i} \tag{3.3}$$

Moreover, it is possible to translate the time-domain damping factor Q into a distance-related attenuation factor α, i.e. into

the real part of the propagation constant of the quasi-TEM Floquet's mode [3.7], [3.10]:

$$\alpha = \frac{v_p}{v_g}\frac{\beta}{2Q} \tag{3.4}$$

where $v_p = \omega / \beta$ and $v_g = \partial\omega / \partial\beta$ are the phase- and group-velocity of the mode, respectively. Equation (3.4) can be simplified in our case, since very low dispersion is expected for the quasi-TEM mode, and β has an almost linear dependence on ω. If this condition holds, $v_p \approx v_g$, and from (3.3) and (3.4):

$$\alpha = \beta\frac{\omega_i}{\omega_r} = \frac{\theta}{d}\frac{\omega_i}{\omega_r} \tag{3.5}$$

Note that Equation (3.5) is consistent with the usual definition of the quality factor of a transmission line (2.1) [3.9]:

$$Q_l = \frac{\beta}{2\alpha} \tag{3.6}$$

The procedure described above can be easily implemented by using HFSS as EM solution engine. In fact, condition (3.2) can be imposed by using a "Master-Slave" boundary condition [3.10] on surfaces S_1 and S_2 of the unit cell, assigning a given value $\overline{\theta}$ for the periodic phase shift. To calculate the propagation constant at a target frequency ω, an initial value of $\overline{\theta} = \omega\sqrt{\varepsilon_r}\,d / c$ is chosen, where c is the velocity of light

and ε_r is the relative dielectric constant of the oxide. Then the structure is analyzed by using the so-called "eigenvalue solution", in order to find the first (i.e. smallest magnitude) eigenvalue $\bar{\Omega} = \bar{\omega}_r + j\bar{\omega}_i$. Its real part gives the value of the frequency corresponding to $\bar{\beta} = \bar{\theta}/d$ and (3.5) is used to calculate α at $\bar{\omega}_r$. By iterating the procedure for different values of $\bar{\theta}$, the dispersion and the attenuation curves of the periodic line in a given frequency range is obtained.

3.1.3 Characteristic impedance calculation

Finally, the resonant electric and magnetic fields $\vec{E}_r$ and $\vec{H}_r$, obtained as eigensolution associated with the eigenvalue $\bar{\Omega}$ found for any value of $\bar{\theta}$, can be used to calculate the characteristic impedance of the quasi-TEM mode at ω_r. The possible definitions of characteristic impedance are in terms of the voltage and current (Z_{VI}), power and voltage (Z_{PV}), or power and current (Z_{PI}) [3.11]

$$Z_{VI} = \frac{V}{I} \qquad Z_{PV} = \frac{|V|^2}{2P^*} \qquad Z_{PI} = \frac{2P}{|I|^2} \tag{3.7}$$

where V, I have the usual meaning, P is the complex power and "*" denotes the complex conjugate. These quantities can

be easily evaluated by using the "Field Calculator" of HFSS [3.12]:

$$V = \int_{\ell} \vec{E}_r \cdot d\vec{l} \qquad I = \oint_{C} \vec{H}_r \cdot d\vec{c} \qquad P = \frac{1}{2}\int_{S} \vec{E}_r \times \vec{H}_r^{*} \cdot \hat{z}\, ds \tag{3.8}$$

where ℓ and C, shown in Figure 3.3, are suitable integration path defined on the surface S (which may coincide with either S_1 or S_2), and $\hat{z}$ is the normal to S. For MS's or CPW's the most used impedance definition is Z_{PI}, but all the definitions in (3.7) provide similar results, in the range of a few percent.

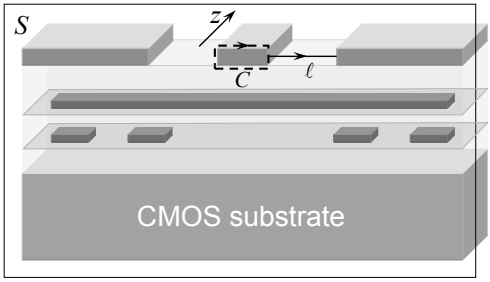

Fig. 3.3 Definition of integration paths for voltage (ℓ) and current (C) determination on CPW section.

Note that, in finding the impedance of the periodic line, the resonant fields of the equivalent resonant-cavity model are used, instead of those of the true Floquet's mode, as it would be required by the theory of periodic structures. Actually, the two fields are slightly different, the former having the same magnitude at both ends of the unit cell (see Equation (3.2)), the latter accounting also for the attenuation across the unit cell (see Equation (3.1)). Therefore, only approximated values

of the impedance can be obtained by the equivalent resonant-cavity model. However, from a practical point of view, the accuracy in estimating the impedance is better than a few percent, provided the attenuation-per-unit cell is reasonably small, e.g. less than 0.01 dB per cell, a condition that applies in any line of practical use.

3.2 Proposed method validation

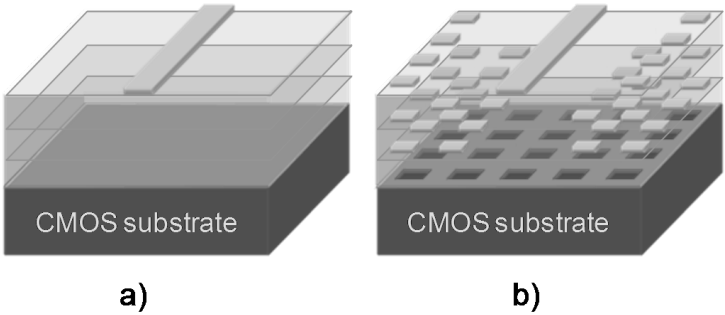

Fig. 3.4 Validation test case. Standard homogenous MS line a) and MS Line with a perforated (periodic) ground plane and dummies.

In order to validate this procedure, a uniform 50 Ω MS transmission line has been simulated, assuming the process parameters of a 65nm CMOS process from STMicroelectronics, featuring 7 metal Cu layers plus an Al metal cover layer. Signal line is in Metal 7 and a solid ground is obtained shunting Metal 1 and 2 together (see Figure 3.4a). This structure, though not compliant with metal density design rules, has been selected since it can be analyzed either by conventional 2D method or by the equivalent resonant-cavity model, defining a fictitious periodicity (d = 1 μm in this case).

Figure 3.5 shows the attenuation, the phase constant and the characteristic impedance as a function of frequency, comparing the results of our method vs. the 2D method of the commercial simulator HFSS. An excellent agreement emerges. To fulfill metal density rules for process planarity, a periodically perforated ground plane has then been introduced (see Figure 3.4b), by using a configuration similar to the one introduced in [3.13] (metal strips of 0.55 μm in the longitudinal and transverse direction; square holes 0.45 μm x 0.45 μm). The MS line is not uniform anymore, but still periodic, with the same period of 1 μm as before. In this case, 2D simulators cannot be adopted while our method can. Results for the periodic MS line are also reported in Figure 3.5. At 60 GHz the design-rule compliant MS line features an attenuation constant of 1.2 dB/mm and a quality factor of 9.2. Note that the slots do not significantly influence the characteristic impedance, since they are much shorter than the wavelength, but they increase the attenuation constant of the MS.

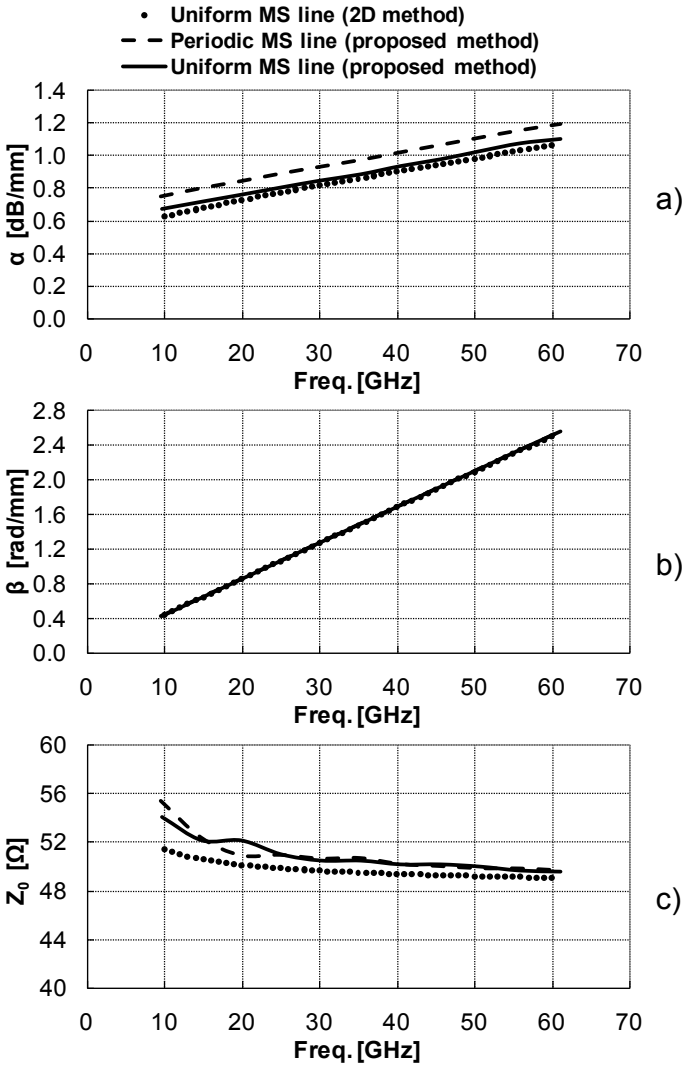

Fig. 3.5 a) Attenuation, b) phase constant, c) characteristic impedance vs. frequency for a MS line. Simulations assuming a uniform line have been performed both by means of 2D simulator (•) and proposed cavity -resonant model (–). Simulations of periodic structures (i.e. perforated ground plane) with proposed model are also reported (— —).

3.3 Conclusions

The developed simulation method proves to be fast and accurate. As previously discussed, 2D simulators are also accurate and fast, but they can be applied to uniform structures only. On the contrary, 3D conventional methods not leveraging the periodicity of the line, require a huge amount of computational resources for an accurate result. As a final example, the shielded CPW of Chapter 2 has been simulated by means of a conventional 3D simulator. In particular, line sections consisting of a variable number of unit cells have been considered. Increasing the number of cells, the results of the 3D method tends to those of the proposed method, of course at the expense of simulation time and required memory. Table II summarizes the results.

Number of Unit Cells	Memory [MB]	CPU Time [s]	α @ 60 GHz [dB/mm]	β @ 60 GHz [rad/mm]	Z_0 @ 60 GHz [Ω]
3D Method					
1	85	36	4.00	3.87	40.60
4	830	257	2.83	3.73	42.69
7	1260	466	1.63	3.69	43.41
10	2410	1092	0.70	3.70	42.35
13	3040	1359	0.66	3.54	45.39
Proposed Method					
1	148	300	0.65	3.33	48.70

Table I Comparison between 3D modal analysis and proposed resonant cavity model.

Note that a conventional 3D simulation of a line section consisting of 13 unit cells still provides results with an error of more than 6% in the characteristic impedance while requiring tens of minutes and some GB of memory. This suggests that an improved accuracy would require a prohibitive computational effort.

Finally, Table II reports simulation time and memory for a single frequency point for the validation case in Section 3.2 and the transmission lines considered in Chapter 2, in the case of a PC using an Intel Core 2 Duo T7250 processor.

	Time [s]	Memory [Mb]
MS Line (Section 3.2)	212	84
CPW (Section 2.1)	330	150
Slow-Wave CPW (Section 2.3.1)	320	163
Shielded CPW (Section 2.3.2)	300	148

Table II Simulation time and memory for the validation case in Section 3.2 and the transmission lines considered in Chapter 2.

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4

mm-Wave passive components modeling

In order to simplify the design process, a good modeling strategy is mandatory. One of the main issue in creating models is to provide equivalent circuits valid both in the time and frequency domain, in order to be able to perform complicate system simulation that involve both transient response and frequency translation. On the other hand, with the increasing level of integration, cross talk between blocks can impair circuit performances, especially at very high frequencies. Thus, it is necessary to develop strategies able to mitigate this phenomena, and to correctly model them when they are not negligible.

Spiral inductors occupy a significant area and are in close proximity with each other. Electromagnetic coupling among

integrated inductors is thus a potential major source of interference. While there are several accurate models for single inductors (which take into account several physical effects, such as skin effect, substrate-induced currents, and current crowding [4.1-4.2]), there is a lack of models to correctly reproduce the coupling between two (or more) inductors on silicon.

On the other hand, transmission lines become attractive at high frequencies to synthesize inductive reactances, and in particular cases (such as Coplanar Waveguides), thanks to their well confined EM field, they are intrinsically isolated from adjacent structures.

A mixed approach, employing both lumped element circuits (that is, spiral inductors) and distributed elements (such as transmission lines) is mandatory in order to obtain the "best of both worlds".

In this chapter the derivation and the validation of an accurate equivalent circuit for the wide-band modeling of a single inductor will be addressed. This model will then be extended to correctly reproduce the cross talk among symmetrical spiral inductors on CMOS substrate.

Furthermore, as it will be show, this equivalent circuit will be used in the case of low-values inductors, such as the ones employed at mm-Wave frequencies, and to create a compact and scalable model of a generic transmission line.

Finally, the described modeling techniques will be applied on a real test case, that is a receiver targeted for mm-Wave

applications. The good agreement between simulations and measurements will validate the proposed modeling approach, giving a solid base to the design process.

4.1 Integrated inductors modeling

Let us consider the symmetric inductor depicted in Figure 4.1. Usually, this device is connected to the circuit through five nodes, i.e., the coil ends (nodes 1 and 2), the coil center tap (node 3), the bulk (node 4), and the shield (node 5).

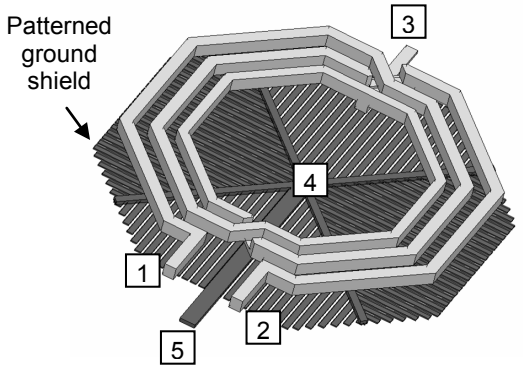

Fig. 4.1 3D view of a symmetric inductor. Nodes 1 and 2 indicate the coil ends, node 3 corresponds to the center tap, node 4 to the bulk and node 5 represents the shield tap.

Figure 4.2 shows a lumped-element model of a single symmetric inductor. Though quite simple, this model has been selected since all its elements are frequency-independent and their values can be easily calculated by means of quasi-static simulators such as Ansoft Q3D, or Asitic [4.2]. We have:

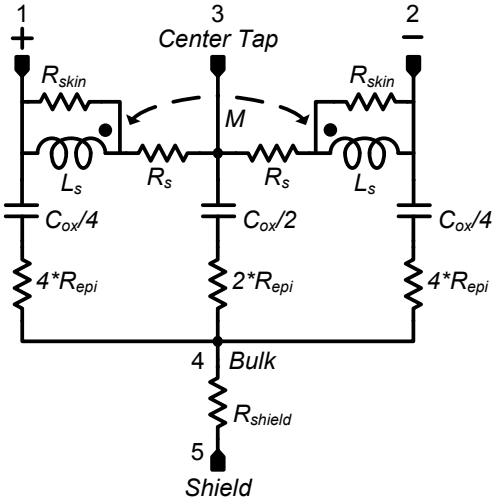

Fig. 4.2 Single inductor lumped element model

$$R_s = \lim_{\omega \to 0} \mathrm{Re}\left(Z_{1,3}\right) \tag{4.1}$$

$$L_s = \lim_{\omega \to 0} \frac{\mathrm{Im}\left(Z_{1,3}\right)}{\omega} \tag{4.2}$$

$$M = \lim_{\omega \to 0} \frac{\mathrm{Im}\left(Z_{1,2}\right)}{2\omega} - L_s \tag{4.3}$$

$$R_{epi} = \lim_{\omega \to 0} \mathrm{Re}\left(Z_{1//2//3,4}\right) \tag{4.4}$$

$$C_{ox} = -\lim_{\omega \to 0} \frac{1}{\mathrm{Im}\left(Z_{1//2//3,4}\right)\omega} \tag{4.5}$$

$$R_{shield} = \lim_{\omega \to 0} \mathrm{Re}\left(Z_{4,5}\right) \tag{4.6}$$

where $Z_{(m,n)}$ denote the impedance seen between nodes m and n, with the other nodes floating, and $Z_{(1//2//3,4)}$ indicates the impedance seen between node 4 and nodes 1, 2, 3 shorted together. R_{skin} is the only term which is deduced from the fitting

of the high-frequency response of the inductor, obtained from full-wave simulations.

Note that the symmetry of the inductor is reflected in the model, and that the total inductance is given by the self-inductance of the two coils plus the mutual inductance M.

4.1.1 Inductors measurements and model validation

The double-π type scheme obtained in this way correctly models the inductor behavior under both single-ended (i.e., when node 1 or node 2 is shorted to node 5) and differential excitations. This is shown in Figs. 4.3 and 4.4 respectively, for the case of a three-turn symmetric inductor with patterned ground shield (diameter = 340 μm, inductance = 4 nH) fabricated in a CMOS065 technology from STMicroelectronics. Model response is compared with measurements (in the case of single-ended excitation) and full-wave simulations from Agilent Momentum, showing a good agreement even above self-resonance. Measurements were de-embedded from pads parasitics by means of a standard open de-embedding procedure [4.3].

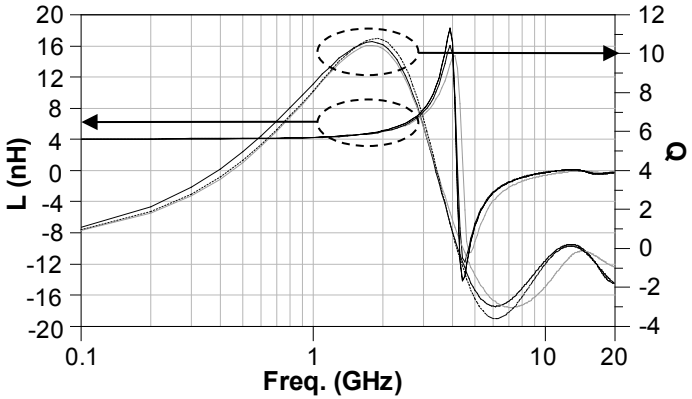

Fig. 4.3 Measured L and Q (black line) vs. model response (grey line) and Momentum simulations (dashed line) of the inductor, for a single-ended excitation.

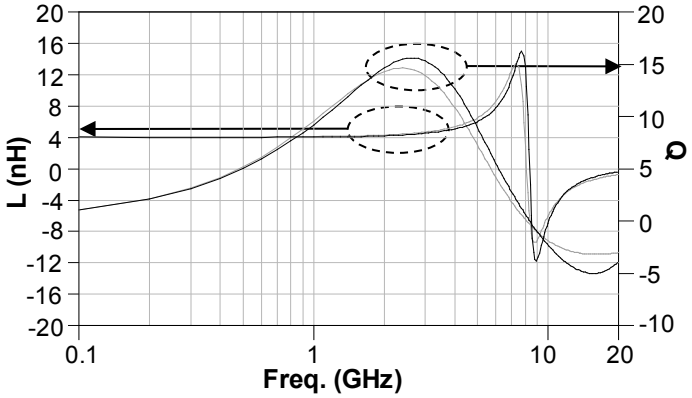

Fig. 4.4 Momentum simulations of L and Q (black line) vs. model response (grey line), for a differential excitation.

This model also proves accurate when considering a common-mode excitation, when the same signal is applied to node 1 and 2, as shown in Fig. 4.5, where model response is compared with Momentum simulations. This is useful when it

is necessary to evaluate the performance of differential circuit topologies respect to common-mode signals, as in [4.7].

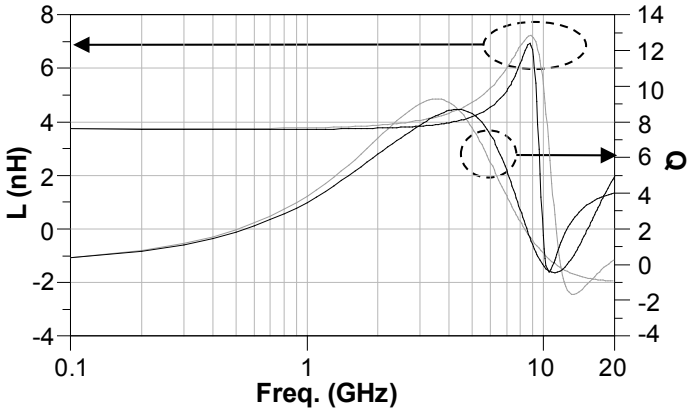

Fig. 4.5 Momentum simulations of L and Q (black line) vs. model response (grey line), for a common-mode excitation.

In all the above simulation we used the value of R_{skin} deduced by fitting the response in the single-ended excitation. The model response of Fig. 4.4 and 4.5 shows that the value of R_{skin} deduced in a particular configuration remains valid also when considering other excitations.

4.2 Coupling modeling

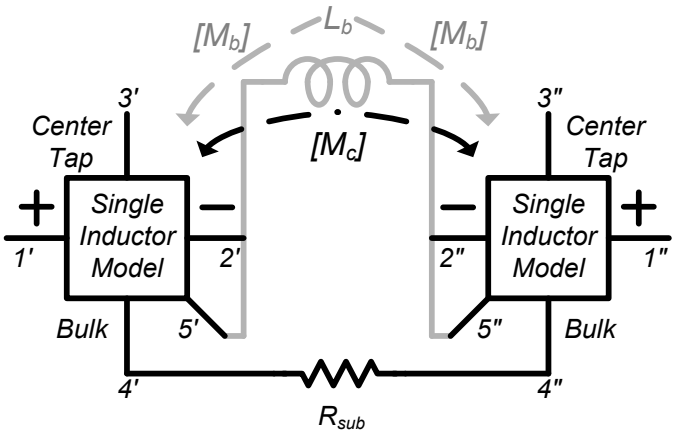

Fig. 4.6 General model for a coupled inductors pair (black) and extension to the measured test cases (grey).

The model in Fig. 4.2 can be easily extended to describe the cross talk between two (or more) different inductors according to the schematic reported (in black) in Fig. 4.6. In particular, the mutual inductance matrix $[M_c]$ models the magnetic couplings between the four halves of the two inductors, and R_{sub} models the substrate coupling:

$$R_{sub} = \lim_{\omega \to 0} \mathrm{Re}\left(Z_{1'//2'//3',1''//2''//3''}\right) - R'_{epi} - R''_{epi} \tag{4.7}$$

$$M_{c_{i,j}} = \lim_{\omega \to 0} \left. \frac{\mathrm{Im}\left(Z_{(i',3'),(i'',3'')}\right)}{\omega} \right|_{i',j''=1,2} \tag{4.8}$$

For experimental validation, we realized a set of test devices including a pair of closely spaced inductors (see Fig. 4.7). Note that in this case the model of Fig. 4.6 must include the

inductor L_b and the mutual inductance matrix $[M_b]$, to take into account the parasitics associated with the metal traces connecting the ground terminals of the GSG pads.

In fact, these parasitics cannot be removed by the de-embedding procedure.

4.2.1 Coupling measurements and model validation

The test structures considered consist in a pair of 4 nH symmetrical inductors (3-turns, 340 µm diameter) integrated in a 7 metals 65nm BULK CMOS process by STMicroelectronics (see Fig. 4). Two versions (shielded and unshielded) and two distances between the inductors centers (D=510 µm and D=680 µm) were considered, which correspond to an edge-to-edge distance of 170 µm and 340 µm.

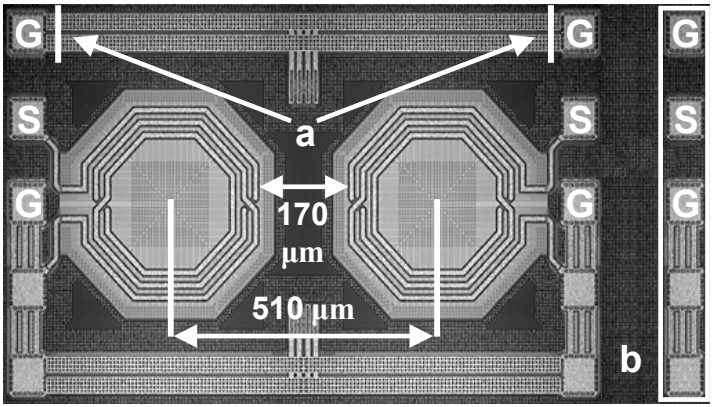

Fig. 4.7 Test chip die microphotograph; a) laser cuts; b) GSG pads for open de-embedding.

All measurements were performed using Picoprobe Model 40 GSG probes with a CS-5 calibration substrate, and the parasitic capacitance between the Ground and Signal pads was removed by standard open de-embedding.

Note that this procedure cannot remove the pads parasitics towards the substrate (see Fig. 4.8), which were taken into account as suggested in [4.4].

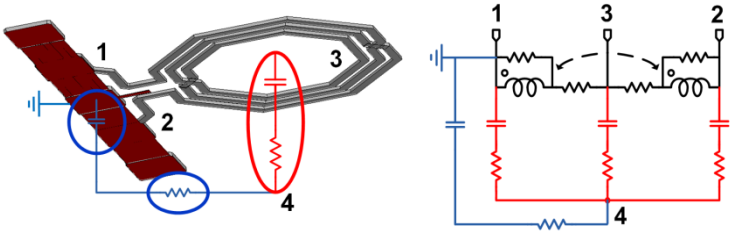

Fig. 4.8 Pads parasitics (blue) versus inductor intrinsic parasitics (red); physical representation and modeling [4.4].

The test structures were designed to allow cutting of the metal traces connecting the ground pads in different areas, in order to consider different grounding-line configurations.

When the metal traces are present, they constitute a ground ring along with the pad structure, and this ground ring produces a large parasitic magnetic coupling [4.5], which increases the overall cross-talk. In fact, as can be seen in Fig. 4.9, the coupling between the inductors (represented as the magnitude of the S_{21} parameter) can be 10 dB higher when the ground ring is present. For this reason, since this effect can mask other important coupling sources, all the results

discussed in the following refer to chips that were cut to obtain a single trace connecting the ground pads of opposite ports (see Fig. 4).

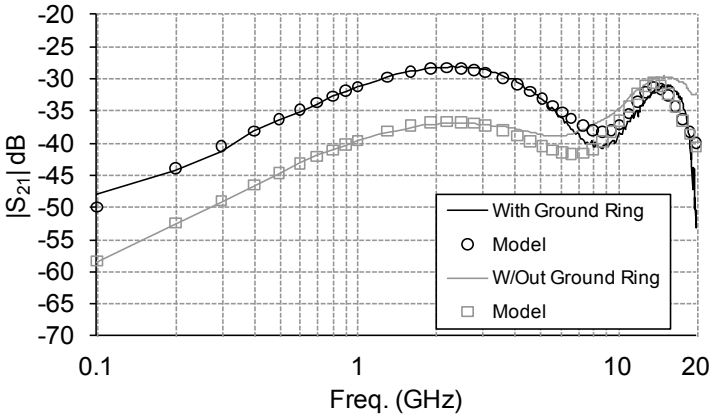

Fig. 4.9 $|S_{21}|$ vs. frequency for shielded inductors with and without ground ring (D=510 μm).

In particular, we report here the experimental validation of the model in the case of inductors placed at different distances, with or without shield.

Fig. 4.10 reports the comparison of the magnitude of S21 obtained from measurements and from the model of Fig. 4.3 in the case of two different separations (D=510 μm and D=680 μm) between shielded inductors (the shield is connected to the ground pads). A good agreement is obtained in a very wide frequency band, up to frequencies well above the self-resonance of the inductors (4.2 GHz).

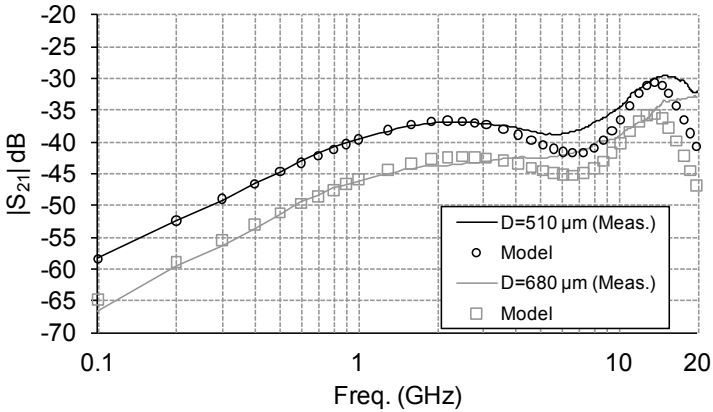

Fig. 4.10 $|S_{21}|$ vs. frequency for shielded inductors.

Note that the cross talk exhibits a relative minimum just above the self-resonance. This can be explained considering that the total coupling results from magnetic (inductive) and substrate (capacitive) coupling. The amplitude and phase of these contributions have different frequency dependences, and, at a certain frequency, they tend to cancel each other, determining the minimum of cross talk.

The effect of the shield on the coupling is shown in Fig. 4.11, which reports the cross talk of unshielded inductors in the case of D=510 µm (the curve of the shielded version of the inductors is also reported for comparison). As well known, the shield provides a low impedance path towards the bulk, through which currents can flow. However, it increases the substrate coupling [4.6], which contributes to the total coupling at high frequencies.

This is confirmed by the results of Fig. 6. In fact, shielded and unshielded inductors exhibit an equal cross talk at low frequency, where magnetic coupling dominates, but, at higher frequencies, a reduction of coupling up to 10 dB can be observed in the case of unshielded inductors.

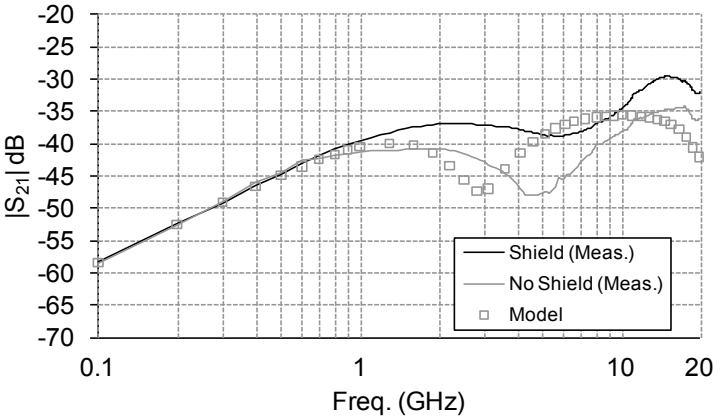

Fig. 4.11 $|S_{21}|$ of shielded and unshielded inductors (D=510 μm).

Again, the proposed model is in good agreement with measurements, apart from a frequency shift of the relative minimum of the cross talk. This is probably due to an imperfect de-embedding of pad parasitics (Fig. 4.8).

In all cases, the low-frequency cross talk is dominated by the magnetic coupling, whereas the substrate coupling becomes important at frequencies of the order of the self-resonance or higher. In fact, this can be proven using the model of Fig. 4.3. It is possible to plot separately the magnetic coupling neglecting the substrate coupling. To do this, it is necessary to employ a differential excitation on both inductors. On the other

hand, to plot separately the contribute due to substrate coupling, it is sufficient to set the matrixes $[M_c]$ and $[M_b]$ to 0. The results are shown in Fig. 4.12:

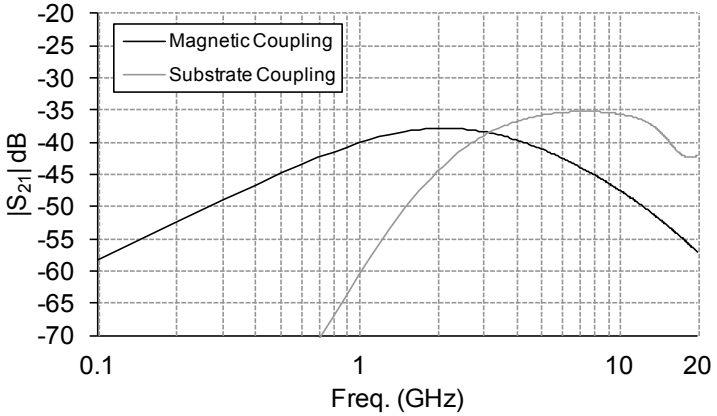

Fig. 4.12 $|S_{21}|$ in the case of Magnetic Coupling only (black line) and in the case of Substrate Coupling only (grey line).

Clearly, magnetic coupling is dominant at low frequencies, while at higher frequencies substrate coupling is maximum. As already stated, there is a particular frequency where the two phenomena are equal; in these conditions, depending on the relative phases between the two contributes, a minimum of the overall coupling can be obtained.

Further investigation showed that, in order to suppress substrate coupling, only one inductor has to be driven by a differential excitation.

4.3 Design considerations

To gain more insight from the circuit design stand-point, let us make few steps forward. First, we can represent the interaction between different blocks inside the IC in terms of voltage or current ratios, rather than scattering parameters. Second, we introduce a simple analytical expression able to accurately capture the mutual inductance of two spirals.

Let us consider the ratio of the voltage induced on an inductor ("target" of interference), assuming an ideally infinite load impedance, and the voltage at the terminals of another inductor ("source" of interference). Being Z the impedance matrix of the 2-port structure, we have:

$$\frac{V_2}{V_1} = \frac{Z_{21}}{Z_{11}}\bigg|_{I_2=0} \tag{4.9}$$

Voltage ratio (1) is easily evaluated from measurements after $S \rightarrow Z$ parameter conversion, or it can be obtained directly from the Z matrix of the model in Fig. 4.3.

In the early phase of a circuit design, an estimate of the voltage ratio (1) at frequencies below the inductor self-resonance is often sufficient for a fast evaluation of coupling effects between different circuit blocks. To this extent, and taking into account the considerations at the end of the previous Section, we can simplify the model of Fig. 4,

neglecting the substrate resistance ($R_{sub} \rightarrow \infty$) and using an estimate of the mutual inductance between the inductors.

We have derived the following closed-form empirical expression, which yields the total mutual inductance M (in nH) between two spiral inductors [4.8]:

$$M = N_1 N_2 \frac{D}{10} e^{15\frac{\sqrt{R_1 R_2}}{D}} \; nH \tag{4.10}$$

In (2) N_1 and N_2 are the numbers of turns, D is the distance (in μm) between the centers, R_1 and R_2 are the averages of the internal and external radii of the inductors. The expression is a numerical approximation of the integral deriving from the use of the Neumann formula, and has been validated for different combination of the inductors parameters (Fig. 4.13).

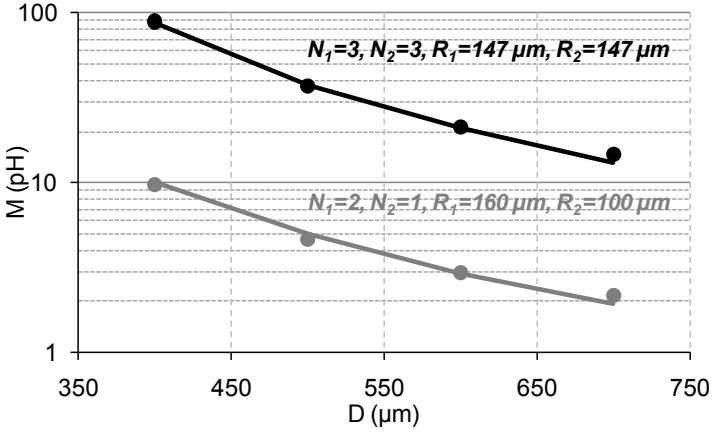

Fig. 4.13 Simulated (lines) and estimated (dots) mutual inductance, for different combinations of N_1, N_2, R_1 and R_2.

The relative accuracy is within 13 % up to $D \approx 5R$, i.e. in all cases of practical interest.

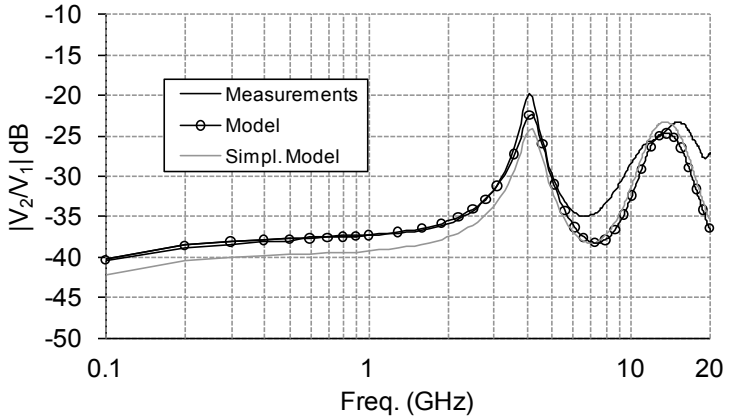

Fig. 4.14 $|V_2/V_1|$ for D=510 μm, shielded inductors.

Fig. 4.9 reports the voltage ratio (1), in the case of shielded inductors with D=510 μm, obtained from measured S-parameters, from the complete model of Fig. 4.3 and from the simplified model, where the mutual couplings are evaluated by using (2). Not only the complete model of Fig. 4.3 is very accurate, predicting the coupling between the two inductors in a wide frequency range, but also the one based on the simple formula of equation (2) proves to be accurate up to the self-resonance frequency, where substrate effects become important.

4.4 Inductor model extension

The inductor model discussed so far can be generalized in order to take into account more effects, such as a more accentuate frequency dependence of the series inductance, resistance and parasitic capacitance, which can be observed in inductors in the range of 50 to 300 pH, which are of common use in the mm-Wave frequency range.

Another possibility is to exploit a single section of the double-π model to represent a small (relatively to the wavelength) section of a transmission line, along with the frequency dependence of the line parameters. As it will be shown, it is also possible to easily create a model scalable with the length of the transmission line, thus simplifying the work of the designer.

4.4.1 Extension to low-values inductors

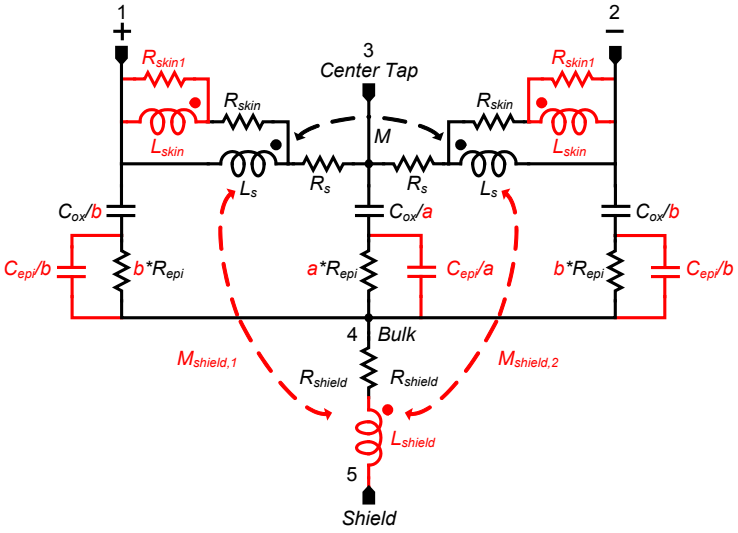

Fig. 4.14 Extended inductor model: differences from the model in Fig. 4.2 are highlighted in red.

A more complicate model of an integrated inductor is shown in Fig. 4.14. New components (highlighted in red) are introduced in order to take into account more complicate frequency dependence of the inductance and quality factor of an integrated inductor.

In order to further model frequency dependence of the series inductance and resistance, more fitting parameters are introduced (L_{skin1} and R_{skin1}), creating an R-L ladder, as suggested in [4.9]. All the considerations of paragraph 4.1 still apply. Regarding parasitic capacitance, a new component (C_{epi}) is introduced in parallel with the substrate resistance R_{epi},

in order to introduce frequency dependence also in the substrate parasitic [4.10-4.11]. Furthermore, in order to capture both the single-ended and differential behavior in the case of low values inductors, it is necessary to alter the ratio between the capacitances in the double-π scheme, introducing two more variables: a and b. These variables control the distribution of the total parasitic capacitance and resistance towards the substrate; so, the following relation must hold:

$$a = \frac{b}{b-2} \tag{4.11}$$

in order to C_{ox}, R_{epi} and C_{epi} to represent the total value of the parasitic components.

Finally, at higher frequencies all the mutual coupling must be considered. In particular, when inductors become small, the coupling between the shield tap and the coil can contribute significantly to the total inductance, especially for single-ended excitation. So, additional terms (the shield tap inductance L_{shield} and the mutual M_{shield} between the shield tap and the inductor coil) have to be introduced, defined as:

$$L_{shield} = \lim_{\omega \to 0} \frac{\mathrm{Im}\left(Z_{4,5}\right)}{\omega} \tag{4.12}$$

$$M_{shield,i} = \lim_{\omega \to 0} \frac{\mathrm{Im}\left(Z_{(4,5),(i,3)}\right)}{\omega} \tag{4.13}$$

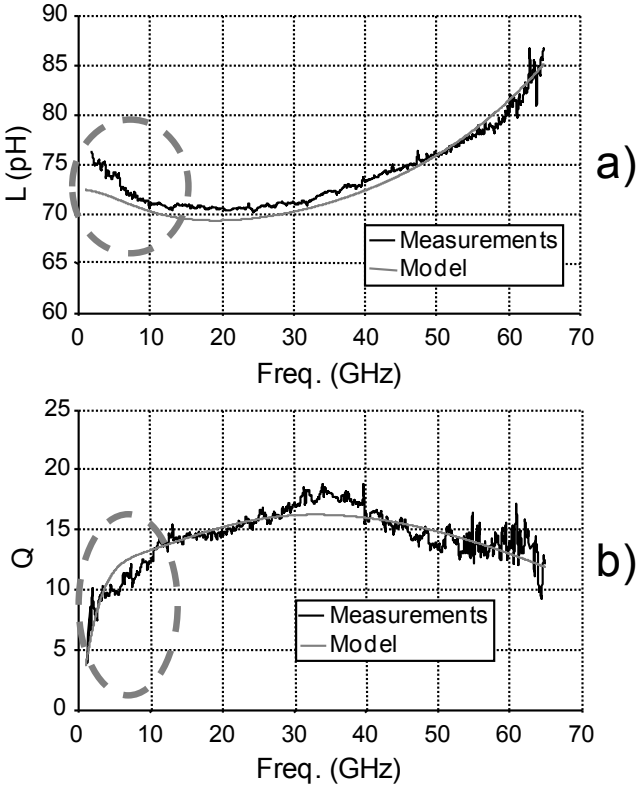

Fig. 4.15 Measurements of a 70 pH integrated inductor (black line) versus extended model (grey line). Inductance (a) and Quality Factor (b).

Fig 4.15 shows the measurements of the inductance and the quality factor of a 70 pH integrated inductor (in a single-ended configuration) and the response of the proposed model. Excellent agreement is found, particularly the highlighted low-frequency drop in the inductance.

4.4.2 Integrated transmission line scalable model

In the second chapter, the design and optimization of integrated transmission lines have been investigated. Transmission line can be used to connect different building blocks or to synthesize very accurate reactances (typically, inductive reactances). In order to exploit all this possibility, an accurate circuital model of their behavior is mandatory; in particular, this model have to be scalable with length and have to be valid both in the frequency and time domain to be of general use.

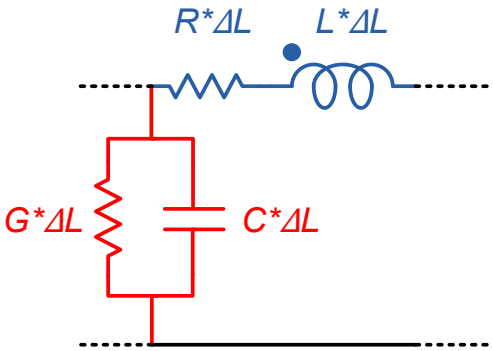

Fig. 4.16 Traditional RLGC model [4.12] of a transmission line.

Fig. 4.16 shows the traditional RLGC model [4.12] for a single-mode transmission line. The terms R, L, G, C are the unit-length resistance, inductance, conductance and capacitance of the line and are directly related to the propagation constant and characteristic impedance. All these terms in general exhibit a frequency dependence.

This form is suitable to be implemented with a circuital model. This model can be made scalable with length by employing per-length values in all terms and by multiplying them by the desired length. Due to the distributed nature of a transmission line, this strategy well approximate the characteristic of a transmission line only for a small length (that is, smaller in respect of the wavelength in the transmission line).

However, it is possible to cascade more sections in order to further mimic the distributed behavior: some experiments show that, in the case of a working frequency of 60 GHz, only 4 sections are needed in order to reproduce the correct behavior for a length of about 500 μm, that is in all practical cases.

A possible equivalent form is shown in Fig. 4.17:

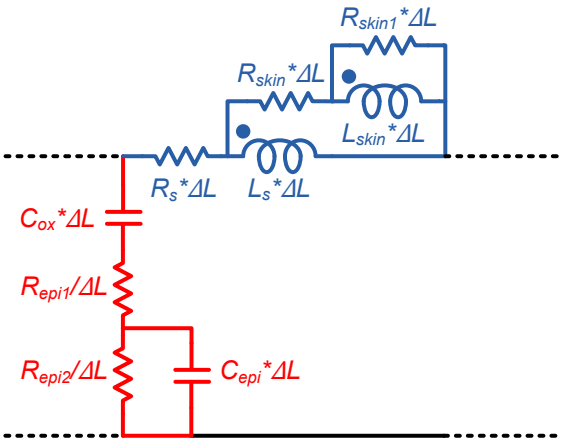

Fig. 4.17 Scalable transmission line model obtained from single inductor model in Fig. 4.15.

Using the inductor model proposed so far, it is possible to re-create the frequency dependence of the series and parallel terms in Fig. 4.16. Note that an additional degree of freedom has been introduced in the substrate parasitic model (R_{epi2}); furthermore, since at DC the parallel impedance has to be an open circuit, a series topology (that is, C_{ox} in series with all the other terms) has been chosen.

4.5 Case study: A Sliding IF Receiver for mm-wave WLANs in 65nm CMOS

All the modeling considerations discussed so far have been of practical use in the design of mm-Wave building blocks targeted to a mm-Wave front ends, both from simulations and design point of view. In this paragraph, some modeling and layout considerations will be discussed, based on a first prototype of a receiver for 60 GHz applications, while in the next chapter a new, wideband receiver will be presented.

The proposed receiver for the 60 GHz band is based on a sliding-IF architecture, relying on a first down-conversion to 1/3 the received frequency, followed by a quadrature down-conversion to DC, as shown in Fig. 4.18. In particular, a quadrature oscillator around 20 GHz provides I and Q signals for second step conversion while a second harmonic is extracted and amplified in order to drive the first mixer. This choice leads to a significant power saving in the Local Oscillator (LO) generator. The LNA is single-ended and made

of 3 stages and employs coplanar wave-guide transmission lines to realize inductors to resonate parasitics. All the mixers use double balanced Gilbert type topology.

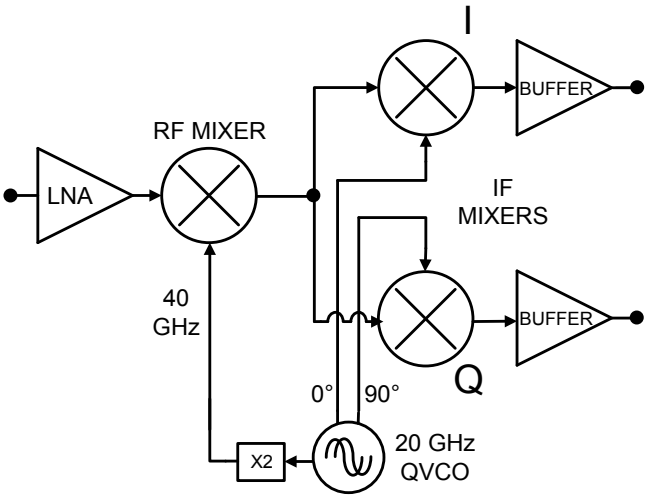

Fig. 4.18 Receiver block diagram.

Fig. 4.19 shows the photomicrograph of the die, along with the main building blocks area allocation. A mixed approach has been adopted regarding passive components: it is evident from the layout that both transmission lines and inductors have been used. Particularly, since transmission lines provide a well defined ground current return path, they have been employed where a single ended topology is present. Furthermore, when a fully differential topology is employed, integrated inductors are attractive due to their more compact area.

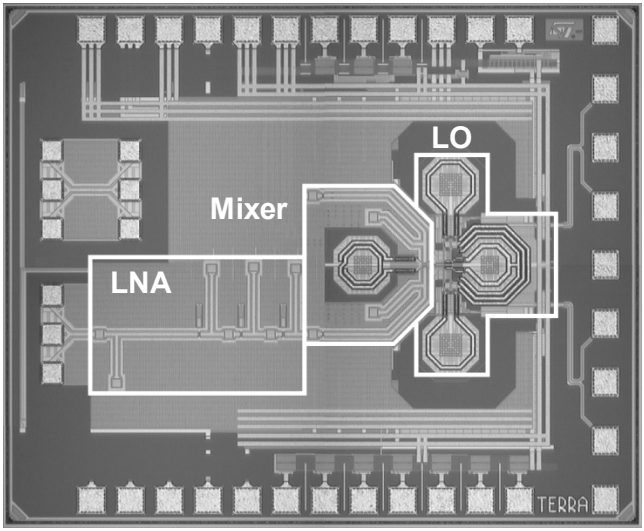

Fig. 4.19 Die photomicrograph (2.15 mm^2 area)

LNA design and layout will be discussed more in detail in the next chapter. Here, modeling and layout of the RF mixer and of the LO generation will be discussed.

4.5.1 RF Mixer

Simplified schematics of the Gilbert type RF mixer is shown in Fig. 4.20, along with the final layout. The fully balanced topology assures best LO suppression. The RF transconductor is driven single ended. Inductors L_1 and L_2 match the input impedance of the switching pair with the output of the transconductor, providing ~ 3 dB current gain boost. A spiral inductor, resonating out device parasitics, loads the RF mixer.

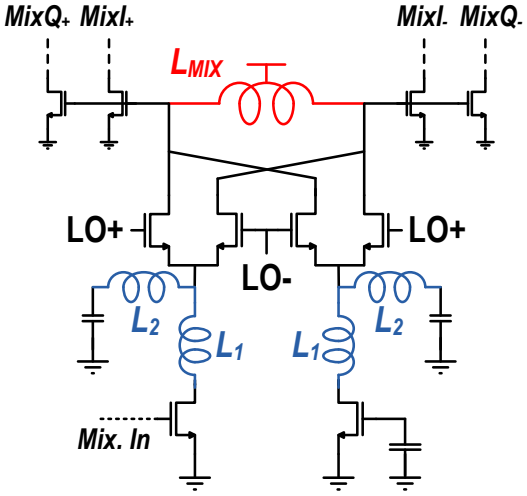

Fig. 4.20 RF Mixer schematic.

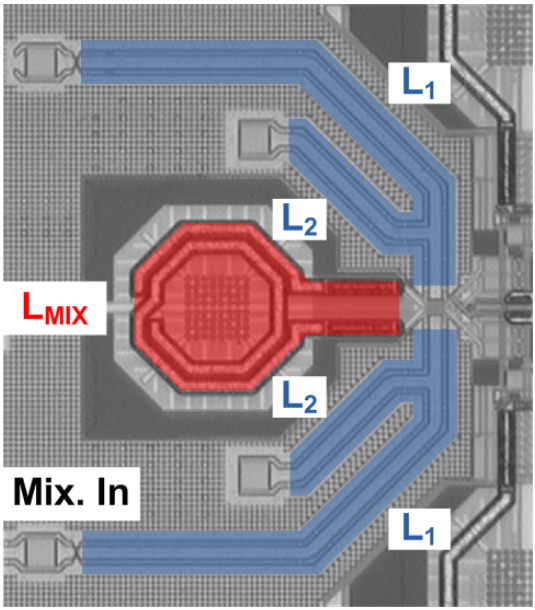

Fig. 4.21 RF Mixer layout.

It has to be noted that, in this implementation, a total of 5 inductors are needed. Furthermore, the ground current return path between the output transconductor and the switching pair has to be modeled correctly in order to optimize the current gain boost.

The solution adopted is to realize inductors L_1 and L_2 using coplanar waveguides transmission lines (highlighted in blue, both in the schematic and layout, Fig. 4.21), while using a standard differential inductor as load for the switching pair. Since the EM field in coplanar waveguides is well confined around the gap region, they are inherently shielded from adjacent devices; so, it has been possible to fold them around the differential inductor in order to save area.

The differential load inductor has been simulated with Agilent ADS Momentum, along with the ground ring surrounding it; a model of the inductor coupler with this ground ring has then been extracted, as described in paragraph 4.2. Transmission lines have been modeled as described in paragraph 4.4.2. Thanks to the particular layout chosen, no coupling has to be considered between either inductors L_1, L_2 and L_{mix}.

4.5.2 LO Generation

Quadrature signals driving the IF mixers are generated by means of two oscillators, coupled via cross-connected transistors M1-M4, as shown in Fig. 4.22. Like in any oscillator, the common sources of the fully differential active pairs have second harmonic content. Moreover, they have

opposite phases because the oscillators run in quadrature. The loop built around Mx-My reinforces the signal amplitude at twice the frequency. After further amplification through pseudo-differential buffer, the extracted signal at twice the frequency drives the RF mixer.

Capacitive parasitic at common sources nodes are resonated out by an inductor.

The discussed topology relies on a total of 4 inductors. The proposed layout is presented in Fig. 4.23. The inductor that loads the pseudo-differential buffer is highlighted in green, and is surrounded by a transmission line (in blue) that resonates the parasitic at the common sources nodes. These two inductor have been simulated together in Agilent ADS Momentum; the inductor and transmission line have been modeled as discussed in paragraph 4.4.1 and 4.4.2, respectively. Thanks to the transmission line, coupling between the signal line and buffer inductor is very low (K ~ 0.07). This residual coupling has been modeled as described in section 4.2.

Coupling between the two VCO inductor (highlighted in red), buffer and mixer inductor have been estimated to be negligible thanks to the coupling estimation formula already discussed (4.10).

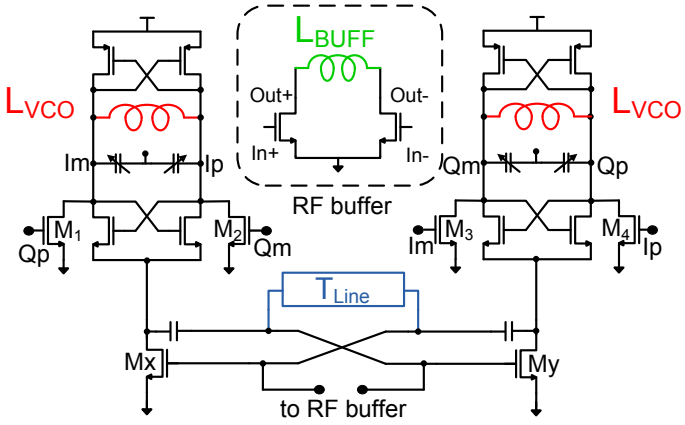

Fig. 4.22 VCO and Buffer schematic.

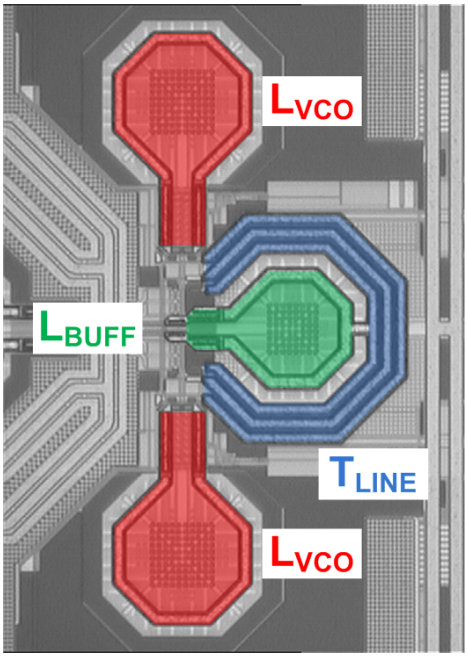

Fig. 4.24 VCO and Buffer layout

4.5.3 Receiver simulations and measurements

The chip draws about 53 mA from 1.5 V supply, including biasing. Measured S11, gain and noise figure have been compared with simulations, in Fig. 4.25. Peak gain frequency is slightly higher than simulated (around 1 GHz) and this is attributed to an overestimation of mixer parasitics. The peak gain is 28 dB roughly 3 dB lower than expected. The -3 dB bandwidth is ~ 5 GHz. Minimum noise figure is 9 dB.

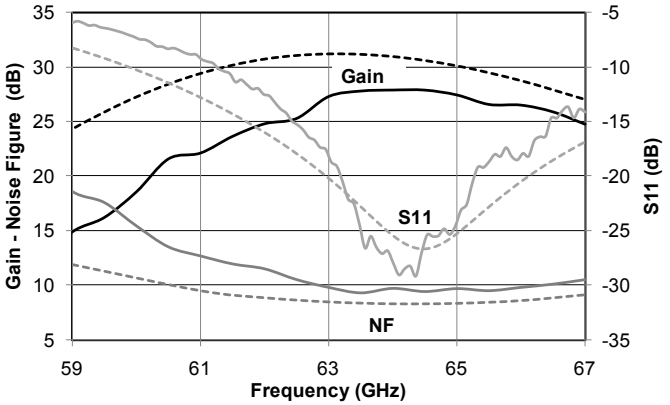

Fig. 4.25 Measured (continuous line) and simulated (dotted line) Gain, S11 and Noise Figure.

A good agreement is found between simulations and measurements, showing the validity of the proposed modeling strategy. This opens the possibility of investigating newer topologies in order to further improve performances, especially in terms of bandwidth of the receiver.

4.6 Conclusions

In this chapter the derivation and the validation of accurate equivalent circuits for the wide-band modeling of integrated passives components has been addressed.

This modeling approach has proven to be extremely flexible, being able to be extended to model coupling between different inductors, low-values inductors and integrated transmission lines.

The described models employ lumped elements that are frequency independent; nevertheless, they are able to correctly reproduce frequency dependence of the modeled characteristic in an extremely wide band, and to correctly reproduce the cross talk among different passive components (such as two symmetrical spiral inductors) integrated on CMOS substrate.

The discussed modeling techniques have been applied in the design of a mm-Wave receiver, simplifying the design process. The good agreement between simulations and measurements has validated the proposed modeling approach, opening to new layout strategies and design techniques, which will be fully exploited in the next chapter.

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5

mm-Wave wide-band LNA and receiver

Multi-gigabit-per-second wireless communications, allocated in the unlicensed spectrum around 60GHz, have been the topic of intense research in the recent past and devices are expected to hit the market shortly. Key aspects behind the increasing interest for technology deployment are the feasibility of the radio in scaled CMOS and the successful demonstration of gigabit-per second transmissions [5.1].

Despite several circuit techniques at mm-waves have been introduced in the public literature, key aspects of the analog processing tailored to the application requirements need to be addressed. Four channels covering 57GHz to 66GHz are specified [5.2]. Considering spreads due to process variation,

an ultra-wide RF bandwidth of more than ~ 12GHz has to be covered with fine sensitivity. In order to allow high-end rate transmissions, the phase noise of the reference signal is extremely stringent. Furthermore, low power consumption is key to enable multiple transceivers on the same chip.

In this chapter, a wide-band LNA for mm-Wave applications is presented. The LNA introduces capacitively coupled inter-stage resonators in the LNA for maximum gain-bandwidth product. A prototype has been implemented and characterized, obtaining optimum agreement between simulated and measured performances.

Furthermore, a 65 nm receiver, employing the proposed LNA has been fabricated. The receiver employs a sliding IF architecture relaxing tuning range requirements of the RF synthesizer and derives I & Q IF driving signals from the RF reference by means of wide-band injection locked frequency dividers by two. Exploiting the proposed modeling approach, it has been possible to fully predict real circuit behavior, obtaining state of the art performances and opening the possibility to a systematic mm-Wave design flow.

5.1 Gain-Bandwidth extension techniques

In order to extract gain at high frequency, inductive tuning of transistor capacitance is an effective technique at least in a narrow-band around LC resonance, and has been widely used

also at mm-Waves [5.3]. The gain-bandwidth product of an LC loaded gain stage has the same expression as the low-pass stage counterpart, i.e. g_m/C where g_m is the driver transconductance and C the total output node capacitance [5.4].

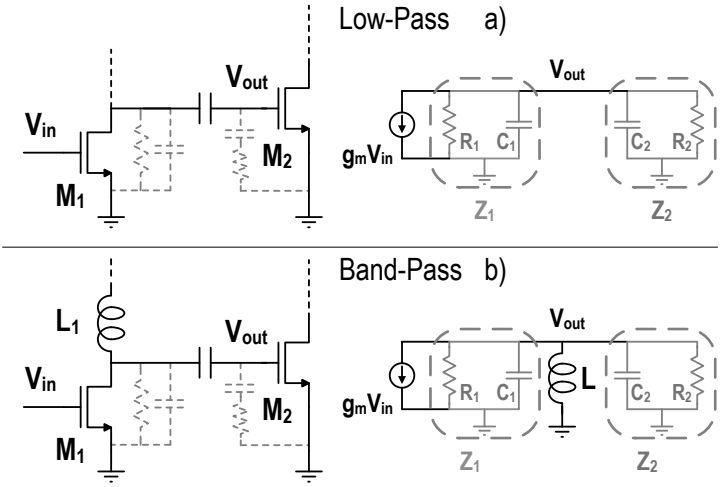

Fig. 5.1 Standard Low-Pass gain stage a) to Band-Pass transformation preserve gain-bandwidth.

Fig. 5.1 shows this basic concept. Considering a first gain stage (transistor M_1) driving a second gain stage (transistor M_2), it is possible to derive a simple small signal model. R_1 and C_1 represent the output resistance and capacitance of the first stage, while R_2 and C_2 are the parallel transformation of the input gate resistance and capacitance of the second stage. In these conditions, it is straightforward to derive the voltage gain and circuit bandwidth:

$$\frac{V_{out}}{V_{in}} = g_m R \qquad (5.1)$$

where g_m is the transconductance of the first stage and R is the parallel of R_1 and R_2. On the other hand, the -3 dB bandwidth of this circuit is equal to:

$$BW = \frac{1}{RC} \quad \text{(rad/s)} \qquad (5.2)$$

where C is the total capacitance (that is, C_1 + C_2). So, the gain-bandwidth product is equal to g_m/C. Equations (5.1) and (5.2) still holds when a low-pass to band-pass transformation is applied at the circuit of Fig. 5.1a, obtaining the circuit in Fig. 5.1b.

In principle, gain can be traded for bandwidth but gain at mm-wave is rare suggesting other approaches for bandwidth extension. Techniques to increase the gain-bandwidth product of low-pass amplifiers are discussed in the literature. In [5.5], an LC ladder where the inductor serves the purpose of isolating the transconductor intrinsic capacitor (C_1) and the load capacitor (C_2) is discussed (see Fig. 5.1b). The low-pass stage can be transformed into band-pass, as shown in Fig. 5.2b, preserving performances. But three inductors are needed and the series inductance value required for operation at mm-Wave is impractical in integrated fashion. An alternative still exploiting separation of the parallel LC resonators by means of a single capacitor (C_c) is viable, creating the so-

called double-tuned circuit [5.6] (see Fig. 5.2c). This topology is based on a band-pass transformation of a standard low pass LC filter; by replacing the series LC with an admittance inverter realized with capacitors.

As an example, the plot in Fig. 5.2d shows the transfer function for various C_c. $C_c \rightarrow \infty$ corresponds to the single LC load case. The gain-bandwidth product can be significantly increased trading with in-band gain variation.

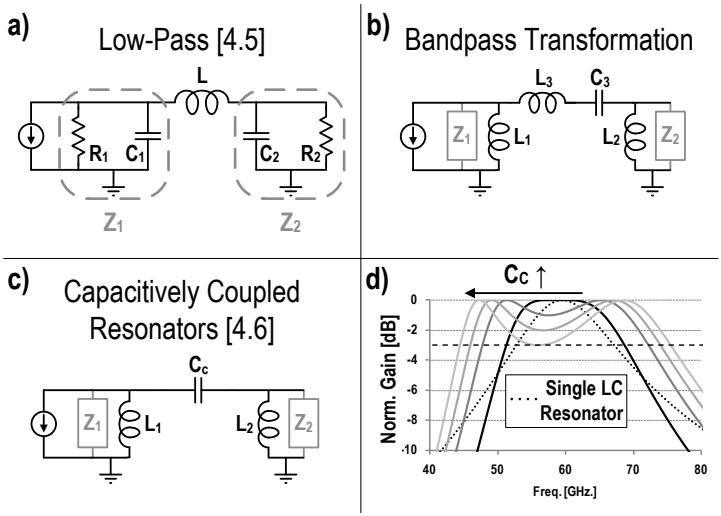

Fig. 5.2 Gain-bandwidth enhancement techniques: low-pass [5.5] a), band-pass transform b), capacitively coupled resonators [5.6] c) schematics; capacitively coupled resonators typical response d).

Inductors L_1 and L_2 must be chosen in order to resonate at the desired center frequency with $C_1 + C_c$ and $C_2 + C_c$, respectively.

5.2 mm-Wave Low Noise Amplifier

A mm-Wave LNA has been designed using the bandwidth enhancement concept exposed in the previous section. A three stage topology has been chosen in order to obtain a voltage gain higher than 25 dB. Each stage uses a cascode structure. Common source and common gate devices have equal size allowing a shared junction inter-digitized layout to minimize stray capacitance at the common node, responsible for gain and noise degradation. Devices are biased at an optimum current density of 250 μA/μm for maximum fT.

The first stage is shown in Fig. 5.3:

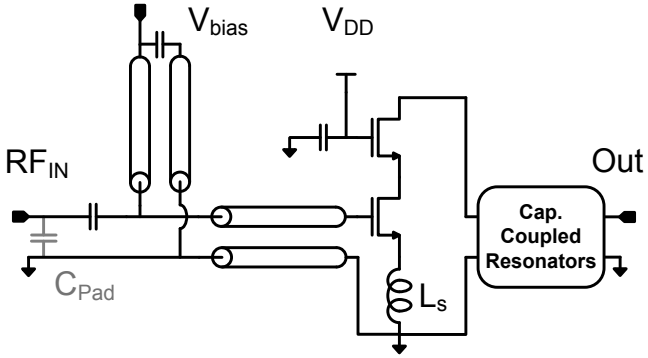

Fig. 5.3 Schematic of the input matching network and first stage of the LNA.

An inductive-degenerated topology has been implemented, along with a matching network realized with a series transmission line and a stub, short circuited to ground via a bypass capacitor. Along with the input pad parasitic

capacitance, this network provides a good, wide-band input match. An AC coupling capacitor is also included.

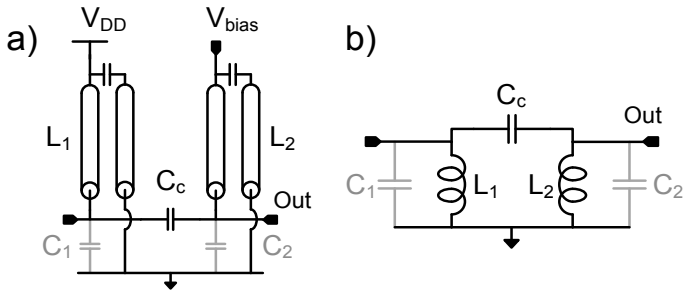

Fig. 5.4 Capacitively coupled resonator implementation with transmission lines a) and equivalent simplified schematic b). C_1 and C_2

Capacitively coupled resonators load the first stage, in order to provide a wide-band gain; this network has been implemented using transmission lines (see Fig. 5.4a) as inductors and parasitics of the first and second stage as parallel capacitors. Bias networks are includes; Fig. 5.4b) shows the equivalent circuit. Transistors width is 40 µm over a minimum gate length (65 nm). The topology of the second and third stage is shown in Fig. 5.5. Transistors width is 20 µm over a minimum gate length (65 nm).

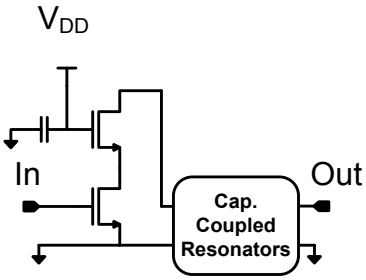

Fig. 5.5 Second and third stage of the proposed LNA.

Since transistor parasitic are an important part of the proposed inter-stage matching network, they have to be carefully modeled. To this extent, measurements of a test chip containing single gain stages have been performed. Parasitics were extracted and compared with values extracted from EM simulation of transistor layout using the approach described in [5.7]. This method consist in extracting the admittance parameters from a simulation of the layout of the transistor from the top to the lowest metal; an example for a cascode topology is shown in Fig. 5.6.

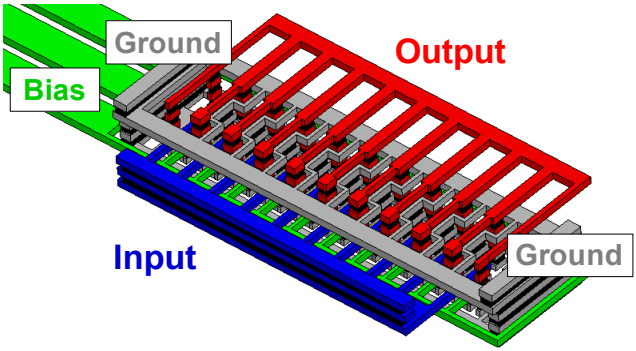

Fig. 5.6 3D view of the layout of the cascode stage in Fig. 5.5.

Good agreement has been found. Then, the extracted parallel capacitances are added to the standard BSIM transistor model.

5.2.1 Experimental Results

The chip micrograph of the proposed three-stages LNA, integrated by STMicroelectronics, is shown in Fig. 5.7. The

chip occupies 0.45mm^2 and draws 20mA from 1V supply. The implemented LNA provides an High Gain mode and a Low Gain mode, by varying the bias voltage of the three gain stages. Inductors were realized by employing coplanar waveguide transmission lines (in order to correctly model ground current return path and to reduce parasitic coupling between adjacent stages) terminated on a bypass capacitor, while the small coupling capacitors were realized as parallel plate capacitors using the two top metal layers. In order to obtain a good accuracy, these capacitors were simulated using a full-wave electromagnetic simulator and an equivalent circuit model has been developed.

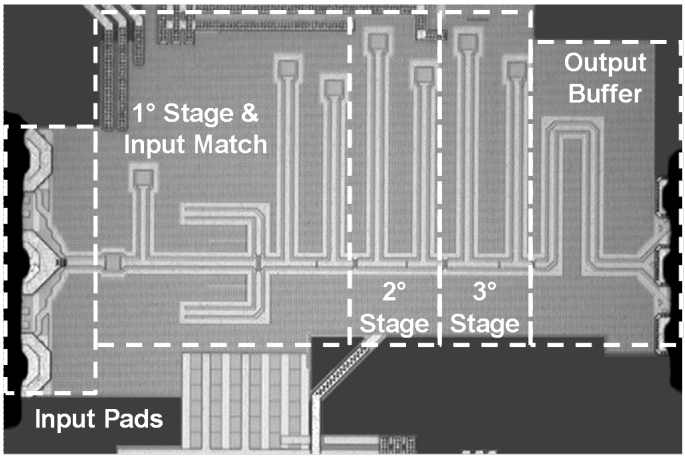

Fig. 5.7 Low Noise Amplifier chip photomicrograph.

Since, as it will be shown in the following section, this LNA will be part of a wide-band receiver targeted for operation in the unlicensed 60 GHz band, for measurement reason an output

buffer (with a flat gain between 0 and 1 dB) has been designed (shown in Fig. 5.8).

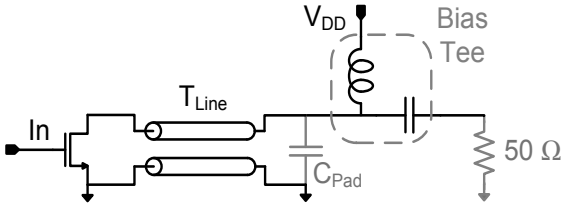

Fig. 5.8 60 GHz output buffer schematic.

This output buffer consist in a common source gain stage driving the output pads parasitic capacitance and the instrument 50 Ω input impedance through a transmission line. The length of this transmission line has been chosen in order to resonate the output pads parasitic capacitance and to provide a flat gain; an external bias tee is used in order to provide the DC current.

Fig. 5.9 shows the measured voltage gain, both in High (black line) and Low (grey line) Gain modes, using an Agilent PNA; simulations are also reported (dashed lines). Good agreement is found, apart from a slight frequency shift (1 GHz), Measured gain is around 27 dB and 16 dB, in High and Low Gain mode, respectively. At higher frequencies, measured gain becomes higher; this is probably due to a small error in designing the output buffer transmission line, due to a wrong output pad parasitic capacitance estimation. Measured -3 dB bandwidth is ~15 GHz, in both gain modes.

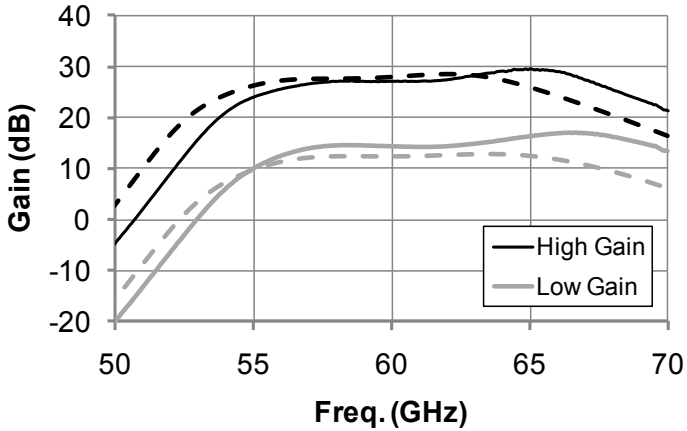

Fig. 5.9 Simulated (dashed line) and measured (continuous line) gain, in High (black) and Low (grey) gain modes.

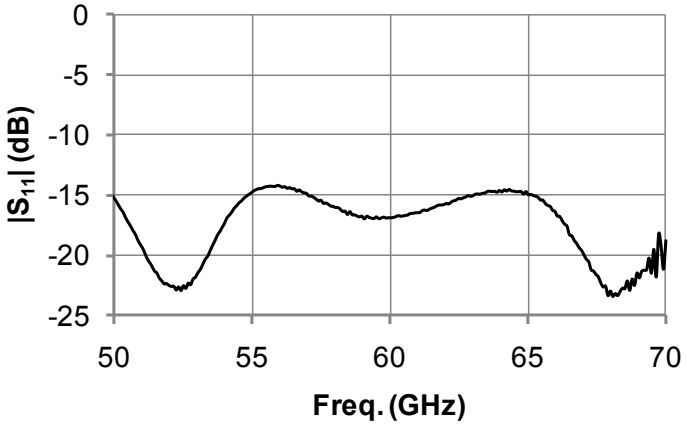

Fig. 5.10 Measured Input return loss.

Measured input match is better than -14 dB in the whole bandwidth (see Fig. 5.10). Considering that the RF input pads were designed to be suitable to be used with flip-chip packaging (and thus presenting a large input capacitance), this is a very good result.

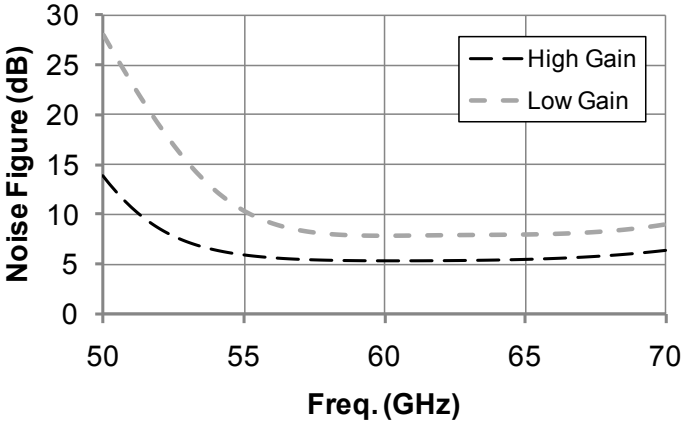

Fig. 5.11 Simulated noise figure in High (black) and Low (grey) gain modes.

Simulated noise figure (Fig. 5.11) is around 5.4 dB in High Gain mode, and drops to 7.8 in Low Gain mode; in both cases, a very flat in-band behavior is observed. Due to the lack of instrumentation, it was not possible to perform a direct noise figure measurements; however, in the following section measurements of a receiver employing the proposed LNA will be presented.

The Input -1 dB compression point of the receiver has been measured, for both High and Low Gain Mode, at the four channels center frequencies of the standard proposed in [5.2]. Results are show in Table I (High Gain Mode) and Table II (Low Gain Mode).

Freq. [GHz]	Input -1 dB Comp. Point [dBm]	Output -1 dB Comp. Point [dBm]
58.32	-26.00	0.26
60.48	-28.40	-2.11
62.64	-27.40	-0.27
64.8	-30.00	-1.33

Table I Input and Output -1 dB Compression point at the four channels center frequencies of the standard proposed in [5.2]; High Gain mode.

Freq. [GHz]	Input -1 dB Comp. Point [dBm]	Output -1 dB Comp. Point [dBm]
58.32	-17.40	-3.70
60.48	-16.40	-2.96
62.64	-16.40	-2.58
64.8	-18.40	-3.04

Table II Input and Output -1 dB Compression point at the four channels center frequencies of the standard proposed in [5.2]; Low Gain mode.

5.3 A wide-band mm-Wave receiver

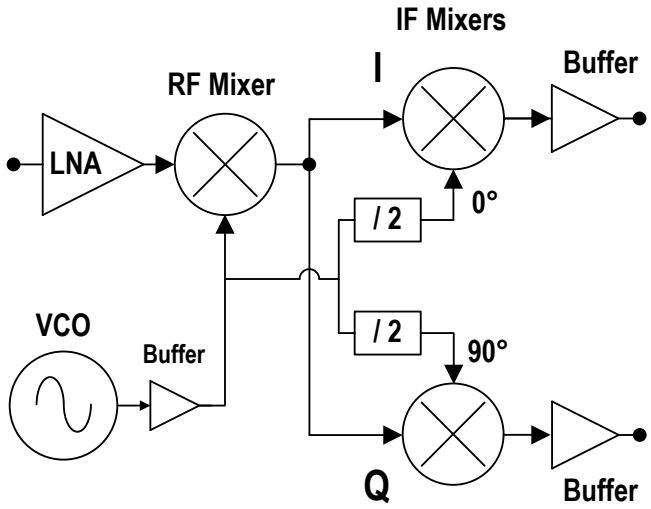

Fig. 5.12 Proposed receiver block diagram.

The circuit diagram of the proposed RF front-end is reported in Fig. 5.12. The LNA adopts three amplifying stages to achieve ~27dB gain and employs capacitively coupled inter-stage matching designed for ~14GHz -3dB bandwidth with ~1dB ripple. A low gain mode can be selected by reducing the biasing current of transconductor devices in each stage. A Gilbert type mixer, driven single-ended, performs frequency translation. A current gain boost is realized by inductors L3, L4 which match transconductor and switching pair impedance. The IF inter-stage network, comprised of the RF mixer load and IF mixers input, realizes a wide-band filter based on transformer coupling (Fig. 5.13). The inductance of the primary

winding resonates out all device parasitic at IF center frequency while the secondary resonates at the same frequency with an explicit MOM capacitor. Optimum performances in terms of bandwidth and ripple are achieved with mild coupling [5.8].

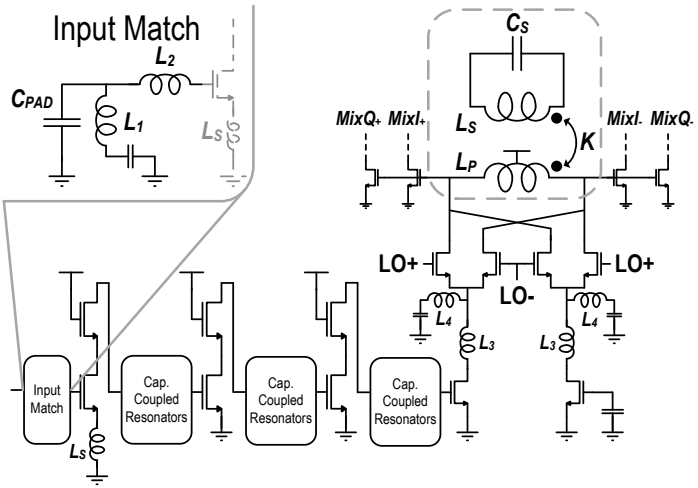

Fig. 5.13 Wide-band low noise amplifier and RF mixer.

Capacitive coupling, adopted in the LNA inter-stages, was also viable leading to even better gain-bandwidth performances but this alternative was adopted for the following reasons: 1. Parallel inductor to resonate out separate parasitic capacitors would require inductances > 1nH occupying a large area and complicating device layout. 2. At IF stage gain is less critical allowing maximum bandwidth as main target. Quadrature mixers use a differential active load to maximize output resistance for given voltage room. PMOS current sources,

controlled by means of a common-mode feedback, bias the mixer. Mixers are cascaded by a VGA, in order to provide an additional gain control. Open-drain differential pairs buffers cascading the receiver are used to drive measurement instruments.

The on-chip reference is tuned at 2/3 the received frequency for signal down-conversion to a sliding intermediate frequency. With respect to a conventional super-heterodyne architecture, the required tuning range is reduced because the reference fractional bandwidth equals the received fractional bandwidth. At the same time, the lower frequency favors reducing phase noise for given consumption. A classic LC-VCO with cross-coupled NMOS differential pair generates the local oscillator signal [5.9]. The tank capacitor comprises MOM switched devices for coarse tuning together with nMOS varactors for fine tuning, in order to maximize capacitor (and resonator) quality factor. LC dividers by two cascading the VCO provide I & Q IF references. The VCO locks the divider by signal injection in parallel to the tank [5.10].

5.4.1 Experimental Results

The chip micrograph of the receiver of Fig.12, integrated by STMicroelectronics, is shown in Fig. 5.14. The chip occupies 2.4mm^2 and draws 75mA from 1V supply.

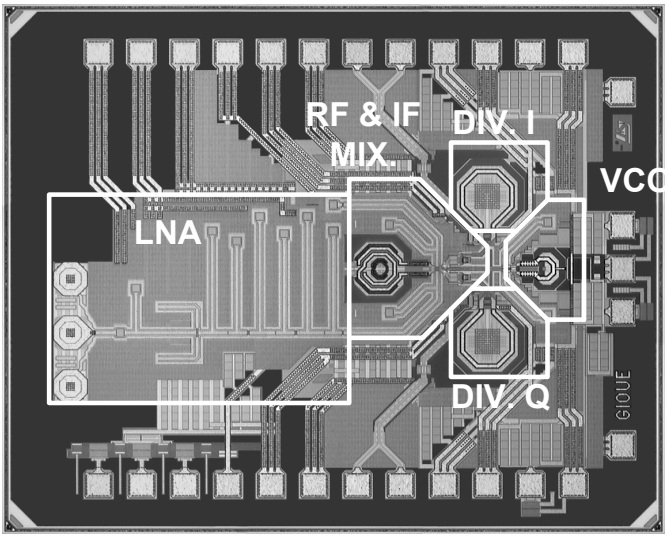

Fig. 5.14 Receiver chip photomicrograph.

A second version, not integrating the on-chip VCO and where the reference is externally provided through a wide-band integrated balun, is also available. Dies were probed for characterization. Fig. 5.15 shows measured (solid line) and simulated (dots) Gain and Noise Figure RF frequency in the case of external LO. Good agreement is found between measurements and simulations, apart from a slightly lower measured gain (~ 3 dB lower). Peak gain is 35.5dB and -3dB bandwidth is > 13GHz, while in-band gain ripple is < 2dB.

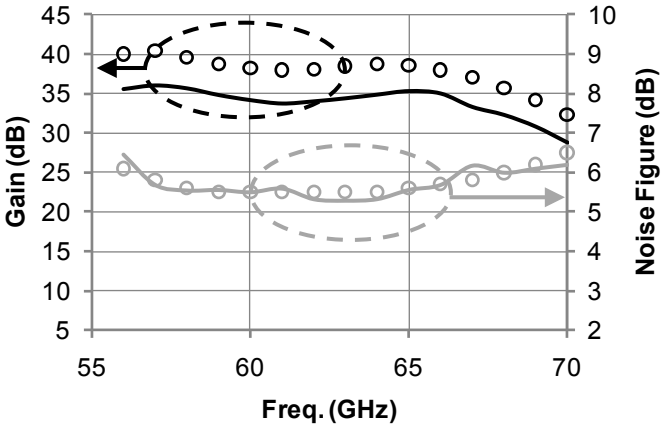

Fig. 5.15 Simulated (dots) and measured (continuous line) gain and noise figure versus RF frequency in the case of external LO driving.

Fig. 5.16 plots measured Gain and Noise Figure versus RF frequency in the case of external LO (solid line) and integrated VCO (dots).

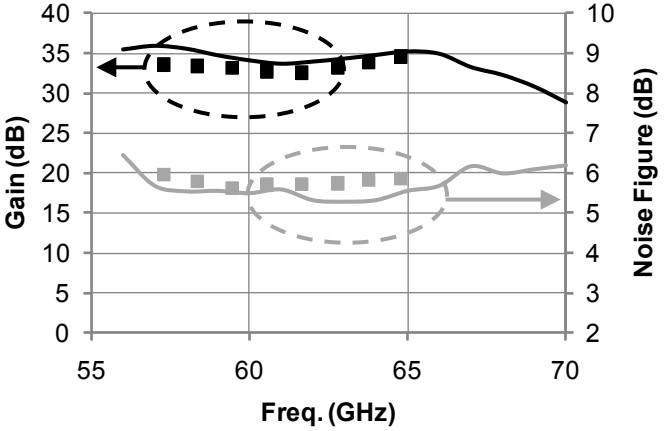

Fig. 5.16 Measured gain and noise figure versus RF frequency: external LO driving (continuous line) and on-chip VCO (dots).

The fully integrated version achieves the same peak gain while the explored bandwidth is limited by the on-chip VCO frequency range of 12.6%. An under-estimation of tank parasitics lead to a slight down-shift of 2.7GHz of the oscillator center frequency. Measurements were performed inserting a small metal plate in close proximity to the VCO tank with the effect of reducing the inductance and shifting the frequency upwards [5.11]. Once re-centered, the VCO was tuned on-chip. The receiver proves to be highly sensitive in the whole bandwidth, with NF always better than 6dB in the VCO frequency range and an absolute minimum of 5.6dB.

The receiver linearity has been measured in three different gain configurations at the frequency of 60 GHz; the results are shown in Fig. 5.17. The -1dB compression gain input power is equal to -39 dBm, -30 dBm and -21 dBm in the case of, respectively: both LNA and IF Mixers in High Gain (a), LNA in High Gain and IF Mixers in Low Gain (b), and both LNA and IF Mixers in Low Gain (c). Small signal gain at 60 GHz is equal to 33.5, 25.5 and 14 dB, respectively.

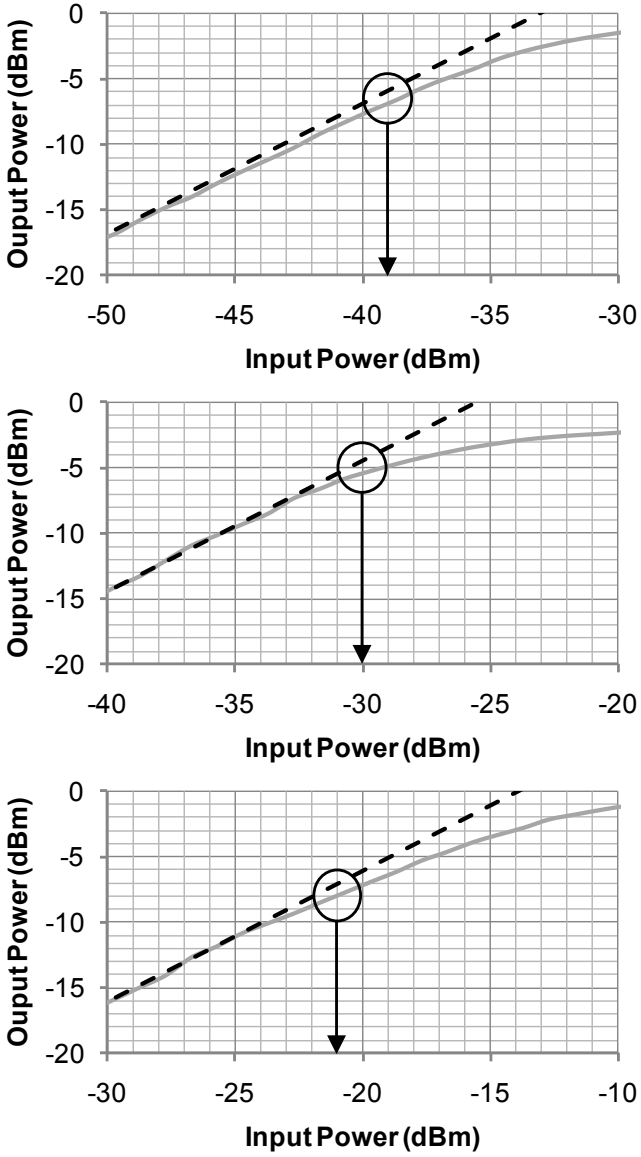

Fig. 5.17 Gain compression measurement: LNA and IF Mixers in High Gain a), LNA in High Gain and IF Mixers in Low Gain b), and both LNA and IF Mixers in Low Gain c).

A large image rejection ratio of better than 80dB has been measured. This is due to the steep out-of-band low-frequency attenuation provided by the three zeros introduced by each capacitively coupled inter-stage network in the LNA, as evident from Fig. 5.2d.

The received signal experiences two frequency translations. The phase noise of an equivalent local oscillator running at received frequency has been derived down-converting an input tone to 200MHz. The measurement is shown in Fig. 5.18.

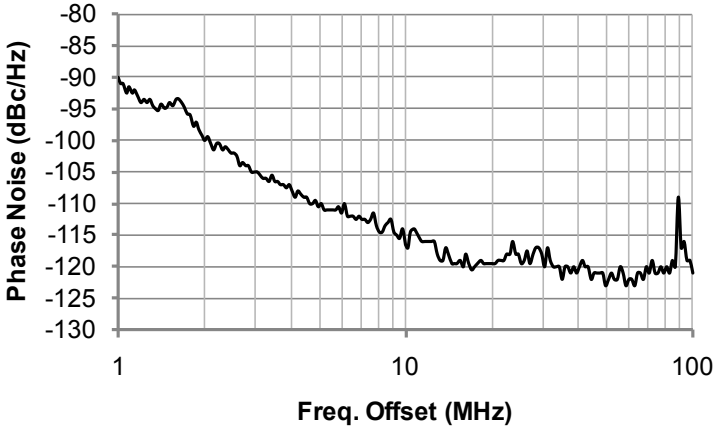

Fig. 5.18 Measured Phase Noise.

The signal source provides a tone much purer than the on-chip VCO signal. Phase noise, thus determined by the VCO, is -115dBc/Hz at 10MHz offset at an equivalent carrier frequency of 60GHz.

5.4 Conclusions

In this chapter, a wide-band LNA for mm-Wave applications based on capacitively coupled resonators has been presented. Main performances are: peak gain of 27 dB with > 15 GHz bandwidth, input match always better than -14 dB, expected noise figure of 5.4 dB. Optimum agreement between simulations and measured has been observed, thanks to the modeling techniques introduced in the previous chapters. Furthermore, a 65 nm receiver has been integrated and characterized. Table III summarizes receiver performances and reports the comparison with the state of the art.

	This Work	[5.12]	[5.13]	[5.14]
Voltage Gain [dB]	35.5	30	22	14.7
Noise Figure [dB]	5.6 – 6.5	7.1 - 9.8	5.7 - 7.1	5.6 - 7.2
RF Bandwidth [GHz]	13	N. A.	4	10
Image Rejection [dB]	80	N. A.	N. A.	N. A.
Tuning Range [%]	12.6	16.6	6.8 *	N. A. **
I/Q Mismatch [deg]	< 3	N. A.	2.1	N. A.
LO Phase Noise [dBc/Hz]	-90 @ 1MHz -115 @ 10MHz from 60GHz	-85 @ 1MHz from 50GHz	-84 @ 1MHz from 60GHz	N. A. **
Input 1 dB Comp. Point [dBm]	-39	-29.9***	-27.5	-22
Power [mW]	75	65	36	151
Supply Voltage [V]	1	1.2	1.2	1.2
Technology [nm]	65 CMOS	90 CMOS	90 CMOS	65 CMOS

*	No varactors – tuned varying the supply and/or placing external conductive plate atop the LO
**	External LO
***	High Gain Mode

Table III Comparison with state of the art.

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