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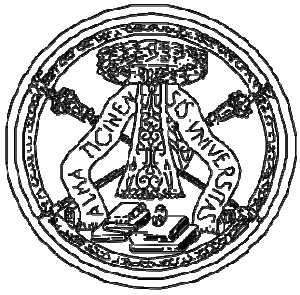

Dottorato di Ricerca in Microelettronica
XXV Ciclo

Filtering ADC based Analog Base-Band for Wireless Receivers Applications

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Introduction

A challenging issue consists in getting the two quantities X and Y separately, when it is given only the sum of them. This is actually impossible if no other information about X and Y is provided. However it is still highly demanding if a way to distinguish X from Y exists, but the absolute value of X is much smaller than the absolute value of Y. Even if Y, in this case, can be well estimated, X needs very high relative accuracy and effort to be detected.

This is what mainly occurs in a wireless receiver chain. X is the desired information signal of interest, Y is the interferer corrupting the reception and the frequency spacing between the two quantities is the way to distinguish them. In a microelectronic implementation, the effort to extract the weak information from a worst-case scenario of surrounding high power blockers is paid in terms of battery power consumption and silicon area.

In the field of CMOS based systems, the trend to reduce costs is moving towards increasing levels of integration, in order to exploit the scaling down of the integrated technology. Up to 22nm digital signal processors are today in production. They benefit of the reduced device (transistor) size to achieve high performance (very fast processing) at low power consumption. Vice-versa, assumed the same performance, less silicon area is required than in the previous technological node, thus saving manufacturing costs, for high level market productions. Transferring the analog processing into the digital world becomes so mandatory, when possible, since the scaling down of the analog circuits in not so attractive. Moreover the integration on-chip of any off-chip functionality strongly contributes to lower the system level costs.

When a wireless receiver chain is considered, Software Defined Radio paradigm implements this trend, proposing a full-silicon fully reconfigurable multi-standard radio. Even if the pure Software Defined Radio is still far to come, different ideas and new designs have been presented in the recent literature to tackle its implementation issues.

Dealing with the low-frequency section of a wireless receiver, the base-band, a filtering Analog to Digital Converter (ADC) family is proposed. Such a topology of circuits operates to move the analog to digital interface as close as possible to the antenna, i.e. just after the down-conversion mixer. Blocker resilient property is combined with digital conversion, to get a clever low-cost and low power processing.

In **Chapter 1** the genesis of a filtering ADC is shown as an implementation step towards the Software Defined Radio. This is in turn presented as the lowest cost ideal solution in the field of wireless receivers. Adopting a filtering ADC requires new signal to noise and distortion ratio and dynamic range definitions, to take into account the circuit selectivity, when defining the base-band specifications. A behavioral comparison between a filtering approach and a more traditional wide-band one is given.

Chapter 2 deals with the Filtering ADC topology. The Filtering ADC architecture is described in detail (structure, continuous time signal and noise transfer functions) together with its benefit in handling a receiver spectrum scenario with respect to a filter-ADC cascaded solution. An evolution Filtering ADC circuit (E-Filtering ADC) is also shown, improving Filtering ADC performance. A brief comparison between the two blocks is provided.

In **Chapter 3** the Filtering ADC, used to represent the entire analog base-band of a full silicon digital terrestrial television tuner, is presented. Due to the Filtering ADC, the receiver is compliant to both the DVB-T European and ATSC American standard. Simulations and measurement results of the integrated 80nm prototype are reported.

In **Chapter 4** the E-Filtering ADC used to represent the entire analog base-band of a GSM-UMTS cellular receiver, is described. First a system level study of a new E-Filtering ADC based receiver chain is proposed. Then a 40nm silicon prototype of an equivalent Rauch based architecture is presented, showing simulations and measurements results.

Chapter 5 deals with the interface between the RF and the base-band section of a wireless receiver chain. Active and passive mixer solutions are shown. Since the passive one is recently the most used in the state of the art, a switched capacitor model of current-driven passive mixer gain and noise is reported.

In **Appendix I** (completing Chapter 2) the discrete time behavior of a Filtering ADC is tackled, in order to show the limitations of the continuous time description given in Chapter 2.

In **Appendix II** (completing Chapter 4) the issue of jitter noise, coming from the clock phase noise, of a Filtering ADC is addressed.

Chapter 1

Towards Software Defined Radio: high dynamic range base-bands

The cost reduction, due to technology improvements, is mainly leading the evolution in the field of CMOS wireless receivers (1.1). In this chapter the Filtering ADC concept is presented as a first step towards the implementation of a Software Defined Radio (SDR) (1.2). A new definition of frequency dependent signal to noise and distortion ratio (SNDR) and dynamic range (DR) is then given (1.3). Finally, the Filtering ADC benefit in the handling of the ATSC-A/74 standard is shown providing a brief comparison with respect to the traditional wide-band ADC solutions (1.4).

1.1 The cost reduction in the field of CMOS wireless receivers

Reducing costs is the primary goal of any microelectronic industrial design, prototype and product. This is true also in the researching area, if the interest goes in the direction to develop new ideas for market applications. In this sense, in the field of CMOS wireless receivers, two main elements act as guidelines (see Figure 1).

First, according to the scaling down of the CMOS integration technology (nowadays down to 22nm transistor channel length), a big effort has been made to create solutions and architectures able to exploit this trend. Since digital circuits actually benefit from the technology scaling down, while for analog ones it is less attractive, this first step mainly consists in substituting all the analog blocks with a lower-cost digital signal processor (DSP). In this way, the low-power, low-size, high-frequency, simply reconfigurable and low-cost scalable resources of the digital can be exploited entirely [1].

Second, over the last decade an important evolution has been carried out towards the reduction of the bill of material (BOM), i.e. removing all the blocks (mainly high selectivity

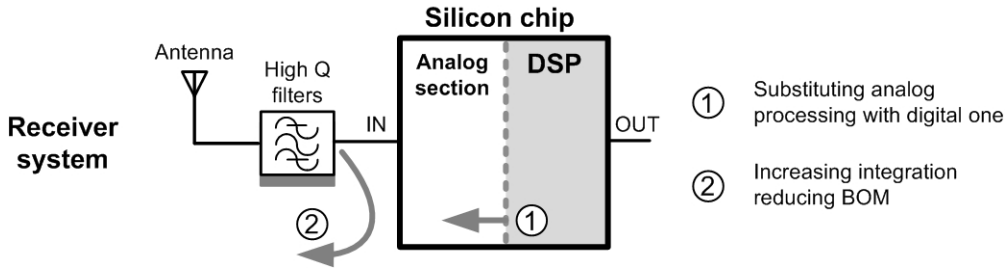


Fig. 1 Cost reduction issues in the field of wireless receivers

filters) which are used off-chip in the signal elaboration from the antenna to the digital receiver core. In the past this was already accomplished substituting the traditional superheterodyne receiver architecture with the direct conversion one (both low-IF and zero-IF). More recently the focus has been moved to the antenna-chip interface (e.g. SAW filters in cellular applications or high Q filters in television ones) [2-3].

Both the previous elements are working with the main purpose to increase the CMOS integration, in order to provide to the market low-cost chips embedding the entire receiver functionality on silicon. This of course has to be achieved without degrading the receiver performance, and still operating in a limited power consumption environment. A full-silicon solution probably can not lead the market, if the proposed receiver sensitivity is not comparable with the one of existing state of the art products. The same is true also if the performance is comparable, but the power consumption is not well constrained. Furthermore nothing "comes for free". The main consequence of this is that more design skills, new ideas, more design efforts and more complexity are continuously required to carry forward the integration demand.

According to the previous aspects, Software-Defined-Radio paradigm is coming of age. The SDR ultimate target is to place the analog to digital converter (ADC) directly at the antenna, thus providing a multi-standard full-digital receiver. Such an ideal radio should be able to receive different standards on a very-broadband RF environment (300MHz-6GHz) only reconfiguring one single DSP. On one hand this would completely eliminate the analog front-end, using only one analog to digital conversion input stage after the antenna. On the other hand this would set to zero the BOM. SDR, in this sense, represent the lowest-cost possible solution in the application field of wireless receiver chains [4-5].

In the following subsections one possible preliminary step towards the realization of a SDR is shown. The on-chip analog to digital substitution is primarily object of interest, since the focus will be given to a base-band block (Chapter 1 and Chapter 2) of a wireless receiver chain. However, the BOM reduction will be also indirectly tackled when discussing the full silicon TV tuner (Chapter 3) and the SAW-less cellular receiver (Chapter 4) applications.

1.2 Towards Software Defined Radio: the Filtering ADC base-band topology

The SDR final solution (i.e. the antenna ADC) is not feasible or extremely power hungry with the present technology [6]. Attempts to move the ADC before the down-conversion mixer [7-8] have been proposed, but their performance is still not competitive with the state of the art. A simpler step towards the SDR implementation brings the analog to digital interface just after

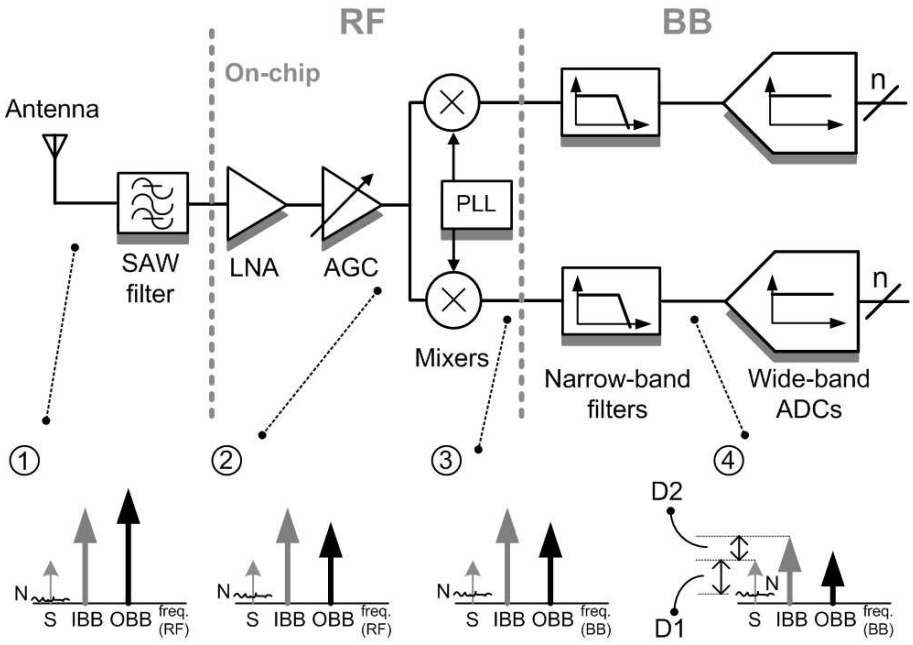


Fig. 2 A traditional direct-conversion wireless receiver chain. Scenario processing through the chain

the down-conversion stage (i.e. as the first element of the base-band section). Removing all the stages located in-between the mixer and the ADC is however not trivial, since the analog base-band implements traditionally a filtering action, which attenuates the interferers to avoid the saturation of the converter. Furthermore, a challenging noise performance is required at the base-band, to make the receiver sense the near-to sensitivity input desired signals. These aspects show the main issue of replacing the analog base-band with a single ADC: the ability of the converter to detect a low-power wanted signal surrounded by a critical scenario of high-power blockers.

The building blocks architecture of a traditional quadrature direct conversion wireless receiver is shown in Figure 2 [9]. An off-chip SAW filter is placed just after the antenna. The RF section comprises a low noise amplifier, a variable gain control block (Authomatic Gain Control), generally controlled by the digital section, and a down-conversion mixer (RF to base-band interface). The base-band (BB) is the cascade of an analog filter, which distinguishes the desired signal from the blockers depending on its filtering order, and of an analog to digital converter. The ADC is assumed with wide-band signal transfer function, since this is the most traditional case. Its most used implementation is recently the one of a continuous-time Sigma-Delta modulator, due to its low-power high performance processing and intrinsic anti-aliasing filtering. Such an ADC topology is so taken here as reference, since it gives the possibility to realize a less selective analog domain channel filtering than the case in which a Nyquist ADC is used [10-12]. The LO generation is considered apart and is assumed given by a Phase Locked Loop able to generate also the quadrature in the LO path. Notice that the chain is described only from the functional point of view and not from the circuit detail one (e.g. the variability of the gain can be implemented also at BB only, or both at RF and at BB).

A typical received input scenario going through the chain is also shown. What is of interest now is not the absolute power of the signal and of the blockers along the chain, but the relative

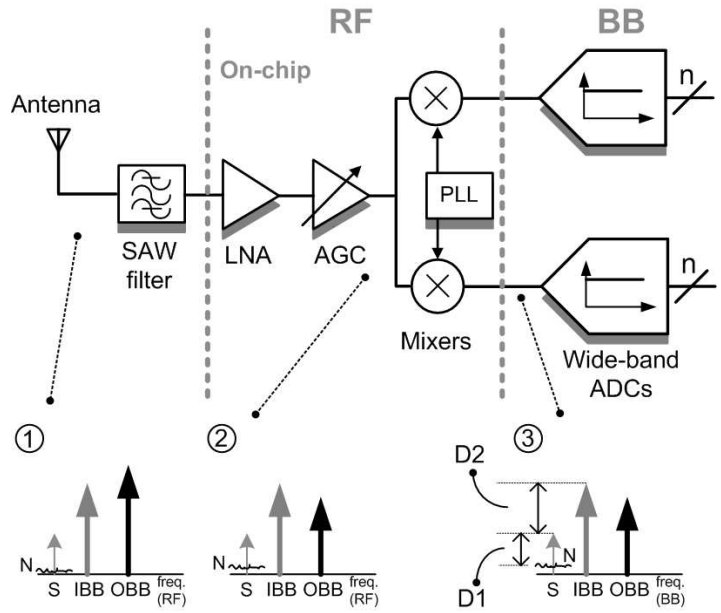


Fig. 3 A wireless receiver chain with post mixer ADC. Scenario processing through the chain

power between them. It has to be in fact taken into account that the main goal of the overall receiver, after the digital selective filtering and de-modulation, is to get the signal to noise ratio (SNR) required by the application standard (corresponding to a bit error rate), and that the filtered blockers count in this context as noise. S is the desired signal, IBB is the in-band blocker, which is out-of-the signal band of interest but into the application band, OOB is the out-of-band blocker, which falls out of the application bandwidth. The application selectivity is in general performed by the SAW (some selectivity is also given by the LNA in resonating implementations), while the signal selectivity is realized by the analog low-pass filtering stage only and not by the RF section. At the same time noise, embedding also intermodulation products for simplicity, is added by the blocks, thus reducing the distance between the signal and the noise floor at every step of the structure.

At the input of the ADC two are the elements that characterize qualitatively the spectrum. First the distance D1 between the desired signal power and the total noise floor. Second the relative power D2 between the desired signal and the interferers (Figure 2). D1 and D2 indirectly give the specifications of the ADC. Taking in fact the signal as a reference, the more D1 is small, the less the ADC can deteriorate accuracy performance of the preceding stages, and so has to have low input referred noise. The more D2 is high, the more the ADC has to be able to handle high power input signals. This in turn requires high input signal dynamic, in order to avoid a saturation, and high linearity, not to undergo the intermodulation products.

Assume now the chain case reported in Figure 3. The only difference with the former is the absence of the base-band filtering stage (the ADC is put after the mixer). Assuming negligible the noise of the filter, the distance D1 is not modified, while the distance D2 is increased. Such situation is also more critical when the SAW filter is planned to be removed. The OOB blocker in fact reaches the base-band without filtering, still increasing D2.

This simple example confirms what stated above, i.e. that demanding base-band noise and linearity performance is required at a post-mixer ADC. It also briefly introduces the problem to

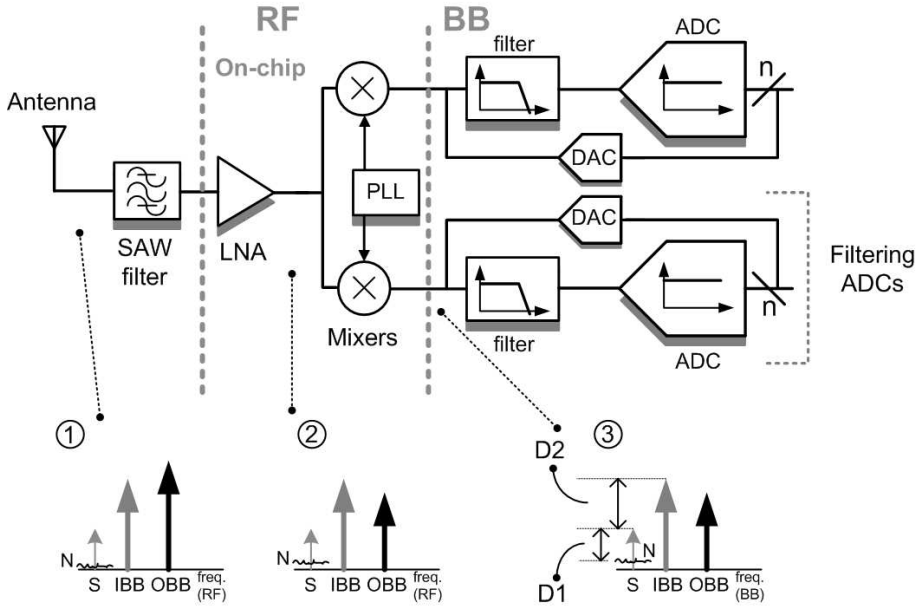


Fig. 4 The Filtering ADC based wireless receiver chain. Scenario processing through the chain

define base-band specifications, when a filtering or not-filtering solution is considered. Such an issue will be tackled in a more detailed way in section 1.3.

In this dissertation a low-pass filtering continuous time Sigma-Delta modulator is presented. It embeds interferers filtering and signal digitization in the Filtering ADC basic architecture (Filtering ADC), and combines the variable gain ability too in the Evolution Filtering ADC structure (E-Filtering ADC). Such architectures conceptually move the analog to digital interface immediately after the mixer, and they are expected to represent the entire analog base-band of a wireless receiver.

The architecture of the Filtering ADC based receiver chain is reported in Figure 4, together with the signal processing through it (for simplicity the Filtering ADC notation is used here to address both the basic and the evolution implementation). A digital to analog converter (DAC) is used to close a feedback loop from the ADC output to the filter input. The specifications D1 and D2 for the overall ADC, if referred at the input of the base-band, are the same as for the wide-band ADC case. In Figure 4 the AGC block has been also embedded into the base-band, since it is the case of the E-Filtering ADC.

The operation of combining the filtering action into the ADC is attractive only if an advantage can be clearly seen with respect to the filter-ADC cascaded topology. The base-band specifications in fact are also equal to the ones required at the filter input (not at the ADC input) of the more traditional base-band. The main consequences of this are that neither the base-band noise can increase, nor the non linearity can be degraded and that the power consumption and area have to be maintained less or equal. In this sense the Filtering ADC is useful only if it gives to the receiver the possibility to get a more efficient elaboration than the cascaded solution.

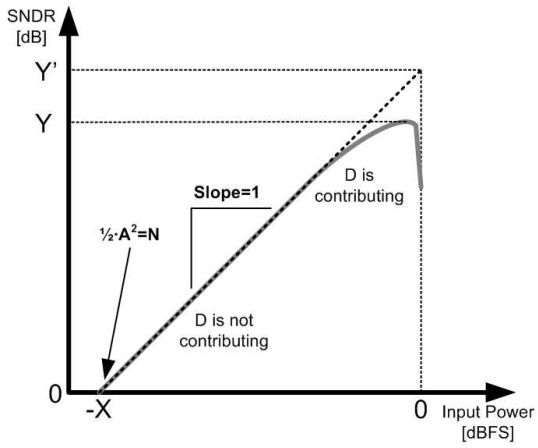


Fig. 5 Traditional SNDR plot for a Sigma-Delta ADC converter

1.3 Signal to noise and distortion ratio and dynamic range profile

Traditionally, ADC specifications are provided in terms of signal to noise and distortion ratio (SNDR) and dynamic range (DR). They are used to address conceptually the capability of a circuit to handle the large signals with good linearity (up to the saturation) and to detect vice-versa the small ones (down to the noise floor) with accuracy, and are so directly linked to the quantities D1 and D2 described before. SNDR and DR are defined in literature as follows: first the SNDR is given and then the DR [13].

As the name suggests, the SNDR is the ratio between the power of the in-band signal processed in an ADC divided for the sum of the noise N integrated in the band of interest and the distortion products D generated in the same band. The SNDR is in general given output-referred, since distortion and noise are physically observed at the block output. Being the ADC traditionally a wide-band system, however, no difference is obtained if the SNDR is input-referred. Assuming a sinusoidal tone at the input with amplitude A, the SNDR is given by the following equation:

$$\mathrm{SNDR} = \frac{\frac{1}{2}\mathrm{A}^2}{\mathrm{N+D}}. \qquad (1)$$

An in-band signal tone is used and the distortion D is in this case the third harmonic distortion of the ADC. N is the noise floor of the converter. The SNDR depends on the amplitude of the input signal. A SNDR plot versus the input power is reported in Figure 5. This graph is always used to characterize the ADC performance, especially in the field of Sigma-Delta converters. At low amplitude A the distortion D can be neglected in comparison to N, and so the SNDR grows proportional with the signal power. At certain amplitude the third harmonic distortion dominates the noise floor and the SNDR loses its slope with respect to the input increase. In a real implementation, when the amplitude is close to the converter full-scale FS, which is the maximum signal that can be handled by the circuit (e.g. at the limit of the converter instability in a Sigma-Delta modulator implementation), other effects arise, thus deteriorating the SNDR more than the non-linearity only. Actually the maximum SNDR (maxSNDR, Y in

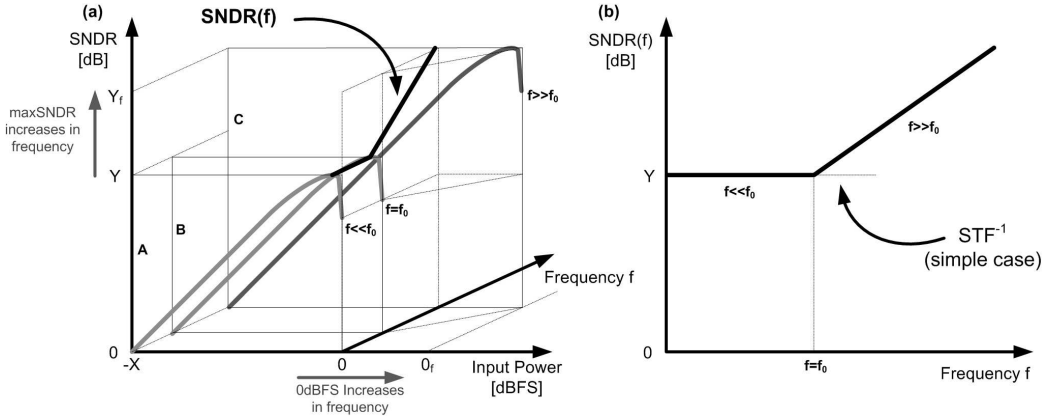


Fig. 6 (a) 3D SNDR(f) profile evaluation. (b) 2D plot of a SNDR(f) profile example

Figure 5) and the distance in dB between the amplitude level at which it is reached and the full-scale reference level of the converter are object of interest. The equivalent number of bits of a converter (ENOB) is in fact calculated from the maximum SNDR, being ENOB=(maxSNDR-1.76)/6.02.

The dynamic range is defined as the ratio between the maximum signal that the converter is able to handle (i.e. 0dBFS) and the noise floor N. It can be read in the SNDR plot as X (x axis, inverting the sign, of the point at which SNDR=0) or as Y'.

The SNDR and DR definitions given so far are valid not only for ADC converters, but can be extended directly to any kind of circuit (base-band) with wide-band signal transfer function response.

When a filtering block is taken into consideration, as e.g. the Filtering ADC, the definitions of SNDR and DR have to be modified, to provide in a more useful and fair way the base-band block specifications. It was shown that the input of the Filtering ADC (or the input of any base-band section) is represented by a desired signal and surrounding interferers. While in a wide-band circuit both the signal and the interferers are inside the converter bandwidth and so are processed in an equal way, a narrow-band solution is able to distinguish the useful information from the blocker. The main consequence of this is that the SNDR and DR definitions can hold not longer, since the filtering dependence has to be analyzed.

The simple difference, in comparison to wide-band architectures, is that the maximum signal that the base-band has to handle is no more inside the band of the circuit. The base-band specification is in fact defined in the worst case reception, i.e. with a noise able to satisfy sensitivity requirements and with linearity able to tolerate high power blockers, falling now out of the circuit band. Vice-versa, and this is valid also without filtering, the information desired signal is not expected to saturate the architecture. This is the case tackled exploiting the AGC functionality, considering also that the receiver performance can be degraded.

In this sense not a single maxSNDR is given, to provide base-band specifications, but instead, at any frequency f, the ratio between the maximum interferer that the filtering base-band is able to handle and the noise added by the base-band in the signal band of interest. The non-linearity intermodulation products have of course to be considered into this noise amount. Since the SNDR depends on frequency, a SNDR profile is obtained (SNDR(f)). Notice that this is not actually a signal to noise and distortion ratio, but an interferer to noise and distortion ratio.

The notation SNDR has been maintained providing the possibility to extend a concept already consolidated in literature. A simplified definition of the SNDR(f) profile is:

$$\mathrm{SNDR(f)} = \frac{\frac{1}{2}\left(\mathrm{A_{int}(f)}\right)^2}{\mathrm{N+D}} \qquad (2)$$

in which $A_{int}(f)$ is the amplitude of the interferer that maximize the SNDR at the frequency f and N and D are integrated in the desired signal band. Due to the intrinsic filtering an input-referred definition is mandatory to correctly define the base-band specifications.

The graphical representation of the SNDR(f) is given in Figure 6. Consider the plot at the frequency $f<<f_0$, where f_0 is the cut-off frequency of the filtering section. The plane corresponds in Figure to the letter A. Being f near-DC, the filtering action has not effect and the SNDR plot is the same as the one reported in Figure 5. The only difference is that intermodulation non-linearity is evaluated instead of the harmonic one. The SNDR($f<<f_0$) is defined equal to maxSNDR=Y. Move now at the plane corresponding to the letter B, in which $f=f_0$ is considered. For simplicity it has been assumed in the plot not to have at f_0 any filtering effect and an in-band equivalent behavior is still obtained (SNDR($f=f_0$)=maxSNDR=Y). The third step is at an out-of-band frequency (plane C, $f>>f_0$). In this case the filtering is working and in consequence the base-band full-scale reference is modified from 0dBFS into 0_f dBFS. Assuming that non linearity products D starts to be comparable, with respect to N, always at a fixed distance from the full-scale, a maxSNDR Y_f greater than Y is achieved, since the base-band structure benefits of the filtering (SNDR($f>>f_0$)=maxSNDR=Y_f). The difference between Y_f and Y is in this case the amount of filtering (equal to the difference between 0_f and 0 in dBFS). The resulting SNDR profile is defined as the plot versus frequency of the maxSNDR and grows from the in-band value as the inverse of the filter signal transfer function (Figure 6.b).

A strong simplifying assumption has been done before. It is not always true that the linearity performance follows one-to-one the full-scale. This is an optimistic situation in a real base-band design and mainly is equivalent to the assumption of having all the filtering before the generation of the distortion. More frequently, every filtering is realized after the distortion, when an active stage is used at the base-band input, or partly the filtering is performed before the active stage and partly after. Furthermore, it has to be considered that the full-scale can change in frequency, following the signal transfer function of the filtering section, only if the output node of the base-band is the one that limits the block dynamic. Otherwise, the internal nodes of the architecture limit the increase of the SNDR(f) profile to a slope less than the inverse of the filtering profile.

The dynamic range profile (DR(f)) is the frequency dependent extension of the DR defined in the traditional case. It can be mathematically obtained from (2) if D is considered equal to zero and $A_{int}(f)$ is substituted with the full-scale of the base-band (i.e. the maximum interferer handled by the base-band) at different input frequencies. The full-scale $A_{int}(f)$ can be simply evaluated injecting at the input a single tone at a frequency f and increasing its power until the level at which base-band clamping (or instability, in a modulator implementation) is reached.

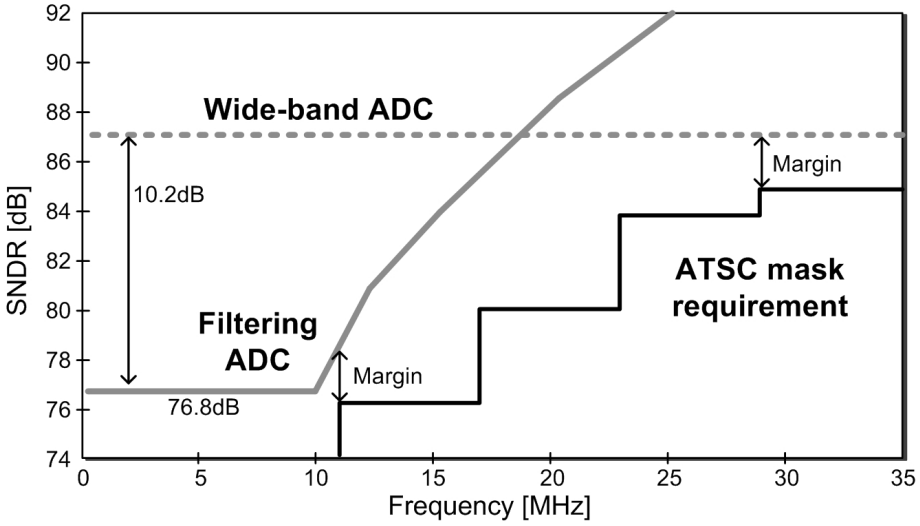


Fig. 7 Filtering ADC versus wide-band ADC requirements

1.4 Filtering ADC versus wide-band ADC

The SNDR and DR profiles will be used in Chapters 3 and 4 to get the specification of the base-band for the proposed Filtering ADC application prototypes and to provide the corresponding measurement results. This section gives some brief insight into the comparison between a Filtering ADC and a wide-band one in terms of SNDR(f) with respect to an application example. The standard chosen is the ATSC-A/74 one. It is satisfied by the integrated Filtering-ADC based receiver presented in Chapter 3.

The SNDR required by the ATSC is reported in Figure 7 (1MHz to 7MHz channel bandwidth). The in-band SNDR is equal to 72dB (level not shown in the Figure). This is due to 18dB of minimum SNR required by the standard (assuming that in this critical condition the base-band dominates the noise), 10dB of peak to average ratio of the OFDM video signal and 44dB of adjacent channel power offset with respect to the desired signal. Since the interferer profile grows in frequency the required SNDR is 76dB at 11MHz, 84dB at 23MHz and 85dB at 29MHz.

A wide-band ADC is not able to follow this behavior. In order to meet the specifications, including also other 2dB of margin due to process spreads and corner worst cases, an impressive ENOB of 14.2bits would have to be implemented over the entire range of frequencies. This is a challenging number considering that it has to be obtained over a pretty-wide bandwidth of 6MHz under power consumption demanding constraints.

A Filtering ADC benefits instead of the embedded selectivity. In the Figure the simplest case of a second order signal transfer function with a 10MHz cut-off frequency f_0 is shown. For the given profile the most critical point is one adjacent channel (11MHz edge). Only 76.8dB are now required in the signal band of interest, still satisfying all the out-of-band requirements. The specification is about 10dB far from the wide-band implementation one, saving almost 1.8bits (12.4ENOB satisfies the specification). The reported filtering profile is probably too much optimistic in comparison to a base-band real implementation. This is true both for the

40dB/decade slope and for the extremely narrow-band solution. In any case a big difference can be appreciated and the Filtering ADC is clearly seen to fit better base-band performance with specifications than a wide-band one.

Chapter 2

The Filtering ADC

In this chapter the Filtering ADC architecture is presented (2.1). Using a straightforward continuous time model the Filtering ADC benefits are analyzed in detail and are compared with the state of the art of wireless receiver analog base-bands (2.2). The wide-band section of the ADC is then addresses (2.3). Finally, a Filtering ADC evolution (E-Filtering ADC) is described (2.4) and a comparison between the two proposed base-bands is shown (2.5).

2.1 The Filtering ADC architecture

The Filtering ADC proposed in this chapter is intended to implement the complete analog base-band of a wireless receiver. Two main elements have to be addressed by its circuit architecture to accomplish this goal.

First, the analog RF front-ends (Low Noise Amplifier and mixer in cascade), proposed in recent literature, mainly down-convert at base-band signals in the current domain. This is the case of the solutions implemented with a Low Noise Amplifier followed by a Gilbert active mixer [14], which has been the mainstay architecture of integrated receivers until about 100nm of transistor channel length. This is more recently the case of a Low Noise Transconductor followed by a passive current mixer, which represents the state of the art design structure [3,15]. The choice to realize voltage to current conversion (V/I) at the RF interface applies for a corresponding current to voltage conversion (I/V) to be operated in the base-band section, because the input sampling of an ADC is traditionally operated in voltage mode. For this reason the Filtering ADC has to implement a transimpedance gain, being able to handle at its input a spectrum composed of current tones, and has to show low input impedance to the front-end.

Second, as already pointed out in Chapter 1, an extremely demanding signal to noise and distortion ratio (or dynamic range) profile is required at the Filtering ADC. Remember that the

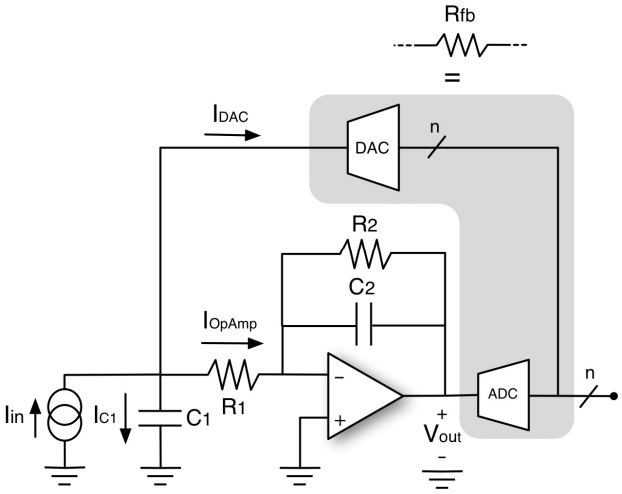


Fig. 1 The Filtering ADC based complete analog base-band. Single ended for simplicity

handling of high power blockers, together with a low noise floor, and low distortion is the challenge of any base-band, especially in a low-power environment.

The proposed Filtering ADC architecture, which has been found to well face the previous issues (transimpedance gain and high SNDR potentiality), is shown in Figure 1 [16]. The block combines in the same feedback loop interferer filtering and signal digitization, thus embedding in a single architecture the functionality of a filter and of an ADC converter. The design structure derives from a current driven biquad cell, in which the main feedback resistance (R_{fb}) is replaced by the cascade of an ADC and of a current DAC.

The input signal is the current down-converted by the mixer (I_{in}), while the output signal is the output code of the filtering ADC. This code is in turn proportional to the current absorbed by the DAC (I_{DAC}), through a transimpedance-like gain. It is crucial at this point to distinguish between the internal ADC block (ADC in Figure 1) from the Filtering ADC itself. The first one acts as a quantizer in the voltage domain, providing the output bits, at a given clock frequency, as the digital/thermometric conversion of V_{out}, and introducing the quantization noise of the system. The second one refers to the complete base-band circuit (Figure 1), and comprises the filter (operational amplifier, resistances R_1, R_2 and capacitances C_1 and C_2), the internal ADC and the DAC.

The output node of the operational amplifier is the limiting point, considering the dynamic voltage swing, and is controlled by the transimpedance overall gain of the block. At the same time the swing at the input voltage node has to be not too high not to deteriorate the DAC functionality, and is regulated by the input impedance of the Filtering ADC. A low pass transfer function is the link between the node V_{out} and the input node. The gray section in Figure 1 is the digital section of the block. No assumptions are given at this level of analysis over the ADC and DAC implementations.

Notice that the structure of the presented Filtering ADC is not different, from the point of view of the topology, from that of a continuous time Sigma-Delta ADC converter. This proves how this category of oversampled ADCs, with intrinsic filtering and anti-alias, can be naturally

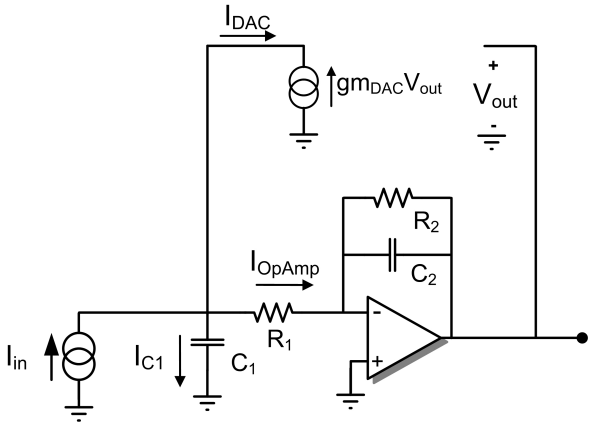


Fig. 2 The Filtering ADC continuous time equivalent model

used and is competitive, if updated with only little modifications, in the wireless receiver low-power environment.

The high SNDR profile required to place the ADC directly at the mixer output is obtained exploiting three intrinsic properties of the circuit. First, the grounded capacitance C_1 increases the ADC tolerance to out-of-band interferers, absorbing the largest part of the blockers down-converted at base-band by the mixer. Second, both analog and quantization noise benefit from an in-band noise shaping effect that is not present in a cascaded filter-ADC design. Third, a couple of complex conjugate poles can be synthesized by the DAC feedback loop, obtaining both a second order filtering profile, with controlled in-band flatness, and a direct digital output. In the next sections these elements will be addressed in detail, showing that the Filtering ADC can be considered a further step, with respect to the base-band solutions recently proposed in literature, in the direction of satisfying the receiver's need to handle critical interferer standard profiles.

A. Continuous time model and signal transfer function

To evaluate the Filtering ADC transfer functions, the ADC-DAC cascade is considered at this level of analysis to operate in the continuous time domain. Moreover, both the internal ADC and the DAC are assumed sufficiently wide-band not to affect the signal transfer function in a significant way. Under these conditions, the continuous time Filtering ADC model reported in Figure 2 is obtained. The internal ADC is considered ideal, however remembering to take into account its quantization noise. The DAC is modeled with a transconductor, whose transconductance gm_{DAC} is the ratio between the full-scale current of the DAC and the full-scale reference voltage of the ADC. In this sense, to get the same signal transfer function (STF) with respect to the original current driven biquad, the value of gm_{DAC} is equivalent to the inverse value of R_{fb}.

The Laplace domain signal transfer function is a second order low pass biquad:

$$H(s) = \frac{R_2}{1+gm_{DAC}R_2+s(C_1R_1+C_2R_2)+s^2C_1R_1C_2R_2}. \qquad (1)$$

The in-band transimpedance gain G, cut-off frequency f_0 and quality factor Q are given by:

$$G = \frac{R_2}{1+gm_{DAC}R_2} \qquad (2)$$

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{1+gm_{DAC}R_2}{C_1R_1C_2R_2}} \qquad (3)$$

$$Q = 2\pi f_0 \frac{C_1R_1C_2R_2}{C_1R_1+C_2R_2}. \qquad (4)$$

Notice that if $gm_{DAC}R_2>>1$ (2) can be simplified to $1/gm_{DAC}$ and so, for a given full-scale reference voltage of the internal ADC, G can be controlled acting on the full-scale DAC current. The 1 weight, with respect to the $gm_{DAC}R_2$ product, represents the quantity of current that is absorbed in-band by the forward path, with respect to the feedback one. In the same case the cut-off frequency f_0 approaches $1/(2\pi)\cdot\sqrt{(gm_{DAC}/(R_1C_1C_2))}$, depending on the time constant of both the input passive R_1C_1 filter and of the feedback of the integrator R_2C_2, multiplied by the in-band loop gain of the system $gm_{DAC}R_2$. The Q is given by the relative time constants values. If the equivalent quality factors of the capacitance C_1 $Q_{C1}=2\pi f_0R_1C_1$ and of the capacitance C_2 $Q_{C2}= 2\pi f_0R_2C_2$ are evaluated, it follows that $Q=Q_{C1}Q_{C2}/(Q_{C1}+Q_{C2})$.

Looking at Figure 2 the input impedance of the Filtering ADC can be also obtained

$$Z_{IN}(s) = \frac{R_1(1+sC_2R_2)}{1+gm_{DAC}R_2+s(C_1R_1+C_2R_2)+s^2C_1R_1C_2R_2} \qquad (5)$$

It shows a low pass behavior, with a zero given by the time constant C_2R_2 and the two poles of the signal transfer function.

To understand from an intuitive point of view the functionality of the Filtering ADC, three main elements can be highlighted from the circuit in Figure 2. First, the capacitance C_1, which is connected from the input node to ground. Second, the resistance R_1, which is connected from the input node to the virtual ground of the operational amplifier. Third, the low pass active-RC filter closed in a loop by the feedback DAC. This latter element is able to drain a current, which is low-pass filtered, in response to a voltage input node variation. In this sense it implements a gyrator, showing from the input node to ground an equivalent inductance. Actually the finite in-band gain of the filter does not synthesize a pure inductance, but a lossy one (inductance/resistance in series). At low frequency ($f<1/(2\pi R_2C_2)$) in fact the relation between the input node voltage and the DAC current is simply proportional and not frequency dependent. The elements described so far directly lead to the equivalent RLC network of the Filtering ADC, which is shown in Figure 3. The inductance L is equal to R_1C_2/gm_{DAC} while its series resistance is equal to $R_1/(gm_{DAC}R_2)$. The quality factor of the L element is $Q_L= 2\pi f_0L/R= 2\pi f_0C_2R_2=Q_{C2}$ and can be controlled by the C_2R_2 time constant sizing, for a given f_0.

The RLC network Filtering ADC model is an immediate tool to evaluate the transfer functions from the input current to the current flowing into the DAC (inductive path), into the input capacitance C_1 and into the operational amplifier (I_{DAC}/I_{in}, I_{C1}/I_{in} and I_{OpAmp}/I_{in} in Figure 3). The first of these transfer function (i.e. providing the current flowing into the feedback) gives also the signal transfer function of the Filtering ADC, if reported in the voltage domain by a $1/gm_{DAC}$ transimpedance multiplication.

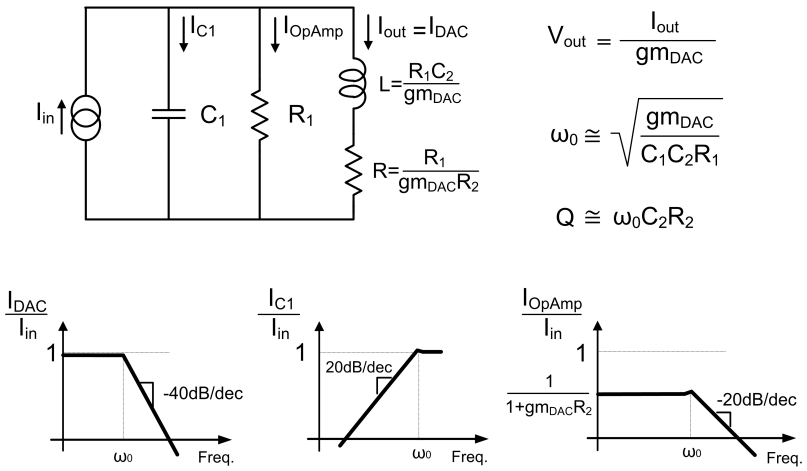


Fig. 3 The RLC Filtering ADC equivalent network

At very low frequency the input impedance is the parallel of the resistances R and R_1. Since R is much lower than R_1 in a usual design ($R=R_1/(gm_{DAC}R_2)$), the in-band current is handled by the DAC. Vice-versa the current in the operational amplifier is reduced by the factor $(1+gm_{DAC}R_2)$. At high frequency, the effect of the DAC is negligible, and all the input current is absorbed by the input capacitance C_1, which represents the input impedance of the architecture much above f_0. The grounded capacitance C_1 ensures a low impedance path at high frequency, thus absorbing with a first order filtering the input blockers. The main consequence of this is that the active elements (DAC and operational amplifier) have to handle out-of-band interferers that are reduced than the input ones. The DAC current experiences a second order filtering, being the converter connected to the output node. The operational amplifier current undergoes a first order filtering. The advantage of the structure relies on the fact that the input filtering due to C_1 is realized in a passive way, so without power consumption penalties. In this sense the proposed structure differs from existing Filtering ADC solutions where an active device (typically the first operational amplifier) has to absorb all the input down-converted current, thus representing the most power hungry element and bottleneck of the design [17].

C_1 may result in a big capacitance. This can affect the circuit area, but this issue is counterbalanced by the beneficial effect that the low impedance of C_1 has also on the operation of the preceding mixer. Very high frequency blockers in fact see the equivalent of a virtual ground at base-band. This is not always true in an integrator-first design when the operational amplifier gain falls below 0dB (after the f_T frequency of the operational amplifier), making the base-band input impedance growing.

As will be explained in detail in Chapter 5, it is not correct to consider the RF front-end, which drives the base-band, as a simple current generator. Both if an active mixer or a passive one is considered, its output impedance could not be so much higher with respect to the input base-band impedance to be neglected. It follows that the signal transfer function of the Filtering ADC is modified by a finite-value driving. The simplest way to model the down-conversion mixer is to put a resistance R_S in parallel to the current generator. The signal transfer function (1) is, in consequence of this, modified as:

$$H'(s) = \frac{R_2}{1+\frac{R_1}{R_S}+gm_{DAC}R_2+s\left(C_1R_1+C_2R_2\left(1+\frac{R_1}{R_S}\right)\right)+s^2C_1R_1C_2R_2} \qquad (6)$$

from which it is possible to derive:

$$G' = \frac{R_2}{1+\frac{R_1}{R_S}+gm_{DAC}R_2} \qquad (7)$$

$$f_0' = \frac{1}{2\pi}\sqrt{\frac{1+\frac{R_1}{R_S}+gm_{DAC}R_2}{C_1R_1C_2R_2}} \qquad (8)$$

$$Q' = 2\pi f_0' \frac{C_1R_1C_2R_2}{C_1R_1+C_2R_2\left(1+\frac{R_1}{R_S}\right)}. \qquad (9)$$

There is an interesting aspect to observe from (7-9). The finite value of R_S affects both the transimpedance gain of the Filtering ADC, its cut-off frequency and its quality factor, representing an issue in the controllability of the signal transfer function if R_S is not well predictable or modeled at the design level.

Although the continuous time model is only an approximated model, it has been verified that, in the band of interest, so at very low frequency with respect to the clock frequency of the internal ADC, almost the same results are provided by a more correct discrete time model [6,18]. Of course the Filtering ADC is not a continuous time system. Any Sigma-Delta ADC converter, even if with continuous time design, is a discrete time block [19]. The internal ADC in fact introduces a sampling and a consequent discrete time operation. This issue is tackled in detail in the Appendix I, providing the discrete time equivalent theory of the Filtering ADC and the discrete time models used for the design. It will be shown that the discrete time effects act to modify the transfer functions of the converter the more the frequency of interest is close to the clock of the architecture.

B. Proposed Filtering ADC solution versus the state of the art of wireless receiver base-bands

In recent works, the problem to be resilient to high power out-of-band interferers has been solved at the base-band with the insertion of an RC passive filter, followed by an additional active RC transimpedance stage, directly at the output of the down-conversion mixer [3,15]. This of course implements a two-real-poles cascade. The Filtering ADC is able to synthesize a couple of complex conjugated poles, thus providing an advantage in the comparison with the previous solutions in terms of selectivity, for fixed in-band flatness. Such a more selective profile is shown with quantitatively insight in Figure 4. Here a second order Butterworth is plotted together with two different two-real-poles transfer functions, obtained moving the poles from the dominant pole solution to the coincident poles one. The ATSC filtering mask is reported also as a reference. The Butterworth solution is able to satisfy the requirements of 0.8dB maximum drooping in-band and 9dB attenuation at 3.3 times the 7MHz signal bandwidth

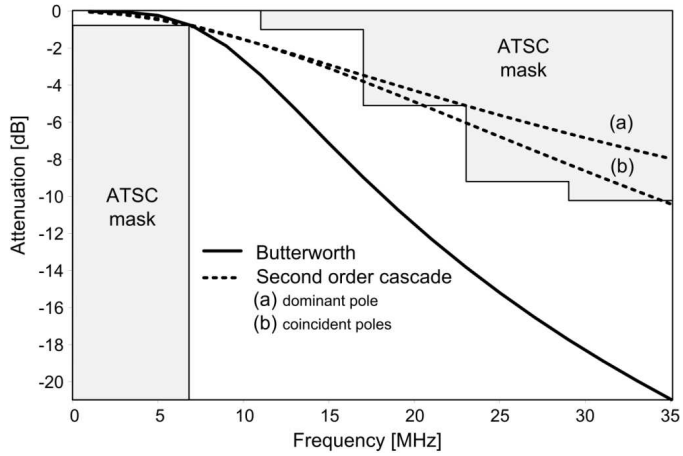


Fig. 4 Comparison between a solution with complex poles (Butterworth) and a second order two-real-poles cascade

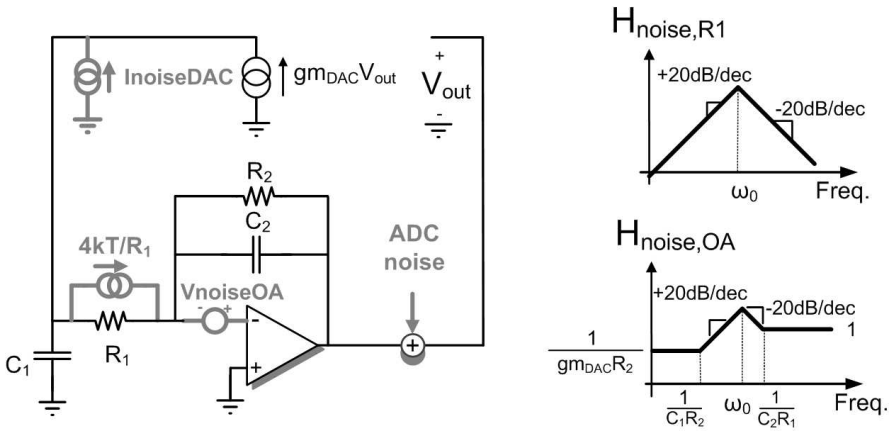


Fig. 5 The Filtering ADC continuous time model and its noise sources. Noise transfer functions of both R_1 and the operational amplifier

corner. This characteristic of the filtering ADC makes this proposal an improving step, with respect to the base-band analog architectures recently proposed, towards the improvement of the immunity of a receiver chain to out-of-band blockers.

2.2 The Filtering ADC noise

A high SNDR (or DR) profile base-band can be designed either by increasing the maximum signal that can be handled by the circuit or vice-versa boosting the resolution lowering the noise floor. The Filtering ADC topology presents also useful characteristics from the point of view of the noise, since the presence of a single feedback loop closing both the filter and the ADC provides a noise shaping effect to the quantization noise and to the thermal noise of the internal ADC. Besides, the main noise contributors of the filter itself benefit from an in-band shaping, due to both the input current driving of the architecture and the output current reading operated by the DAC (I_{DAC}, proportional to the output code, in Figure 1).

The continuous time model shown in Figure 2 can be used also for the noise analysis, and is reported in Figure 5. The main noise sources of the architecture are the resistor R_1, the

operational amplifier, the feedback current DAC and the ADC. While the DAC noise undergoes a flat transfer function to the output, since it injects its noise current directly at the input node (as the input signal), all the other noise sources are high pass shaped, until the cut-off frequency $f_0=\omega_0/2\pi$ of the filter.

An in-band zero is introduced in the transfer functions through two different mechanisms. First, for the digital (quantization) noise and the analog noise of the ADC, it is the direct consequence of having inserted the ADC in a loop with a preceding low-pass filter. Second, for the R_1 noise and the operational amplifier noise, it is due to the current working mode of the structure, as observed also in the current filters proposed in [20]. This second principle can be intuitively view as follows. Assume to consider the in-band behavior of the Filtering ADC, so with C_1 and C_2 as open circuits, and to evaluate the noise transfer function of R_1 (it is almost the same effect also for the operational amplifier noise). The noise current injected by R_1 cannot flow into the feedback high impedance path, because the DAC operates as an ideal transconductor, and is so forced to re-circulate inside R_1 itself without affecting the output. At high frequency, instead, the capacitance C_1 shunts the input node to ground offering an exit path to the noise. The consequence is that noise is able to reach the output in a high pass fashion. Another peculiar characteristic of this topology is that noise, if dominated by the high pass shaping contributions, could be reduced in theory by reducing the input capacitance C_1, and the area (increasing R_1 not to modify the signal transfer function). Vice-versa the input impedance of the architecture would be increased, and this is not always acceptable, since at the input node of the converter both the feedback DAC and the mixer injects their currents requiring a low output swing (noise/input impedance trade off).

The noise transfer function of the ADC and the quantization noise transfer function will be analyzed later in section 2.2.A and 2.3. The noise transfer functions of R_1 and of the operational amplifier are reported in Figure 4. Notice the high pass shape, which is valid below the cut-off frequency f_0 of the Filtering ADC. Notice also that a finite low frequency floor is present for the operational amplifier, due to the presence of R_2. At this plateau, however, noise is already compressed by the loop gain $gm_{DAC}R_2$.

As stated before, the high pass shaping is due to the C_1 shunting to ground of the input node. If a finite driving impedance R_S is considered, it affects the noise transfer function introducing an in-band floor which grows the more R_S is low (it acts at the same mode as C_1 but of course without differences in frequency). This behavior is a characteristic of the current nature of the topology too.

The DAC noise transfer function, in a Filtering ADC, is equal to the signal transfer function. Nonetheless it is not straightforward to estimate the DAC noise source. The DAC in fact is not a continuous time block, but works in the discrete time domain. It is possible to demonstrate that its noise is proportional to the equivalent DAC transconductance gm_{DAC}, and to the ratio between the maximum analog output of the Filtering ADC (V_{OUT}) and the overdrive of a unit DAC cell (V_{OV}). A detailed description will be reported when the class-B DAC will be discussed in section 2.4.E.

R_2 noise is also present. It is almost reduced by the factor R_1/R_2, with respect to the R_1 noise, and can be considered negligible in a typical Filtering ADC sizing.

$$\overline{V_{OUT,OA}^2} = 4kTR_{EQ}\left(\frac{R_2+R_S+R_1}{R_S+R_1+gm_{DAC}R_2R_S}\right)^2 f_B + \frac{16\pi^2}{3}kTR_{EQ}(C_1+C_2)^2\left(\frac{(R_2+R_1)R_S}{R_S+R_1+gm_{DAC}R_2R_S}\right)^2 f_B^3$$

$$\overline{V_{OUT,R1}^2} = 4kTR_1\left(\frac{R_2}{R_S+R_1+gm_{DAC}R_2R_S}\right)^2 f_B + \frac{16\pi^2}{3}kTR_1{C_1}^2\left(\frac{R_2R_S}{R_S+R_1+gm_{DAC}R_2R_S}\right)^2 f_B^3$$

With: $gm_{EQ,DAC} \cong 4\frac{V_{OUT}}{V_{OV}}gm_{DAC}$

$$\overline{V_{OUT,DAC1}^2} = 4kTgm_{EQ,DAC}\left(\frac{R_2R_S}{R_S+R_1+gm_{DAC}R_2R_S}\right)^2 f_B$$

$$\overline{V_{OUT,R2}^2} = 4kT\frac{1}{R_2}\left(\frac{R_2}{R_S+R_1+gm_{DAC}R_2R_S}\right)^2 (R_1+R_S)^2 f_B + \frac{16\pi^2}{3}kT\frac{1}{R_2}C_1^2\left(\frac{R_2R_1R_S}{R_S+R_1+gm_{DAC}R_2R_S}\right)^2 f_B^3$$

Fig. 6 Filtering ADC noise transfer functions (simplified OA expression)

Quantitatively, the high pass shaped contributors, which decide the Filtering ADC noise performance, give origin to a noise-selectivity trade-off in the design. For a given channel bandwidth f_B, a higher cut-off frequency f_0 reduces the in-band noise, since the high pass behavior scales with f_0, but at the same time the out-of-band blocker attenuation is diminished. Such a noise selectivity trade-off is also peculiar of the current mode filter topologies proposed in [20].

Figure 6 regroups the noise transfer functions of the Filtering ADC that have been addressed so far, taking into account the effect of the finite driving impedance R_S. All the equations have been simplified neglecting the low-pass effect of the Filtering ADC poles, and so are accurate the more f_0 is far from the signal bandwidth f_B of interest (the band in which noise has to be integrated). A factor 0.8 of f_B/f_0 is required to get an accuracy of less than 0.5dB in the noise evaluation, in comparison with simulation, of each contributor. The k symbol used in the equations is the Boltzmann constant while T is the absolute temperature.

A. Proposed Filtering ADC noise versus the Rauch filter solution

In terms of noise it is difficult to make a comparison between the Filtering ADC solution and the two-real-poles cascade architecture implemented in the state of the art receivers [3, 15]. These structures have different signal transfer functions than the Filtering ADC, and their dynamic range profile, as defined in Chapter 1, is so affected by the noise in a different way. A fairer and more general comparison has been evaluated between the Filtering ADC and an equivalent base-band architecture composed by a filter-ADC cascade and shown in Figure 7. The converter is the same as the internal one of the Filtering ADC. The filter is realized with the current driven biquad cell from which the Filtering ADC has taken origin (resistance R_{fb}, instead of the feedback DAC, connected to the operational amplifier output). The two solutions have been analyzed considering the same signal transfer function, the same operational amplifier and the same impedance levels for the filter.

First, while the resistance R_{fb} is bilateral, the feedback DAC is unilateral (generates a current in consequence of the output code). The bilateral resistance transfers to the output the voltage noise of the input node with a unitary gain, thus limiting the in-band noise shaping of the architecture with a 0dB low frequency floor in the noise transfer functions of both the R_1 and the operational amplifier source. This does not occur with the DAC, and it is possible to

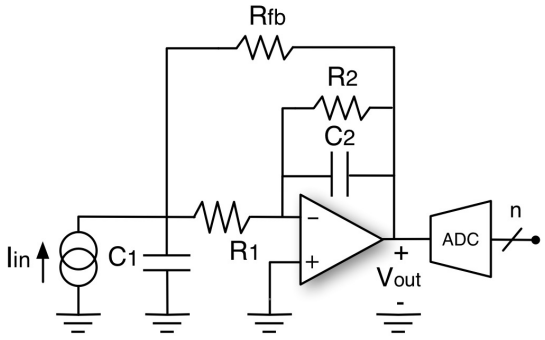


Fig. 7 The base-band filter-ADC cascade used for the noise comparison

demonstrate that the advantage depends on the $gm_{DAC}R_S$ factor, increasing the more R_S is higher.

Second, due to the different loop, the internal ADC quantization and analog noise transfer function, in the Filtering ADC, corresponds to the following high-pass:

$$F'(s) = \frac{\left(1+\frac{R_1}{R_S}+sC_1R_1\right)(1+sC_2R_2)}{1+\frac{R_1}{R_S}+gm_{DAC}R_2+s\left(C_1R_1+C_2R_2\left(1+\frac{R_1}{R_S}\right)\right)+s^2C_1R_1C_2R_2} \quad (10)$$

while a flat transfer function with gain equal to 0dB is obtained for the ADC of the cascaded base-band (assuming an ADC gain of one). This is always true, for the ADC analog noise. For the quantization noise, the overall transfer function depends also on the actual implementation of the converter, but (10) still represent the frequency dependent transfer function ratio between the Filtering ADC and the filter-ADC cascade performance. F'(s) provides a first order shaping since one zero (C_2R_2) is placed near the f_0 of the two poles. The in-band plateau depends on the $gm_{DAC}R_2$ product. As expected the choice of the cut-off frequency of the Filtering ADC determines the quantitative advantage of such a solution in the comparison, since also the ADC quantization and analog noise sources rely on the noise/selectivity trade-off of the Filtering ADC.

A fair comparison has to take into account also how much noise is introduced by the DAC, with respect to the feedback resistance R_{fb}. Again this will be discussed in section 2.4.E. Even if it is possible to demonstrate that a simple resistance is in general less noisy than a DAC, two aspects have to be taken into account. On one hand the noise of the DAC is not one of the dominant Filtering ADC noise contributions. On the other hand it is possible to implement a DAC low-noise solution, as the class-B DAC proposed later.

2.3 The Filtering ADC wide-band section

The internal ADC of the Filtering ADC has been considered for the continuous time model as an ideal connection. Of course this is a strong simplifying assumption. The discrete time behavior of the internal ADC, which makes the overall Filtering ADC a discrete time circuit more than a continuous time one, will be tackled in Appendix I. The dynamic effect of the block

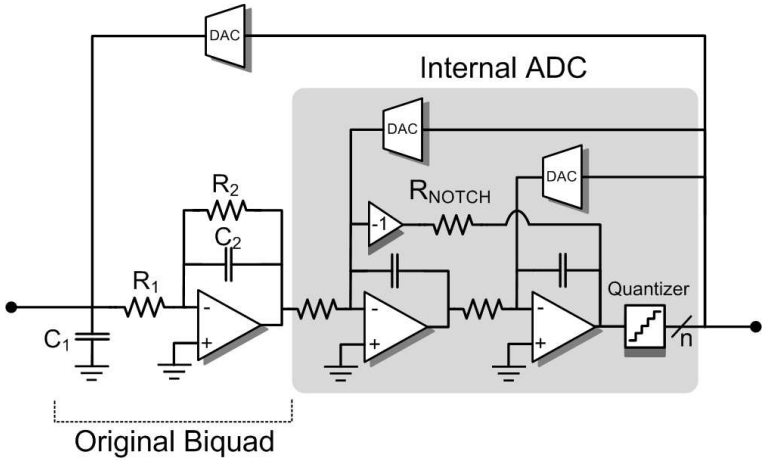


Fig. 8 Substitution of the internal ADC with a wide-band second order Sigma-Delta converter in multi-feedback compensation topology

is instead addressed in this section, providing both its more straightforward implementation and its effects on the signal transfer function and on the quantization noise transfer function of the entire converter. This latter element mostly gives the internal ADC design guidelines.

The internal ADC could be in theory a simple quantizer, realized as a Full-Flash ADC. The main limitation of this solution is that only a first order noise shaping is obtained (see (10)), thus strongly reducing the high dynamic range potentiality of the implemented base-band. As in a traditional continuous time Sigma-Delta converter, increasing the number of bits of the internal ADC would increase also the global converter quantization noise performance. This can be done increasing the number of levels of the quantizer (multi-bit solution), increasing the ADC clock frequency, to exploit oversampling, or designing the internal ADC, in turn, as a Sigma-Delta converter with a noise shaping able to increase the overall order. A trade-off between complexity, loop stability issues and performance determines the final choice of the internal ADC. It has also to be considered that the multi-bit solution is almost mandatory to get the equivalent number of bits (ENOB) required in the wireless base-band applications (Chapter 1), and that often the clock frequency is decided at the system level of the receiver more than at the base-band design one.

The actual topology of the Filtering ADC is completed designing the ADC block with a second order wide-band Sigma-Delta converter, as shown in Figure 8. A resistance (R_{NOTCH}) has been also placed in feedback between the output of the second operational amplifier and the input of the first one in order to create a notch at the corner of the signal band of interest. This does not have effect on the signal transfer function, but increases the in-band quantization noise compression. Notice that the overall Filtering ADC topology seems close to the ADC proposed in [21]. However a different signal transfer function is implemented; narrow-band, for the proposed solution, and wide-band for the latter (the R_1C_1 pole in [21] filters out the high frequency DAC current pulses, while its effect is cancelled by a zero in the signal transfer function).

Defining the input resistances of the first and of the second stage of the wide-band section R_{B2} and R_{B3}, respectively, the corresponding feedback capacitances C_{B2} and C_{B3}, and modeling the DACs as continuous time gm_{DAC2} and gm_{DAC3}, the following cut-off frequency and quality factor can be obtained:

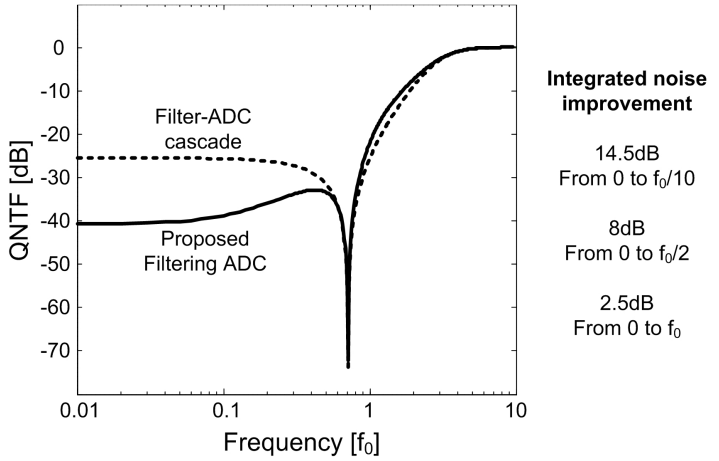


Fig. 9 QNTF of the Filtering ADC versus the QNTF of the corresponding Filter-ADC cascade proposed in section 2.2.A

$$f_{WB} = \frac{1}{2\pi}\sqrt{\frac{gm_{DAC2}}{C_{B3}R_{B3}C_{B2}}}; \qquad Q_{WB} = \sqrt{\frac{gm_{DAC2}}{R_{B3}}}\frac{1}{gm_{DAC3}}\sqrt{\frac{C_{B3}}{C_{B2}}}. \qquad (11)$$

The poles of the wide-band section are placed sufficiently far from the Filtering ADC cut-off frequency not to modify the signal transfer function. Moreover they introduce a wide-band biquad that helps avoiding residual aliasing effects. The gain $1/(gm_{DAC2}R_{B2})$ is generally chosen equal to one both to optimize the voltage swings at the output of the three operational amplifiers and not to move the low pass profile of the original Filtering ADC biquad. The main effect of the new section is that it acts strongly in the quantization noise shaping. Two zeros are in fact added at the F'(s) ((10)) quantization noise transfer function by the two new stages, and they are positioned at DC or at an in-band fixed frequency depending on the tuning of the notch. The overall quantization noise transfer function (QNTF) that can be obtained using the proposed Filtering ADC is reported in Figure 9 (solid curve). In the graph it is possible to recognize both the notch (placed at a frequency of $0.7f_0$), the high pass effect due to F'(s), which acts compressing noise below the notch frequency, and the poles of the wide-band section (when the transfer function flattens to 0dB at high frequency). They determine also the stability issues of the Filtering converter (Appendix I).

The global Filtering ADC topology, in conclusion, combines a narrow-band first stage (the original current biquad of the continuous time model) with a wide-band low pass section (the Sigma-Delta in multi-feedback configuration). The first section operates the frequency channel selectivity, while the second one shapes quantization noise.

The quantization noise performance of the Filtering ADC is now compared with the equivalent behavior of a filter-ADC cascade (Figure 7), when the ADC is implemented in an equal wide-band section fashion. The improvement depends on the choice of the f_0/f_B ratio, where f_B still defines the signal band of interest, and some examples are reported in the right side of the Figure. For a typical sizing the gain is more than one ENOB (integration bandwidth f_B from 0 to $0.8f_0$).

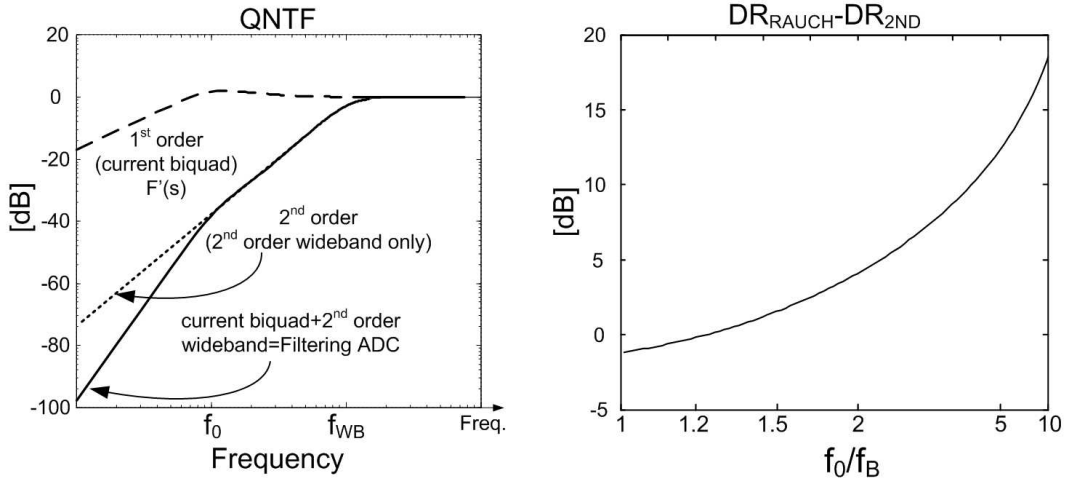


Fig. 10 Quantization noise transfer function analysis in the absence of the notch. Filtering ADC vs. filter-ADC cascaded solution in terms of dynamic range

The wide-band section can be implemented also without the notch in the quantization noise transfer function. This is reported in Figure 10, showing both the first order noise shaping of F'(s), the second order one of the filter-ADC cascade and the Filtering ADC noise transfer function. Still the advantage of the last solution is not negligible.

The quantization noise transfer function can be understood probably in a more simple fashion than the one with the notch. In band the slope is 60dB/decade, since all the stages (both narrow and wide-band) contribute to the noise compression. Above f_0 and below f_{WB} the slope is 40dB/decade accounting for the shaping effect of the second order wide-band Sigma-Delta quantizer. Far below f_0, even if not visible in the graph, the transfer function has also a 40dB/decade slope, due to the finite value of the $gm_{DAC}R_2$ gain. Figure 10 reports also the dynamic range performance difference between the filter-ADC cascaded solution and the Filtering ADC. Again the advantage depends on the choice of the f_0/f_B ratio. The slight degradation of the integrated noise when the filter bandwidth is made to coincide with the channel bandwidth is due to the chosen filter Q. Some peaking can be in fact observed in the F'(s) near the frequency f_0.

Notice that if the first stage were substituted with an active-RC integrator (as those used in the second and third stage), the multi-feedback compensation topology of a traditional third order continuous time wide-band Sigma-Delta converter would be obtained. The consequence would be of course losing the low frequency selectivity properties of the architecture. This could represent another possible way to explain the Filtering ADC genesis. First, design a wide-band traditional Sigma-Delta using the existing traditional design and synthesis tools. Second, substitute the first stage with the filtering one by the introduction of the resistances R_1 and R_2, of the big input capacitance C_1, and by resizing the feedback capacitance of the operational amplifier. This procedure was followed in the design presented in Chapter 3 for DVB-T/ATSC applications.

It is straightforward that the narrow-band Filtering introduction is paid in terms of a reduction of quantization noise shaping. In this context the Filtering ADC operates in between a second order Sigma-Delta (Figure 10) and a third order one. The amount of noise compression of a third order architecture, with respect to the Filtering ADC, and with the same high-

frequency performance (i.e. placing the poles of the wide-band section at the same frequencies in both cases, so providing equal stability margins to the modulators) is less than 1ENOB, in the presence of the notch.

2.4 A Filtering ADC evolution proposal (The E-Filtering ADC)

The Filtering ADC described so far plays the role to implement the entire base-band of a current mode receiver for wireless applications. A new version of the Filtering ADC is proposed in this section. Even if the architecture is only slightly modified with respect to the original structure, the performance benefits are not negligible in terms of SNDR and dynamic range improvement. Only the filtering stage is modified, with the constraint to maintain the same signal transfer function, while the wide-band section, and together the high-frequency behaviors of the complete modulator (i.e. stability), remain equal.

A. Filtering ADC evolution benefits and architecture

The major guidelines, in the design of a wireless receiver base-band, are the reduction of power consumption, the reduction of noise floor and the increasing of linearity. In this context the Filtering ADC evolution reported in this section is able to extend the Filtering ADC range of application to much more challenging wireless scenarios and standards than those covered by the Filtering ADC original implementation.

To extend the dynamic range, the evolution architecture is able to combine the Filtering ADC properties with three key novel elements. They are briefly addressed now, but they will be tackled in a more detailed fashion in the following subsections. First, especially when the RF interface is provided using a passive mixer (see Chapter 5), the sensitivity of the base-band transfer functions to the driving RF front-end equivalent impedance (R_S) is reduced. Second, class-B DAC architecture is introduced in order to face the DAC noise Filtering ADC issue stated in section 2.2.A (i.e. the fact that a class-A traditional DAC is noisier than a simple feedback resistance). Third, a variability of the gain, embedded in the filtering converter structure, is introduced to increase the robustness of the base-band in the presence of high power blockers (and signal power more than the sensitivity one). According to these elements, the new Filtering ADC solution embeds in a single block interferers filtering, signal digitization, and variable gain amplifier operation.

The proposed E-Filtering ADC (Evolution) basic architecture is shown in Figure 11 [22]. The finite driving impedance R_S is directly considered and the continuous time model of the internal ADC (named quantizer in the Figure) and DAC cascade is also depicted. Again I_{in} represents the down-converted input current coming from the RF front-end. The only topological difference comparing the E-Filtering and the Filtering ADC is represented by the presence of the resistance R_2, placed in feedback at the Filtering ADC operational amplifier and missing in the evolution circuit. In this sense the E-Filtering ADC takes origin from a current driven Rauch filter [23] biquad in which the feedback resistance has been replaced with the internal ADC-DAC cascade. Due to the absence of the resistance R_2, the E-Filtering ADC

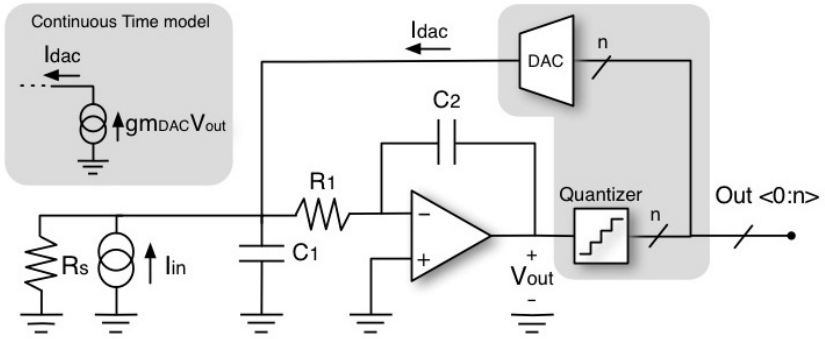


Fig. 11 Proposed Evolution-Filtering ADC (Single ended for simplicity) architecture

solution will be addressed in the following also as the not-damped architecture, while the Filtering ADC as the damped one.

As expected the E-Filtering ADC sizing is different. An area penalty is paid in general in the implementation of the capacitance C_2, which is bigger than in the damped counterpart, for the same signal transfer function.

B. Continuous time model

The continuous time model, except for the damping element, reveals nothing different if compared to the Filtering ADC case. The gm_{DAC} value still provides the in-band E-Filtering ADC input current full-scale (known the full-scale ADC reference voltage). This is truer in the evolution than in the previous architecture. The reason is that, contrary to the damped solution, in which the finite gain $gm_{DAC}R_2$ made a portion of current equal to a factor $1/(1+gm_{DAC}R_2)$ of I_{in} to flow in-band into the feed-forward low-pass filter, in the not-damped architecture very low current is absorbed by the integrator near DC, and the whole I_{in} is handled by the DAC.

The signal transfer function of the architecture, can be obtained from the equations (1-4) and (6-9) (considering or not R_S) by simply evaluating the limit for R_2 moving to infinite. The following expression gives the signal transfer function:

$$H''(s) = \frac{1}{gm_{DAC} + sC_2\left(1+\frac{R_1}{R_S}\right) + s^2 C_1 R_1 C_2} \qquad (12)$$

from which it is possible to derive:

$$G'' = \frac{1}{gm_{DAC}} \qquad (13)$$

(confirming the previous statement about the current full-scale level as provided by the DAC current only), and

$$f_0'' = \frac{1}{2\pi}\sqrt{\frac{gm_{DAC}}{C_1 R_1 C_2}} \qquad (14)$$

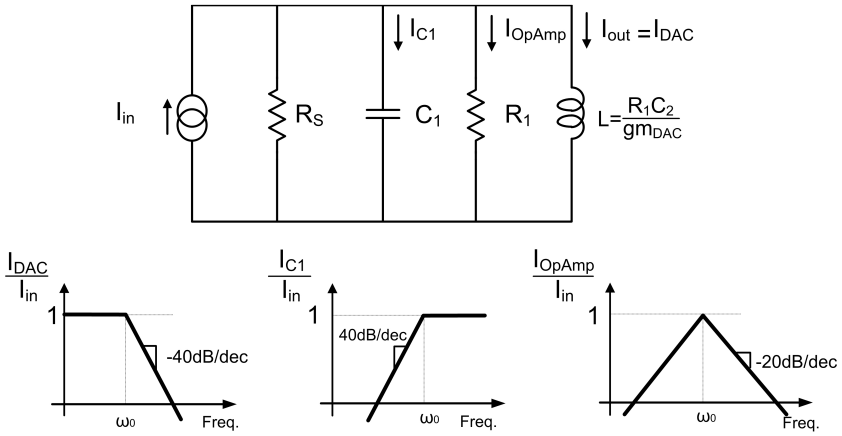


Fig. 12 The RLC E-Filtering ADC equivalent network

$$Q'' = 2\pi f_0'' \frac{C_1 R_1}{\left(1+\frac{R_1}{R_S}\right)}. \qquad (15)$$

With the same procedure the quantization noise transfer function (for the first order shaping only, without considering the wide-band section) is also evaluated:

$$F''(s) = \frac{\left(1+\frac{R_1}{R_S}+sC_1R_1\right)sC_2}{gm_{DAC}+sC_2\left(1+\frac{R_1}{R_S}\right)+s^2C_1R_1C_2}. \qquad (16)$$

A first difference in the comparison with the damped architecture is observed from (13), (14) and (15). Both the gain and the cut-off frequency now does not depend any more on the finite driving impedance R_S, and so the overall signal transfer function is less R_S-sensitive in the implementation. This is not the case of the quality factor. The main reason for these behaviors is again the infinite DC gain of the feed-forward active-RC path, and will be better defined dealing with the RLC model and input impedance of the new circuit. There is not any big difference, instead, about the quantization and the analog internal ADC noise shaping issue. Even if a zero is placed in the not-damped solution at DC, and not at a finite frequency (f_C) as for the damped one, the integrated noise amount is decided by the noise contribution near the corner of f_0, more than by the low frequency contributions. The main consequence of this is that, being f_C about one decade less than f_0 in a practical design, the two solutions have equal performance (i.e. the difference is negligible).

C. RLC model and input impedance

The RLC model of the E-Filtering ADC can be obtained moving R_2 to infinite in the Filtering ADC equivalent RLC network (Figure 3). The model is reported in Figure 12, together with the current transfer functions from the input current into the three paths (i.e. into the DAC, into the operational amplifier and into C_1). A finite resistance R_S has also been included.

The equivalent RLC network becomes a pure shunt resonating RLC, in which no more intrinsic losses are present for the inductance. The main consequence of this is that a different input impedance is displayed than in the damped solution. While out-of-band (above f_0) the

capacitance C_1 decides in both cases the input impedance, the in-band behavior of the E-Filtering ADC is dominated by the presence of the inductance, which is able to guarantee a very low near-DC input impedance level. Compared with the damped solution, this is the reason of the reduced sensitivity of the parameters of the biquad to R_S. In such a context, the results of the previous section can be intuitively seen from the RLC network. The presence of a finite R_S in fact, cannot modify either the in-band gain (current flowing into the DAC path) or the cut-off-frequency (LC shunt), but only the overall quality factor. This characteristic is especially important for a complex quadrature receiver (I and Q path), if the base-band is driven through a current-driven passive mixer interface (Chapter 5). Concerning the current transfer functions of the architecture, one element only differs from the damped Filtering ADC. The current into the operational amplifier is reduced near DC, but is greater near the corner and at high frequency, because the $R_1/(R+R_1)$ partition of the damped solution (see Figure 3), is not verified any more. This has the effect to increase the linearity requirements of the operational amplifier.

The input impedance mathematical evaluation is (starting from (5)):

$$Z_{IN}''(s) = \frac{sC_2R_1}{gm_{DAC}+sC_2+s^2C_1R_1C_2} \qquad (17)$$

D. Analog and quantization noise

The analog and digital noise properties of the E-Filtering ADC do not differ from the Filtering ADC ones. The new architecture still exploits noise shaping for both the internal ADC and the filtering stage noise sources (i.e. the operational amplifier and R_1) and maintains not changed the DAC noise transfer function, if the converter is operated in a traditional class-A mode. Nonetheless, the not-damped solution is able to achieve better noise performance than the damped counterpart, and the main difference relies on the sizing of the resistance R_1. It is possible to demonstrate that for a given cut-off frequency f_0, the same C_1, and the same in-band gain (i.e. the same gm_{DAC}, being $gm_{DAC}R_2>>1$ in the damped solution), the request of a same quality factor too requires R_1 in the damped solution to be higher than R_1 in the not-damped one (for the capacitance C_2 it is the opposite, determining the area penalty of the not-damped solution mentioned above). In the following lines, the * notation is used for the not-damped architecture. An equal $C_2R_1=C_2^*R_1^*$ product is in fact required by the f_0 constraint. The quality factor of the two solutions can be approximated, neglecting R_S, to $2\pi f_0C_2R_2$ for the original Filtering ADC, being $C_1R_1>>C_2R_2$ (vice-versa the not-damped solution would be still implemented), and $2\pi f_0C_1^*R_1^*$ for the E-Filtering ADC. It follows that $C_1^*R_1^*=C_2R_2<<C_1R_1$ and so $R_1^*<<R_1$ is obtained (and then $C_2^*>>C_2$).

In this way, the noise of the second architecture is less than the noise of the previous, being the R_1 noise source reduced (noise at the output is proportional to R_1). This is significant, especially considering that R_1 is in general a big source of noise in a design (Chapter 3 and Chapter 4).

As a less important, but however not completely negligible effect, E-Filtering ADC overall noise performance benefits directly of the absence of the resistance R_2. R_2 noise is no longer contributed.

$$\overline{V_{OUT,OA}^2} = 4kTR_{EQ}\left(\frac{1}{gm_{DAC}R_S}\right)^2 f_B + \frac{16\pi^2}{3}kTR_{EQ}(C_1+C_2)^2\left(\frac{1}{gm_{DAC}}\right)^2 f_B^3$$

$$\overline{V_{OUT,R1}^2} = 4kTR_1\left(\frac{1}{gm_{DAC}R_S}\right)^2 f_B + \frac{16\pi^2}{3}kTR_1C_1^2\left(\frac{1}{gm_{DAC}}\right)^2 f_B^3$$

With: $gm_{EQ,DAC} \cong 4\frac{v_{OUT}}{v_{OV}}gm_{DAC}$

$$\overline{V_{OUT,DAC1}^2} = 4kTgm_{EQ,DAC}\left(\frac{1}{gm_{DAC}}\right)^2 f_B$$

Fig. 13 E-Filtering ADC noise transfer functions (simplified OA expression)

Moving R_2 to infinite the noise transfer functions of the E-Filtering ADC can be evaluated starting from the formulas reported in Figure 6. The results are shown in Figure 13.

Notice that the RLC equivalent network (both damped and not-damped) is a nice tool to evaluate the signal transfer functions of the Filtering ADC (E-Filtering) architecture, and its input impedance. However it is not possible to use it for the noise analysis, since the ground connection of R_1 in the model does not respect the effective virtual ground connection of the circuit.

E. Class-B DAC introduction

The design of an extremely high SNDR and DR base-band requires an accurate work of reduction of all the possible noise sources, both dominant but also non-dominant ones, to achieve the best possible noise figure performance if the block is used in a complete receiver chain (or the lowest absolute noise value if the block is assumed as a stand-alone one).

In the Filtering ADC case, the DAC noise can be considered a non dominant source of noise, since in a typical design the requirement of low input impedance (big C_1) makes the resistance R_1 the first noise contributor, while the low power requirement makes the operational amplifier the second contributor. In section 2.2.A the fact that the main feedback DAC path could introduce more noise than a simple resistance, if the DAC worked in class-A, was introduced. In this subsection how to minimize the DAC noise well below the resistive limit (took as a comparison) is shown. Of course the proposal of a new DAC topology applies to both the damped or not-damped solution. Since it is shown that the not-damped solution has much better overall dynamic range performance, the class-B DAC is now presented as a peculiar characteristic of the E-Filtering ADC only.

In a traditional class-A DAC approach, the DAC noise depends on the DAC full-scale current, which is in turn given by the level of the interferers that have to be handled, as input scenario, by the base-band. This situation is not modified even in the absence of the blockers (e.g. sensitivity test), when the amount of the full-scale current is used only in a very limited percentage, to handle the input signals. The class-B DAC manages in breaking the dependence of the injected noise on the full-scale current in the no-interferer condition.

The first step considers the noise injected by the feedback resistance R_{fb} at the input of the Rauch filter. A current noise spectral density, independent on the signal amplitude, of value

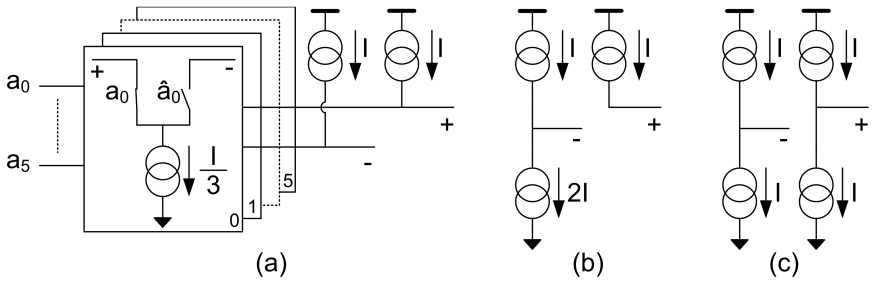


Fig. 14 Classical DAC architecture, class-A

$$i^2_{noise,Rfb} = \frac{4kT}{R_{fb}} \qquad (18)$$

is inserted. A DAC, replacing the feedback path resistor, injects in the simplest non-return to zero implementation rectangular pulses of current according to the control word of the quantizer (internal ADC). If a current steering DAC implementation is provided, each cell injects a noise of value:

$$i^2_{noise,cell} = 4kTgm_{DAC}\left(2\gamma\frac{V_{LSB}}{V_{OV}}\right) = \frac{4kT}{R_{fb}}\left(2\gamma\frac{V_{LSB}}{V_{OV}}\right) \qquad (19)$$

in whichV_{OV} is the overdrive of the transistor (PMOS or NMOS) that implements the current generator, while V_{LSB} is the voltage that at the internal ADC output corresponds to a Least Significant Bit (LSB). The equivalence can be obtained under the assumption to have the same signal transfer function for the Rauch implementation and the E-Filtering ADC one (i.e. $gm_{DAC}=1/R_{fb}$). If a 4bit DAC is considered, and assuming typical values of V_{OV}, the ratio $i^2_{noise,Rfb}/i^2_{noise,cell}$ is expected to be between 4dB and 10dB. The consequence of this is that the noise of the DAC can be smaller or larger than that of R_{fb}, depending on the number of cells which are in on-state each instant of time, therefore contributing noise. The crucial point is if the noise of the DAC has a dependence or not on the output code, and if it is possible to minimize it when large blockers are not present during the reception (so at sensitivity). In the following, the two DAC topologies shown in Figure 14.a and 15.a will be compared. For simplicity a 6 level thermometric architecture has been chosen. In both cases the seven possible outputs go from +I (single ended) to –I with a minimum step of I/3.

The DAC of Figure 14.a, depicted in a fully differential implementation, works in class-A [24]. Each output signal is the difference between the fixed current drained from the positive voltage supply (i.e. I, equal to the DAC current full scale) and that of the 6 current generators, injected into the negative voltage supply. These current sources can be switched to the positive or to the negative output according to the thermometric control word (ranging from 000000 to 111111). Each DAC cell is driven by one thermometric bit.

When the DAC input code is $a_0…a_5$=111111, the positive full-scale output current (+I, -I) is obtained at the DAC output (Figure 14.b). When instead the DAC input code is $a_0…a_5$=000000, the negative full-scale output current (-I, +I) is provided. The sensitivity condition can be considered the case in which the DAC input code is $a_0…a_5$=000111, and a zero output current is

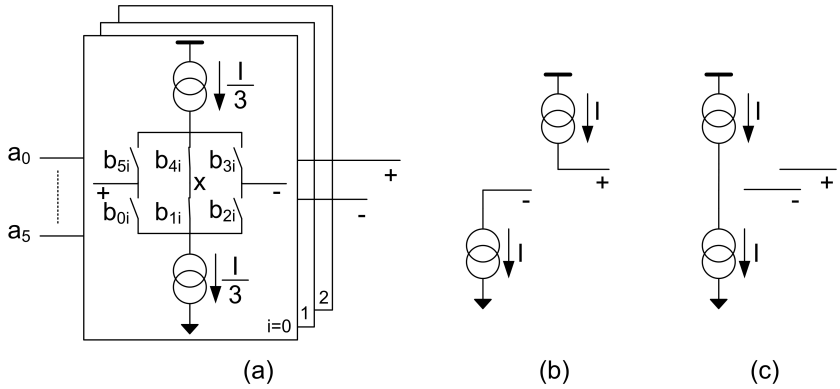


Fig. 15 Class-B DAC architecture

a0=0,1,1,1,1,1,1	b00=1,1,1,0,0,0,0	b01=1,1,0,0,0,0,0	b02=1,0,0,0,0,0,0
a1=0,0,1,1,1,1,1	b10=0,0,0,1,0,0,0	b11=0,0,1,1,1,0,0	b12=0,1,1,1,1,1,0
a2=0,0,0,1,1,1,1	b20=0,0,0,0,1,1,1	b21=0,0,0,0,0,1,1	b22=0,0,0,0,0,0,1
a3=0,0,0,0,1,1,1	b30=1,1,1,0,0,0,0	b31=1,1,0,0,0,0,0	b32=1,0,0,0,0,0,0
a4=0,0,0,0,0,1,1	b40=0,0,0,1,0,0,0	b41=0,0,1,1,1,0,0	b42=0,1,1,1,1,1,0
a5=0,0,0,0,0,0,1	b50=0,0,0,0,1,1,1	b51=0,0,0,0,0,1,1	b52=0,0,0,0,0,0,1

Fig. 16 Driving logic of the class-B architecture. From $a_0 \ldots a_5$ to $b_0 \ldots b_5$

provided (0, 0) (Figure 14.c). The very weak base-band input signal in fact (with its added noise) drives for a large percentage of time only the middle code. In the class-A DAC implementation, the noise of all the current sources (cells) is injected at the output not depending on the DAC input code (even if there is dependence in the positive/negative output node noise distribution). As seen, at any time all the current sources are connected to either the positive or the negative output node.

The DAC of Figure 15.a, depicted in a fully differential implementation, works in class-B [25]. It is a push-pull structure able to inject or absorb current without any fixed bias connected directly from the voltage supply and the output. The proposed class-B architecture makes use of a three way current switching cell [26], paying some penalty in terms of a higher number of switches and an additional driving logic step. However, the controls $b_0 \ldots b_5$ of each elementary cell, can be obtained from $a_0 \ldots a_5$ using a simple logic (Figure 16).

In the elementary cell four switches are used to send the current taken from the negative and positive rail to the negative or positive output node (or vice-versa). The two central switches, that realize the connection to the fixed node X, have the aim to switch off the cell, from the DAC functional point of view, but to maintain in on-state the current sources.

In this way each cell can be also put in a rest condition, and is not used to generate output signal when a large output signal is not required. For I/3 signal level, only one cell operates in on-state. The 2I/3 signal is generated using two cells in parallel, while only the full-scale current signal makes use of all the three cells in on-state. Figure 15.b and Figure 15.c report the positive full scale current (+I, -I) working condition and the zero current level (0, 0), respectively. In this latter case no cells are connected to the output, and no noise can be added.

Analyzing the noise dependence on the DAC code, in the context of the E-Filtering ADC modulator, it is possible to observe that the DAC introduces its maximum noise when large signals (or blockers) are present, and the entire feedback path is active. In this situation also

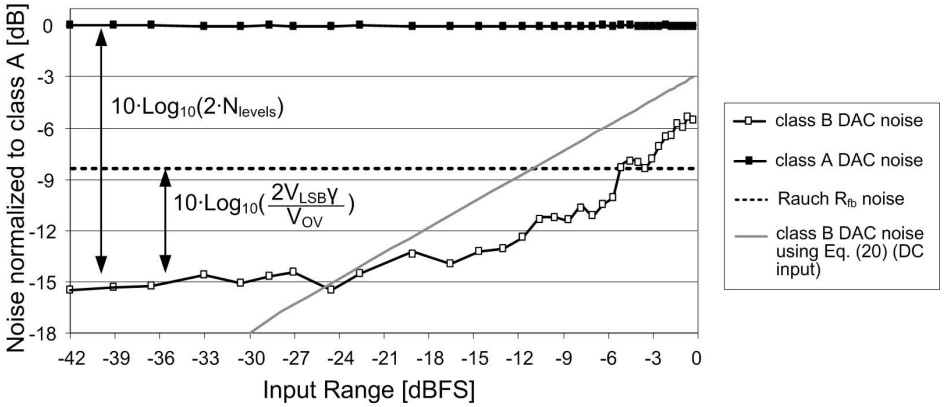


Fig. 17 Simulated (Matlab) and calculated DAC noise in a continuous time Sigma-Delta converter (E-Filtering ADC included) and R_{fb} noise into the equivalent Rauch biquad

noise requirements are expected to be less critical. When the input signal decreases, and less feedback path current is used, a smaller number of cells operates adding noise. The limit is the sensitivity test-case, in which almost zero noise can be injected by the DAC. This behavior is quantitatively described by the following equation, providing the noise injected by a class-B DAC, when used in the E-Filtering-ADC (but more in general in a continuous time Sigma-Delta), at each clock cycle:

$$i^2_{noise,BDAC} = 4kTgm_{DAC}\left(2\gamma\frac{V_{QUANT}}{V_{OV}}\right). \qquad (20)$$

V_{QUANT} is the voltage at the input of the quantizer. Notice that if a DC signal is present at the input of the modulator (20) gives also the Sigma-Delta rms input noise. The noise in the presence of a sinusoidal input tone has been evaluated through Matlab simulations for both a class-A and a class-B DAC. In this case a 13 levels quantizer has been chosen, and the noise, normalized to that of the class-A solution, is plotted in Figure 17 versus the input amplitude. For comparison the figure reports also (20).

The class-B DAC solution has always an advantage in comparison to the class-A one. The difference is about 14.5dB at low signal amplitude and about 6dB at the full-scale input. For the choice of the 13 levels code, it has been assumed that the LSB cell is never switched off, and this gives the low signal noise plateau of the class-B DAC noise. For inputs larger than a few LSBs, (20) overestimates the simulated noise of the class-B DAC by an amount equal to the peak to average ratio (PAR) of the input signal (3dB in a sinusoidal tone). The useful consequence is that the advantage of using a class-B DAC in an E-Filtering ADC could be in theory even bigger than the simulated, in the case of input signals with high PAR (like those used for high spectral efficient modulators). The last curve reported in Figure 17 is the noise of the equivalent Rauch resistance R_{fb}, when the ratio $i^2_{noise,Rfb}/i^2_{noise,cell}$ is chosen to be 6.5dB (V_{OV}=235mV, V_{LSB}=38mV).

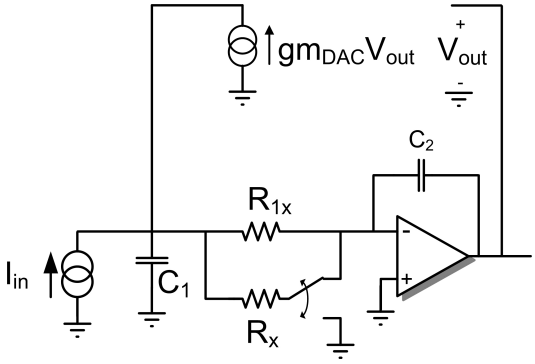


Fig. 18 Variable gain E-Filtering ADC architecture. The continuous time model is shown for simplicity

F. Variable gain function

Some receiver standards are so critical to be handled that neither the intrinsic filtering, and noise shaping, of the Filtering ADC family, nor the use of a class-B DAC are still enough to get sufficient SNDR and DR profile to match the specifications. This is in particular true if also the required receiver robustness to the fading and to the signal PAR is taken into consideration. In such a critical environment the dynamic range of the E-Filtering ADC based base-band can be further increased implementing some variable gain amplifier (VGA) control.

The E-Filtering ADC is able to embed in its structure some VGA action too (this would be more complicated in the damped structure). In this situation the absolute value of noise is no more the first concern, since larger signals than sensitivity are expected at the input. However the base-band transfer function is expected to be modified into the low-gain mode (increasing the current full scale) without changing f_0 and Q, and providing to the front-end the same input impedance as for the high-gain case. This in fact is required to ensure good linearity performance for both the feedback DAC and the mixer.

The simplest way to do this would be increasing gm_{DAC} and C_2 of the same amount. However the latter operation would increase also the parasitic capacitance of C_2 to ground. This element, together with the C_2 increase itself, can be critical in a low power design, as will be seen also for the operational amplifier explained in Chapter 4.

The variable gain is here implemented modifying not only the feedback capacitance C_2 and the full-scale current level (gm_{DAC}), but also adding in the circuit the resistance R_X, as shown in Figure 18. In high-gain mode R_X is put in parallel to R_{1X}, to give the original R_1 value. When low-gain is performed R_X is switched to ground (the common DC mode in the fully differential implementation). Two are the benefits of this strategy. First, this changes the equivalent bandwidth of the active-RC integrator without increasing the input impedance of the block, since the parallel of R_{1X} and R_X is still seen at the input node (this would be true also for the simplest way described before). Second, this gives the possibility to reduce the base-band gain limiting the increase in the C_2 value, with respect to the simplest approach, due to the current partition at the integrator input.

2.5 Filtering ADC versus E-Filtering ADC

Both the Filtering ADC and its evolution proposal, the E-Filtering ADC, can well implement the entire analog to digital base-band section of a receiver. They have been presented in this chapter like a first solution and its evolution one, because in general the not damped architecture can reach higher performance than the damped version. However, different specifications could lead to use one or the other architecture, to optimize the base-band design.

In the following, the main points of difference between the two circuits are reported and briefly compared, to provide immediate guidelines for the design.

- The topology of the E-Filtering ADC is obtained from the topology of the Filtering ADC removing the resistance R_2 from the operational amplifier feedback.

- In the original damped architecture the time constant C_1R_1 is the dominant one, while C_2R_2 falls not far from f_0. In the not-damped solution C_2R_2 is placed at DC while C_1R_1 approaches f_0. The loop gain $gm_{DAC}R_2$ (finite and infinite value respectively) makes the two architectures provide the same signal transfer function.

- The E-Filtering ADC, for the same signal transfer function, is less sensitive to the driving impedance R_S, since only the quality factor of the converter depends on R_S and neither f_0 nor the in-band gain.

- The in-band input impedance of the E-Filtering ADC is less than in the counterpart, due to a pure inductance synthesized near-DC. This is also the reason of the aspects explained in the previous point.

- The Filtering ADC occupies less area than the evolution one. To get the same sizing, C_2 in the damped case is smaller than C_2 in the not-damped one. Notice that in general C_1 is expected to dominate the overall area, so the penalty could be limited depending on the application.

- The E-Filtering ADC is less noisy than the counterpart. To get the same sizing R_1 in the damped case is bigger than R_1 in the not-damped one. Notice that in general R_1 is expected to dominate the overall noise, so the advantage could be significant.

- The current that flows into the operational amplifier is bigger in the E-Filtering ADC because of the smaller R_1 for the same input node swing. This can bring to better linearity performance of the damped solution, for the same power consumption. Observe that this element and the previous one respect a global linearity-noise trade-off.

Chapter 3

The Filtering ADC based DTT base-band

In this chapter the Filtering ADC structure is exploited as the entire analog base-band of a Marvell Digital Terrestrial Television (DTT) tuner (3.1). The Filtering ADC makes the receiver compliant to the critical ATSC American standard (3.2-3.3). Simulation and measurement results of the integrated 80nm prototype are reported (3.4-3.6). Finally the comparison with the state of the art of other possible base-band solutions is provided (3.7).

3.1 The tuner overall architecture: LNA and mixer

The Filtering ADC proposed in Chapter 2, in its damped original version, was integrated and tested as the complete analog base-band of a Marvell Digital Terrestrial Television tuner [27]. The introduction of the Filtering ADC in an existing receiver chain tailored for DVB-T led to a dual DVB-T/ATSC compatible full integrated silicon tuner. The Filtering ADC replaced an existing wide-band traditional continuous time Sigma-Delta converter, providing the possibility to exploit its intrinsic high dynamic range potentiality and blocker resilient operation.

The tuner and the front-end architecture are briefly described in the following, in order to give the main context in which the Filtering ADC design took place. Then the base-band is addressed in detail.

The TV receiver requires only one single ended RF input for the entire 40MHz-1GHz band, has no external SAW filter or balun, and supports in the back-end channels from 5MHz to 8MHz. A low-IF architecture is implemented, able to handle the RF input scenario thanks to a low-noise programmable RF filter, an harmonic rejection mixer and the Filtering ADC. Figure 1 reports the TV tuner silicon chip, while Figure 2 shows the receiver scheme.

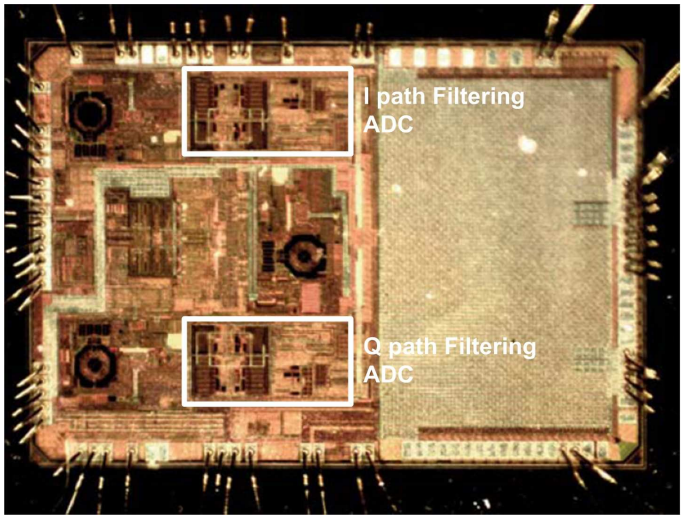


Fig. 1 The full silicon 80nm Marvell DTT tuner picture (the I and Q Filtering ADCs have been highlighted

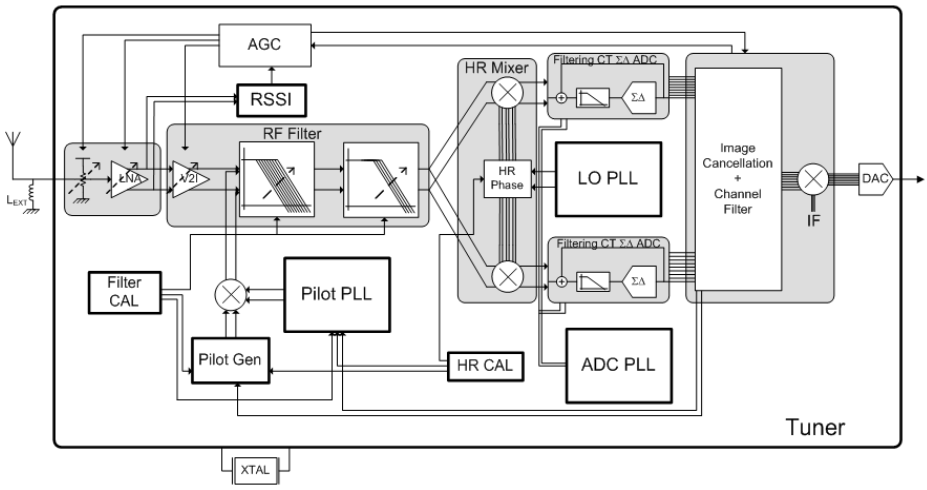


Fig. 2 The full silicon 80nm Marvell DTT tuner scheme

The tuner front-end is matched to 75Ω input impedance. The LNA is the classic common gate-common source noise canceling topology [28] with an embedded programmable attenuation. The broadband receiver target makes the harmonic mixing issue to be critical. This problem is solved combining the harmonic rejection active mixer, whose architecture is the traditional Gilbert one, with a tunable RF current filtering implementing a 4^{th} order Butterworth. The filter operates in the current domain, thus allowing for low noise and high linearity performance. The output of the mixer (after the recombination of the harmonic rejection paths) is a current signal. This signal is the differential input of the Filtering ADC.

Due to the active mixer implementation, as will be seen in Chapter 5, the mixer can be modeled as a couple of resistances going from the input nodes to the DC common mode of the base-band. They correspond to the single ended R_S considered in Chapter 2. The value of R_S was evaluated through Spectre PSS-PAC simulations.

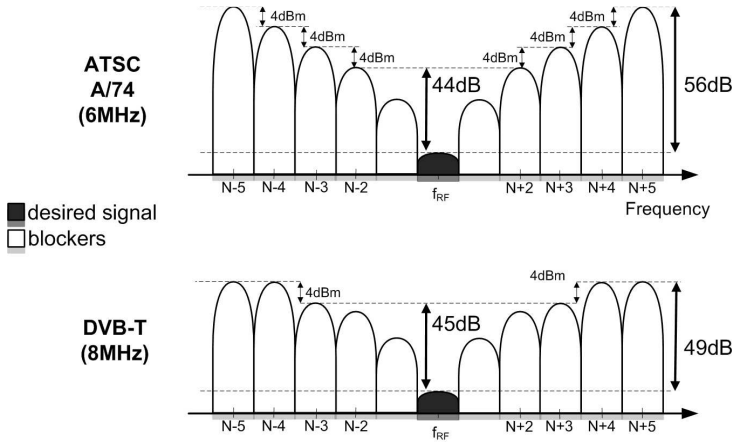


Fig. 3 RF frequency interferer profile for both the ATSC-A/74 and the DVB-T standard

3.2 The DVB-T and the ATSC-A/74 standards

In the field of Digital Terrestrial Television, DVB-T stands for Digital Video Broadcasting-Terrestrial, and corresponds to the standard of the DVB European consortium for the transmission of the digital television signal through the terrestrial mean, via air interface (there is also DVB-C for via cable transmission, DVB-S for satellite one, and DVB-H for the transmission of the television signal to the phone mobiles).

ATSC Standard stands for Advanced Television Systems Committee Standard, and corresponds to a set of standards developed by the ATSC consortium for the transmission of the digital television signal mainly in North America.

A tuner able to handle in a single silicon chip both of them has the big advantage to cover and face a worldwide market.

What is really of interest, from the RF front-end and the base-band designers point of view, are not directly the digital communication characteristics of the received signal provided by the standard (i.e. the modulation type, the guard interval, the bit-rate and the bit-error-rate, the spectral efficiency, the channel distribution), but more circuit oriented specifications. Among this information set it is important to know the desired signal bandwidth (both RF bands and base-band channel bandwidth), the peak to average ratio (PAR) of the modulated signal, the SNR required at the input of the demodulator and the consequent receiver noise figure, the received channels profile, including the corresponding power of both the useful signal and the blockers, and the non linearity and selectivity tests. This in turn translates, from the base-band point of view, into the dynamic range (or signal to noise and distortion ratio) specification, expressed versus frequency as explained in Chapter 1.

The RF front-end is rather broad-band. In this sense the relative profile of the in-band and out-of band channels that reaches the antenna is not modified through the chain, especially considering the adjacent channels interferers. The RF tunable filter in fact is able to filter out the far out-of-band interferers, which could be problematic for harmonic down-conversion, but not the near out-of-band ones.

The interferer input profiles (at RF) of the ATSC-A/74 and of the DVB-T standards are reported in Figure 3. The desired channel is centered at the f_{RF} frequency, while the adjacent

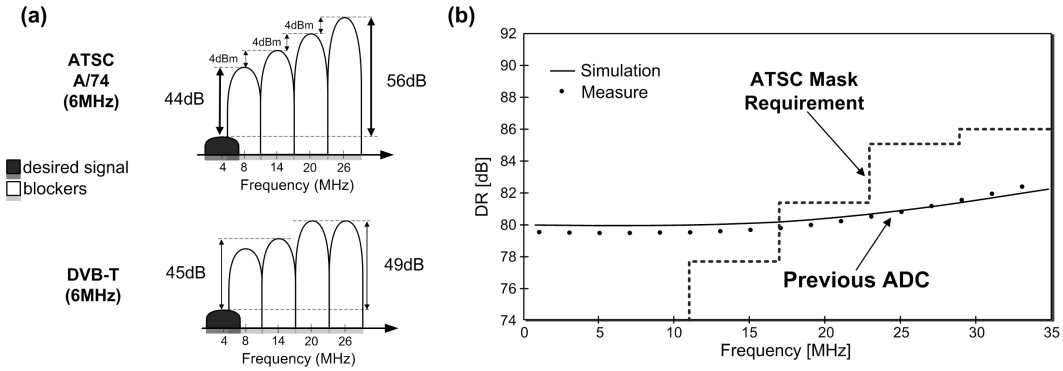


Fig. 4 (a) IF frequency interferer profile for both the ATSC-A/74 and the DVB-T standard (b) Evaluated ATSC-A/74 dynamic range profile requirement

channel power is provided in difference with the useful channel one [29-30]. The ATSC-A/74 operates only with 6MHz channel bandwidth. The DVB-T has 5MHz to 8MHz channel bandwidth, depending on the RF frequency and on the country of the broadcasting. The 8MHz channel bandwidth reported in the Figure is the most common.

The low-IF front-end down-converts at base-band the input spectrum, aligning to 1MHz the frequency of the left channel edge of the desired signal. In this way, the N-X (with X=1…5) channels are partly folded in-band, representing the signal and interferer image. To give an example, the N-2 adjacent channel, placed at an RF offset going from -6MHz to -12MHz from f_{RF}, is folded from 4MHz to 10MHz. Image rejection, operated through the recombination of the I and Q paths, is able to distinguish the desired channel from the interferer folded channel image. However, this un-wanted signal has still to be handled by the base-band, and is critical since it requires a high dynamic range at a very short distance in frequency from the signal useful band.

The critical spectrum that the base-band is required to accept at its input, after image folding, is shown in Figure 4.a for both the standards. The DVB-T specifications are reported for 6MHz channel bandwidth to simplify the comparison. Notice that ATSC-A/74 requirements are more demanding (up to 7dB higher dynamic range is required at channels N±5) than the DVB-T one. For this reason, in the following, only ATSC case is addressed in detail.

From the ATSC spectrum reported in Figure 4.a, the base-band DR profile requirement can be obtained (Figure 4.b). First, knowing the front-end gain, i.e. the gain preceding the base-band section, the current level of the interferers reaching the base-band input can be evaluated. Second, the absolute noise level that the base-band has to satisfy, in order to make the receiver respect the noise figure specification, is decided by system level simulations.

The designed Filtering ADC had to respect such a demanding request with margin, in order to ensure a robust DTT compatibility. It has been told that the Filtering ADC substituted an existing wide-band traditional continuous time Sigma Delta converter. The DR profile provided by this old base-band is shown in Figure 4.b too. The old wide-band ADC design failed in handling the ATSC-A/74 standard (not the DVB-T).

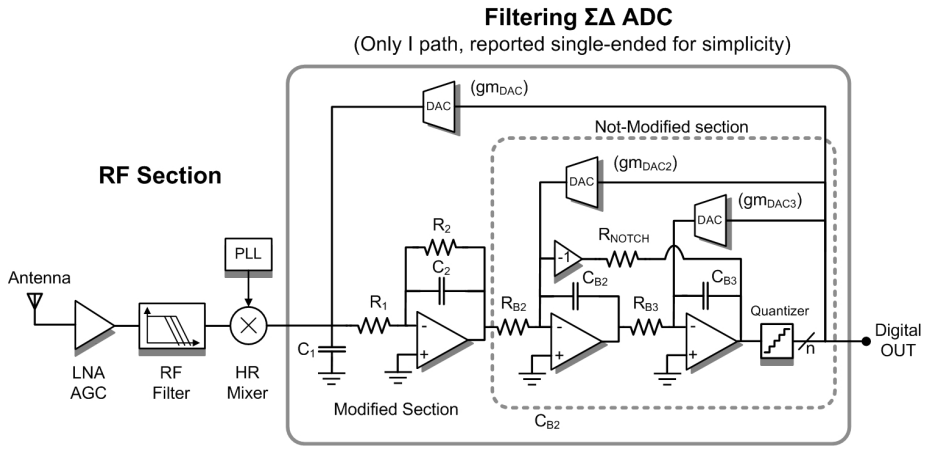


Fig. 5 The Filtering ADC in the simplified TV Tuner block diagram

3.3 The DTT Filtering ADC design

The Filtering ADC complete scheme, depicted in a simplified building blocks representation of the whole tuner, is reported in Figure 5, providing also the names of the components of the architecture. The Figure highlights the section of the base-band existing modulator that was maintained without changes with respect to the previous version and the Filtering ADC core introduction. Except for the value of the resistance R_{NOTCH}, which was slightly modified to optimize quantization noise performance, the wide-band section of the modulator (i.e. the 2nd order wide-band Sigma-Delta quantizer) was not replaced. The first active-RC original integrator was instead changed into the filtering structure of the proposed narrow-band ADC.

The operational amplifiers were maintained from the original DVB-T project. The filtering behavior of the new section was in fact expected not to degrade (but instead to increase) the overall linearity performance. The operational amplifiers are designed in a feed-forward/Miller (four stages) compensation topology, as that reported in [31]. About 1GHz f_T (i.e. the 0dB gain frequency of the loop composed by the operational amplifier with its feedback network) is provided, with a 40dB/decade in-band gain slope ($f<f_T$), and 60dB gain value is realized at 10MHz frequency. The current consumption of the first operational amplifier is 8mA. The input noise is that of an equivalent 1.5kΩ resistance placed in series to the input nodes (R_{EQ} used in Chapter 2, section 2.2). The current consumption of both the second and the third operational amplifier is 6mA.

The DAC2 and the DAC3 were also maintained the same as for the old wide-band design. The first DAC was modified, increasing of the 25% its current full-scale in order to ensure bigger robustness to blockers in the first silicon prototype. In the industrial final one the original current value of the DAC is used, since the margin of the prototype versus the specifications was oversized also in the worst case testing conditions [27]. The architecture of the DAC is a traditional class-A one [25], in which cascoded PMOS current sources act as the fixed full-scale current generator (Chapter 2, section 2.4.E) while cascoded NMOS ones switch on or off depending on the thermometric feedback code.

Clock frequency	Signal BW	Scaling Factor
337.5MHz	5MHz	0.625
405MHz (ATSC)	**6MHz**	**0.75**
472.5MHz	7MHz	0.875
540MHz (DVB-T)	**8MHz**	**1**

Fig. 6 Clock Frequencies, channel bandwidths and scaling factors

The quantizer is a full flash architecture. It uses switched-capacitors comparators, and generates a 14 levels thermometric digital code. The feedback path is completed with a DWA (Data Weighted Averaging) cell, to ensure sufficient linearity to the DACs. Process mismatches in fact, which makes the unitary DAC cells different one to the other, could deteriorate the linearity of the feedback, thus directly reducing the ENOB of the entire converter. This is avoided using the cell randomizer [32].

The existing Sigma-Delta embedded also a calibration machine, in order to calibrate the time constants of the modulator to avoid process spreads moving the ADC towards instability. The calibration was extended to the Filtering ADC implementation. The calibration acts as follows. The process spread of resistances is firstly sensed. Then a capacitance C (nominal ±25%) is tuned in order to regulate an RC time constant to a precise clock frequency, used as timing reference. Finally the digital code, used for the tuning of C, controls all the capacitances in the Sigma-Delta.

The DVB-T tailored base-band was able to cover, due to two control bits, channel bandwidths from 5MHz to 8MHz (5,6,7,8). The corresponding reconfigurability was reproduced also in the Filtering ADC. The clock frequencies are shown in Figure 6, together with the frequency scaling factors applied to the RC time constants. All the poles of the converter have in fact to be moved with the clock frequency to maintain equal margin from the instability. The time constants are tuned acting on the resistances values.

A low-jitter PLL was also re-used from the DVB-T project to get the ADC clock frequency, thus avoiding jitter noise issues in the modulator (Appendix II). The entire internal generation of the clock phases (to drive the comparators and the DACs) was not modified too.

The base-band analog supply is 1.8V, while the digital section uses a 1.2V supply.

A. The Filtering ADC sizing guidelines

Even if the Filtering ADC was designed in a fully differential topology, in the following the single ended reference values used in Chapter 2 are used. The wide-band section guidelines are now presented in a brief summary. The equations (11) proposed in the continuous time study of Chapter 2 were first used. Then, the discrete time models of the Filtering continuous time Sigma Delta ADC (Appendix I) were exploited to confirm the effective transfer function of the converter:

1. $gm_{DAC2}=gm_{DAC3}$, $R_{B2}=R_{B3}$ in order to control the Q of the wide-band biquad using only the capacitances ratio (C_{B3}/C_{B2}) and to fix equal the in band dynamic of the voltage nodes of the structure (i.e. the output of the three operational amplifiers). The gain of the wide-band section is constrained to be 0dB, so $gm_{DAC2}=1/R_{B2}$. The wide-band cut-off frequency f_{WB} sets the value of $C_{B2}C_{B3}$. f_{WB} is chosen, for a given clock frequency, as the maximum one that guarantees the stability of the ADC for a total loop delay of 1 clock

cycle T_S ($T_S/2$ for the comparators and the digital DWA logic, plus $T_S/2$ extra-loop-delay margin). The biquad is designed as a Butterworth to increase the margin against instability (a higher Q would give a smaller margin). The discrete time equivalent models (Appendix I) have to be strongly employed at this level to verify the modulator performance.

2. In order to satisfy noise and power constraints, the impedances of the wide-band section are scaled with respect to the first stage ones. The chosen impedance values are sized to limit the DACs power consumption and capacitances area (C_{B2} and C_{B3}), while providing at the same time an acceptable noise level.
3. The resonator resistance R_{NOTCH} is used to tune the notch of the quantization noise shaping, when the other wide-band parameters are fixed. There is a single notch frequency that minimizes the in-band quantization noise amount (optimum), but it has to be taken into account that process variation could move the notch also outside the signal band, thus drastically reducing performance, if some safety margin is not allocated.

The sizing of the Filtering ADC narrow-band section is based on the equations (5) and (6-9) given in Chapter 2. A value of R_S equal to 2.5kΩ was estimated to model the mixer driving, and has to be taken into account. Useful guidelines are provided as follows.

1. The four design constraints of the Filtering ADC are the cut-off frequency, the quality factor, the high frequency input impedance and the in-band gain. There is then a fifth relationship between the DAC current full scale (i.e. gm_{DAC}) and the feedback damping resistor R_2. Realizing an effective noise-shaping for the narrow-band section too, applies in fact for the product $gm_{DAC}R_2$ to be sufficiently bigger than one.
2. The value of C_1 is given by the input impedance/noise performance trade-off (Chapter 2). The lower limit for C_1 is given by the input impedance constraint, since a low voltage swing has to be designed at the input of the Filtering ADC to achieve good linearity results for both the mixer and the main feedback DAC. The upper limit for C_1 is selected by the noise budget, being R_1 and the operational amplifier the dominant noise sources of the architecture. Increasing C_1 (reducing R_1) would increase the noise amount of the structure (see Figure 6, Chapter 2) if the high pass section of the transfer function dominates the noise, as it is the case for such a high expected R_S.
3. The value of gm_{DAC} is defined by the transimpedance gain of the ADC. It is given by the analysis of the current input scenario that the converter must be able to handle since it is directly linked to the DAC current full-scale.
4. The values of R_2, R_1 and C_2 are given in consequence by the desired cut-off frequency and quality factor.

The cut-off frequency is chosen according to the noise/selectivity trade-off described in Chapter 2. Increasing it would reduce the base-band noise, however limiting the handling of the out-of-band blockers. The cut-off frequency is so pushed to the highest possible frequency, still maintaining some dB of margin for the interferers dynamic.

The in-band flatness of the base-band signal transfer function, which is related to the Q value, represents another constraint in the DTT application. According to this element, remember that it is possible to demonstrate that in a damped design the approximation $R_1C_1 >> R_2C_2$ is valid, and this simplifies the Q expression. The dominant pole of the open loop

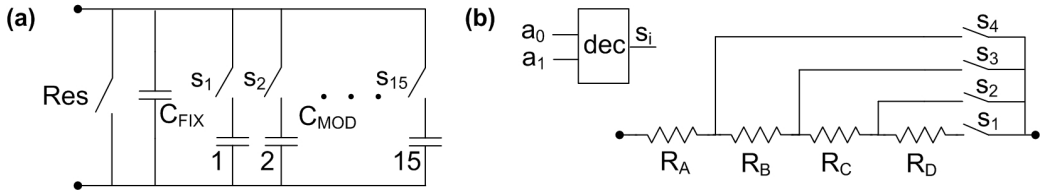


Fig. 7 (a) Capacitance unit to be calibrated against process resistance variation (b) Resistance unit to be reconfigured over different signal bandwidth

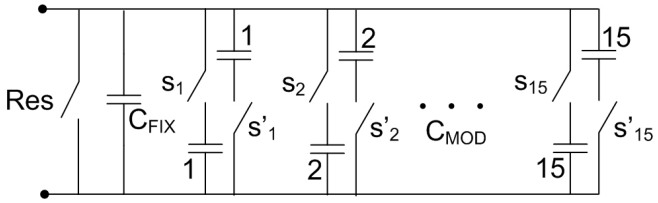


Fig. 8 Input differential capacitance implementation

biquad (i.e. the low pass current R_1C_1 filter plus the active-RC R_2C_2 stage), in fact, is given by the R_1C_1 time constant and is moved by the loop gain ($gm_{DAC}R_2$) to the cut-off frequency of the converter. The secondary pole of the loop (R_2C_2) is placed after the cut-off frequency and is used to control the quality factor of the biquad.

Dealing now directly with the integrated design, the cut-off frequency f_0' ((8), Chapter 2) was positioned at a factor 2 than the desired signal frequency edge (18-16-14-12MHz for 8-7-6-5MHz signal bandwidths). A 0.55 nominal value for the continuous time narrow-band section Q' was used ((9), Chapter 2). This optimized the in-band signal transfer function flatness, according to the discrete time architecture modeling. Be aware that sampling and loop delay tend to increase the quality factor value of synthesized complex conjugate poles. Moreover, the presence of a wide-band biquad not so far in frequency from the narrow-band one modifies the signal transfer function of the latter, at least near and above the f_0' frequency, still increasing the effective quality factor in comparison to the nominal Q'. In this sense f_{WB}, Q_{WB}, f_0' and Q' can be considered only as nominal reference values. The wide-band section cut-off frequency f_{WB} ((11), Chapter 2) was placed at a factor 5 than the desired signal frequency edge. A 0.7 value for the Q_{WB} ((11), Chapter 2) was used to optimize the stability properties of the converter against extra-loop delay.

B. Calibration and reconfigurability implementation

A thermometric control word can be active in the design to tune the capacitances values, in the entire modulator, according to a calibration machine output. This has the aim to counter-balance the process spreads of the resistances. By looking at the physical implementation, calibration was embedded by separating the overall capacitance into a constant module C_{FIX} and a tunable one C_{MOD}, being the latter controlled by the calibration bits. The 15 levels thermometric digital code translates directly into 15 unitary modules, as shown in Figure 7.a. The $s_1 \ldots s_{15}$=000000001111111 code sets the nominal case (7 modules connected), providing about +30% and -26% control of the RC time constants, into 15 discrete steps (i.e. about 3.5% precision of the calibrated RC time constants). The switch named Res in the Figure was also added to be able to completely discharge the capacitance in a reset operating mode. The

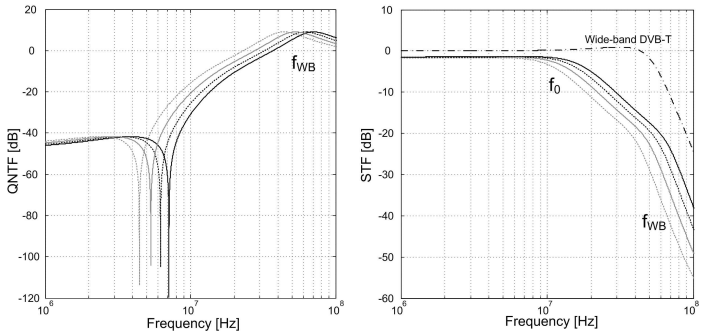


Fig. 9 Reconfigurable Filtering ADC simulated quantization and signal transfer function

switches were implemented with minimum channel length to reduce the on-state resistance, in a complementary PMOS-NMOS realization.

Impedance scaling for frequency reconfigurability was instead implemented modifying the value of the resistances, as depicted in Figure 7.b. Two bits (a_0 and a_1) work as control word. A simple digital logic is able to provide the $s_1 \ldots s_4$ bits that drive the switches. A complementary implementation of the switches was used also in this case. A single resistor strip was given, and the output node can be changed operating on the switches (only one is in on-state at any time). A resistor module equal to the module used in the calibration unit was chosen, while giving at the same time the possibility to obtain the desired resistances with a limited number of cells.

C. Input capacitance (C_1) implementation

The calibration algorithm applies also to the input capacitance C_1. Now, two are the elements that have to be taken into consideration. First, the input capacitance was splitted into a differential capacitance and a single-ended one, to provide some low input common-mode high frequency impedance, while still keeping reduced as better as possible the silicon area. While the first module is connected from the positive to the negative input node, the latter is realized using two elements connected from the positive and the negative input nodes to ground. Second, the calibration implementation, embedded entirely into the differential capacitance since the value of the ground connected modules is smaller than the differential one, had not to un-balance the differential operation of the circuit. Due to these reasons, the differential part of the passive element was implemented as shown in Figure 8. With respect to the other capacitances of the converter, any discrete module of C_{MOD} was in turn divided into two sections, in order to put the doubled calibration switches at the left and right side of the passive, at the same moment. This ensured perfect differential operation, and allowed for a fully differential high matched layout.

The fixed single-ended modules were chosen to allocate about the 5% of the total capacitance C_1. Layout extraction tools were intensively used to get the correct value of the capacitance, taking into account also the parasitic capacitance to ground of the differential section. M1-M5 MOM capacitances were in fact used for a high density implementation, thus not minimizing the parasitic effect.

(a)

Source	%	Noise [V^2]
1st op-amp	23.2%	2.44n
R_1	17.3%	1.82n
DAC_2	12.4%	1.31n
R_2	7.8%	0.82n
DAC_1	5.4%	0.57n
2nd op-amp	4.4%	0.46n
Quantization	26.6%	2.8n
Total		**10.5n**

(b)

Source	%	Noise [V^2]
1st op-amp	19.8%	2.12n
R_1	17.2%	1.84n
DAC_2	14.4%	1.54n
DAC_1	6%	0.64n
R_2	5.4%	0.58n
2nd op-amp	4.3%	0.46n
Quantization	28%	3n
Total		**10.7n**

Fig. 10 Simulated noise summary for DVB-T (a) and ATSC (b) mode

3.4 Simulation Results

Some simulation results are now shown to give further insight into the reconfigurability of the Filtering ADC structure, and into the design procedure, and to provide more details about the noise analysis.

A. Reconfigurability and general simulations

The discrete time signal transfer functions and quantization noise transfer functions evaluated for the four different clock frequencies are reported in Figure 9. They were simulated considering half a clock cycle nominal loop delay and the discrete time Matlab equivalent representation of the Filtering ADC (Appendix I). It is possible to recognize both the effective f_0 and f_{WB}. The wide-band signal transfer function of the DVB-T existing base-band is reported also for comparison. The in band gain is normalized in the graph to the $1/gm_{DAC}$ value, which was also the gain of the old design. The in-band loss of the Filtering solution, with respect to the original one, is due partly to the damped design ($gm_{DAC}R_2 \approx 10$, see Chapter 2) and partly to the finite driving impedance gain reduction effect (partition between R_S and the input impedance). For each standard (ATSC-A/74 and DVB-T):

1. Signal transfer function analysis was performed using the discrete time equivalent model and the Simulink one (Appendix I) and then was confirmed using circuit transient simulations.
2. The handling of the maximum signal versus frequency was simulated with Simulink, considering the representation of video OFDM input signals as multiple sinusoidal tones to take into account the PAR.
3. Quantization noise estimation was provided using the discrete time equivalent model, and then was refined with Simulink.
4. Analog noise estimation was obtained simulating, with the circuit simulator, the continuous time model of the architecture.
5. Non-linearity two-tone tests were performed through circuit transients.
6. Power-up from reset mode and from power-down were verified.

Circuit transient simulations considered the entire converter architecture, both analog and digital. Together with the signal transfer function, the large amplitude stability (maximum signal amplitude) of the converter was characterized, increasing the amplitude of the input current tone, at each frequency, until the level at which modulator instability was produced.

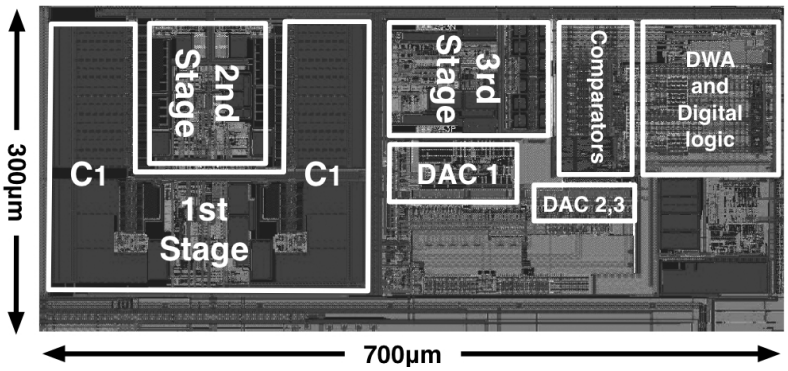


Fig. 11 Filtering ADC picture (layout)

Corner analysis was also performed, in order to show the robustness of the architecture to process and temperature variations and to bias and voltage supply reduction or increase.

B. DVB-T and ATSC simulations and noise summaries

The DVB-T in-band (1MHz-9MHz) gain drop from the $1/gm_{DAC}$ normalized gain level is almost 1.6dB. About 1dB is due to the intrinsic effect of damping (R_2), the remaining 0.6dB is due to the driving impedance partition with the input one, which is estimated in 180Ω. The DVB-T noise summary is given in Figure 10.a. The main analog noise contribution is the input operational amplifier, which was not optimized for noise performance. The third analog contributor is the DAC of the second stage. Quantization noise estimation represents about the 26% of the total noise amount. The two-tone test performed to evaluate the linearity of the converter, using sinusoidal tones stimulating 3rd order intermodulation effects due to adjacent channels, showed intermodulation products always more than 10dB below the noise floor, even if choosing worst case current levels for the input tones with respect to modulated video signals.

The ATSC in-band (1MHz-7MHz) gain drop from the $1/gm_{DAC}$ normalized gain level is almost 1.75dB. About 1dB is due to the intrinsic effect of damping (R_2), the remaining 0.75dB is due to the driving impedance partition with the input one, which is estimated in 230Ω. The ATSC noise summary is given in Figure 10.b. The main noise contribution is still the input operational amplifier. Almost the same comments as for the DVB-T case can be given. Quantization noise estimation represents about the 28% of the total noise amount. The two-tone tests performed for the linearity evaluation of the converter showed intermodulation products always more than 10dB below the noise floor also in this case.

3.5 The Filtering ADC prototype

The Filtering ADC was fabricated in a 90nm (then shrinked to 80nm) CMOS process. The layout of the prototype is reported in Figure 11. Only the base-band for the I (Q) path is depicted for simplicity. All the sections of the continuous time modulator are highlighted. The active area of the entire base-band is 0.21mm^2. As expected, it is mainly dominated by the input capacitance C_1.

The operational amplifier of the first stage is placed in the middle of C_1, together with the Filtering ADC narrow-band section remaining passives (R_1, R_2 and C_2). The operational

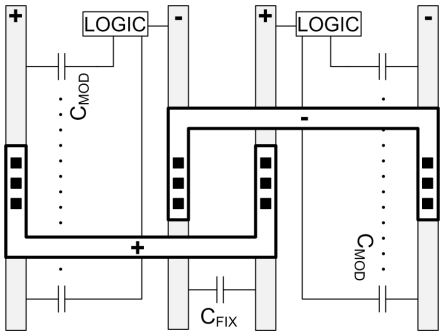


Fig. 12 Scheme of the implementation of the differential section of the capacitance C_1

amplifiers of the second and of the third stage are equal. The only small difference in the consumed area is the different value of the feedback capacitances C_{B2} and C_{B3}. A careful layout was carried out for the switching pairs of the DAC cells, since any parasitic or spur coupling would have deteriorated the DAC linearity performance. Comparators, DWA, digital logic and voltage regulators (the area not named in the picture) occupy a non negligible amount of area (about 25% of the total).

As mentioned, another critical point of the layout was the interconnection of the differential section of the first capacitance C_1, in order not to degrade the differential properties of the modulator. The scheme of the adopted solution is shown in Figure 12, and exploits a double "U" common centroid interconnection shape. A thick metal layer with low resistivity for square is used for the long interconnections. This layer is not visible from the layout in Figure 11, but can be appreciated from the entire tuner photograph in Figure 1.

If the base-band section is compared with the existing wide-band original one, 10% of extra area is consumed. This corresponds to only less than 2% area increase if the entire analog section of the receiver is computed. Remember, however, that this is not a fair comparison, since the original solution was not able to satisfy the ATSC-A/74 standard. A fairer comparison can be provided with the equivalent filter-ADC cascade presented in section 2.2. In this case the cascaded solution would have required about 35% more area (estimated) in the capacitances than that of the Filtering ADC solution, to get the same noise and the same voltage swing at the mixer output (required to preserve the modulator and mixer linearity). This is because the overall noise advantage of the Filtering ADC in comparison to the equivalent filter-ADC cascade is quantitatively simulated in about 2dB. The only way for the cascaded solution to get the equivalent noise figure performance, when used in a receiver chain, of the Filtering ADC, would be to increase the gain preceding the base-band (by 2dB). A reduction of the base-band impedance levels would be so required (e.g. higher C_1).

3.6 Measurement Results

The measurement results are reported only for the ATSC-A/74 6MHz channel bandwidth operating mode. In this case the IF signal bandwidth goes from 1MHz to 7MHz. The Filtering ADC dynamic range profile (Chapter 1) is reported in Figure 13. The required ATSC-A/74 base-band dynamic range mask, evaluated in section 3.2, is also reported for comparison. Contrary to a traditional ADC (see also Figure 4) the proposed one has a frequency dependent

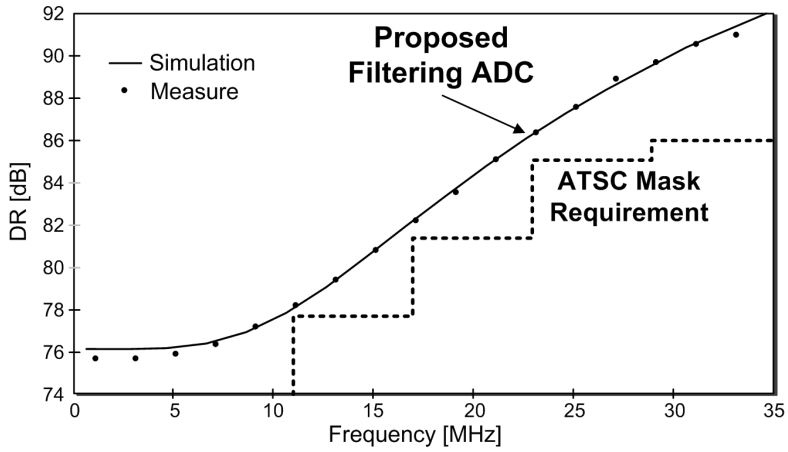


Fig. 13 Filtering ADC dynamic range versus frequency (DR(f))

Main Parameters		DR and FoM	
Supply	1.2V-1.8V	In band DR/SNDR	75.6dB/74.6dB
Power	54mW	DR/SNDR@15MHz	81dB/80dB
Clock	405MHz	DR/SNDR@30MHz	90dB/89dB
Bandwidth	1-7MHz	In band FoM	1.03pJ/c-s
Technology	90nm CMOS	FoM@15MHz	0.55pJ/c-s
ADC area	0.21mm^2	FoM@30MHz	0.2pJ/c-s

Fig. 14 Measurement result summary

dynamic range that matches the blocker mask. In this sense the Filtering ADC can be considered a further step, with respect to the existing solutions, in the optimization of the fitting of the base-band performance to the system specifications. The result perfectly follows the requirements.

The in-band dynamic range is 75.6dB and it grows in frequency due to the embedded filtering action. It is 81dB at 15MHz and 90dB at 30MHz. This almost corresponds to the frequency at which the interferer profile stops to increase, according to the standard. The noise measurement provided only about 0.2dB discrepancy with simulations for the integrated in-band noise, showing good accuracy also for the quantization noise analysis and estimation. A slightly narrower ADC signal transfer function was obtained than simulated, however respecting the 0.8dB maximum value of in-band gain loss required by the system level simulations. The ATSC condition is handled with margin. A 4dB margin was measured in the overall tuner in the ATSC selectivity tests. The margin seen in Figure 13 would seem smaller. This is due to the fact that the entire PAR was considered to get the specification mask and this was then measured to be a worst case condition.

The signal to noise and distortion ratio varies with frequency too (Chapter 1, SNDR(f)), and resulted only 1dB below the dynamic range. The signal to noise and distortion ratio is 74.6dB in-band, 80dB at 15MHz and 89dB at 30MHz. These values correspond to 12.2bits, 13bits and 14.5bits ENOB, respectively. The power consumption of the entire base-band is 54mW, the main contribution to power consumption are the 36mW from the three not optimized operational amplifiers. If the figure-of-merit (FoM) of the filtering sigma-delta converter is evaluated using the following formula:

Main Parameters		Performance	
Standard	DVB-T/ATSC	NF @ max gain	3dB
Analog Power	340mW	Selectivity DVB-T (N+1)	40dB (spec 29)
Digital Power	100mW	Selectivity DVB-T (N+2)	46dB (spec 40)
Channel Bandwidth	5,6,7,8MHz	Selectivity A/74 (N+6)	59dB (spec 57)
Technology	80nm CMOS	Image Rejection	>65
Die Area	5.6mm^2	IIP2 IIP3	+20/+66 -15/+30

Fig. 15 Measurement result summary of the Marvell DTT Tuner

$$\text{FoM} = \frac{\text{Power}}{2^{\text{ENOB}+1}.\text{BW}} \qquad (1)$$

where BW is the desired signal bandwidth in which noise and distortion are integrated (i.e. 6MHz for the ATSC-A/74 case), values of 1.03pJ/conv-step, 0.55pJ/conv-step and 0.2pJ/conv-step are achieved in-band, at 15MHz and 30MHz respectively. A complete summary of the measurements result is given in Figure 14.

Since the Filtering ADC base-band provided to the entire TV Marvell tuner the ability to extend its range of application managing the ATSC standard too, modifying only the base-band topology in the entire architecture, a measurement summary of the complete receiver is also reported in Figure 15. The numbers are those of the industrial TV tuner implementation. As stated in section 3.3 a Filtering ADC first implementation was realized increasing the first DAC current full-scale to be conservative in the ATSC interferers handling margin (then measured in 4dB). A new sizing was then provided to report the base-band gain equal to that of the original version, thus measuring a 2dB final margin. The numbers provided in Figure 15 deals with this second implementation. The selectivity performance exploits directly the Filtering ADC benefits shown in Chapter 2. The base-band does not deteriorate the global noise figure and linearity (IIP2 and IIP3) performance.

The Marvell TV tuner is now in production, representing a section of the Marvell ARMADA 1500 high performance high definition media processor powering the new Google TV platform [33].

3.7 Comparison with the state of the art

A comparison with the state of the art of Sigma Delta converters is given in the following, updated to the year of the Filtering ADC main paper publication [16]. A first comparison is reported with the state of the art of filtering ADC. This is a pretty new concept, and poorly present in literature. A comparison with the state of the art of traditional wide-band continuous time Sigma-Delta converters is then shown.

A. Comparison with the state of the art of filtering ADCs

Figure 16 reports the comparison table. The proposed solution shows the best performance both in-band and out-of-band, thus revealing its benefits in the implementation of an interferers immune base-band. The out-of-band measured results are chosen at a frequency equal to four times the signal band right edge.

Work	BW [MHz]	Fclock [MHz]	Power [mW]	SNDR peak [dB]	DR [dB]	In-band FoM [pJ/step]	Out-of-Band FoM [pJ/step]	Area [mm^2]	Technology
This work	6	405	54	74.6	75.6-90	1.03	0.2	0.21	0.09µm
[17]	1	64	2	59	65-71	1.37	0.7	0.14	0.18µm
[34]	6.5	96	122.4	70.9	75	3.28	-	2.15	0.18µm

Fig. 16 Comparison with the state of the art of filtering ADCs

The solution reported by Philips et al. [17] has an in-band behavior similar to the proposed architecture (1.37pJ/conv-step versus 1.03pJ/conv-step). However, only a first order filtering transfer function is implemented. Furthermore, the low pass narrow-band filter (a passive voltage one) is placed after the first operational amplifier of the converter, so it does not help to relax the linearity requirements of the active elements, since they still have to manage all the input current. In the proposed Filtering ADC it was shown that the input capacitance is able to passively filter out the interferers, in the current domain, before reaching the first active integrator.

The architecture presented by Pandita et al. [34] has a very high frequency selectivity, even if the power consumption is more than two times the Filtering ADC, for almost the same bandwidth and the same in-band SNDR. First, it is not possible to evaluate which is the maximum signal that the architecture is able to handle simply looking at the signal transfer function. A filtering signal transfer function in fact prevents the saturation of the quantizer present at the end of the converter, but does not guarantees the absence of clamping in the internal stages. Second, a discrete time complex implementation of the modulator has been designed, thus explaining also the ten times area consumed than the Filtering ADC.

B. Comparison with the state of the art of traditional wide-band ADCs

In Figure 17 the most relevant continuous time wide-band ADCs are reported. A first group [35-38, 31] is based on a voltage quantizer (Full-Flash internal ADC) while a second one [39-40, 21] is based on a time-domain quantizer. A comparison with traditional continuous time implementations can be useful, even if a completely different signal transfer function is implemented, under the assumption that the out-of-band performance of a filtering solution is compared with the in-band performance of a flat wide-band one. This becomes a fair comparison, between the two structures, if the out-of-band filtering achievement is evaluated at the frequency of the most critical interferer that the base-band has to handle. Actually, the entire base-band dynamic range (SNDR) profile should be compared.

Two elements have to be taken into account to better understand the previous statements. First, the wide-band structures, if not preceded by any low-pass filter, must be able to handle the same out-of-band interferers of the filtering architectures. In this sense their in-band dynamic range is still decided by out-of-band specifications. Second, in consequence of the previous aspect, the in-band (considering the application band, not the converter one) dynamic range of a wide-band system could be also oversized, and not really requested.

The proposed solution achieves very low area, since only the architecture reported in [40] is smaller, competitive power consumption ([38] consumes only 7mW but has also a very low signal to noise and distortion ratio) and dynamic range, over a bandwidth that is only slightly

Work	BW [MHz]	Fclock [MHz]	Power [mW]	SNDR peak [dB]	In-band FoM [pJ/step]	Out-of-Band FoM [pJ/step]	Area [mm^2]	Technology
This work	6	405	54	74.6	1.03	0.2	0.21	0.09µm
[35]	8.5	264	375	84	1.7	-	2.5	0.18µm
[36]	10	640	100	82	0.49	-	0.7	0.18µm
[31]	20	640	20	74	0.12	-	1.2	0.13µm
[37]	20	340	56	69	0.61	-	0.5	0.09µm
[38]	10	400	7	52	1.08	-	n.a.	0.09µm
[39]	25	400	48	67.7	0.48	-	2.6	0.18µm
[21]	10	950	40	72	0.61	-	0.42	0.13µm
[40]	20	250	10.5	60	0.32	-	0.15	0.065µm

Fig. 17 Comparison with the state of the art of traditional wide-band ADCs

narrower than the other applications. Normalizing the values to the signal bandwidth (i.e. considering the oversampling ratio) a clock frequency a little bit faster than the other solutions is used. In terms of FoM the best number is obtained, except for the architecture proposed by Mitteregger et al. [31]. A FoM of 0.2-0.15pJ/conv-step was the state of the art number for the oversampled ADC also at the International Solid State Circuit Conference 2012, at least looking at the high dynamic-range and high bandwidth applications. [31] presents then a FoM significantly lower than the others present in literature (even considering the most recent works).

Finally, it has also to be considered that the proposed solution was developed in a complete receiver tailored for industrial production, with safe-margins to guarantee the reliability of the product.

Chapter 4

The E-Filtering ADC based GSM-UMTS base-band

In this chapter the E-Filtering ADC structure is studied in its ability to represent the entire analog base-band of a cellular receiver (4.1-4.2). The detailed system level study of a new E-Filtering ADC based receiver chain is shown. Simulation results of the entire architecture are given (4.3). Finally a silicon prototype of an equivalent Rauch based receiver is presented, together with measurement results (4.4-4.5).

4.1 The E-Filtering ADC based receiver architecture and its system level analysis

In the application field of wireless receivers, cellular standards represent probably the most challenging environment, requiring at the same time very low-noise, to provide high sensitivity receivers, extremely linear circuits, to handle large input blockers (up to 0dBm power), with the constraint of a limited power consumption [41]. Critical trade-offs are expected to lead any design (both at the RF section and at the base-band one) and innovative strategies are always required to achieve increasing performance.

The proposed quadrature low-IF/direct conversion receiver architecture is shown in Figure 1 in a simplified building blocks scheme. Such architecture is intended to face both GSM and UMTS scenarios exploiting a current-mode intrinsic processing. The chain is reduced to a minimum number of blocks. Figure 2 depicts a more detailed, even if still simplified, picture of the receiver structure [22]. The SAW (GSM) and the Duplexer (UMTS) are not shown for simplicity.

The RF section is realized with a Low Noise Transconductor (LNT). It is characterized by a transconductance gain gm_{LNT} and conceptually provides the matching to the 50Ω antenna (there

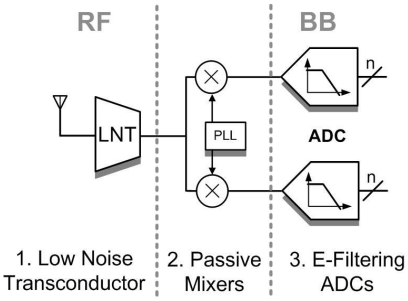


Fig. 1 The new proposed receiver scheme

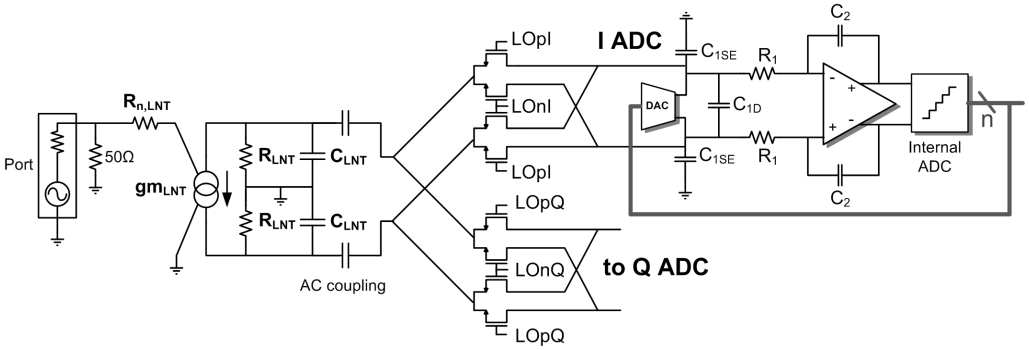


Fig. 2 The new proposed receiver scheme (more detailed)

will not be a physical 50Ω to ground in the effective implementation). The output current is driven with the highest possible output impedance, minimizing C_{LNT} and maximizing R_{LNT}. $R_{n,LNT}$ models the LNT noise.

The interface between the RF and the base-band (BB) is realized with current-driven passive mixers, implementing also the quadrature if a 0/90° LO control signal generated by a Phased Locked Loop (PLL) is used. Passive mixer receivers have become the solution of choices in recent times primarily for their low flicker-noise, high linearity and low power consumption [3, 15]. The RF/BB interface realized with the passive down-conversion, i.e. the equivalent base-band driving, is tackled in detail in Chapter 5.

The base-band relies on the E-Filtering ADC architecture described in Chapter 2. A 2^{nd} order narrow-band signal transfer function is realized, translating the input current in a output digital code through a transimpedance like gain, and performing a 2.5 equivalent quantization noise shaping (i.e. the intermediate performance between a 2^{nd} order and a 3^{rd} order Sigma-Delta).

As expected, the major attention in the analysis will be given to the base-band section, assuming fixed (and reasonable) RF section and passive mixer sizing and performance. Only one source of noise was not considered in Chapter 2 dealing with the Filtering ADC and the E-Filtering ADC: the noise due to the jitter of the clock frequency of the modulator. This element, whose theory and analysis is addressed in Appendix II (together with a large number of literature references), is also assumed for the presented system level study.

The system-level analysis of the entire architecture was led exploiting different evaluation and simulation tools:

1. Microsoft Office Excel was used to describe in an analytical way the entire architecture, embedding the analysis of the non-linearities (for the RF section), of the noise (for the whole chain, I and Q considered) and of the voltage swing at all the nodes of the circuit.

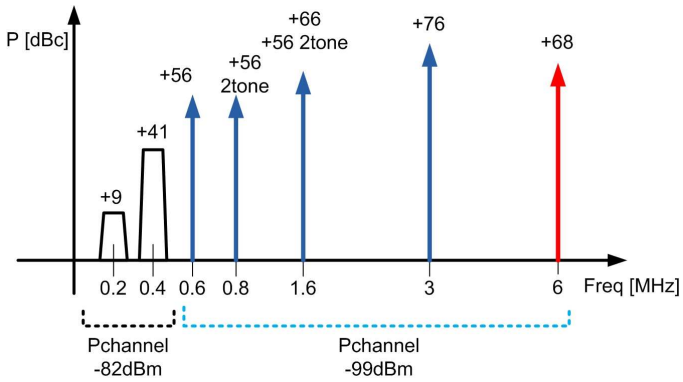


Fig. 3 GSM interferer profile

2. Matlab and Matlab Simulink were used to get the discrete time behavior of the Sigma-Delta ADC and to estimate the quantization noise and clock jitter noise contribution.
3. Cadence circuit simulations (Spectre PSS PAC and PNOISE) were performed to confirm the results of the previous points and to simulate passive mixer non predictable effects.

4.2 GSM and UMTS cellular standards [41]

GSM bandwidth is 200kHz. Its sensitivity target (-102dBm from the standard) is in the order of -110dBm, to achieve a competitive receiver for the commercial applications. This translates into 2dB noise figure requirement (5dB SNR at the ADC interface) evaluated at the front end input. A worst case 4dB SAW plus antenna switch attenuation is assumed.

The interferer standard profile is severe. It is shown in Figure 3, reported centered at DC assuming zero-IF receiver architecture. The profile is given in dBc with respect to the in-band desired signal power. The PAR of the blockers has also to be taken into account.

A first group of interferers considers the near out of-band modulated 200kHz bandwidth channels (100kHz and 300kHz distance from the 100kHz channel edge) that can be present with -82dBm channel power. The reference interferer (+41dBc at 400kHz offset from DC) can be particularly critical in terms of the absolute current level that has to be handled by the base-band, since it could be difficult to operate such a narrow-band base-band filtering to attenuate it. A second group considers the intermediate out-of-band interferers that can be received with -99dBm channel power. In this case both the +66dBc continuous wave blocker at 1.6MHz distance from DC and the +76dBc 3MHz one are almost equally challenging. They reach in fact -33dBm and -23dBm power, respectively. If the far out-of-band blockers are considered, there is also a very demanding 0dBm interferer at 20MHz/80MHz offset from DC, depending on the GSM RF band. Of course this situation is tackled only when a SAW-less chain is taken under investigation, since the 0dBm interferer falls out of the GSM RF global band. Two tone tests have also to be considered in order to verify 2nd and 3rd (e.g. the +56dBc at 0.8 and 1.6MHz offset from DC) order linearity performance.

UMTS channel bandwidth is 3.84MHz, with 5MHz channel spacing. Its sensitivity target is in the order of -107dBm (competitive commercial applications). This translates into 2.2dB noise figure requirement (-5.5dB SNR at the ADC interface) evaluated at the front end input. Worst case 4.3dB duplexer attenuation is assumed. The UMTS blockers profile is shown in Figure 4.

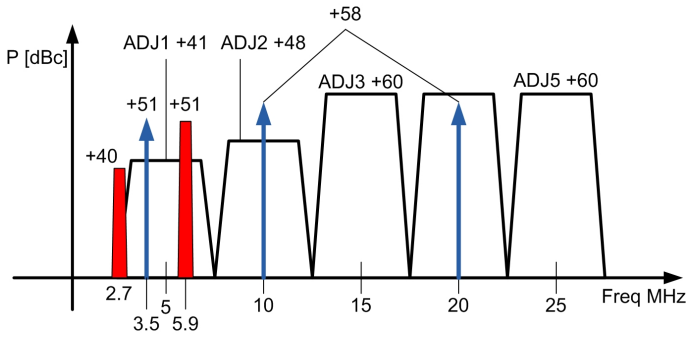


Fig. 4 UMTS interferer profile

Again the PAR of the interferers has to be taken into account besides the dBc average power value given in the graph.

The adjacent channel test (indicated as ADJ1) is particularly critical in the UMTS standard. Not only it can reach a power of +41dBc at only 5MHz distance from the desired signal, but also this power level grows together with the desired channel power (up to -66dBm desired signal and -25dBm interferer). Not shown in the Figure, the estimated -25dBm at 45MHz leakage from the transmitter (through the duplexer), operating UMTS in frequency division duplexing mode, has to be also analyzed. Notice (and this is valid for GSM too) that the near out-of-band blockers can become difficult to handle in terms of clock jitter of the base-band ADC, since the phase noise skirts can be not negligible, for a given timing reference generation, during the sampling that takes place at the ADC section (Appendix II).

Since the proposed receiver chain is broad-band for both the Low Noise Transconductor and the mixer, narrow-band filtering is introduced by the E-Filtering ADC only. The consequence of this is that the E-Filtering ADC has to be able to handle at its input the same scenarios as those reported in Figure 3 and Figure 4. In order to translate these informations into a useful dynamic range profile specification (Chapter 1), both the absolute level of noise produced by the RF section, and its gain, and the chosen cut-off frequency of the base-band have to be known. In this sense, an intensive evaluation and simulation work was carried out to investigate the noise/selectivity E-Filtering ADC intrinsic trade-off, in order to get the less demanding base-band requirements and to find the less power hungry way to satisfy such specifications in a limited silicon area environment.

The Low Noise Transconductance gain is equal to 50mS for both the standards. 1kΩ R_{LNT} and 400fF C_{LNT} represent the estimated transconductor output impedance (see Chapter 5 to get the equivalent base-band driving impedance). NMOS mixers were simulated driven with 900mV square wave 25% duty-cycle LO at 2GHz (UMTS) and 1.8GHz (GSM). Low Noise Transconductor plus passive mixer noise figure is equal to 1.5dB, which is considered a reasonable value achievable at low power consumption with the state of the art technology.

Using these parameters in the GSM case, a base-band noise floor of -128.5dBm (input referred at the receiver front end) has to be satisfied to get the total 2dB noise figure. The 400kHz +41dBc reference interferer test, and the 3MHz +76dBc one, set a required base-band dynamic range of 83.5dB and 101.5dB respectively (i.e. these values correspond to the dynamic range profile specification plot at 400kHz and 3MHz). If a cut-off frequency f_0''=1.4MHz is chosen for the E-Filtering ADC, the worst case (in-band referred) dynamic range is that

(a)

	GSM	High gain	Low gain
Internal wide-band ADC	ADC order	2	2
	clock	64MHz	64MHz
	ADC levels	14	14
E-Filtering ADC core	gm_{DAC}	160µS	500µS
	R_1 (R_{1X} R_X)	280Ω	560Ω 560Ω
	C_1	266pF	266pF
	C_2	24pF	34pF
	gm_{DAC2}	40µS	40µS
	gm_{DAC3}	40µS	40µS
Wide-band section	R_{B2}	25kΩ	25kΩ
	C_{B2}	1.65pF	1.65pF
	R_{B2}	25kΩ	25kΩ
	C_{B3}	0.9pF	0.9pF
	R_{NOTCH}	null	null

(b)

UMTS	High gain	Low gain
ADC order	2	2
clock	256MHz	256MHz
ADC levels	14	14
gm_{DAC}	280µS	560µS
R_1 (R_{1X} R_X)	100Ω	140Ω 350Ω
C_1	340pF	340pF
C_2	17pF	24pF
gm_{DAC2}	140µS	140µS
gm_{DAC3}	140µS	140µS
R_{B2}	7.2kΩ	7.2kΩ
C_{B2}	1.65pF	1.65pF
R_{B2}	7.2kΩ	7.2kΩ
C_{B3}	0.9pF	0.9pF
R_{NOTCH}	null	null

Fig. 5 GSM and UMTS E-Filtering ADC sizing

corresponding to the 3MHz blocker and is equal to 88.3dB, since the 3MHz blocker can be equivalently attenuated by 13.2dB by the low-pass biquad (101.5dB-13.2dB=88.3dB). If the RF section parameters are instead used in the UMTS case, a base-band noise floor of -113.7dBm (input referred at the receiver front end) has to be satisfied to get the total 2.2dB noise figure. The adjacent channel test sets a required base-band dynamic range of 84.4dB. This becomes 88.8dB if the signal PAR is added (worst case). If a cut-off frequency f_0=3.4MHz is chosen for the E-Filtering ADC, the worst case (in-band referred) needed dynamic range is reduced to 77.4dB (81.4dB with PAR), since the 5MHz blocker can be attenuated by about 7dB by the E-Filtering ADC.

4.3 Simulation results of the receiver chain

A. GSM case

The GSM sizing, decided after performance system level optimization of the E-Filtering ADC and following the same general considerations as reported for the DTT Filtering ADC sizing in Chapter 3 (section 3.3.A), is reported in Figure 5.a. The base-band can work in high-gain mode or in low-gain mode. The first one is used at the sensitivity condition, while the second one is used in the presence of critical blockers (when it is also possible to relax noise figure requirements). The high-gain is 48.5dB (from the front-end input). This corresponds to the 50mS LNT gain, -7dB passive mixer loss and 12kΩ base-band transimpedance. In low gain mode the gain is reduced by 9.5dB, acting on the base-band only. To get such an equivalent transimpedance high-gain, the DAC full-scale current is set to 80µA (160µS equivalent DAC transconductance). The clock frequency is 64MHz, to get enough quantization noise compression using only a second-order wide-band internal ADC (without notch). The number of internal ADC levels is decided the same as for the DTT case (Chapter 3), and the same stability constraint of up to half a clock cycle accepted extra-loop delay are taken. Considering the narrow-band E-Filtering ADC core, 266pF are chosen for the capacitance C_1 and 280Ω for the input resistance. Even if the value of the base-band input impedance is not so small at the cut-off frequency, the intrinsic E-Filtering ADC inductance-like in band behavior provides less than 25Ω in the signal band of interest (100kHz zero-IF). The 24pF/34pF capacitance C_2 gives

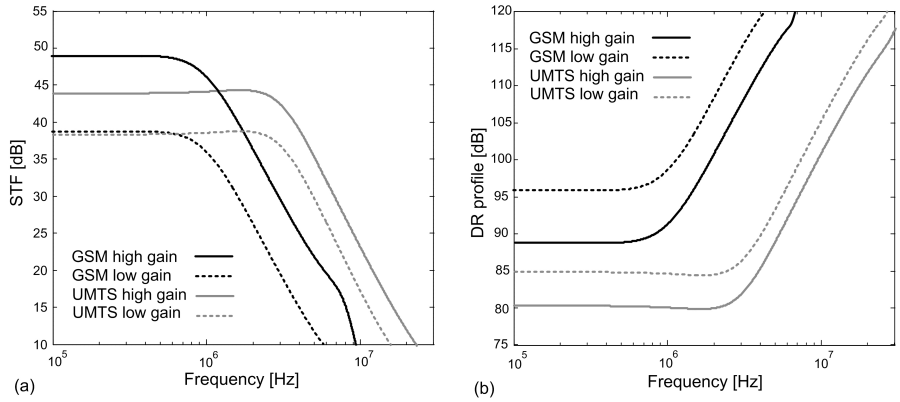


Fig. 6 (a) GSM and UMTS STFs E-Filtering ADC STF (high gain and low gain mode). (b) GSM and UMTS E-Filtering ADC dynamic range (high gain and low gain mode)

an estimated value of about 1.6pF parasitic to ground, that has to be carefully considered for the operational amplifier design, together with the absolute high C_2 value. The second and the third stage are scaled according to an estimated power consumption/noise trade off. All the values are shown single-ended in the table (Figure 5.a).

The GSM receiver signal transfer functions are given in Figure 6.a (notice the 1.4MHz cut-off). The simulated corresponding dynamic range profiles are instead plotted in Figure 6.b. Noise simulation shows that 2dB receiver noise figure and 89dB in-band dynamic range can be obtained for the given high-gain sizing. The low gain dynamic range increases to 96 dB (always in-band) because of the 9.5dB gain reduction and 2.5dB more base-band noise. The BB analog noise is contributed as follow: R_1 65%, operational amplifier 25% (assuming 100Ω equivalent noise input resistance), DACs 6% and others (i.e. second stage contributions) 4%. Noise results well agree (inside 0.5dB error) with the formulas provided in Chapter 2, once R_S is given as explained in Chapter 5.

The complete noise summary, for each standard test, is given in Figure 7.a. Here not only the noise contributions (in percentage) of all the sections are provided, but also the quantization noise estimations and the jitter E-Filtering ADC noise evaluations. For this latter case, the achieved numbers rely (see Appendix II) on the phase noise specification assumed for the ADC clock. Reasonable phase noise profiles are considered (Figure 8, gray curve). Such numbers in fact are expected not to require huge power consumption in the PLL to be realized. They were taken from an existing integrated prototype). Quantization noise is almost negligible, since a high oversampling ratio is chosen. The jitter coming from the quantization noise is also always below 1%. The jitter due to the phase noise skirts is important in the presence of high power interferers, as expected. The E-Filtering ADC contributes for about the 10% in all the cases. Its contribution grows up to 33% in low-gain mode. Except for the test named “sensitivity” the noise contribution of a class-A DAC was computed for evaluation simplicity. The noise figure varies between 1.9dB and 2.1dB in high-gain mode (2dB required), while reaching 3.3dB in low-gain mode. The potentiality of the class-B DAC was evaluated for the “sensitivity” test, showing further 0.2dB improvement. The corresponding SNR (required 5dB) is also plotted.

(a)

INPUT			GAIN	NOISE							NF	SNR
test name	signal	interferer	Gain									
ref interferer	-82	-41@400k	low	0.05	0.62	3.22	46.57	14.01	2.85	32.66	3.32	28.2
CW in band	-99	-43@600k	high	0.01	0.11	0.75	64.35	19.36	4.06	11.36	1.91	14.09
CW in band	-99	-33@1.6M	high	0.01	0.10	4.89	61.67	18.55	3.89	10.88	2.10	13.9
CW in band	-99	-23@3M	high	0.01	0.11	4.35	62.02	18.66	3.91	10.95	2.07	13.93
IM3	-99	-43@800k	high	0.01	0.11	0.78	64.33	19.36	4.06	11.35	1.92	14.09
	-99	-43@1.6M	high	0.01	0.11	0.51	64.51	19.41	4.07	11.39	1.9	14.1
AM suppress	-99	-31@6M	high	0.01	0.11	0.04	64.81	19.5	4.09	11.44	1.88	14.12
ref interferer	-82	-73@200k	high	0.01	0.11	0	64.84	19.51	4.09	11.44	1.88	31.1
sensitivity	-108	null	high	0.01	0.11	0	66.14	19.9	4.17	9.67	1.8	5.2
				quantization %	jitter quantization %	jitter skirts %	port %	LNA %	mixer %	ADC analog %		

(b)

INPUT			GAIN	NOISE							NF	SNR
test name	signal	interferer	Gain									
adj1	-66	-25@5M	low	3.88	1.69	13.28	34.27	10.25	2.49	34.14	4.65	33.07
IM3 1	-104	-46@10M	high	1.68	0.73	0	59.39	17.84	4.34	16	2.26	-2.43
	-104	-46@20M	high	1.68	0.73	0	59.40	17.85	4.34	16.01	2.26	-2.43
IM3 2	-97	-46@3.5M	high	1.67	0.73	0.62	59.03	17.73	4.31	15.91	2.29	4.54
	-97	-46@5.9M	high	1.68	0.73	0.08	59.35	17.83	4.33	16	2.27	4.57
transmitter	-107	-22@45M	high	1.68	0.73	0,01	59.39	17.84	4.34	16	2.26	-5.76
narrow band	-95	-55@2.7M	high	1.68	0.73	0.06	59.36	17.83	4.33	16	2.27	6.57
adj2	-104	-56@10M	high	1.68	0.73	0	59.40	17.85	4.34	16.01	2.26	-2.43
adj3	-104	-44@15M	high	1.68	0.73	0	59.40	17.85	4.34	16.01	2.26	-2.43
adj4	-104	-44@25M	high	1.68	0.73	0	59.40	17.85	4.34	16.01	2.26	-2.43
sensitivity	-107	-22@45M	high	1.78	0.77	0	62.69	18.84	4.58	11.35	2.03	-5.53
				quantization %	jitter quantization %	jitter skirts %	port %	LNA %	mixer %	ADC analog %		

Fig. 7 (a) GSM and (b) UMTS complete noise summary (each main standard test is shown)

The chip area is expected to be dominated by the input capacitance C_1 and by the feedback capacitance C_2. Exploiting partial differential implementation for C_1, a total capacitance of 230pF is given on-chip. The estimated power consumption of the E-Filtering ADC is 5mA (I+Q paths) with a voltage supply of 1.8V.

B. UMTS case

The UMTS sizing, decided after system level optimization of the E-Filtering ADC performance, and following the same general considerations as reported for the DTT Filtering ADC sizing in Chapter 3 (section 3.3.A), is reported in Figure 5.b. The base-band can work in high-gain mode or in low-gain mode. The high-gain is 44dB (from the front-end input). This corresponds to the 50mS LNT gain, -7dB passive mixer loss and 7.2kΩ base-band transimpedance. In low gain mode the gain is reduced by 6dB, acting on the base-band only. To get such an equivalent transimpedance high-gain, the DAC full-scale current is set to 140µA (280µS equivalent DAC transconductance). The clock frequency is 256MHz, to get enough quantization noise compression using only a second-order wide-band internal ADC (without notch). The number of internal ADC levels is decided the same as for the GSM case using also the same stability constraints. Considering the narrow-band E-Filtering ADC core, 340pF are chosen for the capacitance C_1 and 100Ω for the input resistance. This provides about 50Ω input impedance at the edge of the signal band of interest (1.9MHz). The 17pF/24pF capacitance C_2 gives an estimated value of about 1.1pF parasitic to ground. The second and the third stage are scaled according to an estimated power consumption-noise trade off. All the values are shown single-ended in the table (Figure 5.b).

The UMTS receiver signal transfer functions are given in Figure 6.a (Notice the 3.4MHz cut-off). The simulated corresponding dynamic ranges are instead plotted in Figure 6.b. Noise

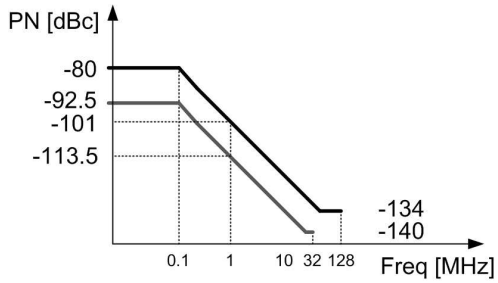


Fig. 8 GSM (64MHz clock, gray) and UMTS (256MHz clock, black) internal ADC clock phase noise profiles

simulation shows that 2.2dB receiver noise figure and 80dB in-band dynamic range can be obtained for the given high gain sizing. The low gain dynamic range increases to 85dB (always in-band) because of the 6dB gain reduction and 1dB more base-band noise. The BB analog noise is contributed as follows: R_1 35%, operational amplifier 35% (assuming 100Ω equivalent noise input resistance), quantization 18%, DACs 6% and others (i.e. second stage contributions) 6%. Also in this case noise results were seen to well agree with the formulas provided in Chapter 2.

The complete noise summary, for each standard test, is given in Figure 7.b. Quantization noise is below 2% in high gain mode and reaches 4% when low gain is switched on. The jitter coming from the quantization noise is also always below 2%. The jitter due to the phase noise skirts is important in the presence of high power interferers, as expected, and especially in the adjacent channel test, since the high power blocker is also not far from the band of interest (the clock phase noise profile is given in Figure 8, black curve). The E-Filtering ADC contributes for about the 15% in all the cases. Its contribution grows up to 34% in low-gain mode. As for the GSM analysis, except for the test named “sensitivity” the noise contribution of a class-A DAC was computed for evaluation simplicity. The noise figure is about 2.2dB 2.3dB in high gain mode (2.2dB required), while reaching 4.6dB in low gain mode. The potentiality of the class-B DAC was evaluated for the “sensitivity” test, which is simply the “transmitter” test when the class-B DAC is used, showing further 0.25dB improvement. The corresponding SNR (required -5.5dB) is also plotted.

The chip area is expected to be dominated by the input capacitance C_1 and by the feedback capacitance C_2. Exploiting partial differential implementation for C_1, a total capacitance of 255pF is given on-chip. The estimated power consumption of the converter is still 5mA (I+Q paths, 1.8V voltage supply).

C. Conclusions on the GSM-UMTS simulation results

The presented work and the simulation results described show that the E-Filtering ADC (Chapter 2) is a low-power candidate suitable to implement the base-band analog section of a cellular receiver. All the test-cases were passed with margin (SNR≥SNR required). All the benefits of the Filtering ADC are exploited, and challenging dynamic range is also achieved embedding the architecture without damping (E-Filtering ADC), some VGA action and class-B DAC proposal. Of course the reported system analysis comes from simulations and evaluations. In this latter case, however (i.e. for the quantization noise and the jitter analysis) some worst-case margin was considered. The two GSM and UMTS receiver chains, sharing the same RF

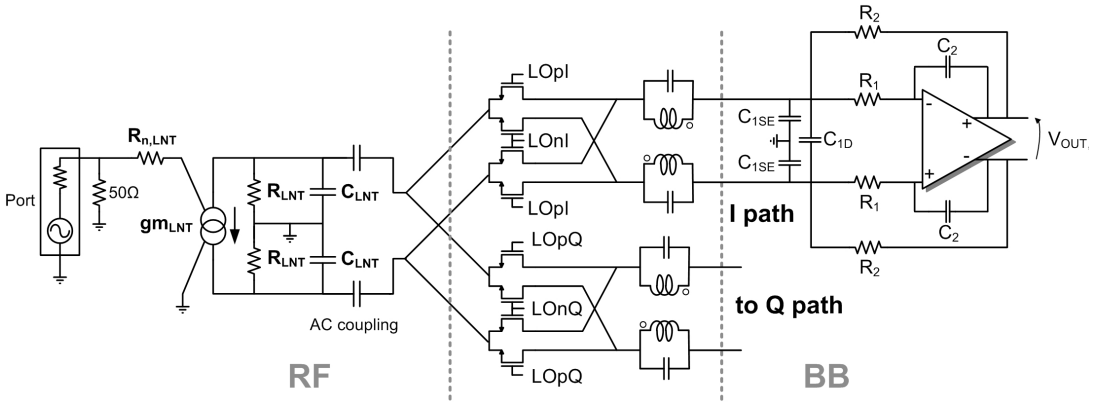


Fig. 9 The Rauch based receiver chain

section, could be merged in a single reconfigurable base-band. To give an idea of the quality of the achieved result, the FoM of the E-Filtering ADC, evaluated for the GSM (3MHz) and the UMTS (5MHz) case, is 160fJ/conv-step and 80fJ/conv-step respectively.

4.4 Continuous time equivalent E-Filtering ADC Rauch filter

In the previous chapter it was shown through simulations that E-Filtering ADC based analog to digital base-band is able to satisfy the stringent requirements of cellular receiver applications. This was obtained first assuming a given RF section, and then modeling and simulating the E-Filtering ADC architecture of Chapter 2. This second step, in order to be evolved into a silicon design, requires the handling of the analog to digital interface of the receiver, which in turn demands digital design skills, tools (i.e. simulation tools, standard cells, layout tools) and time. It was explained in Chapter 2 that the Rauch filter biquad can be seen as the continuous time equivalent of an E-Filtering ADC. The Rauch filter was also used in section 2 as a suitable base-band to perform a comparison with the E-Filtering ADC performance. The result of the comparison was that the E-Filtering ADC could reach best performance than the Rauch cell, at the same time implementing the same selectivity functionality and the same impedances level (area) and power consumption. Furthermore, it was pointed out that the first stage of a complete Filtering ADC architecture is expected to dominate both non-linearity and noise performance, while deciding most of the power consumption of the overall ADC. In this sense, the Rauch biquad is the solution and architecture which provides the closest overall performance with respect to the E-Filtering ADC converter, and so its implementation in a silicon prototype can be seen as an intermediate step in the E-Filtering ADC realization, and can be used for useful noise, power consumption and non-linearity measurements.

In the following, the design of a Rauch biquad filter for GSM and UMTS applications, in a reconfigurable multi-standard approach, is shown. First, a glance at the overall receiver chain is given. Then the Rauch biquad design (i.e. sizing of the passives and operational amplifier design) is given. Finally the 40nm prototype is presented together with system simulations and measurement results.

		GSM	UMTS
Rauch biquad	Gain	47.5/41.5	45/39
	f_0,Q	1.4MHz,0.78	3.2MHz,0.71
	R_2 [Ω]	7k/3.5k	3.5k/1.75k
	R_{1X}	350Ω	150Ω
	R_X	900Ω	300Ω
	R_{1X} || R_X	250Ω	100Ω
	C_{1SE}	18pF	18pF
	C_{1D}	168pF	168pF
	C_2 [F]	20p/28p	20p/28p

Fig. 10 GSM and UMTS base-band sizing

A. The GSM-UMTS receiver chain

The overall architecture of the receiver chain is reported in Figure 9 [42]. The system is the same as the one already studied in sections 3.1-3.3, if the E-Filtering ADC base-band is substituted with a Rauch biquad. In the silicon prototype two different RF sections (i.e. two different low noise transconductors) and mixers share a single reconfigurable GSM-UMTS quadrature base-band. A SAW less application is the target for the GSM chain.

The RF gm stage is implemented in one case (GSM) with a single ended input, while in the second case (UMTS) with differential input. A transformer-based blocker resilient active fully differential common gate topology core is exploited in both cases [42]. The equivalent gm_{LNT} of the two architectures was simulated in 35mS and 46mS for the GSM and UMTS case respectively. The output impedance was estimated in about 1.5kΩ resistive contribution and <250fF capacitive one (including 100fF parasitic coming from the mixer switches and 80fF from the 2pF AC coupling capacitance).

The mixer is a passive one operated in current mode. The switches are NMOS to implement about 20Ω of on-resistance when driven with a 25% duty-cycle 900mV amplitude square wave LO signal. The down-conversion stage includes also an LC tank resonating at four times the LO frequency ($4f_{LO}$) in series with the base-band input. Up-converting and down-converting, at the LNT output node, the high impedance of the tank at $3f_{LO}$ and $5f_{LO}$, this creates a notch in the receiver transfer function around the RF signal 3rd and 5th harmonic. This improves harmonic rejection, which is crucial in a SAW-less application. As a secondary benefit, this also reduces the LNA and transformer noise folding, improving the receiver noise-figure.

A low-power divider is also integrated to generate the 25% duty cycle LO phases at f_{LO}, starting from a $2f_{LO}$ external clock reference [42].

B. Rauch base-band sizing

The base-band was sized following the general guidelines of the section 3.3 (and the general Filtering ADC guidelines of Chapter 2, section 3.3.A). The values of the capacitances were decided equal between GSM and UMTS case in order to get a more uniform design. Furthermore, this simplifies the possibility to introduce an open-loop three bits reconfigurability on the capacitances, in the direction of embedding a future calibration action. The sizing is reported in Figure 10. In the first line the entire receiver gain is provided. It was maintained almost not-changed from the system level E-Filtering ADC analysis. A Butterworth biquad was

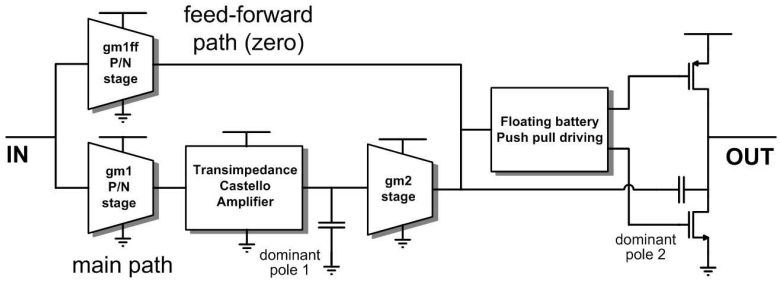


Fig. 11 Operational amplifier simplified architecture

designed for the UMTS case, while a Q slightly bigger than a Butterworth one was chosen for the GSM case. Remember that the Q value is dependent on the driving impedance (Chapter 2). The effect of the passive mixer interface (see Chapter 5) is also to give an asymmetry in the signal transfer function, thus modifying the cut-off frequency and the quality factor, which also becomes difficult to be defined in a complex transfer function environment.

The large value of the input capacitance C_1 is expected to dominate the prototype base-band area, considering that the reported value increases of the 25% with calibration. Also in this case a two gain base-band configuration is used, with 6dB gain difference. The VGA action was implemented the same way as for the E-Filtering ADC. The feedback capacitance is 20pF in high gain mode and 28pF in low-gain mode. These are not small values, and give also about 1.5pF of parasitic to ground. The consequence is that the operational amplifier output is loaded in a not-negligible way.

C. Operational amplifier architecture

The operational amplifier is the core of the base-band. This is true for both the E-Filtering ADC and for the equivalent Rauch biquad. The input operational amplifier determines the power consumption of the Rauch and represents the major contribution for the converter implementation. It also decides the non-linearity performance of the base-band (this would be true also for the E-Filtering ADC assuming a completely linear DAC), and contributes in a non-negligible way to the base-band noise.

Considering non-linearity, the best base-band performance can be achieved increasing the operational amplifier open-loop gain at the frequency of the signal to be processed. In fact the higher is the operational amplifier gain, the smaller is the swing at the virtual ground node (i.e. a better virtual ground is achieved). This reduces the generation of non-linear terms, for a given output swing, thus improving the base-band linearity. According to this, a three-stages operational amplifier with feed-forward compensation is chosen [31]. The feed-forward compensation (used also for the operational amplifier of the Filtering ADC presented in Chapter 3) consumes some bias current in order to increase the open-loop gain slope of the operational amplifier from the traditional -20dB/decade to -40dB/decade. The consequence is that the virtual ground effect is improved in the range of frequencies of the application blockers (which are the responsibles of intermodulation non-linear effects).

Considering noise, it was shown in section 3.3.A/B that a 100Ω equivalent noise resistance contributed the 25% of the total base-band noise in the GSM case and the 35% in the UMTS

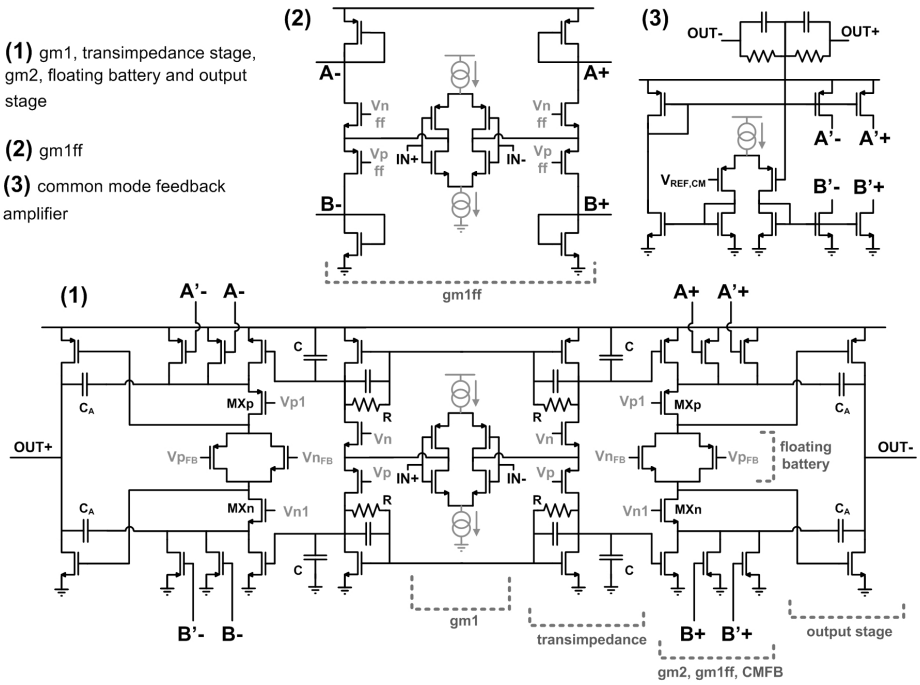


Fig. 12 Operational amplifier detailed architecture

one. The 100Ω value is assumed as a noise design reference. Notice that it is not completely fair to model the operational amplifier noise performance with a white noise source only, the flicker term has also to be considered, especially in a direct-conversion environment.

The operational amplifier simplified architecture is given in Figure 11. The main path is implemented by a input complementary gm stage (gm1), which defines the noise floor of the entire block, a transimpedance amplifier based on the topology proposed by P. W. Li et al. [43], but operating the driving from the source of the transistors (in current mode), and a second gm stage (gm2), which feeds current to the floating battery [44-46]. The feed-forward path is given conceptually by a simple gm stage (gm1ff), which sums its current with the one of the main path. The floating battery stage drives the push-pull class-AB inverter-based output stage. This latter section is compensated introducing a dominant pole (dominant pole 2) in the architecture.

The compensation for the stability works as follows. The main path has more gain than the feed-forward (auxiliary) one, but less bandwidth (due to the dominant pole 1, Figure 11). In this way, at low frequency, the parallel gain of the two paths is dominated by the main path gain, and sees a -40dB/decade slope (dominant pole 1 and 2 operate). At a given frequency the gain of the main path becomes less than the gain of the auxiliary, due to the dominant pole 1, and the wide-band gain of the feed-forward path determines a -20dB/decade slope (dominant pole 2 is always working). In this way a zero is introduced in the overall gain, and the theory of conditioned stability is approached. According to this the open loop gain could also be higher than one, and with 180 phase shift, but oscillation is not generated, since Nyquist theorem is still respected (no encircling of the open loop gain around the -1 point in the complex plane). The dominant pole 2 is actually not implemented using the traditional Miller compensation technique, but using an Ahuja compensation mode [47], to avoid the problem of the right plane zero and to save some current consumption in the biasing of the output stage.

	Current [mA]	%
gm1	0.6	33%
transimpedance	0.16	8.8%
gm1ff	0.24	13.2%
Floating battery	0.3	16.4%
output	0.36	19.8%
CMFB+bias	0.16	8.8%
Total	1.82	
Total (I+Q)	3.64	

Fig. 13 Current consumption of the operational amplifier stages

Figure 12 shows, without the bias section, the complete operational amplifier schematic. The gm1 stage is implemented with a PMOS-NMOS architecture. In this way PMOS and NMOS input differential pairs work in parallel to increase by a factor 2 the input gm with respect to an NMOS (PMOS) only implementation. Consider that the first stage (gm1) uses about the 33% of the power consumption of the operational amplifier, and the another 33% would have been required to get the same noise performance using a traditional implementation.

In the transimpedance stage the input current coming from gm1 is brought to a high impedance load through PMOS and NMOS common gate current buffers. The gain is decided by choosing the value of the differential resistance (R). Such a resistance is seen in differential mode, while in common mode the 1/gm of the transistor connected to the voltage supply is seen. The high-impedance node is loaded with the capacitance C, in order to set the first dominant pole of the architecture. The transimpedance stage consumes the 8.8% of the power consumption. The gm2 stage is simply implemented with common source transistors. The gm1ff stage is a scaled replica of gm1, consuming the 8.8% of the total power consumption in its core (differential input pairs) and 4.4% in its buffer stage. The output current of gm2 and gm1ff is summed at the source of MXp and MXn, which act as cascodes. In this way both MXp and MXn (which are crucial for the Ahuja compensation) and the floating battery re-use the bias current of gm2, gm1ff and of the common-mode-feedback output stages. As a consequence their small signal gm is increased. The Ahuja compensation capacitance C_A is closed at this node. PMOS and NMOS currents are summed into the floating battery, which drives the push-pull output stage, and consumes the 16.4% of the total current. The output stage is a simple CMOS inverter, driven by the floating battery, consuming 19.8% of the total current. The common mode feedback uses the architecture proposed by Degrauwe et al. [48]. The amplifier has 4 current outputs and consumes a negligible current (less than 3%). The bias section consumes 6% of the total. The current consumptions of the stages are reported in Figure 13. The voltage supply is 1.8V.

The high power consumption of the floating battery and of the output stage are mostly required by a stability constraint. The output stage is biased with 180µA (single ended), while dynamically about 600µA of interferer current have to be handled by the operational amplifier during the most critical test. In this sense an aggressive class AB operating mode is not implemented. A reduction of the 180µA bias, however, is not possible due to the need to ensure safe margins to avoid the oscillation of the circuit.

The output node of the operational amplifier is loaded with the parasitic of the feedback capacitance C_2 and, at high frequency, with the parasitic of the input transistors of the gm1

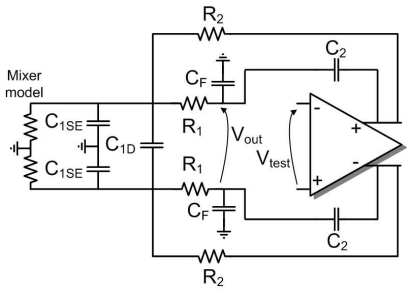


Fig. 14 Operational amplifier differential stability analysis

stage, which is seen through the Rauch feedback network. This latter is not always negligible; on the contrary it can be the most contribution in zero-IF low frequency applications, when the input transistors have to be very large in order to lower the flicker noise. Actually, the series between C_2 and the input parasitic is seen, so that also a big value of C_2, even if assuming fixed parasitics, goes in the direction to increase the output load. The main consequence of a big capacitive load is that a high output current is required to push the non-dominant pole (which mainly depends on the output capacitance) sufficiently far from the loop unity gain frequency f_T of the network.

The stability analysis is performed as indicated in Figure 14 for the differential case (V_{out}/V_{test}). The mixer is modeled with simple resistances connected to ground (see also Chapter 5). C_F is the input capacitance of the operational amplifier that is reported at the output node of the loop for the analysis. The main effect of the feedback network is to introduce a two-poles/two-zeros transfer function in cascade to the operational amplifier forward open loop transfer function. This increases the phase shift in the open loop transfer function at low-frequency, approaching 150 degrees at about 1MHz (corresponding gain >50dB). However, due to the zeros, the phase shift returns to a safe value at the unity gain frequency. The loop is designed to have more than 90MHz bandwidth in all the working conditions (GSM/UMTS, high/low gain, calibration) with >65 degrees phase margin and >14dB gain margin. The -40/-20 dB per decade dual slope approach gives the possibility to achieve 40dB open loop gain at 2MHz (i.e. the edge of the UMTS signal band) and 75dB at 200kHz (i.e. the edge of the GSM low-IF one). Notice that considering only the operational amplifier gain, these values are significantly higher (90dB and 62dB respectively).

The Ahuja loop stability is then carefully considered. The model of the Ahuja compensation is shown in Figure 15. The open loop analysis can be performed by switching off I_{IN} and opening the loop at the gate of MOn. The three nodes of the loop (A, B, C) are highlighted in the Figure. C_P models the entire parasitic capacitance due to MOn and MXn at the node C.

The Ahuja loop has a DC zero (due to C_A) and three poles. The first is associated to the output node (A), the second is associated to the source of MXn (B), and the third is associated to the drain of MXn (C). In a traditional implementation (e.g. audio operational amplifiers) C_P is big (MOn is big to drive a small load resistance $1/g_{OUT}$). Due to this, the pole associated to the node C is the dominant one together with the output pole (associated to A), while the pole associated to B is the non-dominant one ($f_{PB}=1/(2\pi)\cdot gm_{MXn}/C_A$). In closed loop, i.e. when the amplifier transfer function $Vout/I_{IN}$ is considered, the non-dominant pole of the network is

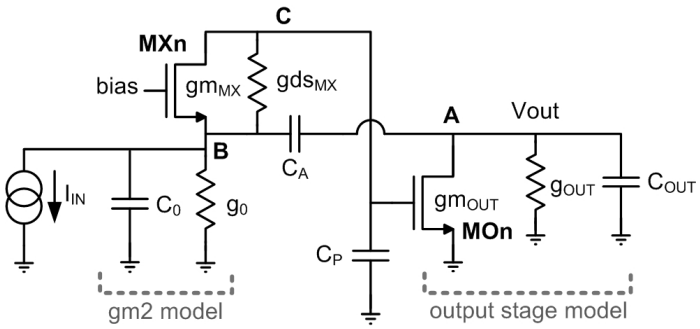


Fig. 15 Ahuja compensation technique. Simplified model (gm2 and output stage)

placed at a frequency $f_{PCL}=1/(2\pi)\cdot gm_{OUT}/C_{OUT}\cdot C_A/C_P$. This is the frequency of the non-dominant pole, if Miller compensation were used, moved by a factor $C_A/C_P>1$.

In the Rauch operational amplifier design C_P is small since small transistors are used at the output stage. For this reason the pole associated to the node C is no longer the dominant one of the loop, but operates as non-dominant. Vice-versa, the pole associated to B depends no longer on the conductance gm_{MXn} but on gds_{MXn} and this lowers its frequency ($f_{PB}'=1/(2\pi)\cdot gds_{MXn}/C_A$). The reason for this is that the drain of MXn tends in this case to an high impedance (no longer to a low impedance), and so the impedance gds_{MXn} (instead of gm_{MXn}) is seen from the MXn source. Under this condition, the factor that pushes at high frequency the output pole of the closed loop network is no longer C_A/C_P, but gm_{MX}/gds_{MX} (still>1), and so corresponds to the intrinsic DC gain of the cascode transistor MXn ($f_{PCL}'=1/(2\pi)\cdot gm_{OUT}/C_{OUT}\cdot gm_{MX}/gds_{MX}$). The stability of the Ahuja loop is ensured in the Rauch design with more than 80 degrees of phase margin.

The operational amplifier is analyzed also with respect to the stability of the common-mode feedback. Finally, closed the common-mode feedback, the common-mode stability of the Rauch architecture is evaluated. In this latter case the open loop gain is designed not to go above the 0dB level in the whole range of frequencies. This is achieved connecting some compensation capacitance of the dominant pole 1 (Figure 11) to ground, and not only in differential mode.

Due to the complexity of the entire architecture, the stability behavior is finally confirmed through transient simulations, evaluating also the presence of a correct start-up phase.

Only one external reference current is used to bias the whole operational amplifier together with a voltage reference for the transimpedance stage. All the other bias voltages are generated internally using current mirrors and diode-connected transistors.

In the following some numbers are given to understand the operational amplifier design, especially when considering the noise constraint (input stage) and the stability issue (output one).

The equivalent noise resistance of the operational amplifier simulated at the system level for the E-Filtering ADC based chain was 100Ω. This value is maintained for the Rauch design. It corresponds to 6mS small signal transconductance of gm1 (single ended) if a Γ factor approaching 0.6 is considered for the transistor working in under-threshold region. Assuming some margin, to take into account the active load of the transimpedance stage, and the flicker noise, 10mS are designed (i.e. 5mS for the PMOS and 5mS for the NMOS). At 40nm technology this small signal transconductance can be obtained in under-threshold mode with

(a)

	Low-IF	Zero-IF
PORT	50.7%	47.5%
LNA	38.5%	36.9%
Mixers	4%	4%
Rauch base-band: OTA fn	2%	6.8%
Rauch base-band: OTA id	0.8%	0.8%
Rauch base-band: R_1	3.5%	3.5%
Base-band	6.8%	11.6%
NF	2.95	3.25

(b)

	Zero-IF
PORT	65.4%
LNA	26%
Mixers	2.9%
OTA id	1.65%
OTA fn	0.3%
R_1	3.3%
Base-band	5.7%
NF	1.84

Fig. 16 (a) GSM and (b) UMTS simulated noise summary

0.3mA current supply, so that 0.6mA of total current are given for the differential implementation of the input stage.

The total capacitance loading the output node at high frequency is estimated in about 12pF (9pF is the parasitic capacitance (C_F) of the input stage, 3.5pF are the parasitic of C_2 (right and left side, considering calibration) and 2.5pF are taken as estimation of the pad and of the off-chip capacitance). With this load, 15mS equivalent output stage small signal transconductance would be required to push the non-dominant pole at a frequency of about 2 times the network f_T target (200MHz), if Miller compensation were used. This would ensure 60 degrees phase margin, assuming a single non-dominant pole architecture. The required current bias would be 0.5mA (1mA differential) for the output inverters, thus increasing of almost the 40% the total power consumption with respect to the designed (assuming gm/I_{DRAIN}=15 for the output transistors). The Ahuja compensation technique is exploited to limit the output stage current to 0.175mA (0.35mA differential) for >65 degrees phase margin.

D. Rauch base-band noise and non-linearity simulations

Some simulation results are now provided since it was not possible during measurements to directly drive the base-band from its input nodes, but only from the receiver RF inputs.

The simulated gain of the entire receiver is 47.5dB for the GSM case and 45dB for the UMTS case. The corresponding noise summary is given in Figure 16 for both the GSM (a) and UMTS (b) case. The 50Ω port noise is also given. In the GSM case the low-IF summary integrates the noise between 1kHz and 199kHz. The base-band (I and Q) contributes almost the 7% of the overall noise. 2% is due to the flicker noise of the operational amplifier input pairs, while 0.8% is due to its thermal one. The resistance R_1 represents the base-band major contribution with 3.5%. When the base-band noise performance is integrated in zero-IF band (10Hz-100kHz) the flicker contribution increases to the 7%, to give a total base-band noise that is almost the 12% of the total. In the two cases 2.95dB and 3.25dB noise figures are obtained. The zero-IF UMTS band is considered between 1kHz and 1.92MHz. The receiver noise figure is 1.84dB, while the base-band noise (in this case the flicker contribution is of course minimum) is below 6%. I/Q noise crosstalk is explained in Chapter 5.

Base-band non-linearity was simulated driving the single base-band (I or Q path) with current sinusoidal tones. The GSM IM3 test was performed in high-gain mode using 35μA (-43dBm at the RF input, as specified by the standard) at 0.8MHz and 1.7MHz. The input referred 3rd order current intermodulation (IM3) is equal to 0.2nA at 100kHz, thus showing an IM3 about 100dB smaller than the input tones and obtaining more than 50dB signal to distortion

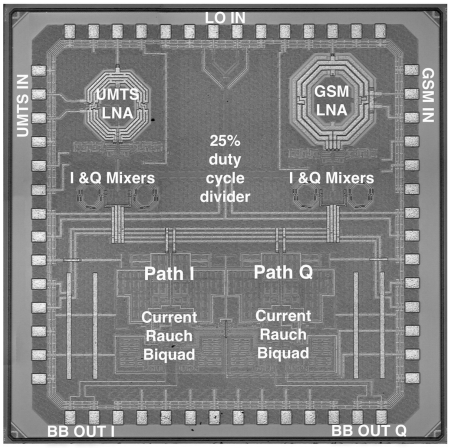


Fig. 17 Rauch prototype. Entire receiver

ratio for the equivalent test. A non-linearity UMTS IM3 was simulated modeling the adjacent channel power with two sinusoidal signals of 400μA current at 3.5MHz and 6MHz (-25dBm at RF). In such a critical condition the UMTS low-gain mode was exploited. The input referred 3rd order current intermodulation (IM3) is 6nA at 1MHz, thus showing an IM3 more than 90dB smaller than the input tones and obtaining more than 50dB signal to distortion ratio for the test.

Simulating the base-band in the entire chain (with a simplified transconductor LNT stage but with quadrature architecture and real mixers) it was shown that equivalent interferer output tones, with however higher IM3 results, were achieved in both the standards. This ensured that the base-band is not degrading the non-linearity performance of the overall chain.

4.5 The Rauch prototype

The silicon prototype of the receivers (i.e. GSM and UMTS front end with a single reconfigurable Rauch base-band) was fabricated in 40nm CMOS technology and is depicted in Figure 17. The base-band occupies an active area of about 0.6mm^2. About 70% of the base-band area is due to the input capacitance C_1, while about 15% is due to the feedback capacitances. The remaining 15% is mainly due to the operational amplifier core (8% of it are the compensation capacitances).

The measurement results were performed for the entire receiver only. The board that gives the possibility to directly measure the base-band is currently under design and fabrication. The GSM/UMTS receiver signal transfer functions are reported in Figure 18.a and 18.b respectively, for high-gain and low-gain mode, if the base-band reconfigurable bits are moved from the “000” configuration to the “111” one (“100” corresponds to the nominal sizing). The frequency selectivity is of course only due to the base-band while the complex asymmetry is due to the passive mixer interface (Chapter 5). The transfer functions are normalized to the high-gain. Notice how it is no more possible to define, in such a complex environment, a cut-off frequency and a quality factor for the biquad. The -40dB/decade slope is instead still present. The base-band selectivity is able to filter the 0dBm GSM interferer at 20MHz frequency by 34.5dB/40.5dB (depending on the calibration), thus ensuring a blocker resilient base-band. The UMTS adjacent channel is filtered by 6.2/12.2dB.

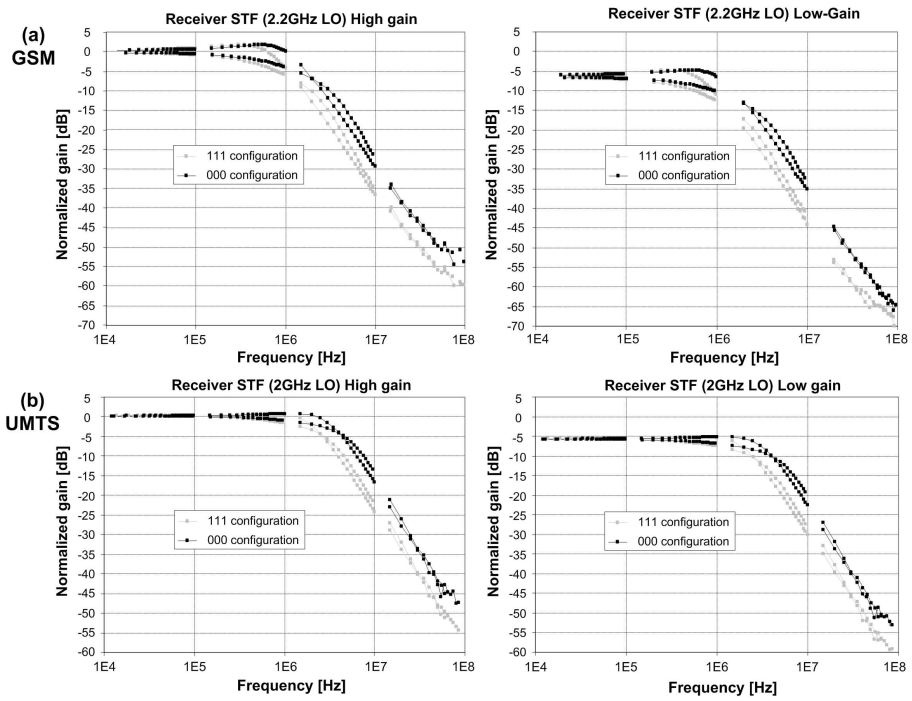


Fig. 18 Receiver signal transfer functions (a) GSM, (b) UMTS. High-gain and low-gain mode normalized to high-gain one

Other measurement results are reported in Figure 19. The in-band (RF band) gain for the GSM and UMTS receivers is the same (45dB). At the center frequency of 2.2GHz for the GSM and 2GHz for the UMTS minimum receiver noise figures of 3.8dB and 1.8dB are obtained respectively. This is true only when the LC tank post-mixer resonates at the correct $4f_{LO}$ frequency (it can be in fact tuned). The reported DSB noise figure values are considered at a single IF frequency (100kHz) and the noise figure performance should be instead integrated in all the desired signal band, obtaining slightly worse results due to flicker noise effects. Moreover, the base-band noise should also grow approaching the cut-off frequency due to the high pass base-band noise shaping (Chapter 2). While the UMTS noise figure fits acceptably well with the simulations, the GSM noise figure is 1dB far from the simulated. In correspondence to this, however, 2dB less gain (45.5dB versus 47.5dB) were also measured, due probably to a misalignment of a resonant section of the LNT or to a third coil gain loss [42]. According to this the noise figure is reasonably degraded by the gain loss, and not through intrinsic bad base-band noise estimation.

A comparison with the state of the art is also provided in [42] to confirm how the proposed receiver architecture, thanks also to the Rauch based filtering base-band, is able to be competitive with existing solutions. In this sense the Rauch (and in consequence of this its equivalent and also better E-Filtering ADC realization) can be seen as a further step, with respect to the other receiver solutions reported in literature, in the direction of improving the cellular receiver immunity to out-of-band blockers. The Rauch base-band gives to the receiver the possibility to perform all measurements with 0dBm interferers at only 20MHz offset from the desired signal. If the comparison with narrow-band solutions is pointed out [2-3], the proposed receiver uses a fraction of the area and power to get better linearity and harmonic rejection with comparable noise. The Rauch based receiver reaches overall better performance

Main Parameters		Performance GSM/UMTS	
Standard	GSM/UMTS	NF @ max gain	3.8/1.9dB
Supply Voltages	1.2-1.8	max gain	45.5/45.5dB
Channel Bandwidth	0.2/1.92MHz	LNA+Mixer+BB Power	24/24mW
Technology	40nm CMOS	LO Power	6/6mW @ 2GHz
Active Area	0.84/0.74mm^2	IIP2 @ max gain	64/66dBm
		IIP3 @ max gain	18/16dBm

Fig. 19 GSM-UMTS Rauch based receiver chain measurement result summary

than [49], which is presented by the authors as an example of software defined radio oriented receiver design. Compared with the best wide-band receiver proposed by Murphy et al. [50], the chain has a worse noise but better linearity, harmonic rejection and area. In addition the power consumption is 20% less.

Chapter 5

BB/RF interface: a switched capacitor current driven passive mixer model

In this chapter the interface between the RF section and the base-band, in a wireless receiver, is discussed. Current driven active and passive mixers are shown (5.1). Since the state of the art is moving towards the use of the passive solution, this latter is addressed in detail, focusing on the base-band equivalent driving impedance issue (5.2). A switched capacitor model able to explain both gain and noise performance of a current passive mixer based receiver is proposed. The verification of the model is given for a Rauch based base-band (5.3).

5.1 The BB/RF interface

A single down-conversion mixer represents nowadays, in state of the art of CMOS wireless receivers, the only intermediate stage between the RF section and the low/zero-IF base-band one (direct conversion). The evolution of technology, complexity and design skills has the goal to move the analog to digital interface as close as possible to the antenna, and so also before the mixer. However, RF sampling in the digital domain would require unacceptable power consumption to be performed. For this reason the first down-conversion stage is still until now in the field of the analog processing.

Two possible mixer implementations exist [51]. On one hand the active solution, on the other the passive one. Even if both are based on transistors switching on and off, in the first case the on condition of a switch (MOS transistor) corresponds to the saturation region, in the latter to the triode one. This gives many differences in the behavior of the down-conversion stages.

Even if active mixer theory is well known and consolidated in literature, active mixers have a minimum use in the state of the art of wireless receivers. Passive mixer based zero-IF

receivers, instead, are becoming the solution of choice in the last years, even if their theory is not complete, or at least it is not always intuitive. For this reason, in the following, only the passive solution is tackled in detail, while the active one is only addressed briefly. The main purpose of the analysis is not to explain mixer theory, but to evaluate how the BB/RF interface affects the receiver behavior, i.e. which is the equivalent driving provided by the down-conversion stage to the base-band and how this affects base-band transfer functions (both for the signal and for the noise).

A. The active mixer interface

The active mixer main implementation is the Gilbert cell. The mixer switches, driven by the LO signals, act as current switches, leading the current at the positive or at the negative output. When a switch is in on-state, it is biased to work in the saturation region, since the DC bias current is switched together with the RF signal. From this point of view the output impedance of the mixer can be very high, since the on-switches, working with intrinsic gm/gds gain, create a shield between the RF section that drives the switching mixer pairs and the mixer output. Assuming not to consider overlap or disoverlap in the LO phases, so an ideal LO signal with 50% duty-cycle, it can be assumed that the output impedance of the mixer stage is that of a cascoded stage, since at any time a switch is connected to the output nodes implementing a cascode configuration. More probably, due to limited voltage swing, it is not possible to cascode the active mixer load, and this dominates the output impedance. This was the case for the harmonic rejection mixer used in the DTT tuner presented in Chapter 3.

Due to these reasons, modeling the active mixer as a simple resistance (R_S) driving the base-band is correct. This was done during the DTT base-band design. As shown R_S modifies the base-band signal transfer function (f_0, Q and gain for the Filtering ADC and Q only for the E-Filtering ADC) and has to be taken into account into the noise evaluations. Corresponding the R_S value to the gds of a transistor, eventually with cascode stage, values >1kΩ can be obtained also in scaled technologies. About 2.5kΩ were simulated for the DTT mixer (90nm).

B. The passive mixer interface

In the passive mixer implementation, contrary to the active one, the mixer switches, driven by the LO signals, work in on-state in the triode region, since they do not have any DC bias current [52]. In the field of wireless receivers, passive mixers can be operated either in voltage mode [53] or in current mode [54-56], depending on the relative value of the RF and BB impedance. They can also be used as mixer-first receivers [57].

Passive mixers have become the solution of choice in recent times for three main reasons: the zero power consumption, intrinsic high linearity (especially in current driven architectures) and low-flicker noise (no DC bias). This has lead to a large number of papers tackling mixer issues, but most of the time a simple intuition, providing the possibility to get straightforward hand design guidelines, is missing. A possible reason for this is that a passive mixer is not able to shield the BB to the RF, and vice-versa (impedance transformation property [54-57]). The base-band driving impedance is not simply evaluated or, more in general, the receiver signal transfer function (STF) is not correctly given. Moreover the base-band noise is affected. These issues are then complicated in the most used case of a quadrature receiver.

Since the current driven mixer topology is the most chosen in recent literature, and it is the one of interest also for the current driven base-band circuits proposed in Chapter 2, it will be presented only in the following. The literature has approached the STF and the noise of a passive current mode mixer from different points of view. The STF has been analyzed by Mirzaei et al. providing the down-conversion gain versus frequency (analyzing the architecture from the RF side) through detailed circuit calculations (50% duty-cycle) and up-conversion to RF of the BB input impedance (25% duty-cycle) for non-quadrature and quadrature architectures [54-56]. Notice that the down-conversion gain indirectly provides the equivalent driving impedance for the base-band, if the architecture is analyzed from the BB point of view. The BB noise in a current mode passive mixer based receiver has been first studied in a qualitatively way by Redmann White et al. using a switched-capacitor (SC) approach [52]. This latter result however applies to non quadrature architectures only.

In the next section a current driven passive mixer model is presented. The approach is based on an intuitive switched-capacitor analysis that derives the equivalent base-band driving impedance looking from the BB point of view. The STF driving impedance theory holds also for voltage mixers, but not the noise one. To validate the analysis, a low-pass BB input impedance, with a cut-off frequency f_0 below the LO frequency f_{LO}, is assumed. The assumption of a BB f_0 at least one decade before f_{LO}, almost always verified in a RX chain, ensures accurate fitting also for a simple first order filtering.

5.2 Intuitive current driven passive mixer model [58]

At point (A) the base-band equivalent driving impedance displayed by a passive mixer interface is evaluated for a 50% duty-cycle non quadrature receiver. The analysis is extended to the 25% duty-cycle case at point (B) for the STF and at point (C) for the noise. Point (D) confirms the mixer model by evaluating theory versus simulations when an RLC parallel input impedance base-band (e.g. the one implemented with the Rauch structure) is used. Chapter Appendix I.A extends the results removing some of the simplifying assumptions of the model. Chapter Appendix I.B shows how the model is able to explain also the mixer switches noise.

A. 50% duty-cycle single chain equivalent BB driving impedance

For a single chain RX, both BB noise and mixer noise can be studied using switched-capacitor techniques if low switches on-resistance R_{SW} is assumed. It follows that the switched-capacitor approach can be used as a general theory for current driven passive mixers provided that also the STF can be evaluated in the same way.

Figure 1 shows a fully differential implementation of a non-quadrature passive mixer receiver. The switches are assumed ideal (i.e. $R_{SW}=0$ and the parasitic are embedded in the RF and BB sections) and Z_{BB} is the BB input impedance. The LO is assumed ideal, having non-overlapping 50% duty-cycle square-wave phases with negligible rise and fall times and enough amplitude to turn-on the MOS transistors with good overdrive. The LNT is modeled as a current generator $I_{IN,RF}$ (phasor at frequency f_{RF}) in parallel with a capacitance C_{LNT}.

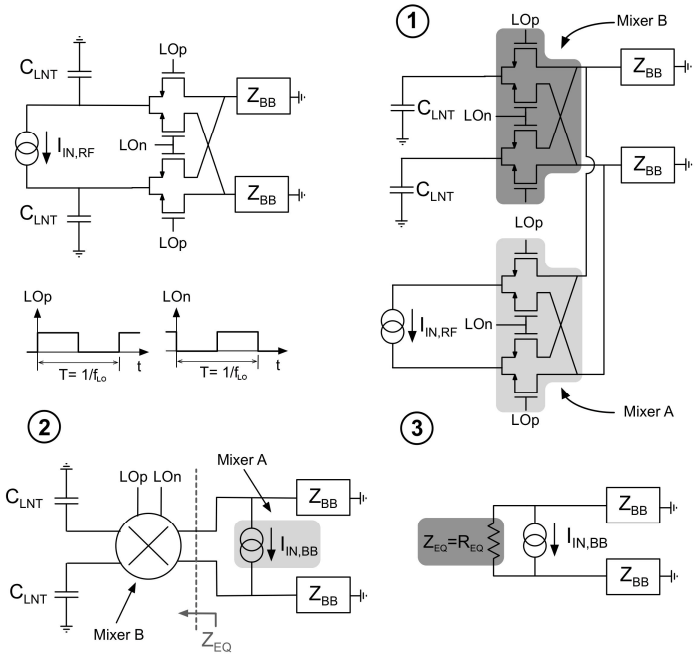


Fig. 1 50% duty-cycle receiver: the 3 steps procedure to get the switched capacitor model

Figure 1 shows the three step procedure used to derive the switched capacitor model proposed in this section:

1) Separate the RF current generator $I_{IN,RF}$ from the impedance C_{LNT} substituting the mixer with two mixers in parallel driven by the same LO, one connected to $I_{IN,RF}$ (mixer A), the other to C_{LNT} (mixer B). This transformation does not modify the circuit since R_{SW}=0 has been assumed.

2) Down-convert $I_{IN,RF}$ to BB via mixer A. The down-converted signal is the current generator $I_{IN,BB}$ (Figure 1) whose amplitude at f_{RF}-f_{LO} is equal to $(2/\pi)\cdot I_{IN,RF}$. Although $I_{IN,BB}$ contains replicas of the RF signal around the LO harmonics, the voltage at BB is only significant at f_{RF}-f_{LO} since Z_{BB} has a low pass shape with a cut-off frequency much below f_{LO}.

3) Replace mixer B with the equivalent impedance seen looking into its output (Z_{EQ}). For a 50% duty-cycle, Z_{EQ} can be evaluated using a classical switched-capacitor approach and corresponds to a SC resistance $R_{EQ}=1/(2C_{LNT}\cdot f_{LO})$ [59].

The above model can also produce, given the base-band driving impedance R_{EQ}, the mixer STF (performing a simple current partition of the down-converted current signal $I_{IN,BB}$ between R_{EQ} and Z_{BB}) and the transfer functions of the BB noise sources.

B. 25% duty-cycle quadrature chain equivalent BB driving impedance for the STF evaluation

The derivation of point (A) is extended to a quadrature receiver chain with 25% duty-cycle LO (Figure 2.a), making the same assumptions of the 50% duty-cycle case. A quadrature 50% receiver is expected to get much worst performance and so it is not considered [54-55].

By using the same procedure of point (A), the RF current generator $I_{IN,RF}$ is down-converted into two BB ones $I_{IN,BB,I}$ and $I_{IN,BB,Q}$ both with a $\sqrt{2}/\pi$ down-conversion gain (for a 25% duty-cycle) but displaying a $\pi/2$ relative phase difference (Figure 2.b).

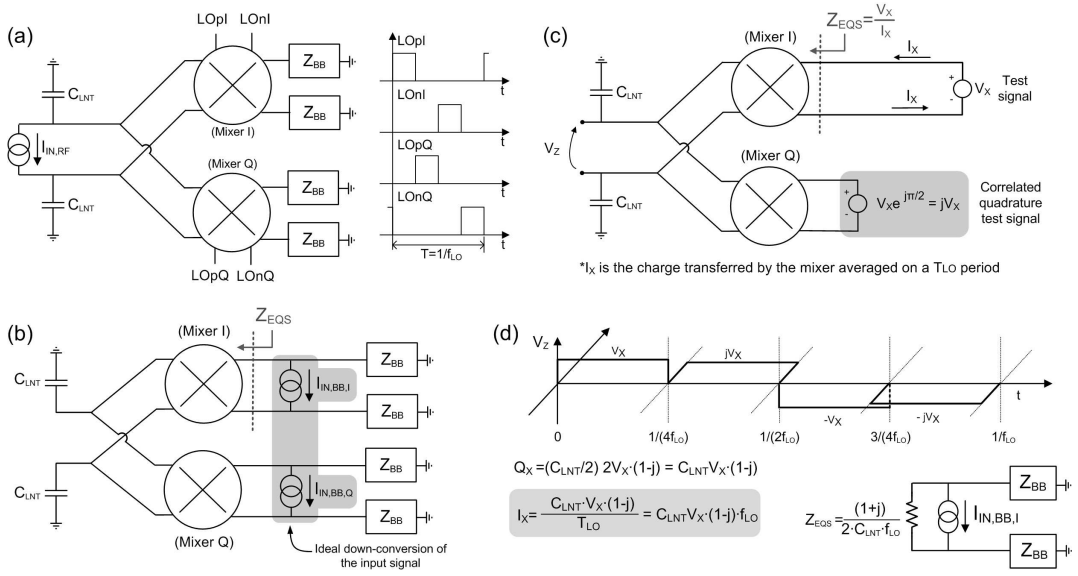


Fig. 2 (a) 25% duty cycle quadrature receiver (b) Ideal down-conversion of the RF signal in quadrature base-band (c) Equivalent base-band driving impedance calculation scheme (d) Differential voltage at C_{LNT} in the impedance test and STF quadrature chain model

The equivalent driving impedance Z_{EQS} seen from BB for the I (Q) path is computed as reported in Figure 2.c. A test voltage phasor V_X is placed at the I (Q) mixer output together with a correlated one jV_X ($\pi/2$ shifted) at the Q (I) mixer output. Z_{EQS} is then evaluated as the ratio between the test generator voltage and the average current I_X flowing through it.

I_X is obtained multiplying the charge absorbed by the capacitors during the different phases of the LO period times the clock frequency. As reported in Figure 2.d, capacitors C_{LNT} alternatively sample the test signals V_X and jV_X. This implies that the charge absorbed by the mixer every LO cycle is equal to $(1-j)V_XC_{LNT}$ giving the following driving impedance

$$Z_{EQS} = \frac{1}{(1-j)C_{LNT}f_{LO}} = \frac{(1+j)}{2C_{LNT}f_{LO}}. \quad (1)$$

Z_{EQS} corresponds to a complex resistance (i.e. there is a complex relation between the current and the voltage in the time domain). The real part comes from the charge sampled by C_{LNT} in the I path while the imaginary part comes from the charge sampled in the Q path.

Figure 2.d depicts also the final model for the I (Q) path. As for the 50% duty-cycle case, given Z_{EQS}, the STF is obtained from the partition of the down-converted current signal $I_{IN,BB}$ between the driving and the BB impedance. The presence of a complex value element (resistor) makes the STF a-symmetric around DC. This behavior captures the a-symmetry around the LO of the RF transfer function (different gains for frequencies below and above f_{LO}) already reported in literature [55]. Such a complex Z_{EQS} is responsible for the asymmetric signal transfer functions measured in Chapter 4 for the Rauch based receiver prototype. At point (D) a Rauch based base-band is chosen to verify the accuracy of the proposed theory versus simulation results.

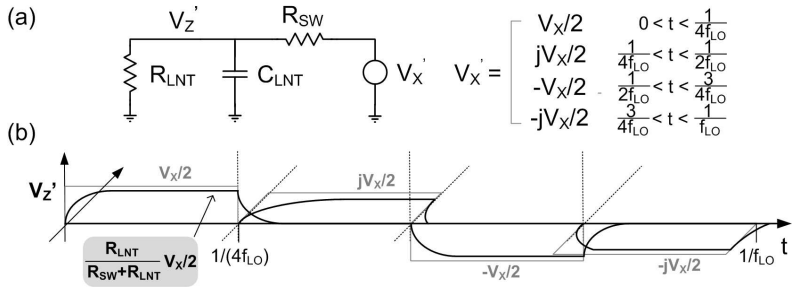


Fig. 3 (a) Equivalent base-band driving impedance calculation for $R_{SW}\neq 0$ and finite R_{LNT} (b) Voltage V_Z' across C_{LNT} during the impedance test

The equivalent impedance Z_{EQS}' for $R_{SW}\neq 0$ and for a finite resistance R_{LNT} in parallel to C_{LNT} at the LNT output is computed as follows (Figure 3.a), making also use of the result of the Chapter Appendix I.A. The impedance calculation using the switched capacitor theory cannot be directly applied. The voltage across C_{LNT} during each clock phase has an exponential response to the input test voltage V_X' (Figure 3.b). The average current flowing into C_{LNT} is given by the charge stored on it times the LO frequency, and depends only on the value of V_Z' at the end of the phase. On the other hand, the average R_{LNT} current is obtained integrating $I_{RLNT}=V_Z'/R_{LNT}$ in the same phase and observing that only half of the phases have to be considered in the evaluation. Separating the contributions, the differential equivalent BB driving impedances due to C_{LNT} and to R_{LNT} are respectively:

$$Z_{EQSC} = \frac{(1+j)}{2C_{LNT}f_{LO}} \cdot \frac{R_{LNT}+R_{SW}}{R_{LNT}} \cdot \left(1 - e^{-\left(\frac{1}{4Tf_{LO}}\right)}\right) \quad (2)$$

$$Z_{EQSR} = 4(R_{LNT} + R_{SW}) \cdot \frac{1}{\left(1-4Tf_{LO}+4Tf_{LO}e^{-\left(\frac{1}{4Tf_{LO}}\right)}\right)} \quad (3)$$

where T is the time constant of the $R_{SW}||R_{LNT}$-C_{LNT} network. The equivalent BB differential impedance Z_{EQS}' is the parallel of Z_{EQSC} and Z_{EQSR}, and can then be used to get the mixer STF by current partition, as explained above.

When $R_{SW}=0$, Z_{EQSC} correspond to Z_{EQS} (as expected) and Z_{EQSR} is equal to $4R_{LNT}$. The latter result can be understood noting that R_{LNT} is seen from BB, during each LO period, for a time equal to $1/(4f_{LO})$, and so its value is multiplied by 4. $Z_{EQSC}=Z_{EQS}$ is also true if $R_{SW}\neq 0$ but R_{LNT} is infinite, under the assumption that the network settles completely within the 25% DC time slot.

C. 25% duty-cycle quadrature chain equivalent BB driving impedance for the BB noise evaluation

When analyzing the BB noise, the main difference with the STF situation is that, to compute the driving impedance of the I (Q) path, the correlated test signal on the Q (I) path has to be substituted with Z_{BB}. Therefore the driving impedance is no more independent from Z_{BB}, as it was for the STF. To simplify calculations an ideal TIA (i.e. $Z_{BB}=0$) is assumed (Figure 4.a). This implies that when C_{LNT} is connected to the Q path it is fully discharged. For a real BB, this simplification introduces an error in the model. It has to be considered, however, that in a real

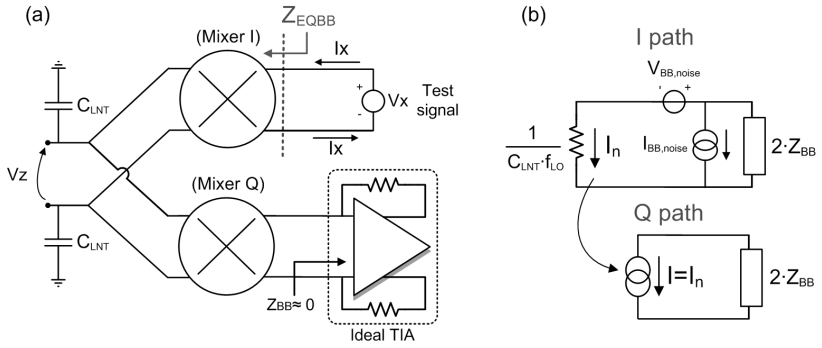


Fig. 4 (a) Impedance test for the BB noise (b) BB noise quadrature chain model

current driven approach the BB impedance is always much smaller than the RF output one, thus ensuring a limited magnitude for such an error.

For this simple case, a real driving switched-capacitor impedance $Z_{EQBB}=1/(C_{LNT}f_{LO})$ results. Moreover, since in each clock cycle the I (Q) noise stored on C_{LNT} is discharged in the Q (I) path, the noise originating from the I (Q) path is also observed in the Q (I) path (I-Q noise crosstalk). The final BB noise model is shown in Figure 4.b. Notice that Z_{EQBB} (the noise driving impedance) is 3 dB larger (in modulus) than Z_{EQS} (the STF driving impedance) but an additional noise source is present in the Q path.

An alternative mixer model can be developed to explain also the noise of the mixer switches. It is not object of interest to report it here, but the analysis can be found in the Chapter Appendix I.B.

5.3 Passive mixer model versus simulations

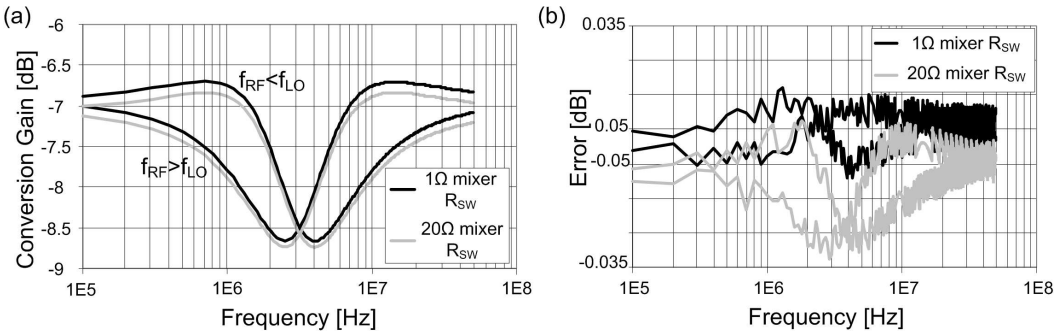
The comparison with simulations is now given only for the quadrature architecture, since it is the most used solution in practice, and implementing the base-band with a Rauch filter (i.e. the E-Filtering ADC continuous time equivalent, Chapter 4, Figure 9). As seen a parallel RLC input impedance is displayed in this way, with a cut-off frequency f_0 and a quality factor Q. This is also a representation of a more general case, including the simpler RC parallel load. The simulations have been done using Spectre PSS-PAC-PNOISE. All the simulations have been performed assuming simplified switches without embedded parasitics. The LO frequency assumed for the comparison is 2GHz.

A. BB STF driving impedance confirmation through STF simulations

Assuming that a complex input current tone $I_{IN,RF}=I_A\cdot\exp(j2\pi f_{RF}t)$, with amplitude I_A and frequency $f_{RF}=f_{LO}+f$, is injected by the RF differential current generator, and using the derived model for $R_{SW}=0$, the expression of the down-conversion gain (i.e. the ratio between the RF current and the current into Z_{BB} is (see Figure 2.a):

$$G(jf)=\frac{\frac{\sqrt{2}}{\pi}\cdot\frac{(1+j)}{4C_{LNT}f_{LO}}}{\frac{(1+j)}{4C_{LNT}f_{LO}}+\frac{j2\pi fL_{BB}}{\left(1-\frac{f^2}{f_0{}^2}\right)+j\frac{f}{f_0Q}}} \qquad (4)$$

being L_{BB} the BB equivalent inductance. When the more general Z_{EQS}' is used, the following



1Ω mixer R_{SW}
Z_{EQSC}=312.5Ω(1+j)
Z_{EQSR}=4kΩ

20Ω mixer R_{SW}
Z_{EQSC}=316Ω(1+j)
Z_{EQSR}=4.27kΩ

(c)

RF load [fF-kΩ]	800-2		800-0.25		400-2		400-0.25		100-2		100-0.25	
R_{SW} [Ω]	1	20	1	20	1	20	1	20	1	20	1	20
Max Error [mdB]	16	36	55	95	17	32	68	80	14	19	80	87

Fig. 5 25% (a) Down conversion mixer gain (STF) (R_{LNT}=2kΩ, C_{LNT}=400fF) (b) Spectre PAC versus STF model (c) PSS-PAC simulations versus model for different RF loads

STF is obtained (R_{LNT} is neglected in the first factor):

$$G(jf) = \frac{1}{1+j2\pi f_{RF} C_{LNT} R_{SW}} \cdot \frac{\frac{\sqrt{2}}{\pi}\cdot\frac{Z_{EQS}'}{2}}{\frac{Z_{EQS}'}{2}+\frac{j2\pi f L_{BB}}{\left(1-\frac{f^2}{f_0{}^2}\right)+j\frac{f}{f_0 Q}}} \qquad (5)$$

The simulated down-conversion current gain at the I (Q) output, obtained using typical parameters values (C_{LNT}=400fF, R_{LNT}=2kΩ, f_0=3.2MHz, Q=0.7, R_1=100Ω (Rauch input resistance)), is reported in Figure 5.a versus frequency. The curves represent the down-conversion gain for $f_{RF}>f_{LO}$ and $f_{RF}<f_{LO}$ for the two cases of R_{SW}=1Ω and R_{SW}=20Ω. If the gain obtained using (5) is drawn in this graph, the difference would be almost impossible to detect. To get a quantitative feel for the accuracy of the model the difference between the value of the conversion gain obtained with simulation and the analytical prediction obtained using the model is plotted in Figure 5.b versus frequency. The four curves correspond to positive and negative frequency for both R_{SW}=1Ω and R_{SW}=20Ω. The values of the equivalent SC base-band driving impedance (single ended), which are the values of interest in this context, are also shown. Figure 5.c reports the magnitude of the max error if C_{LNT} is varied from 100fF to 800fF, and R_{LNT} from 250Ω to 2kΩ. The small difference versus simulation for such a large variation of the parameters shows the solidity of the model. The error is within 0.1dB in the whole 50MHz frequency range, ensuring that the driving impedance is correctly estimated.

The frequency behavior of the gain (Figure 5.a) can be understood in an intuitive way as follows. Near DC ($f_{RF}<<f_{LO}$), and at high frequency ($f_{RF}>>f_{LO}$), the gain approaches that of an ideal mixer. This is because in both these cases either the BB inductance or the BB capacitance represents a short circuit, thus preventing any possible current partition with C_{LNT} at RF. On the other hand near f_0 the finite BB input impedance causes a gain reduction. Finally the new model can correctly predict the asymmetry in the conversion gain between positive and negative frequency around the carrier. This effect is embedded in the model through the imaginary part of Z_{EQS}', which gives rise to a complex transfer function.

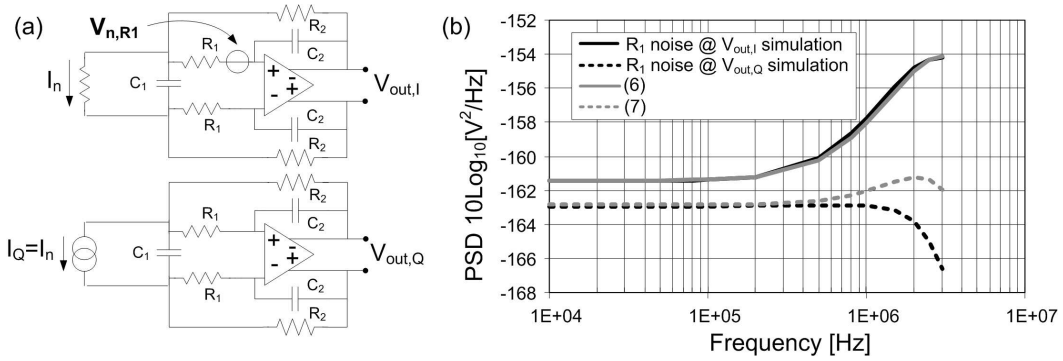


Fig. 6 (a) 25% BB noise model applied to the Rauch filter base-band (b) BB noise PSDs. Spectre PNOISE versus model

B. BB noise driving impedance confirmation through noise simulations

Consider the noise contributed by the resistor R_1 in the I (Q) path (Figure 6.a). The simulated noise power spectral densities (PSDs) due to R_1 at the differential outputs $V_{out,I}$ and $V_{out,Q}$ are reported in Figure 6.b (solid and dashed black line respectively) for $R_{SW}=20\Omega$ and the same typical parameters of the previous subsection. The frequency range of interest has been chosen equal to f_0. BB noise SC model has been used to derive the corresponding PSDs expressions:

$$\frac{dV_{out,I}^2}{df} = 4k_B T R_1 \left| \frac{R_2+Z_{EQBB}}{Z_{EQBB}} \cdot \frac{1+j2\pi f C_2 (R_2 || Z_{EQBB})}{1-\frac{f^2}{f_0^2}+j\frac{f}{f_0 Q^*}} \right|^2 \qquad (6)$$

$$\frac{dV_{out,Q}^2}{df} = 4k_B T R_1 \left| \frac{R_2/Z_{EQBB}}{1-\frac{f^2}{f_0^2}+j\frac{f}{f_0 Q^*}} \cdot \frac{1+j2\pi f C_2 R_2}{1-\frac{f^2}{f_0^2}+j\frac{f}{f_0 Q}} \right|^2 \qquad (7)$$

where $Q^*=Q\cdot Z_{EQBB}/(R_1+Z_{EQBB})$ i.e. Q_{BB} takes now into account the Z_{EQBB} load.

These formulas are compared with simulation in Figure 6.b (gray lines). I path model PSD fits simulation with great precision. The max PSD error, in the whole frequency range, is only 0.3dB and remains low even if C_{LNT} is swept from 100fF to 800fF (65mdB and 0.75dB error respectively). Q path PSD is affected by a not negligible error (4 dB max) when the frequency is near to the Rauch cut-off frequency f_0 and the error increases if C_{LNT} is increased. This error is due to the fact that zero BB impedance in the Q path (TIA) has been assumed for simplicity in the theory. However, as the frequency approaches f_0, the BB input impedance of the Q path reaches its maximum value (parallel RLC network at resonance) giving rise to a significant charge partition loss in the I-Q noise crosstalk effect. The amount of the total integrated in-band noise error is limited to about 1.75dB. It has to be observed also that this error affects the non-dominant source of noise, and so is completely negligible if I and Q contribution are added. Finally notice that the error becomes considerable only when C_{LNT} is really larger than practical ones (more than 0.5pF). These results still ensure that also in the BB noise case the base-band driving impedance is estimated with accuracy.

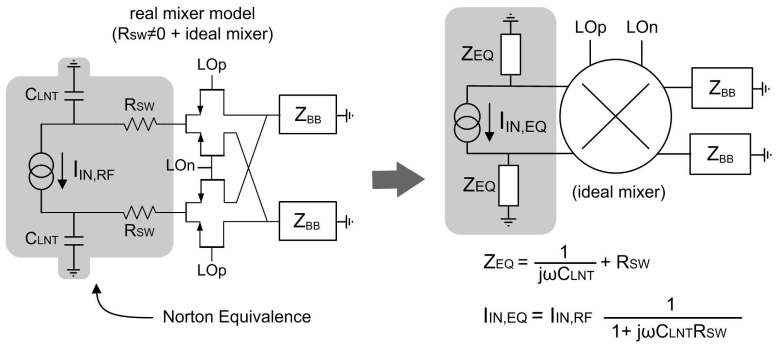


Fig. 7 Finite switches on-resistance R_{SW} case. The equivalent Norton model

C. Useful passive mixer rules

The main purpose of this last subsection is to provide some design numbers, in order to give a direct link between the passive mixer analysis and the design issues of Chapter 4 (describing the E-Filtering ADC and the Rauch use into a cellular receiver chain).

In this sense, it has to be taken into consideration that a reasonable value of C_{LNT} goes from 200fF to 400fF, with the state of the art 40nm and 65nm CMOS technologies. It is due to about 100fF/150fF of switch parasitic (20Ω R_{SW}), 50fF of parasitic of the AC coupling capacitance (2pF, used between the LNT and the mixer) and 50fF/200fF of parasitic of the LNT output stage. The corresponding Z_{EQS}, i.e. the equivalent differential base-band driving impedance, is equal to 1.25(1+j)kΩ/625(1+j)Ω respectively (625(1+j)Ω/312.5(1+j)Ω single ended) for a 2GHz LO. These are not extremely high values, and for sure are smaller than those of an active mixer solution. This requires synthesizing a very low input impedance base-band, to work correctly in current mode. The differential driving impedance of the noise case is 2.5kΩ/1.25kΩ (1.25kΩ/625Ω single ended). This low value can amplify the base-band noise of a not-negligible amount.

Chapter Appendix I

A. Non ideal switch and LO

Section 5.2.A/B made two simplifying assumptions, i.e. R_{SW}=0 and ideal LO phases. It turns out that removing the first one also removes the second since it is possible to demonstrate that the presence of overlap or dis-overlap can be described (with an acceptable error) with an equivalent non-zero R_{SW}.

If R_{SW}≠0, it is no longer possible to directly separate I_{IN} from C_{LNT} at RF (using doubled mixers A and B) but an intermediate step has to be performed (Figure 7). First, the mixer is converted into the cascade of the resistance R_{SW} (placed on the RF side) and an ideal mixer with R_{SW}=0 [60]. Second the RF circuit is substituted with its parallel Norton equivalent (evaluating $I_{IN,EQ}$ and Z_{EQ}). The equivalence is valid if constant R_{SW} during the on-period is considered, so assuming that the circuit is a linear-time-invariant network. At this point the base-band driving impedance equivalent calculation can be performed as in section 5.2.A/B. The RF current generator can be down-converted and substituted with its BB equivalent. For the 50% duty-cycle case the conversion gain from $I_{IN,RF}$ to $I_{IN,BB}$, is still equal to 2/π at low frequency but

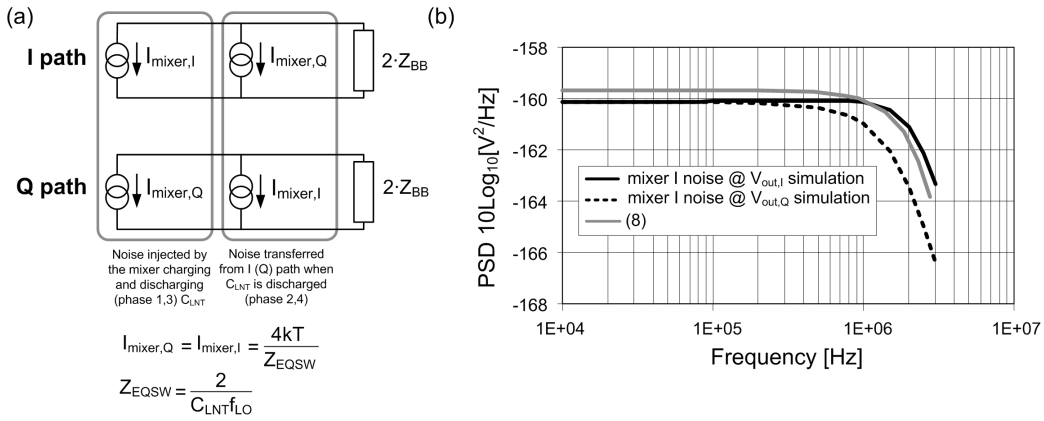


Fig. 8 (a) Mixer switches noise model applied to the Rauch filter base-band. (b) Switches noise PSDs. Spectre PNOISE versus model

shows a low pass shape. When a 25% duty-cycle quadrature LO is used, the gain from $I_{IN,RF}$ to $I_{IN,BB,I\,(Q)}$, is $\sqrt{2}/\pi$, and shows the same low-pass effect too. For typical values of R_{SW}, the effect is negligible for f comparable with f_{LO}. On the other hand, the value of the equivalent impedance evaluated from the BB is affected by the presence of R_{SW}.

B. Mixer switches noise

Extending to the quadrature case the approached proposed in [61] to explain the noise of the mixer switches completes the passive mixer model. Consider the noise of a switch. When a switch is on, it injects its noise both into the I (Q) base-band and into C_{LNT}. The amount of noise charged stored on C_{LNT} at the switch off instant of the transistor depends on the value of the R_{SW}-C_{LNT} time constant with respect to the $1/f_{LO}$ time. This charge is discharged into the Q (I)-I (Q)-Q (I) paths during the next three phases of the LO in which the switch is off. This behavior is the same for all the switches. Due to the symmetric architecture, and assuming Z_{BB}=0 during the discharging phases, the noise of both the I and the Q mixers is perfectly divided into the two base-band paths.

If $1/(2\pi R_{SW}C_{LNT}) >> f_{LO}$, the noise is that of an equivalent switched capacitor resistance. Such a resistance is $Z_{EQSW}=2/(C_{LNT}f_{LO})$ while the model is depicted in Figure 8.a.

The simulated noise PSDs at the differential outputs $V_{out,I}$ and $V_{out,Q}$ due to the I (Q) mixer are shown in Figure 8.b (solid and dashed black line respectively) for the typical sizing. Real switching transistors have been used in the simulation i.e an R_{SW}=20Ω has been assumed and parasitics have been included.

The SC noise model for the mixer switches (Figure 8.a) has been used to evaluate the corresponding predicted noise PSD. Remember that the model considers equal contribution to the I and the Q BB noise from the I (Q) mixer noise. The PSD is:

$$\frac{dV_{out,I}^2}{df} = \frac{4k_B T}{Z_{EQSW}} \left| \frac{R_2}{1 - \frac{f^2}{f_0^2} + j\frac{f}{f_0 Q}} \right|^2 . \quad (8)$$

(8) is reported for comparison in Figure 8.b (gray line). The values of Z_{EQSW} have been evaluated considering also the parasitic capacitance of the switches. Good precision is obtained in the fitting. A higher precision is obtained if the noise (in an un-correlated way) in the I and Q path is summed (about 0.45dB in band integrated error results). If C_{LNT} is varied from 100fF to 800fF and the noise due to the mixer I is computed the integrated in-band noise errors are -0.08/-0.25dB for the I BB and 0.65/2.3dB for the Q BB. The presence of a bigger error in the Q is explained by the ground discharging approximation (Z_{BB}=0) used in the model and is still observed for much worse values of C_{LNT} than expected reasonable ones.

Appendix I

Filtering ADC equivalent discrete time analysis

In Chapter 2 the Filtering ADC narrow-band core is presented exploiting a continuous time model. When the wide-band section of the Filtering ADC is introduced, the need to carry out a more correct discrete time analysis arises. The Filtering ADC (both the core and the complete architecture) has the topology of a continuous time Sigma-Delta. Such converters, in spite of their name, are discrete time circuits, since the quantizer is driven by a clock. An implicit sampling action is so performed in the modulator loop and sampled blocks are discrete time blocks [18, 62].

In this section a discrete time equivalent representation of the Filtering ADC is given. The theory can be generalized to any continuous time Sigma-Delta design (of any order) and is based on the continuous time/discrete time equivalence described by Norsworthy et al. in [19]. An equivalent analysis based on the Impulse Invariant Transformation [18] has been also evaluated but it is not reported here, since very small differences have been observed in the overall modulator behavior in the frequency range of interest.

The main purpose of studying a continuous time Sigma-Delta in a discrete time fashion is to analyze its stability. The sampling in fact introduces an intrinsic delay in the modulator loop, which has to be taken carefully into account to avoid the circuit instability. This delay is mainly due to the comparators time finite response, to the feedback digital logic (i.e. DWA randomizer, see Chapter 3) and to the DACs response. Moreover, the finite bandwidth of the operational amplifiers of the loop filter contributes, since phase delay is time delay. The loop delay is the most critical non-ideality of continuous time Sigma-Deltas [18, 6], since it affects directly the functionality of the converter. Different methods have been developed in literature to compensate the extra loop delay effects, but they have not been tackled here, not to lose the generality of the approach. It is possible to demonstrate that the implementation of a loop delay compensation technique [31] works for the Filtering ADC proposed family as well as for the traditional wide-band Sigma-Delta converters.

Then, a discrete time analysis is useful since a sampled (Z-domain) expression of the signal and of the quantization noise transfer function of the Filtering ADC can be also achieved, to

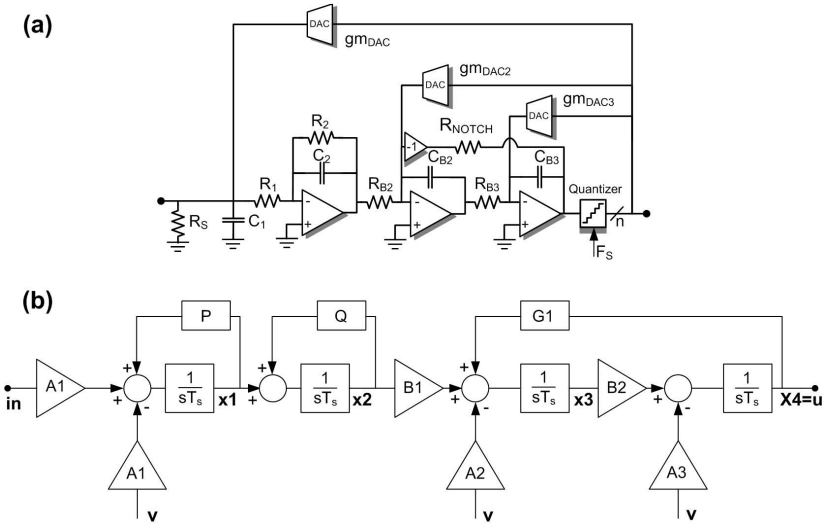


Fig. 1 (a) The Filtering ADC scheme (b) The Filtering ADC integrator based equivalent block diagram

characterize the converter behavior with more accuracy than in the continuous time domain. Notice that this second element is less critical in a filtering approach than in a traditional wide-band one, since the band of interest in a selective system is similar to the desired signal narrow band. Oversampling is in fact used and the sampling dependent effects are intuitively stronger the more the frequency of interest is close to the clock.

The Filtering ADC scheme is reported in Figure 1.a (the damped original solution is shown while the not-damped is obtained moving R_2 to infinite). The clock has a frequency F_S and a period T_S. The theory [19] considers a single-bit quantizer but it has been verified that it works also when a multi-bit sampler is used since it is performed neglecting the quantization error in the amplitude, but focusing only on the discrete time sampling.

The first step of the procedure builds an integrator based equivalent block diagram of the Filtering ADC, as shown in Figure 1.b. The coefficients of the scheme are obtained comparing the transfer functions of the circuit and of the diagram. All the time constants are normalized to T_S. The continuous time models of the DACs are used (Chapter 2). The coefficients are:

$$\begin{aligned} A1 &= \frac{gm_{DAC}T_S^2}{C_1C_2R_1} \qquad B1 = \frac{T_S}{C_{B2}R_{B1}} \qquad P = \frac{-T_S}{C_1(R_1||R_S)} \\ A2 &= \frac{gm_{DAC2}T_S}{C_{B2}} \qquad B2 = \frac{T_S}{C_{B3}R_{B2}} \qquad Q = \frac{-T_S}{C_2R_2} \\ A3 &= \frac{gm_{DAC3}T_S}{C_{B3}} \qquad G1 = \frac{-T_S}{C_{B2}R_{NOTCH}} \end{aligned} \quad . \qquad (1)$$

The only difference with the original circuit is that a voltage normalization of the gain architecture is given, multiplying the input current signal by A1. Moreover, the feedback loop is open, to evaluate the loop gain of the system. The block diagram is useful to get the state-equation description of the modulator, in the time domain. The outputs of the integrators are the state-variables and the Filtering ADC is described by the following continuous time equations [19, pa 158]:

$$\begin{cases} \dot{X} = A_{ct}X + B_{ct}v \\ u = C_{ct}X \end{cases} \qquad (2)$$

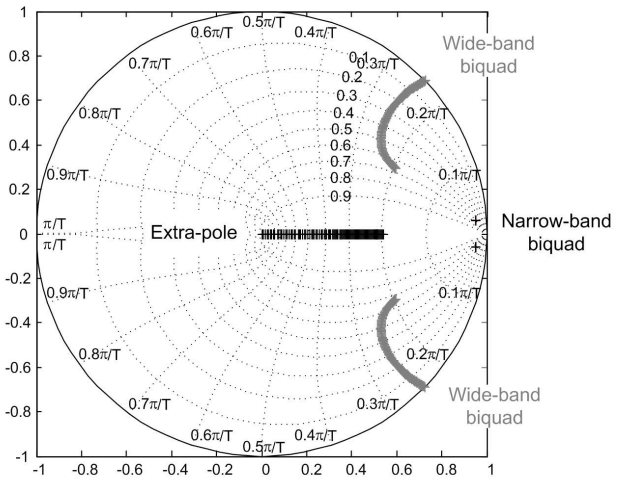


Fig. 2 Closed loop Filtering ADC poles versus the modulator loop delay. Delay from 0 to T_S.

in which X is the state-variables vector X=[x1; x2; x3; x4], $\dot{X}$ is 1st the derivative of the state vector, v is the feedback input signal, u is the output signal and A_{ct}, B_{ct} and C_{ct} are the continuous time matrices of the architecture. The input signal in is not considered since only the loop gain is of interest for the stability.

The continuous time matrices of the structure are:

$$A_{ct} = \begin{bmatrix} P & 0 & 0 & 0 \\ 1 & Q & 0 & 0 \\ 0 & B1 & 0 & 0 \\ 0 & 0 & B2 & 0 \end{bmatrix}; \quad B_{ct} = \begin{bmatrix} -A1 \\ 0 \\ -A2 \\ -A3 \end{bmatrix}; \quad C_{ct} = [0 \quad 0 \quad 0 \quad 1]. \qquad (3)$$

At this point the continuous time system can be transformed in the discrete time domain by solving the state-equation and sampling the solution using the clock reference T_S. The impulse response of the DAC is also evaluated to get the final result. Assuming a simple non-return to zero DAC implementation, which is the most simple to be realized, an equivalent discrete time state-equation modulator is given as follows:

$$\begin{cases} X(n+1) = A_{dt}X(n) + B_{ddt}v(n) + B_{edt}v(n-1) \\ u(n) = C_{dt}X(n) \end{cases}. \qquad (4)$$

Notice that the response of the DAC is divided into a first response multiplied by B_{ddt} (during the n^{th} sample) and a second one multiplied by B_{edt} (during the delayed n^{th}+1 sample) to model the feedback loop delay. The equivalence is performed for the discrete time matrices

$$A_{dt} = e^{A_{ct}}; \; B_{ddt} = A_{ct}^{-1}\left(e^{A_{ct}(1-t_D)} - I\right)B_{ct}; \; B_{edt} = A_{ct}^{-1}\left(e^{A_{ct}} - e^{A_{ct}(1-t_D)}\right)B_{ct} \qquad (5)$$

where t_D is the total loop delay normalized to T_S.

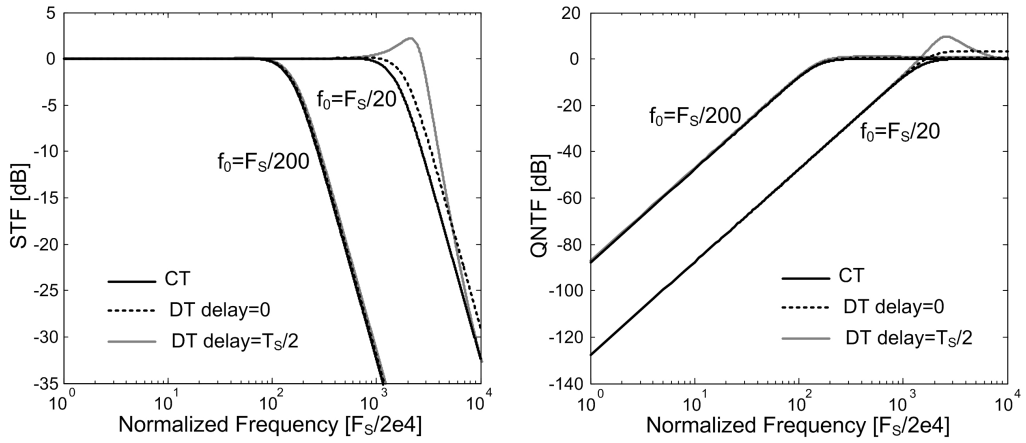


Fig. 3 QNTF and STF for different converter cut-off frequencies and loop delays. A second order wide-band traditional Sigma-Delta is taken as example

Finally the state equation can be moved in the discrete time frequency domain (Z domain) by performing the Z-transform. The $G_{loop}(z)$ of the modulator is defined as:

$$G_{loop}(z) = \frac{u(z)}{v(z)} = \frac{x4(z)}{v(z)} \qquad (6)$$

and through it all the stability performance of the Filtering ADC are displayed, as a function of the loop delay. $1+G_{loop}(z)$ gives in fact the closed loop poles of the Filtering ADC. They can be plotted versus the loop delay to evaluate not only the stability of the block for a given delay and ADC sizing, but also the maximum accepted loop delay that keeps the modulator stable. In this way a stable and robust design can be performed (Chapter 3 and Chapter 4). It is possible to see that increasing the loop delay, the high frequency poles of the wide-band section of the Filtering ADC architecture tends to exit the unitary Z-domain circle, thus making the circuit unstable (example in Figure 2, wide-band biquad). The poles of the narrow-band biquad are almost not modified by the delay and an additional pole (Extra pole) is introduced.

The discrete time quantization noise transfer function (QNTF) and the signal transfer function (STF) of the Filtering ADC, are also given as follows

$$QNTF(z) = \frac{1}{1+G_{loop}(z)}; \qquad STF(z) = QNTF(z) \cdot F_W(z) \qquad (7)$$

where $F_W(z)$ is the transformation in the Z-domain of the $F_W(s)$ transfer function, i.e. u(s)/in(s) (see Figure 1.b) assuming v=0. The QNTF can be used in a design for a preliminary estimation of the modulator noise shaping and of the absolute quantization noise level at the circuit output. It has been verified, through simulations, that even if STF(z) is not perfectly accurate approaching F_S, it remains sufficiently precise in the low frequency range of interest.

The continuous time/discrete time comparison is reported in Figure 3 for a second order traditional continuous time Sigma-Delta ADC (for simplicity). The solid black lines are the continuous time responses. The dashed black lines are the discrete time responses for zero loop delay (ideal). The solid gray lines for a $T_S/2$ loop delay. For a given F_S the cut-off frequency of the ADC is moved from $F_S/200$ to $F_S/20$. As expected (and stated before) in the latter case only the discrete time behavior gives not negligible differences.

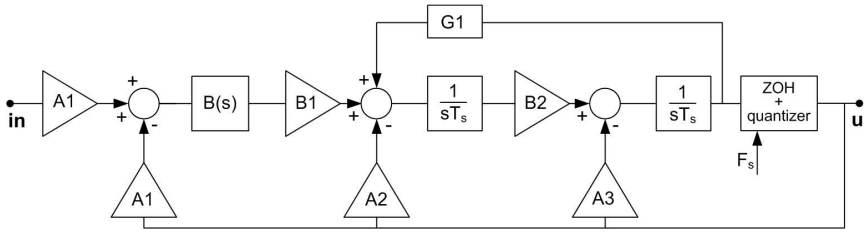


Fig. 4 Simulink model of the Filtering ADC

A Matlab Simulink model has been also built to simulate, using transient analysis, the behavior of the complete Filtering ADC, neglecting the non idealities of the circuit implementation. In this way, the STF, the QNTF and the dynamic range profile (Chapter 1) of the modulator can be achieved reducing of a big amount the simulation time, with respect to the real transistor-level simulations. The Simulink model cannot be used to analyze the thermal noise, but vice-versa considers the quantization noise not only as a white representation (quantizer), and takes into account all the effects of the sampled data behavior (Zero Order Hold, ZOH). The model is shown in Figure 4. B(s) is the continuous time equivalent transfer function of the narrow-band Filtering ADC biquad (the original Filtering ADC architecture) and models also the presence of the finite base-band driving impedance R_S.

Appendix II

Clock jitter noise in the Filtering ADC

Clock jitter noise is probably the most important continuous time Sigma Delta non ideality after the loop delay one. The sampling operated in the quantizer is affected by a timing error, if the clock reference is not pure. The quantitative measure of such a timing precision is given by the clock phase noise, in the frequency domain, and by the corresponding clock jitter noise, in the time domain. The purpose of this section is to briefly explain how the phase noise profile translates into jitter noise, and how much this limits the performance of a Filtering ADC Sigma-Delta (Chapter 2). The analysis can be generalized to the entire family of continuous time Sigma-Delta converters. It has been developed starting from the literature that has faced the jitter issue in the last 15 years [62-73].

An error, in the timing reference of the Filtering ADC internal sampling, generates both an amplitude error and a time error. While the first is high pass shaped by the Sigma-Delta loop

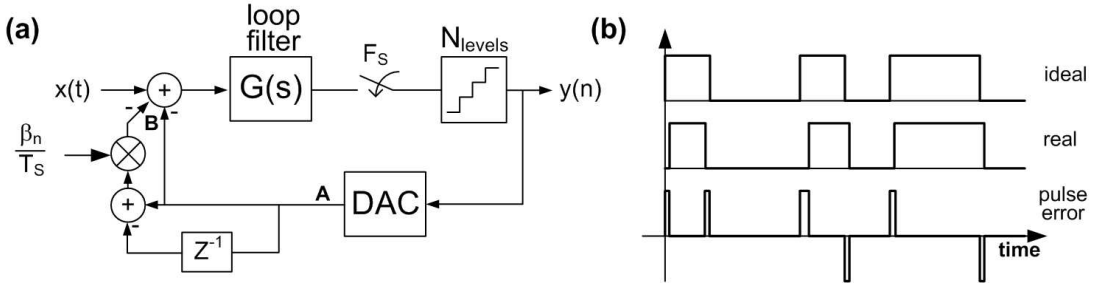


Fig. 5 (a) Clock Jitter noise model of a continuous time Sigma-Delta ADC (b) Feedback waveforms

filter, as it occurs for the quantization noise, and is so negligible, the latter is transmitted at the modulator input node, through the feedback DAC, thus directly affecting the maximum dynamic range achievable by the converter. Figure 5.a reports the model of a continuous time Sigma-Delta converter when clock jitter noise is of interest. The clock frequency F_S in the Figure is assumed ideal. Figure 5.b shows the corresponding feedback path responses, i.e. the ideal one without jitter (A), the jitter noisy one (B), and the real one (A+B). It is known that the use of a shaping of the DAC response can have different effects on the jitter [62-63]. In this case the simplest non-return to zero DAC is considered.

The jitter error is a pulse shaped error (Figure 5.b). It can be simply expressed as follows [63]:

$$e_{NRZ}(n) = [y(n) - y(n-1)]\frac{\beta_n}{T_S} \quad (8)$$

where n is the n^{th} time instant, β_n is the n_{th} timing error, y is the signal sampled in the loop and T_S is the clock period. A single-bit feedback is assumed at this level. The sampled signal y is the sum of two quantities [64]; the first is the signal due to the quantization error, the second is the effective signal (desired in-band one and interferers). Both are evaluated at the output of the modulator. Due to this, in the following, the jitter noise contribution is divided into two sub-sections. From one hand the jitter noise contribution due to the quantization noise is considered (jitter quantization noise), then the signal dependent contribution is described (jitter skirts noise). Jitter quantization noise is typical of a continuous-time Sigma-Delta modulator, it has to be considered also in the absence of input signal and depends on the number of levels of the quantizer. Jitter skirts noise is equivalent to the noise introduced by each sampler, even outside a Sigma-Delta loop and can be not-negligible in the presence of high interferers.

Quantization noise jitter is traditionally tackled in literature [62-63] [65-68]. The pulse error described in (8) is re-written as:

$$e_{NRZq}(n) = [q(n) - q(n-1)]\frac{\beta_n}{T_S} \quad (9)$$

in which q is the quantization noise dependent signal. The corresponding error variance is:

$$\sigma^2_{enrzq} = \sigma^2_y \frac{\sigma^2_\beta}{T^2_S}. \quad (10)$$

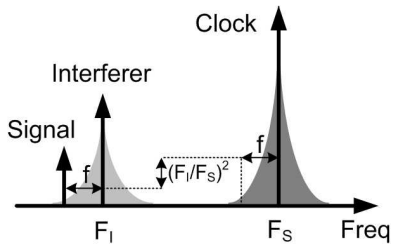


Fig. 6 Clock Jitter phase noise skirts spurious effect

σ_β is the standard deviation of the timing error β_n and σ_y^2 takes into account the probability distribution of the quantization signal, i.e. is linked to the probability of having or not a transition between the output quantizer levels. This is a key element since only the presence of a transition introduces jitter noise ((9)).

From literature different expressions of quantization jitter noise are reported, and they mainly come from intensive time domain simulations. The differences among them rely on the σ_y^2 value. In [63] it varies from 2.8 to 4.5, in [62] it is 2.8, in [65] it is 1, in [66] it is 3, in [64] and [67] it is 1.2 and in [68] it is 3.7. Due to the more than 6dB variation of the presented results, the worst case value 4.5 has been chosen for the evaluation used in Chapter 4. According to the analysis proposed in [69] and [64] the quantization noise jitter could be also evaluated analytically starting from (9). The procedure has been implemented using Matlab and a factor 6.2 for σ_y^2 has been obtained.

The final expression achieved for the estimation of the quantization jitter noise contribution, measured in V^2 and integrated in the signal band of interest, at the output of a Filtering ADC (continuous time Sigma-Delta) is:

$$\overline{V_{OUT,QUANT\_JITTER}^2} = 4 \cdot (V_{REF})^2 \cdot \sigma_y^2 \frac{\sigma_\beta^2}{T_S^2} \cdot \frac{1}{OSR} \cdot \frac{1}{N_{levels}^2}. \qquad (11)$$

The factor 4 takes into account the differential implementation, V_{REF} is the single ended reference voltage of the quantizer (internal ADC), N_{levels} is its number of levels, and OSR is the oversampling ratio of the Sigma-Delta.

The literature explains also how the jitter variance $(\sigma_\beta/T_S)^2$ can be obtained from the phase noise profile of the clock reference. In this context the period jitter is of interest (i.e. the variance of the difference of each period with respect to the ideal period T_S) and the formula is:

$$\frac{\sigma_\beta^2}{T_S^2} = \frac{2}{\pi^2} \cdot \int_0^{F_S/2} L(f)\, \mathrm{sen}^2(\pi f T_S) df. \qquad (12)$$

L(f) is the double side band phase noise profile of the clock and, being the phase noise evaluated at sampled instants, the integration limit is $F_S/2$ [70-73].

Jitter skirts noise is due to the fact that the clock spectrum phase noise skirts are reported over the sampled signal, thus increasing the noise floor and affecting the SNR. The most critical situation is the presence of a high power interferer, since the phase noise skirts of the sampled blockers fall in-band corrupting the weak desired signal. This case is depicted in Figure 6. When sampling a signal at frequency F_I, the phase noise skirts "pass" on the signal attenuated by the factor $(F_I/F_S)^2$ [70]. The final expression achieved for the estimation of the jitter skirts noise

contribution, integrated in the signal band of interest, at the output of a Filtering ADC (continuous time Sigma-Delta) is so:

$$\overline{V^2_{OUT,SKIRTS\_JITTER}} = \int_{F_1}^{F_2} L(f)\,df \cdot \frac{V^2_{OUT,I}}{2} \cdot \left(\frac{F_I}{F_S}\right)^2 . \qquad (13)$$

in which $V_{OUT,I}$ is the peak differential amplitude (measured in V) of the interferer at the sampling interface and F_2-F_1 is the RF channel band of interest. Notice that the Filtering solution, with respect to a wide-band one, benefits of the filtering, since $V_{OUT,I}$ corresponds to a filtered amplitude.

(11) and (13) have been used during the GSM-UMTS analysis shown in Chapter 4. They provide only a first level estimation of the jitter issue in a Filtering ADC, but the result is still sufficiently accurate for the purpose of the study. The main difficulty in the simulation is the very long simulation time required to model and to detect with accuracy a small timing error in comparison to the large numbers of clock periods required to get an acceptable statistic.

Conclusion

In the application field of wireless receivers, Software Defined Radio oriented architectures are arising great interest. Even if a full-silicon, fully digital, reconfigurable and multi-standard radio is still unfeasible, over the last decade different structures have been facing the issue to handle critical RF scenarios in a low-cost fashion.

In this thesis two architectures of Filtering Analog to Digital converter, able to represent the entire analog base-band of a wireless receiver chain, were presented. Their main benefits are two. On one hand they move the analog to digital interface after the down-conversion mixer, to exploit the lowest-cost scalable and highly reconfigurable digital processing as soon as possible in the reception. On the other hand they attempt to reduce the bill of material, which is bulky and expensive, due to an intrinsic blockers resilient and high performance nature.

In Chapters 1 and 2 the Filtering ADC based receiver was introduced as a concrete step to the CMOS software defined radio. New definitions of signal to noise and distortion ratio and dynamic range were given to address the frequency dependent environment which is object of interest. Besides the Filtering ADC topology and its E-Filtering ADC evolution were described.

Chapters 3 and 4 showed three different applications of the proposed base-band. First the Filtering ADC was used as the complete analog base-band of a digital terrestrial television (DTT) tuner (Marvell Semiconductor). The receiver exploits the Filtering ADC benefits to handle both the European DVB-T standard and the ATSC American one, thus facing a worldwide market. Second, the ability of an E-Filtering ADC based receiver chain to detect the desired information in the challenging cellular environment was demonstrated through simulations. Third, a GSM-UMTS multi-standard chain, embedding the E-Filtering ADC Rauch filter counterpart, was integrated and measured.

In Chapter 5 the RF/base-band interface issues, if the down-conversion stage is realized with a current driven passive mixer, were tackled. A mixer intuitive model, able to predict the equivalent base-band driving impedance for both the noise and the signal transfer function, was described and verified through simulations, showing good accuracy.

Appendix I and Appendix II dealt with the discrete time equivalent representation of the Filtering ADC and with the clock jitter noise issue of the presented base-band.

The DTT and the GSM-UMTS base-band prototypes were fabricated in 90nm and 40nm CMOS technology. In both cases a comparison with the state of the art was provided, showing a performance in line or even better. In this sense the Filtering ADC analog base-band was proposed as a smart and low-power further step, with respect to the existing solutions, in the direction of improving the immunity of receivers to high power blockers.

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