Università degli Studi di Pavia

Facoltà di Ingegneria
Dipartimento di Ingegneria Industriale e dell'Informazione
Dottorato di Ricerca in Microelettronica
XXV Ciclo

Analog and Digital Blocks for Calibration and Readout of Active Pixel Sensors with Advanced Functionalities

Tutor:
Chiar.mo Prof. Valerio Re

Coordinatore del Dottorato:
Chiar.mo Prof. Franco MALOBERTI

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Emanuele QUARTIERI

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Contents

Introduction

This thesis discusses the design and the measurement results of two analog and digital building blocks for calibration and readout of semiconductor pixel detector for particle tracking and vertexing in high energy physics experiments as well as for X-ray imaging, in particular for synchrotron light sources and XFELs. A high accuracy injection circuit for pixel-level calibration of readout electronics is discussed in the firs part of the work. In hybrid pixels the sensor matrix is connected to a front-end Application Specific Integrated Circuit (ASIC) by small conducting bumps applied using bump-bonding technology, whereas in monolithic pixels the amplifying and logic circuitry as well as the radiation detecting sensor are integrated in the same chip. In both cases, pixel sensor readout chips require a fine-tuning of front-end analog parameters at pixel-level, such as sensitivity, noise, discriminator offset and threshold dispersion. In the second part of the work a fast data link for serial data communication is illustrated. Both blocks will be part of an ASIC, known as DSSC chip [3], to be fabricated in a 130 nm CMOS commercial process by IBM with maximum supply voltage V_{DD}=1.2 V. The DSSC device will be used for the readout of a novel non-linear DEPFET Sensor with Signal Compression (DSSC) [4] developed for X-ray imaging at the European X-ray Free Electron Laser (XFEL) facility under construction in the Hamburg area (Ger-

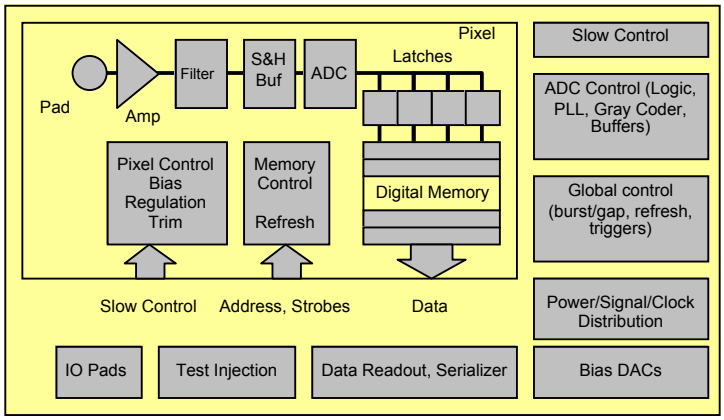

Figure 1: Building Blocks of the Pixel Chip.

many) [5]. The DSSC chip, which will be connected to the sensor throughout bump bonding technique, is composed of 64×64 channels with a pixel size of 236 μm $\times$ 204 μm. Each pixel includes a readout channel which is comprised of an analog input stage with filtering, an 8-bit Wilkinson type (single slope) ADC and a large SRAM memory.

Fig. 1 shows a simplified overview of the most important building blocks of the chip.

In a Hit/No hit readout channel, including, in its most common version, a charge preamplifier and a shaping filter followed by a discriminator, the measurement of the main analog parameters can be performed by measuring the firing efficiency of the discriminator. To do this a charge scan procedure or a threshold scan technique may be employed. In both cases a well-known signal must be injected at the channel input and the noise contribution of the injected signal must be negligible with respect to the noise of the readout channel to be measured. In multichannel readout circuits for radiation detectors where a digital-to-analog converter enabling the reduction of the possible channel-to-channel threshold non-uniformities is included, a high accuracy injected signal must be used also for trimming the discriminator thresholds. Analog testability and trimming of the chip can be achieved by an internal calibration circuit which makes it possible to inject a well-known signal into each indi-

vidual readout channel without accessing the input pads. The features of the injection circuit can be exploited in particular in hybrid pixels where full electrical functionality tests and measurements of main analogue parameters of the front-end have to be performed in different phases of the module assembly: wafer level, testing after assembly of chips on hybrids, hybrid testing after burn-in, testing of complete modules after assembly with silicon sensors. These simple procedures can be an issue in a high-granularity large pixel matrix with complex signal processors. Two test prototypes has been realized, a detailed description of the circuit has been provided in [1], while experimental results coming from the characterization of the first fully functional test structure have been presented in [2]. In this thesis, chapter 1 will discuss the design and the characterization of the last version of the prototype, focusing on the performance of the circuit in terms of linearity, noise and timing. Chapter 2 will present the performance of the injection circuit in the working condition foreseen for the DSSC chip. The same chapter will describe an improved version of the injection circuit designed for the new requirements for the DSSC chip calibration. Presently a prototype of this circuit is not yet ready, but it is submitted to the foundry. Because of this simulation results are shown in chapter 2 and they are compared with the results obtained for the injection circuit described in chapter 1. For data communication between the DSSC chip and the FPGA used for data acquisition, an LVDS communication link is used. The second buildings block discussed in this work is a fast data link for serial data communication from the DSSC chip and the FPGA hosted in the data acquisition module of the detector

In chapter 3 the design of an LVDS transceiver will be presented. This same chapter also presents the measurement results of a prototype with an integrated full LVDS transceiver.

Chapter 1

Injection circuit for detector readout calibration

1.1 Circuit architecture and specifications

The injection circuit presented in this work is a building block of an ASIC, known as DSSC chip [3], to be fabricated in a 130 nm CMOS commercial process by IBM with maximum supply voltage V_{DD}=1.2 V. The DSSC device will be used for the readout of a novel non-linear DEPFET Sensor with Signal Compression (DSSC) [4] developed for X-ray imaging at the European X-ray Free Electron Laser (XFEL) facility under construction in the Hamburg area (Germany) [6]. The DSSC chip, which will be connected to the sensor throughout bump bonding techniques, is composed of 64 $\times$ 64 channels with a pixel size of 236 μm $\times$ 204 μm. Each pixel includes a readout channel which is comprised of an analog input stage with filtering, an 8-bit Wilkinson type (single slope) ADC and a large SRAM memory. The injection circuit developed in this work is also included and will be used for health-check and calibration purposes. Besides this specific project, the injection circuit, it can be easily adapted to other applications and its architecture can be described by referring to a generic $n \times m$ pixel matrix as shown in Fig. 1.1. The injection circuit, as shown in Fig. 1.1, consists of two main parts: an 8-bit high-accuracy current steering DAC (with an additional bit for gain setting), which is located in

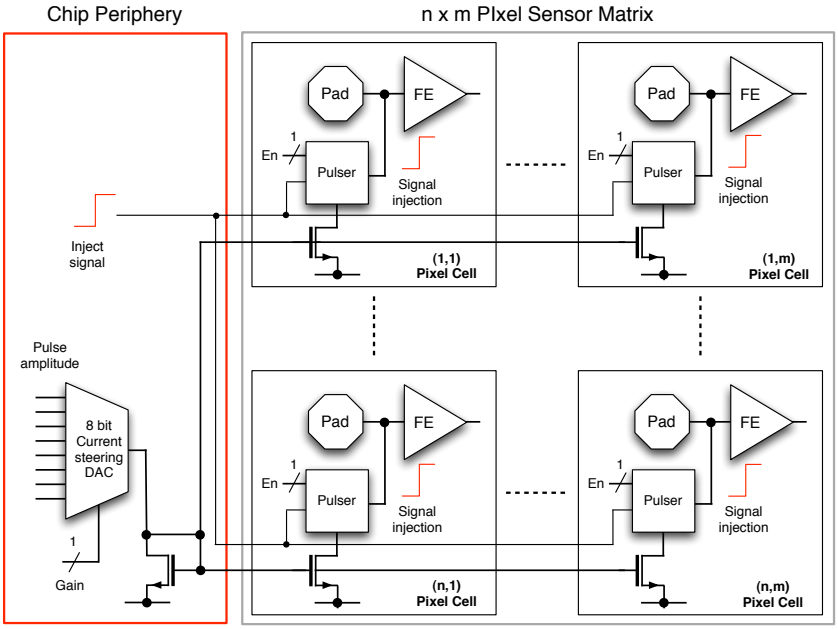

Figure 1.1: Conceptual block diagram of the injection circuit architecture comprising the 8-bit current steering DAC, in the chip periphery, and the pulser, in each pixel cell.

the matrix chip periphery and is suited to the purpose of setting the pulse amplitude, and the Pulser, one in each pixel cell. The current provided by the DAC is mirrored into each pixel, where the Pulser circuit generates a signal corresponding to the one delivered by the detector and feeds it into the input of the front-end (FE).

There are two fundamentally different topologies for the readout of the DEPFET devices as shown in Fig. 1.2 : Source Follower Readout (SFR) mode and Drain Current Readout (DCR) mode. The signal from the DEPFET is a voltage step (resulting in an injected charge by means of a 0.5 pF coupling capacitor integrated on the detector itself) in the SFR mode and a current step in the DCR mode. In order to evaluate the best choice for the DSSC project, both methods have been investigated in the early part of the DSSC design. As a consequence, the injection circuit is required to inject either a

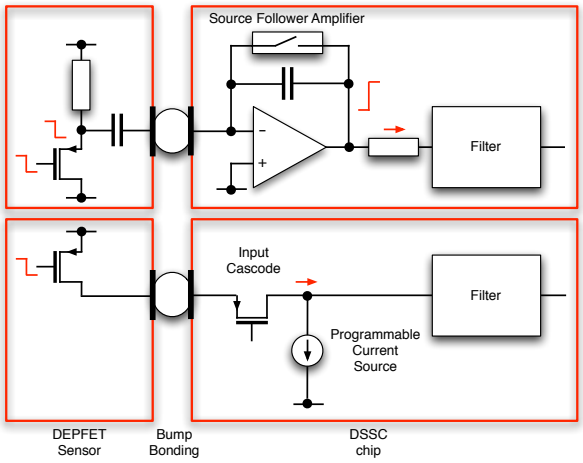

Figure 1.2: Simplified schematic view of the SFR mode (upper design) and DCR mode (lower design) of the DEPFET sensor.

charge or a current at the input of the front-end electronics. To comply with this requirement two Pulser architectures for the two different options of the analog front-end have been designed:

- **Charge Injection Pulser** (to be used in SFR mode): the circuit feeds a charge at the input of the preamplifier for charge-sensitive amplification;
- **Current Injection Pulser** (to be used in DCR mode): the input of the readout electronics is fed with a known current provided by the injection circuit. This solution can be used both for transresistance readout and for charge amplifier calibration by steering the current into the preamplifier input during a fixed time interval.

Signals corresponding to up to 10^3 photons at 10 keV or 10^4 photons at 1 keV are foreseen for a single pixel. Moreover, single photon resolution for 1 keV photons is required. To comply with this huge dynamic range, while maintaining single photon resolution, a new type of non-linear DEPFET sensor has been developed (A complete description of the sensor will be provided in appendix A). At low dynamic range the DEPFET output response is almost linear and

the gain is about 2.8 $\mu V/e^-$ for the SFR mode and 360 pA/e^- for the DCR configuration [7]. The injection circuit is required to cover the full dynamic range of the signals delivered by the DEPFET sensor with the necessary resolution. The requirements taken into consideration in the design of the circuits are summarized in the following list:

- The first 1 keV photon (generating a charge of 277 electrons) collected by the pixel produces a voltage step at the source of the DEPFET of about 0.8 mV (corresponding to an injected charge of 0.4 fC by means of the 0.5 pF coupling capacitor) in SFR mode and a current step at the drain of the DEPFET of about 100 nA in DCR mode.

- At the end of the input range (corresponding to $8{\cdot}10^3$ photons at 1 keV) the sensitivity of the sensor is reduced and, according to device simulation results, the expected output swing is about 220 mV (corresponding to 110 fC) in SFR mode and 25 μA in DCR mode [4],. The injection circuits must cover the entire range.

- In DRC mode, the pulser is required to emulate the DC bias current of the DEPFET in a range from 10 μA to 150 μA.

- The injection circuit is also required to allow for simultaneous stimulation of several pixels in a freely programmable spatial pattern, that is, signal injection into each pixel can be enabled or disabled. This feature has been implemented with a local control bit (`En`) set by means of the so called inject mask loaded into the matrix. The mask consists of 64×64 bits; bits are pushed into the matrix by means of a shift register which connects all the pixels in a row-by-row fashion. The inject mask bit is fed to the matrix within an inject mask clock period.

To meet the requirements concerning the range and resolution (at least 1 point into the lowest energy level) of the injected signal, 9 bits are mandatory to set the amplitude of the signal. In order not to increase the complexity and area of the current steering DAC we have decided to use an 8-bit DAC and an additional bit for selectable gain has been introduced. In the low gain setting,

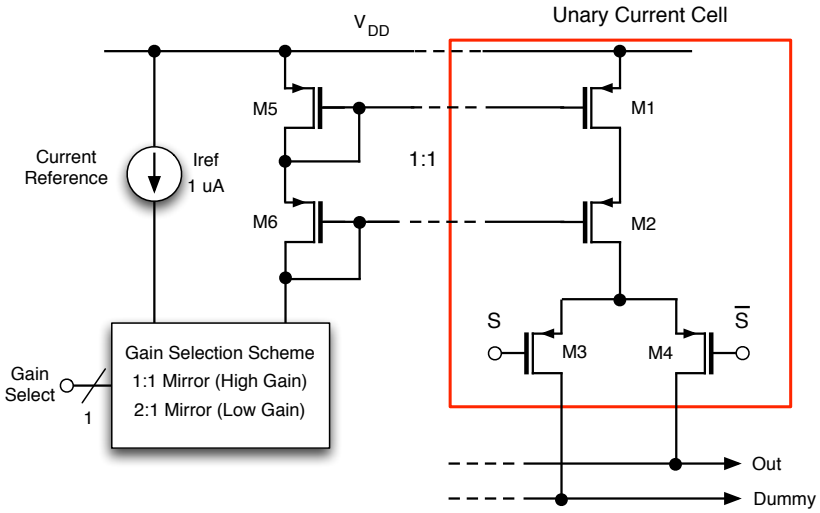

Figure 1.3: Switching scheme for the unary current source.

the injection circuit provides high resolution with a reduced range while in the high gain setting a reduced resolution with a large range is available for injection.

1.2 8-bit Current steering DAC

The *8-bit* Current Steering D/A Converter, which is responsible for setting the amplitude of the signal to be injected, is based on a unary current source architecture. It switches k out of 2^8-1 unity current generators toward the output node or to a dummy load, as show in Fig. 1.4, under the control of the *8-bit* digital input. The current generated by the reference cell is mirrored into each unary cell by means of a 1:1 cascode current mirror scheme. The reference provides a current I_{ref}=0.5 μA in the low gain configuration and I_{ref}=1.0 μA in the high gain setting, which can be selected by a control bit and the circuit in Fig. 1.4. A reference current provided off-chip is mirrored into the reference cell of the DAC. By the switches shown in the Fig. 1.4 that current can be doubled, so the high gain setting can be selected. The current of the unary cell is sent to the output when phase `S` of the current-steering switches is high, or

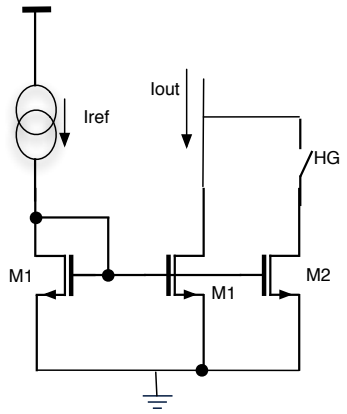

Figure 1.4: Schematics of gain selection scheme.

to the dummy load when `S` is low.

1.2.1 Unity current generator

The current cell, consisting of a cascoded current source (M_1, M_2) and current-steering switches (M_3, M_4), is shown in Fig. 1.3, together with the current reference cell. The current generated by this cell is mirrored into each unary current cell by means of a 1:1 cascode current mirror scheme. The current-steering switches send the current of the cascode current mirror to the output when phase S is high, and routes the current to the dummy load when S is low. As compared to a solution in which a single MOSFET switch, in series with the output, is used to turn on and of the current generator, this switching method avoids pushing the transistors into the triode region when the current generator is not being used and keeps the transistors in saturation.

1.2.2 DAC architecture

The 255 current cells of the converter are arranged in a 16×16 array. Two additional layers of dummy cells surrounding the active cells were added to avoid boundary effects. Two different architectures have been considered to

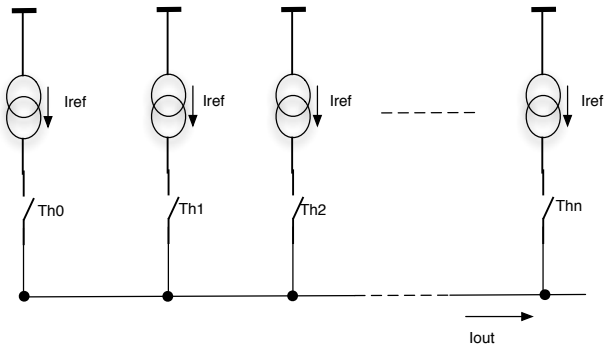

Figure 1.5: Scheme of Unary cells DAC, binary to thermometric converter was omitted.

switch the 16×16 array of matched unity current sources: the unary decoded and the binary weighted architecture.

The Unary Decoded Architecture [8]

This architecture transforms the binary input code into a thermometric code to switch the unity current generators one by one as shown in Fig. 1.5 where the control signals Th_n are the output of the binary to thermometric converter. The great advantage of this solution is the intrinsic monotonicity. In fact increasing the input code increases the number of unary current generators connected to the output, so that monotonicity is insured. In Fig. 1.6 an example of unary cells layout for this architecture is shown. In order to reduce the complexity of the bin-to-thermo converter some logic is included in every cell. To reduce mis-match it is necessary to arrange the current generator matrix in a random pattern, in order to avoid gradient effects. So an out-of-matrix binary-to-thermo converter have is used, and 255 lines have to be routed over the matrix increasing of the complexity of the circuit.

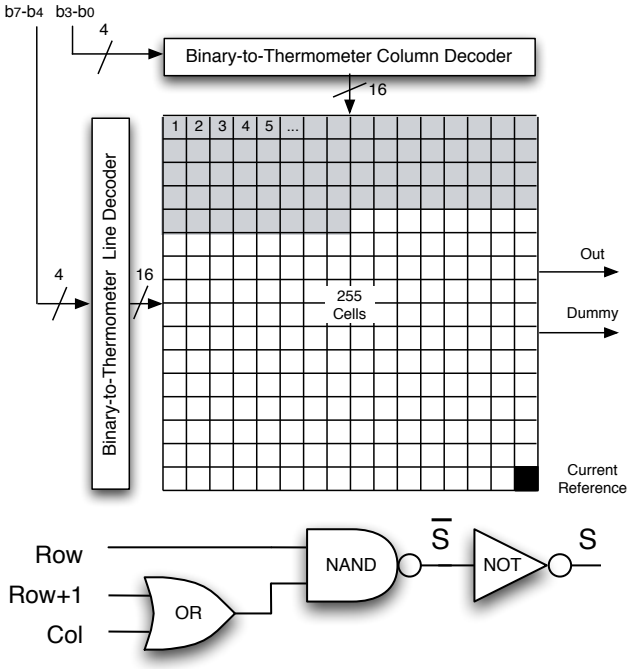

Figure 1.6: A principle scheme of a unary current architecture (top), with the control logic (bottom).

The Binary Weighted Architecture [9]

It consists of 8 current generators each one combining 2^{k-1} unity current sources in parallel ($0 \leq k \leq 7$) and uses the *k-th* bit to switch the entire parallel connection to the output node or to the dummy load. The advantage of such an approach is its simplicity: the digital inputs directly control the switches and no decoding logic is required in the unit current source or in the periphery of the matrix, resulting in a reduced area with respect to its unary decoded architecture counterpart. In the actual implementation the layout is realized using 255 unity generators arranged in a common-centroid layout to reduce the effects of doping gradients, with the reference current generator at the center of the array, as shown in Fig. 1.8.

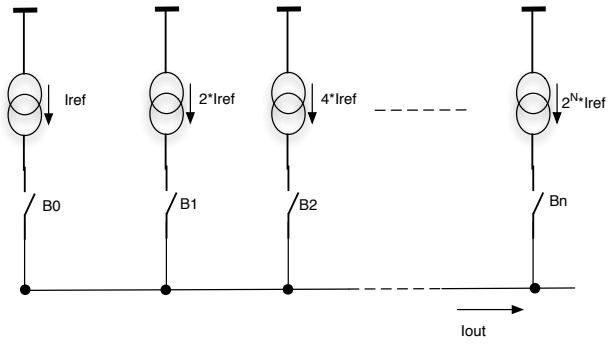

Figure 1.7: Principle scheme of binary weighted architecture.

1.2.3 DAC Specification

For a current-steering DAC, the INL is mainly determined by the matching behavior of the current sources. Inaccuracies on the generated currents can be caused by random and systematic variations of device parameters. Both effects have been taken into account in the DAC design. One source of systematic non linearity is the finite output impedance of the current source: when the input

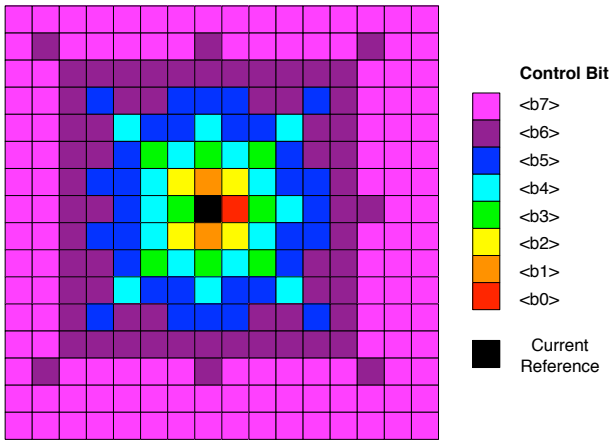

Figure 1.8: Flor plan of the 8 current sources in the binary Weighted Architecture.

code varies between zero and the full scale an increasing number of current sources are connected in parallel, resulting in a decreasing impedance at the output node. This effect on the output current has been reduced by means of a cascoded current source in the unary current cell, which increases the output impedance. Moreover, the random error of the current source, which is mainly given by device mismatch, has been considered in determining the dimension of the critical unit current cell transistor M_1. A parameter that is well suited for expressing the relation between technology parameter variations and DAC-specifications is the INL yield, which is defined as the ratio of the number of D/A converters with an INL smaller than 0.5 LSB to the total number of tested D/A converters. Assuming a normal distribution for the unit current sources, the required accuracy on these current sources is given by [10]:

$$\frac{\sigma_{I_{LSB}}}{I_{LSB}} \leq \frac{1}{2C\sqrt{2^N}} \tag{1.1}$$

where $\sigma_{I_{LSB}}/I_{LSB}$ is the relative standard deviation of the unit current source, N is the resolution of the DAC and C is a coefficient depending on the yield according to the inverse of the cumulative normal distribution function [10]. For a yield of 99.7% a value of C=3.1 has been found, resulting in a required relative current matching $\sigma_{I_{LSB}}/I_{LSB} \leq 1\%$ for an 8-bit DAC. As far as CMOS processes are concerned, differences in the threshold voltage V_{Th} and in the current gain factor β are the predominant mismatch sources in closely spaced, identical-by-design MOS transistors. In the widely accepted model of V_{Th} and β mismatch, the variation in the MOSFET threshold voltage and in the current gain factor have a normal distribution with zero mean and a variance inversely proportional to the device gate area WL. Using this mismatch model, the relative standard deviation of the unit current source $\sigma_{I_{LSB}}/I_{LSB}$ can be expressed in terms of the process-matching parameters and the transistor biasing according to the following equation [11]:

$$\frac{\sigma^2_{I_{LSB}}}{I^2_{LSB}} = \frac{4A^2_{V_{Th}}}{WL(V_{GS} - V_{Th})^2} + \frac{A^2_{\beta}}{WL\beta^2} \tag{1.2}$$

where V_{GS} is the gate-to-source voltage of the transistor, $A_{V_{Th}}$ and A_β are proportionality constants obtained from the characterization of a statistically significant number of device pairs and generally provided by the foundry together with the device models. Based on this mismatch model, the active area W_1L_1 of the unit current cell transistor M_1 is derived. Once the gate-to-source voltage V_{GS} has been established in order to bias the transistor in strong inversion, the current I_{LSB} can be used to calculate the aspect ratio W_1/L_1 of the LSB current source device according to the square-law model of the drain current:

$$I_{LSB} = \frac{1}{2}\beta\frac{W}{L}(V_{GS} - V_{Th})^2 \tag{1.3}$$

Based on these indications and on results coming from Monte Carlo analysis of the device, the transistors dimensions was chosen.

1.3 Charge Injection Pulser

The charge pulser injects a charge directly into the input of the source follower amplifier by applying a voltage step to an injection capacitor C=500 fF as shown in Fig. 1.9. The current from the 8-bit current steering DAC is mirrored into each pixel by means of a 10:1 mirror. Therefore, the mirrored current is found to be I_{LSB}=50 nA in the low gain and I_{LSB}=100 nA in the high gain configuration of the 8-bit DAC. By means of the inject signal control bit, this current is switched from the left branch of the differential stage to the right one to produce a negative voltage step applied to the injection capacitance C. The injected charge can be obtained by the following equation

$$Q_{inj} = k \cdot C \cdot R_B \cdot \frac{I_{DAC_{LSB}}}{10} \tag{1.4}$$

where $1 \leq k \leq 255$ is the input DAC code. In order to fit the requirements on resolution and dynamic range of the injected charge, a resistor R_B=8 kΩ has been chosen. Charge injection into each pixel cell can be disabled by opening a switch in series with the injection capacitance. The status of the switch is established by a local control bit which, in turn, is set by means of the kill mask

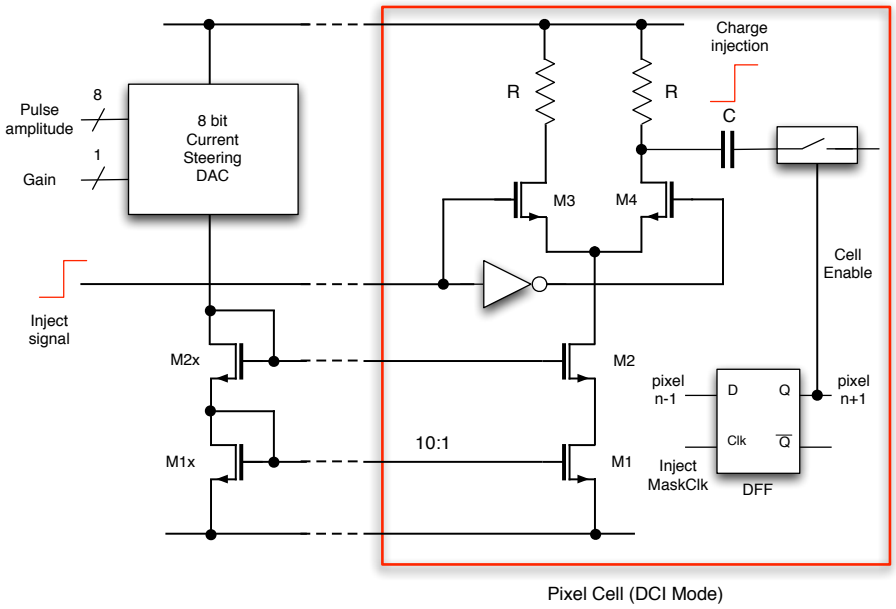

Figure 1.9: Simplified block diagram of the charge injection pulser architecture.

loaded into the matrix of 64×64 pixels; the bits of the mask are pushed into the matrix by means of a shared shift register realized with 4096 edge triggered Flip Flop Delay (FFD), one in each pixel, and connecting all the pixels in a row-by-row fashion; the inject mask is fed to the matrix by means of the kill mask clock, at the rate of one bit per clock period. Charge injection into each pixel cell can be disabled by opening a switch in series with the injection capacitance. The status of this switch is established by a local control bit which, in turn, is set by the `InjectMask` loaded into the matrix of pixels. The bits of the mask are pushed into the matrix by a shared shift register realized with one edge triggered Delay Flip Flop (DFF) in each pixel, and connecting all the pixels in a row-by-row fashion. The `InjectMask` is fed to the matrix by means of the `InjectMaskClock`, at the rate of one bit per clock period.

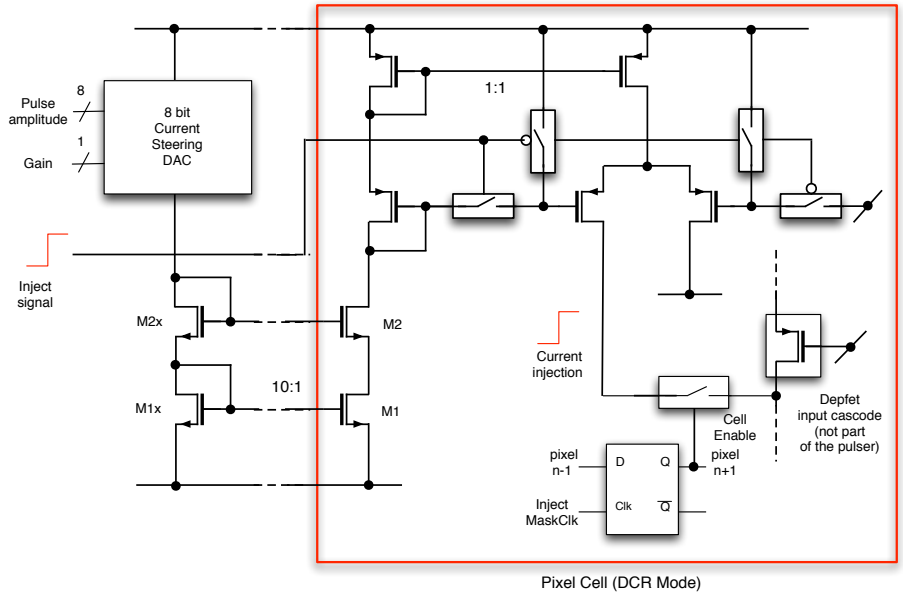

Figure 1.10: Block diagram of the Current injection pulser architecture.

1.4 Pulser for Current Injection

The pulser injects a current step into the drain of the input cascode. It has to be noticed that since the voltage reference at the gate of the DEPFET input cascode is kept at about 1.0 V, there is no voltage room to inject current exactly in the same point as the sensor, that is at the source of the input cascode, so the only possible solution is to inject a current into the drain of the input cascode, which is a low impedance virtual ground thanks to the amplifier of the filtering stage of the front-end. As shown in Fig. 1.10, the current from the 8-bit current steering DAC is mirrored into each pixel by means of a 10:1 cascode current mirror. Once inside the pixel the current is mirrored once again by means of a 1:1 mirror to obtain the right polarity of the signal to be injected. The inject signal control bit allows for switching the mirrored current from the right branch of the differential stage to the left one to produce a current step applied to the drain of the input cascode. Due to the very low voltage budget (≈200 mV), a circuit solution has been adopted in which the cascode current

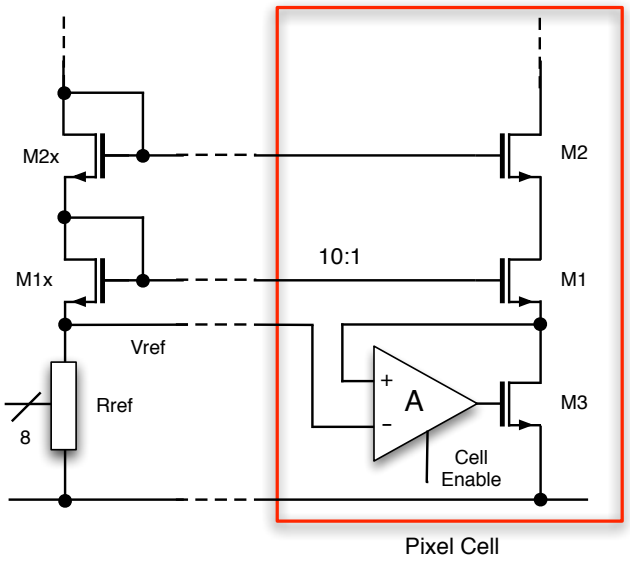

Figure 1.11: Schematic of the circuit used for the compensation of the voltage drop on the ground line.

mirror and the differential switch share a transistor.

1.5 Voltage drop compensation circuit

In the injection circuit developed in this work, the current provided by the 8-bit DAC in the chip periphery is mirrored inside each pixel cell, where a Charge Injection or a Current Injection Pulser can be used depending on the front-end to be calibrated. In order to have a good mirror factor, transistors placed in close proximity are usually recommended. On the contrary, transistors which are hundreds of microns apart are affected by several sources of mismatch. This is the case of a large sensor matrix. In particular, the voltage drop along the ground line is responsible for a mismatch in the gate-to-source voltage V_{GS} between the reference and the current source resulting in a degraded mirror factor. In the pixel matrix of the DSSC chip the power lines are distributed by rows, and the current of the 8-bit DAC must be mirrored in the whole matrix of 64×64 pixels, featuring a ≈200 μm pitch. If we assume that a separate ground

line is used for the mirror, with the converter close to the first cell of the row, then the voltage drop ΔV_n in the ground line of the n^{th} pixels is equal to:

$$\Delta V_n = \sum_{i=0}^{n} ik \frac{I_{DAC_{LSB}}}{10} R_{cell} \approx \frac{1}{2} k \frac{I_{DAC_{LSB}}}{10} R_{cell} n^2 \tag{1.5}$$

where $1 \leq n \leq 64$ is the column number, $I_{DAC_{LSB}}$ is the value of the DAC current for the LSB, $1 \leq k \leq 255$ is the coefficient accounting for the amplitude setting of the injected signal and R_{cell} is the resistance of the metal line within two adjacent pixels. In our application, a value of $R_{cell} \approx 0.5\ \Omega$ has been estimated, therefore generating a voltage drop on the ground line of the 64^{th} cell of each row of about $\Delta V_{64} \approx 30$ mV in the worst case, that is, in the high gain configuration where the current mirrored inside each pixel is 100 nA and for the maximum amplitude of the injected signal $k=255$. This voltage drop causes that the first and last pixels in each row get different reference currents. Moreover, it has to be noticed that, according to equation (1.5), the voltage drop is a function of the 8-bit DAC code k. Therefore, the voltage drop on the ground line has a detrimental effect also in terms of linearity, more markedly so for the cells far away from the side of the chip periphery where the DAC is located (see Fig. 1.1). In the proposed injection circuit, this problem has been completely overcome by means of a novel Voltage Drop Compensation circuit whose schematic, shown in Fig. 1.11, is comprised of R_{ref} resistor, the amplifier and the M_3 transistor. If the voltage gain A of the amplifier is sufficiently high, and its offset voltage negligible, then the source terminals of transistors M_{1x} and M_1 are kept at about the same reference voltage V_{ref} so that the current mirror is almost unaffected by the voltage drop on the ground line.

In Fig. 1.12 the designed amplifier is shown. In order to reduce the output voltage the input transistors (M_1, M_2) designed a with WL in agreement with [11] and a second stage (M_5, M_6) were added to achieve a sufficient high voltage gain.

In order to generate the voltage reference V_{ref} the circuit show in Fig. 1.13 is used. The current provided by the current steering DAC can be written as a function of the control bit in the following equation

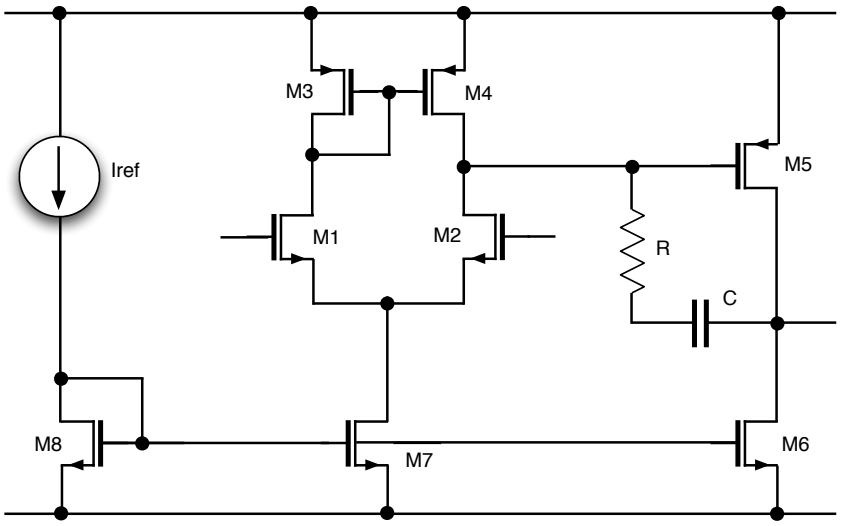

Figure 1.12: Schematic of the amplifier used for the compensation of the voltage drop on the reference ground line.

$$I_{DAC} = \sum_{n=0}^{N} 2^n I_{LSB} b_n \tag{1.6}$$

where N is the number of control bits of the DAC, I_{LSB} is the current reference and b_N is the N-th control bit. The equivalent resistance of the circuit in Fig. 1.13 can be written in the following equation in terms of its conductance as a function of the control bits.

$$G = \sum_{n=0}^{N} 2^{n-N} G_0 b_n \tag{1.7}$$

where G_0 is the inverse of the unary resistance. So the voltage reference V_{ref} is given by the following equation.

$$V_{ref} = \frac{I_{DAC}}{G} = \frac{\sum_{n=0}^{N} 2^n I_{LSB} b_n}{\sum_{n=0}^{N} 2^{n-N} G_0 b_n} = I_0 R_0 2^N \tag{1.8}$$

This is valid in HG mode. For the low gain operation the previous equation

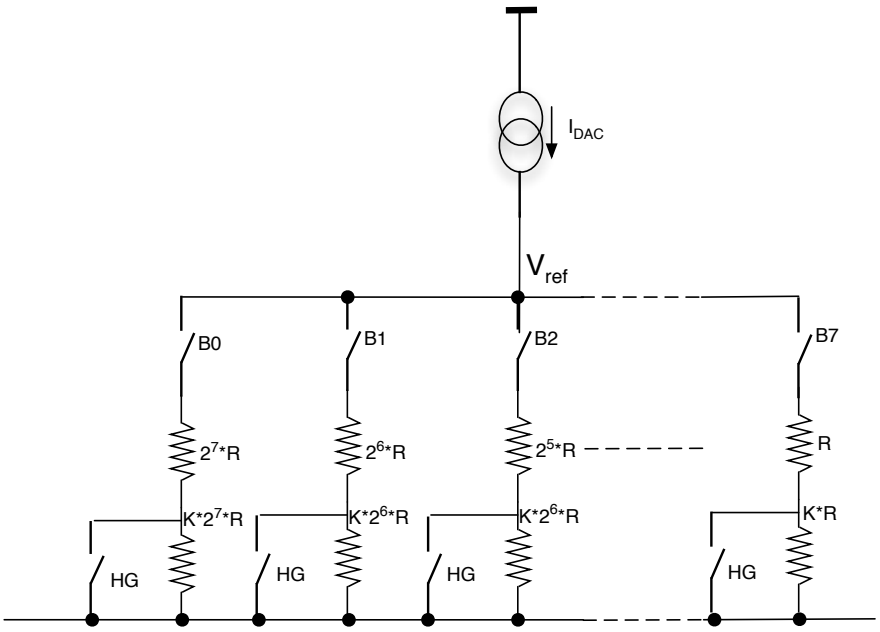

Figure 1.13: Schematic used to generate the reference voltage of the voltage drop compensation circuit.

is still valid changing R_0 with $R(k+1)$ where k is the current ratio between high and low gain operations $k = \frac{I_{HG}}{I_{LG}}$ In this solution the value of k parameter is 2.

1.6 4-bit coarse DAC

The current injection pulser is required to emulate the DC bias current of the DEPFET to be sunk by the programmable current source in order to verify the behavior of such a block at pixel level. For this purpose, an additional 4-bit Coarse Current D/A Converter has been added in the chip periphery. Since no particular constraints on the accuracy of the generated current are required, an architecture based on a binary weighted current network using scaled MOS devices only has been adopted as show in Fig. 1.14 . The current generated by the DAC in the chip periphery is mirrored in each pixel cell by

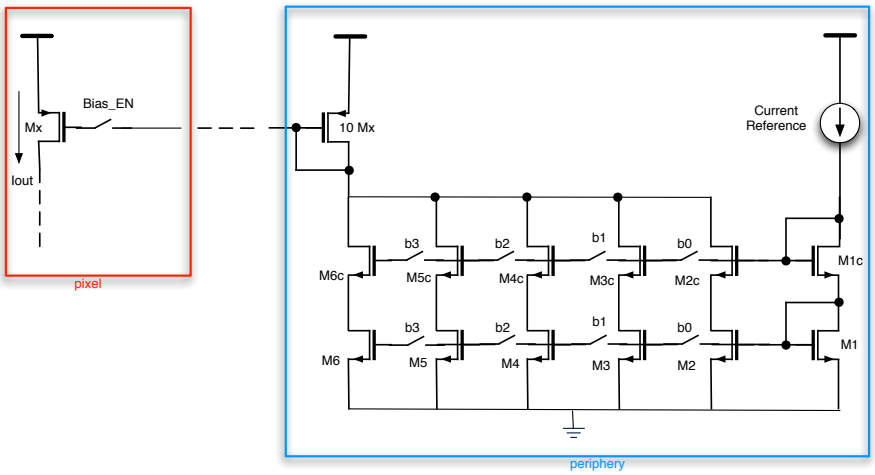

Figure 1.14: Schematic of coarse DAC.

means of a 10:1 current mirror and is fed in the drain of the input cascode. The devices of this DAC have been dimensioned in order to generate a DC current in the pixel cell which covers a range of about 140 μA with a resolution of 9 μA. The transistors has been designed in other to minimize the output noise contribution. After mounting the ASIC onto the sensor, is possible to disable the bias current opening the switch controlled by the Bias_EN control bit.

1.7 Measurement Results

Two prototypes of the circuit have been produced: the `DSSC_INJ1` submitted to the foundry in May 2010 and delivered in February 2011, and the `DSSC_INJ2` submitted to the foundry in August 2011 and delivered in Jenuary 2012. Compared to the first version of the circuit, the one presented in this work shows, in particular, a reduced area occupancy inside the pixel. Moreover, on the basis of results provided by the `DSSC_INJ1`, a review of critical aspects of the design has been performed and these limits have been overcome in the `DSSC_INJ2`. The experimental results of the second version of the injection circuit are presented in this work.

1.7.1 Test System

In order to perform a systematic, efficient and automated characterization process, a software control system has been developed. The primary aim of the system is to provide an automated way to perform measurements at the output of the components (current and charge injection mode, Current Steering DAC and coarse current DAC) of the injection circuit with increasing DAC codes, in order to provide dynamic range information and linearity results.

The developed test system takes advantage of the following technologies and instrumentations:

- Multimeter (Agilent 34401A) to perform voltage and current measurements.
- Pulser-Pattern generator (Agilent 81104A) to send the control bits to the circuit.
- Waveform generator (Agilent 33120A) to synchronize and trigger the latter two instruments.
- GPIB (aka IEEE 488) protocol to control the instrumentation.
- Client computer controlling the instrumentation by means of a software.
- GPIB-USB converter to interface the computer with the GPIB.
- Test board: in order to perform the measurements on the injection circuit, a test board has been developed. This board aims at generate all the bias voltage and current needed by the circuit, to provide the control signal and to sense the output signals.

A software using the following features has been implemented:

- Linux based OS as platform and CERN ROOT as data analysis framework, in order to make the software more portable than the previous version. The Scientific Linux release 5.6 distribution has been chosen, accordingly to the requirements of the low level libraries to control the GPIB-USB module. Other alternative OSs can be Red Hat Enterprise

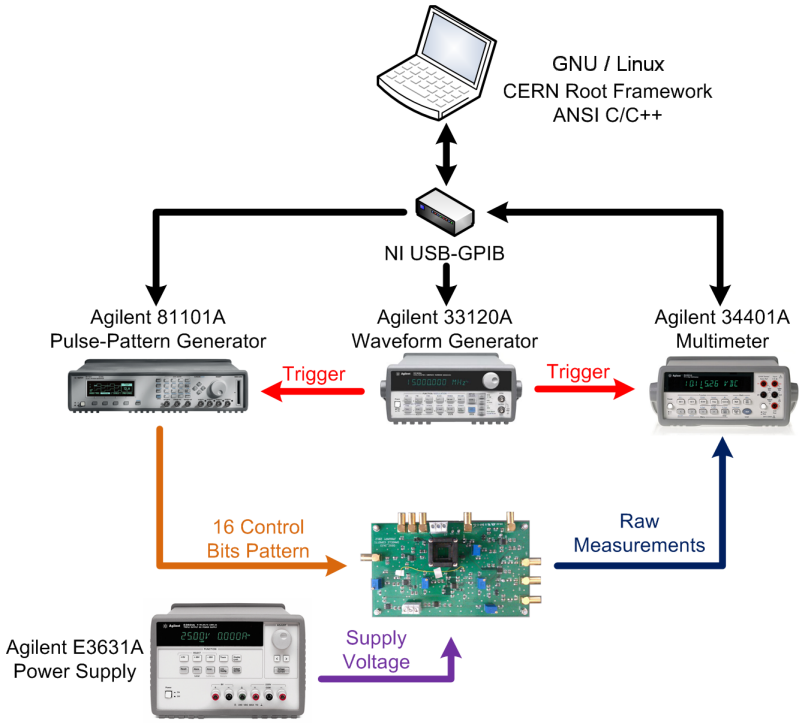

Figure 1.15: Hardware architecture view with the related adopted technologies.

Linux based OSs (RHEL, Centos, Fedora, Scientific Linux) and Open Suse.

- C++ (C plus plus) and C as programming languages, in order to take advantage of the available low level GPIB libraries freely provided by the producer of the GPIB-USB module.

The hardware architecture of the system and the adopted technologies are shown in Fig 1.15.

1.7.2 Experimental Results

In this part the results from the characterization of the second prototype of the injection circuit will be presented. The content is organized as follows. First the

linearity results, performed at different bias conditions, will be shown. Finally, the noise measurements results will be presented.

1.7.3 Input - Output Characteristics

In this section the input-output characteristics of the Current Steering DAC, of the Coarse Current DAC and of the current and charge pulsers will be presented. The transfer characteristic of the block can be expressed as the trend of its output as a function of the increasing input DAC code, between the minimum value and the maximum value. The linearity of each block has been evaluated by means of the following parameters:

- The Least Significant Bit (LSB), which represents the mean increment of the output in the considered range. It is computed as follow:

$$LSB = \frac{\sum_{i=1}^{n-1}(m_{i+1} - m_i)}{n-1} = \frac{m_n - m_1}{n-1} \tag{1.9}$$

  where n is the number of measurements performed and m_i is the output corresponding to the i-th input DAC code.

- The Differential Non Linearity (DNL), which is a non-linearity parameter of the input-output characteristic in terms of deviation from the LSB at a specific input code. Although each output measurement can be associated to a DNL value, the most relevant DNL is the greatest one in absolute value and expressed in LSB units. A common requirement for a DAC is DNL<1 LSB, in order to provide a monotonic trend of the output. The DNL is computed as follow:

$$DNL_i = \frac{m_i - m_{i-1} - LSB}{LSB},\ i > 1 \tag{1.10}$$

- The Integral Non Linearity (INL), which is a non-linearity parameter of the input-output characteristic in terms of deviation from the best fit straight line. The deviation is usually expressed in LSB units, and a common requirement for a DAC is INL<0.5 LSB. Indeed, if the INL<0.5LSB, then DNL<1LSB because of the deviation from the best fit straight line

is such that $m_i - m_{i-1} < 2 \cdot LSB$, ensuring the monotonicity of the DAC. The INL is computed as follow:

$$INL_i = \frac{m_i - a \cdot i - b}{LSB} \tag{1.11}$$

where a and b are respectively the slope and the intercept of the best fit straight line.

The input-output characteristic has been studied at different bias conditions, in order to evaluate the flexibility of the circuit, and in both High Gain and Low Gain configuration.

8 Bit Current Steering DAC

In figure 1.16, the characteristic of the Current Steering DAC, the DNL trend and INL trend in both the gain configurations are shown .
The transfer function of the 8-bit current steering DAC has been evaluated by measuring its output current as a function of the DAC input code in both low and high gain configuration. The result obtained for one of the tested samples is shown in Fig. 1.16 together with the relevant Differential Non Linearity (DNL) and Integral Non Linearity (INL) errors. Here and below, the INL profile has been obtained by evaluating the deviation of the transfer function from the best-fit line. The INL error is smaller than ±0.5 LSB, which is a common specification for precise digital to analog converters. The DNL, smaller than 1 LSB, ensures that the converter is monotonic: every increase of the digital input code leads to an increase of the analog output value. Up to twenty chips have been tested. Though the number of measured samples is limited, a statistical analysis has been performed. Table I summarizes the mean value of DAC main parameters together with the spread across different samples expressed in terms of ± the relevant standard deviation. The $I_{DAC_{LSB}}$ is about 1-2 % higher with respect to the nominal value leading to an analog output range of the DAC, $I_{DAC_{MAX}}$, increased by almost the same amount. A relative standard deviation of 4-5 % is found for the LSB current. The module of the values for INL and DNL quoted in the table represents the maximum over

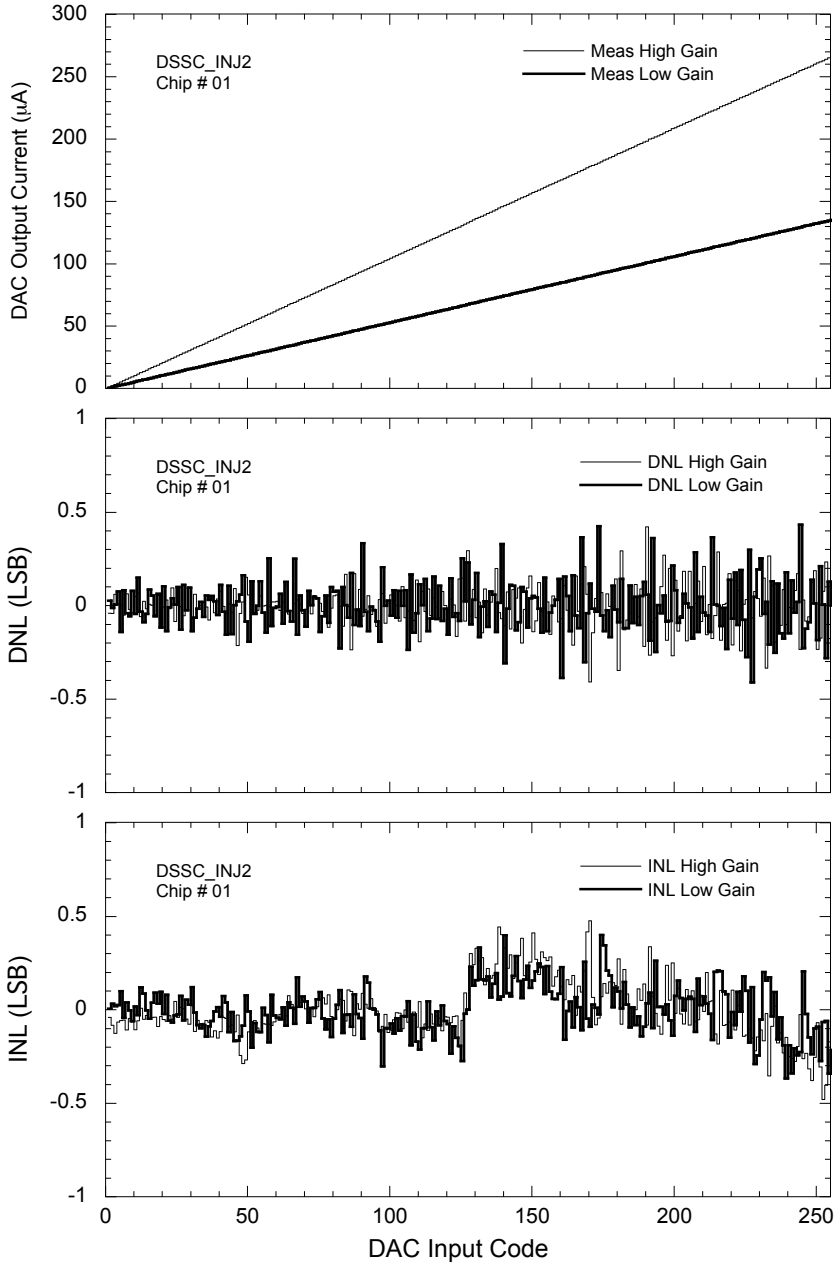

Figure 1.16: DAC output current as a function of the input DAC code both in the low and high gain setting (upper plot), together with the relevant DNL and INL error (lower plots).

Table 1.1: 8-bit DAC measured main parameters.

	Low Gain	High Gain
$I_{DAC_{MIN}}$ [μA]	0.50 ± 0.05	1.02 ± 0.07
$I_{DAC_{MAX}}$ [μA]	131.08 ± 6.30	258.20 ± 10.40
$I_{DAC_{LSB}}$ [μA]	0.51 ± 0.03	1.01 ± 0.04
$\sigma_{I_{DAC_{LSB}}}/I_{DAC_{LSB}}$ [%]	4.81	4.02
$\|DNL\|_{MAX}$ [LSB]	0.45 ± 0.10	0.44 ± 0.09
$\|INL\|_{MAX}$ [LSB]	0.42 ± 0.06	0.44 ± 0.05

the measured error profile of each sample. It can be observed that the DAC achieves good linearity performance: the module of both DNL and INL exhibit mean values <0.5 LSB. These results are comparable with the ones obtained for the `DSSC_INJ1` with the exception of the dispersion across different samples which is higher by about a factor of 3 [2]. This effect can be ascribed to the gain selection scheme which is the only difference introduced in the DAC of the `DSSC_INJ2` with respect to the one designed for the first prototype.

4 Bit Coarse Current DAC

The 4 bit coarse current DAC is suited to emulate the bias current of the DEPFET sensor in a range between 14μA and 140μA. The input-output characteristic, at nominal working conditions, together with the trend of INL and DNL is shown in figure 1.17.

Moreover, the output current has been studied varying the reference voltage at the output, which has a nominal value of 0.9V as shown in Fig. 1.14. As can be seen in figures 1.18, the I_{LSB} is inversely proportional to the output voltage.

Finally, table 1.2 summarizes the Coarse Current DAC results at nominal working conditions.

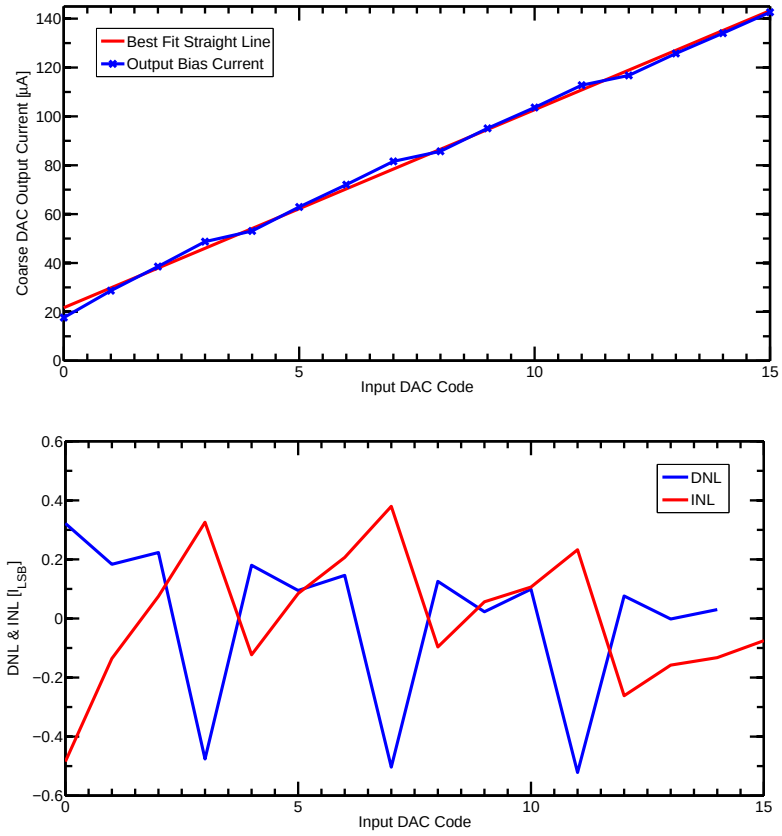

Figure 1.17: Trend of the input-output characteristic with increasing input DAC code(upper plot), together with the trend of INL and DNL (lower plot).

Table 1.2: 4-bit Coarse DAC measured main parameters.

	Value
$I_{DAC_{MIN}}$ [μA]	16.08 $\pm$ 1.6
$I_{DAC_{MAX}}$ [μA]	140.09 $\pm$ 12.42
$I_{DAC_{LSB}}$ [μA]	8.27 $\pm$ 0.73
$\sigma_{I_{DAC_{LSB}}}/I_{DAC_{LSB}}$ [%]	8.79
$\lvert DNL\rvert_{MAX}$ [LSB]	0.56 $\pm$ 0.06
$\lvert INL\rvert_{MAX}$ [LSB]	0.47 $\pm$ 0.063

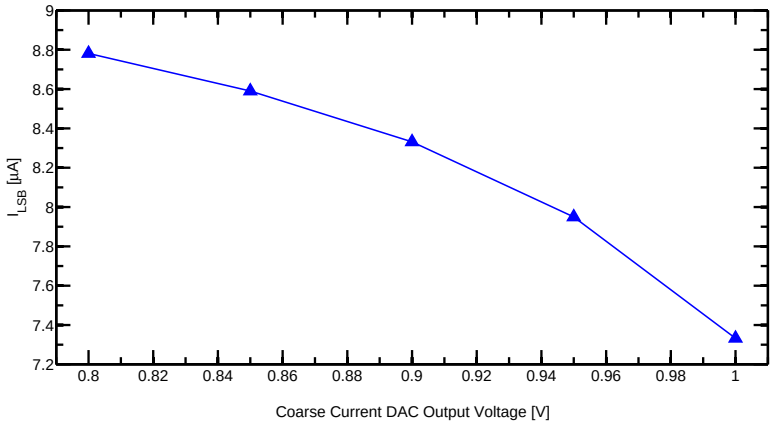

Figure 1.18: Trend of the I_{LSB} with increasing output voltages.

Current Injection Pulser

The output of the current injection pulser has been measured both in the nominal working conditions and with different V_{DD} values ranging from 1.1V to 1.3V with 0.05V step. Moreover, the linearity has been studied also by varying the pulser output voltage in a range between 0.8V and 1.0V with a 0.05V step. Figure 1.19 shows the output current, the DNL trend and the INL trend as functions of the Current Steering DAC input code, in low and high gain configuration respectively and at nominal working conditions.
Data coming from statistical analysis of the results obtained from twenty different samples of the investigated circuit are summarized in Table 1.3. The resolution of the pulser fulfills the specification of $I_{inj_{MIN}}$<0.1 μA corresponding to the current generated by 1 photon at 1 keV hitting the DEPFET sensor. An $I_{inj_{LSB}}$ about 5 % lower with respect to the expected value and with a relative standard deviation of about 5-6 % has been found. This lower $I_{inj_{LSB}}$ reduces the dynamic range of injectable currents, represented by $I_{inj_{MAX}}$, of the same amount. Good performance are obtained in terms of DNL error, while the INL shows mean values higher with respect to the 0.5 LSB limit.
The performance of the current injection pulser has been studied with different voltage supply values; as in figures 1.20, with respect to the nominal value at $V_{DD} = 1.2V$ the I_{LSB} is about 3% lower at 1.1V and 2% higher at $V_{DD} = 1.3V$.

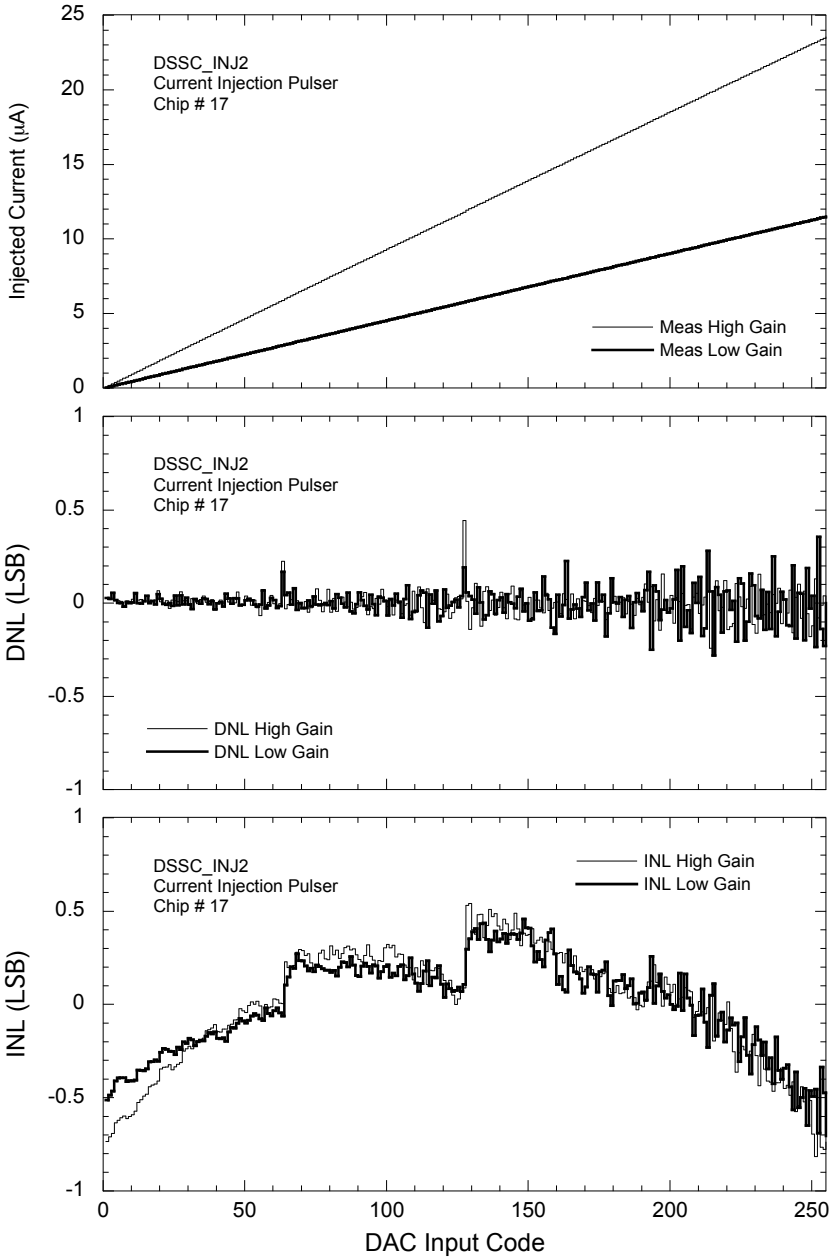

Figure 1.19: Current Injection output current as a function of the input DAC code both in the low and high gain setting (upper plot), together with the relevant DNL and INL errors (lower plots).

Table 1.3: Current Injection mode measurement results

	Low Gain	High Gain
$I_{inj_{MIN}}$ [nA]	43.60 ± 6.30	89.70 ± 11.50
$I_{inj_{MAX}}$ [μA]	12.30 ± 0.80	24.20 ± 1.20
$I_{inj_{LSB}}$ [nA]	48.40 ± 3.00	94.40 ± 4.70
$\sigma_{I_{inj_{LSB}}}/I_{inj_{LSB}}$ [%]	6.1	4.9
DNL_{MAX} [LSB]	0.50 ± 0.10	0.50 ± 0.20
INL_{MAX} [LSB]	1.50 ± 1.00	1.50 ± 0.80

As far as the linearity is concerned a detrimental effect of V_{DD} on the INL is observed at 1.1V.

The performance of the current injection pulser has been evaluated also as a function of the output reference voltage (V_{OUT}), which in nominal conditions is 0.9V. Fig. 1.21 shows the trend of the main pulser parameters in both the gain configurations as a function of V_{OUT}.

Finally, the output of the current injection pulser has been measured with increasing Current Steering DAC input code and with the enable bit set to 0. Results for both the gain configurations are shown in figure 1.22.

Charge injection Pulser

The charge injected in the relative function mode is expected to be in the range between 0.2 fC and 50 fC or 0.4 fC and 100 fC, in low gain and high gain configuration respectively. The output voltage of the charge injection pulser has been measured as a function of the DAC input code and the relevant injected charge has been obtained by considering an ideal 500 fF capacitance. Fig. 1.23 show the trends of the injected charge, of the DNL and of the INL with increasing Current Steering DAC input code, in low gain and high gain configuration and at nominal working conditions, Table 1.4 summarizes the results coming from the statistical analysis of data provided by the set of twenty measured samples. Though, in both low and high gain, the LSB value of the injected charge Q_{LSB} is about 10 % higher with respect to the nominal

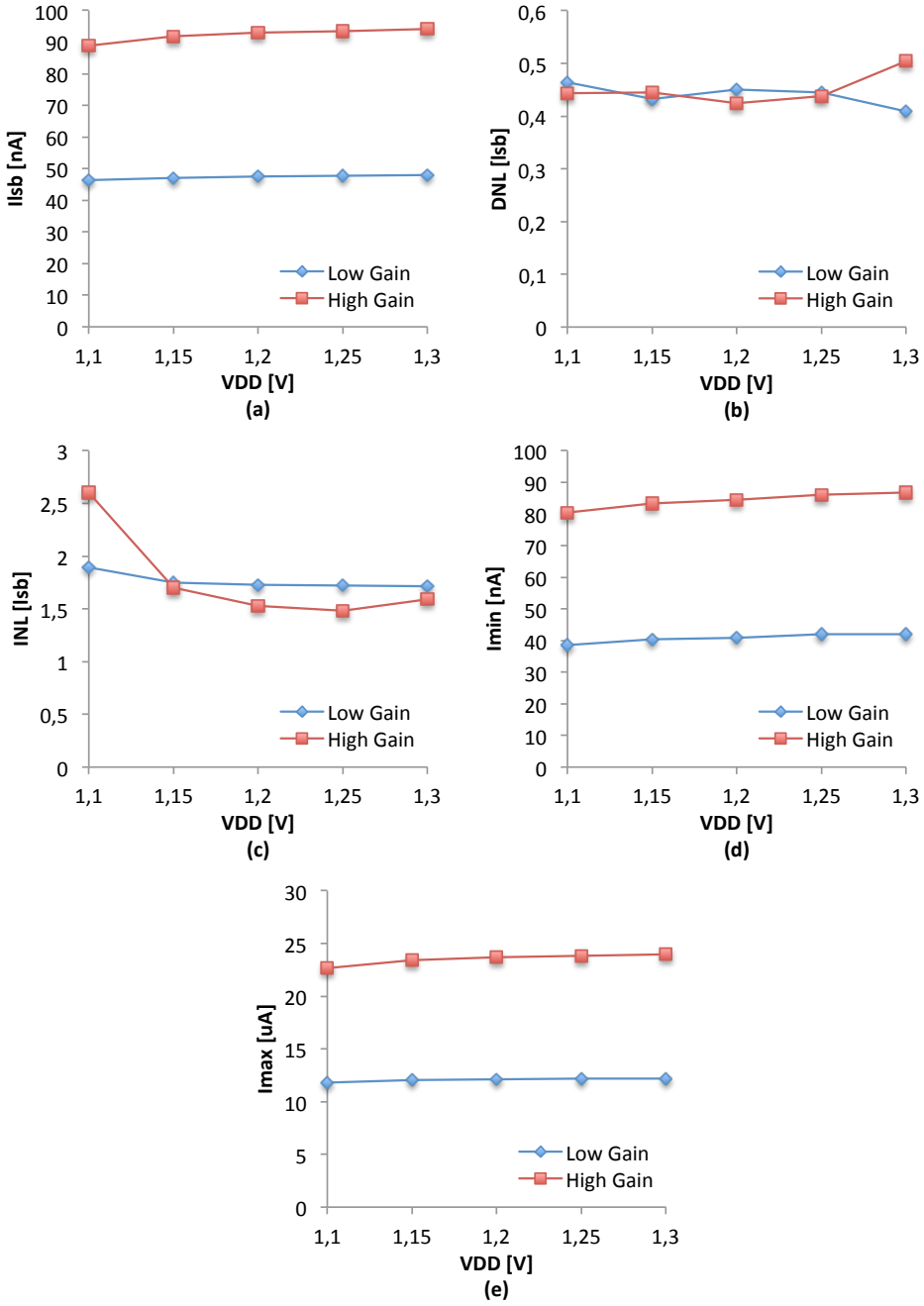

Figure 1.20: Trend of:I_{LSB}(a), DNL (b), INL (c) minimum (d) and maximum (e) injected current with increasing voltage supply at low and high gain configuration.

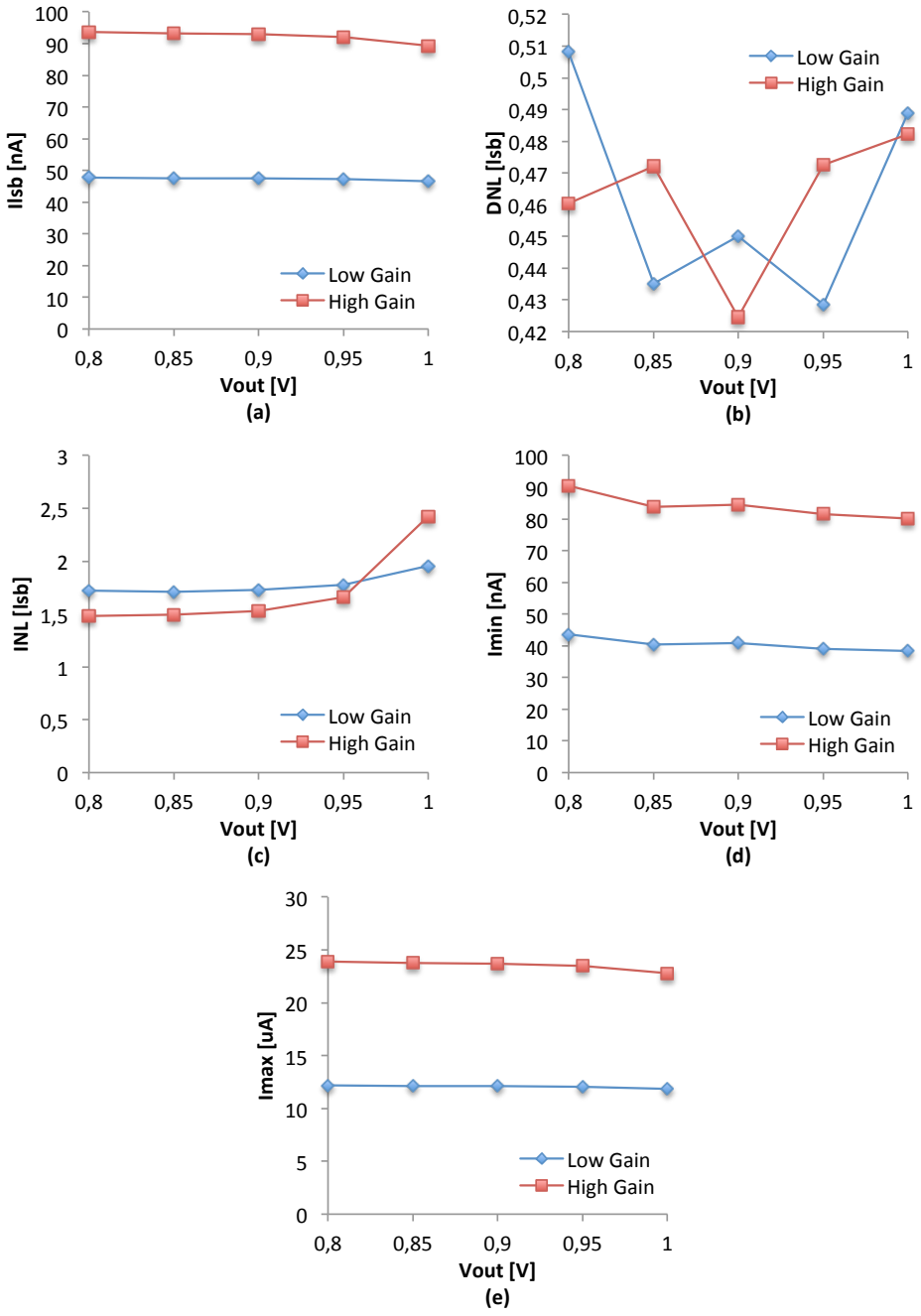

Figure 1.21: Trend of:I_{LSB}(a), DNL (b), INL (c) minimum (d) and maximum (e) injected current with increasing the output bias voltage (V_{OUT}). at low and high gain configuration.

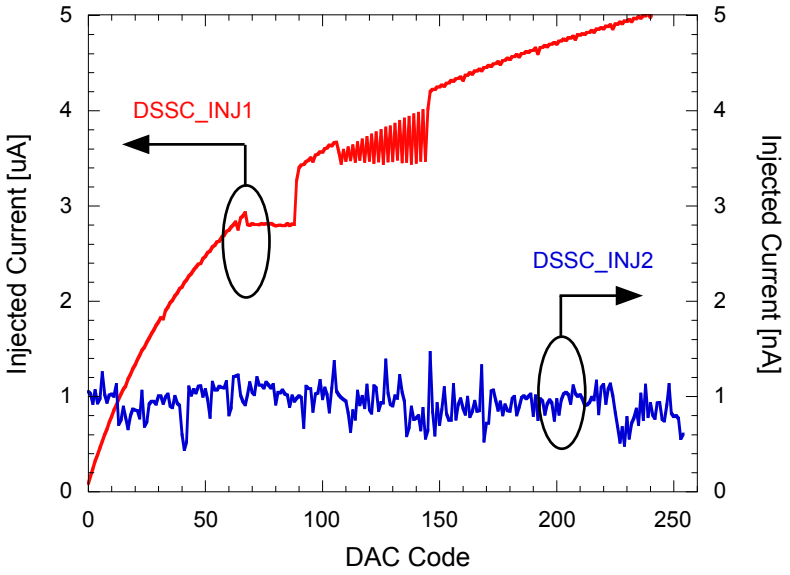

Figure 1.22: Current pulser output for the whole range of the Current Steering DAC input code in high gain configuration when the pixel is disabled.

value foreseen in equation (1.4), the circuit, in low gain, allows for a minimum injected charge lower than the one corresponding to the first 1 keV photon collected by the pixel as requested (Q_{MIN}<0.4 fC). In high gain, the output range of the injected charge, expressed by Q_{MAX}, fulfills the requirements of Q_{MAX}>110 fC. A relative standard deviation of about 8 % in low gain and 7 % in high gain is obtained for Q_{LSB}. The Injection circuit shows good performance in terms of DNL error, which stays smaller than ±1 LSB ensuring the monotonicity of the injected charge, while the module of the INL error is higher with respect to the commonly adopted limit of 0.5 LSB. This can be an issue or not in relation to the specific application and to the linearity of the front-end to be calibrated.

The performance of the charge injection pulser has been evaluated for different values of the voltage supply; as in Fig. 1.24, the Q_{LSB} increases with V_{DD} along with the linearity and the maximum current do.

Finally, the output of the charge pulser has been measured with increasing Current Steering DAC input code and with the enable bit set to 0. The results

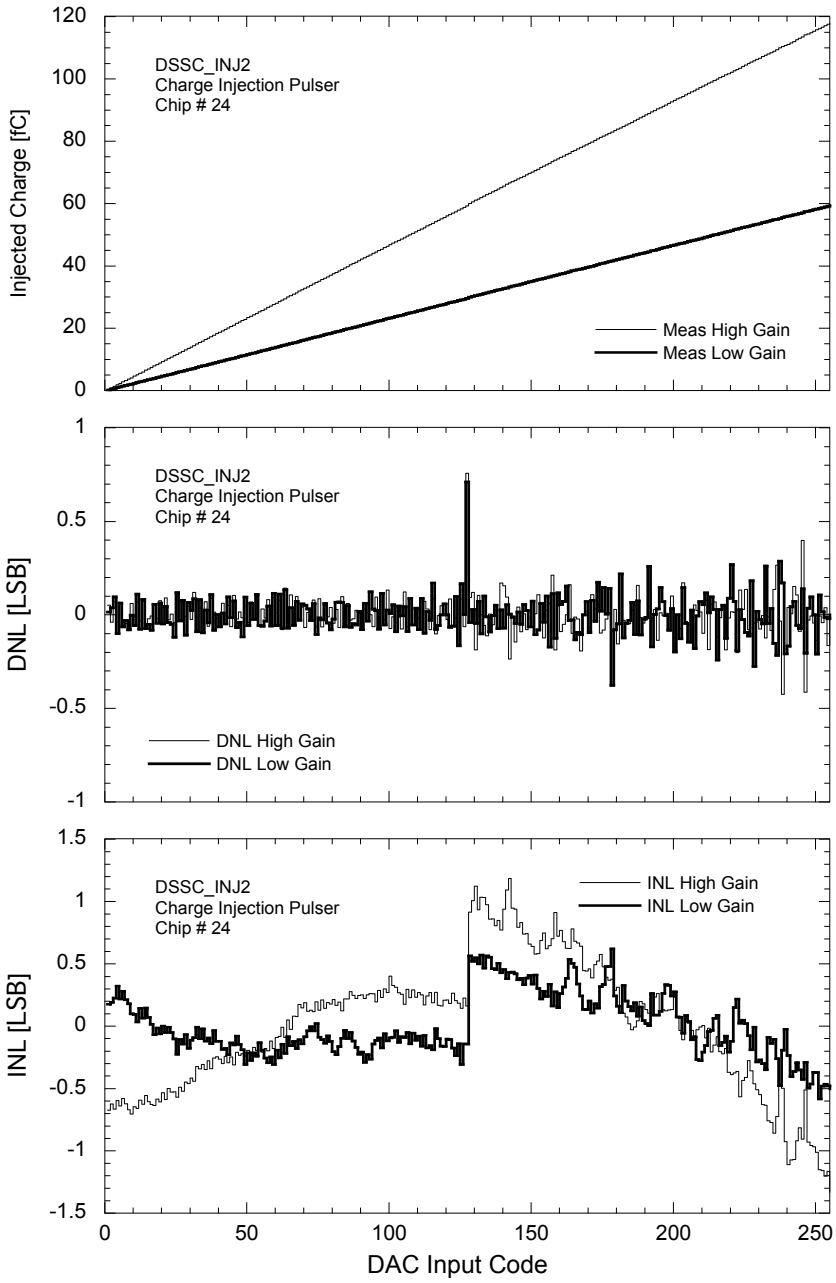

Figure 1.23: Charge Injection Pulser output charge as a function of the input DAC code both in the low and high gain setting (upper plot), together with the relevant DNL and INL errors (lower plots).

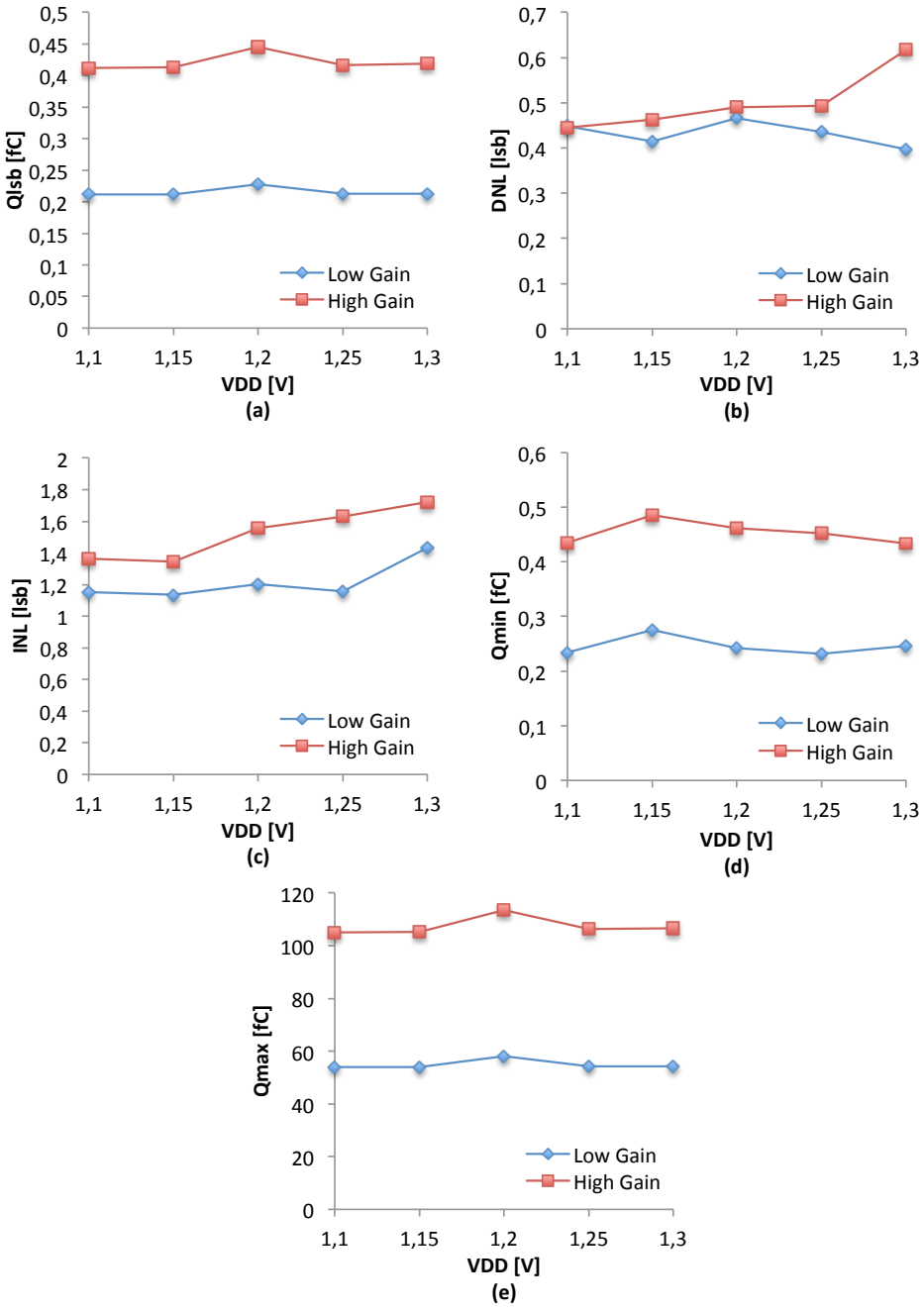

Figure 1.24: Trend of:Q_{LSB}(a), DNL (b), INL (c) minimum (d) and maximum (e) injected charge with increasing the supply voltage at low and high gain configuration.

Table 1.4: Charge Injection mode measurement results

	Low Gain	High Gain
Q_{MIN} [fC]	0.24 ± 0.09	0.46 ± 0.11
Q_{MAX} [fC]	58.14 ± 4.83	113.12 ± 8.23
Q_{LSB} [fC]	0.23 ± 0.02	0.44 ± 0.03
$\sigma_{Q_{LSB}}/Q_{LSB}$ [%]	8.3	7.2
$\|DNL\|_{MAX}$ [LSB]	0.47 ± 0.13	0.49 ± 0.14
$\|INL\|_{MAX}$ [LSB]	1.20 ± 0.89	1.56 ± 0.78

Table 1.5: Mean and standard deviation of the injected current when the charge pulser is disabled at both the gain configurations.

	$\overline{Q_{INJ}}$ [fC]	$\sigma_{Q_{INJ}}$ [%]
Low Gain	0.510	2.94
High Gain	0.520	4.08

are summarized in table 1.5.

1.7.4 Voltage Drop Compensation Circuit

In this section the beneficial effect of the voltage drop compensation circuit will be shown. The 100 mV reference voltage, generated in the chip periphery and sent into each pixel has been measured with ground voltages increasing between 0 V and 40 mV (10 mV step), in both the gain configurations and with increasing Current Steering DAC input codes between 1 and 255. Experimental results are summarized in Table 1.6, for the charge injection.The trend of the reference voltage at nominal working conditions for the charge injection configuration is shown in Fig. 1.25.

The beneficial effect of this block has already been verified in the `DSSC_INJ1` prototype as shown in Fig. 1.26 where the normalized LSB and the maximum INL are reported as a function of the voltage drop on the ground line with and without the compensation circuit for one sample. Data are rel-

Table 1.6: Experimental results of the measurements of the 100 mV reference voltage into the charge injection pulser.

$\overline{V_{GND}}$ [mV]	$\overline{V_{REF}}$ [mV]		$\sigma_{V_{REF}}$ [mV]	
	Low Gain	High Gain	Low Gain	High Gain
0	116.6	127.6	2.4	8.8
10	116.3	127.6	3.0	9.1
20	116.3	127.7	2.9	9.0
30	116.5	127.7	2.8	9.1
40	116.5	127.6	2.8	9.1

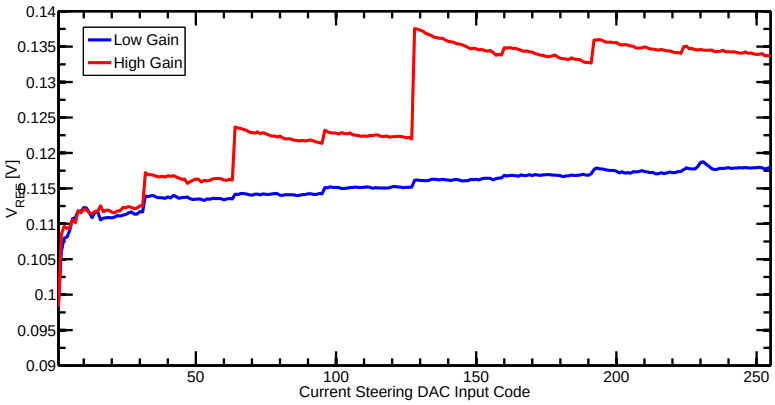

Figure 1.25: Trend of the 100 mV reference voltage of the charge injection pulser as a function of the Current Steering DAC input code.

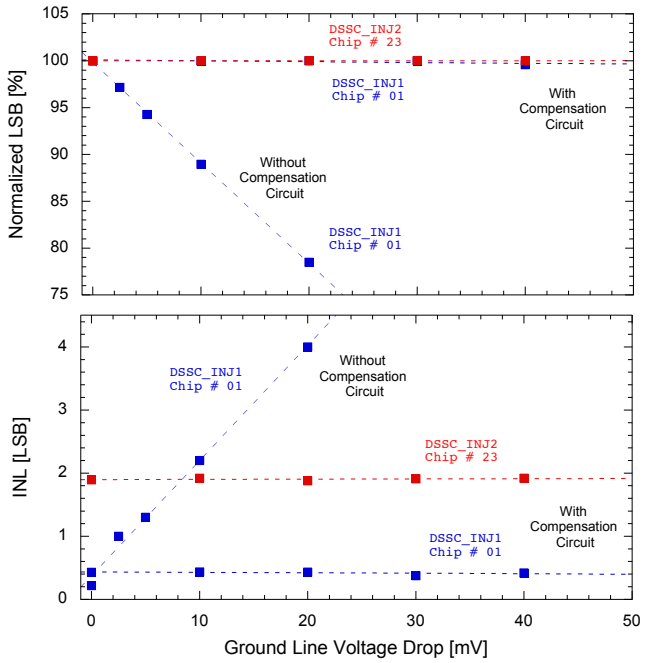

Figure 1.26: Measured effect of the Voltage Drop Compensation circuit in Current Injection Mode: normalized amplitude of the LSB (upper plot) and maximum INL error (lower plot) as a function of the voltage drop on the ground line both with and without compensation circuit.

evant to the Current Injection Pulser in high gain but the same results hold for the Charge Injection Pulser and for the low gain setting. If the compensation circuit is bypassed, the LSB amplitude decreases with the increase of the voltage drop on the ground line. The introduction of the compensation circuit makes the LSB amplitude insensible to this source of mismatch up to 40 mV of voltage drop. As far as the linearity is concerned, the introduction of the compensation circuit makes the INL worse when no voltage drop is present, probably due to the non negligible offset voltage of the amplifier, but it keeps this value constant when few mV of voltage drop turn up. The effectiveness of this circuit has been proved also for the `DSSC_INJ2` as shown in Fig. 1.26. For this second prototype data obtained without the compensation circuit are not available since it can not be bypassed in this second version.

1.8 Noise Measurements

In applications where the injection circuit is employed to measure the main analog parameters of the readout channel by means of a charge scan procedure or a threshold scan technique, its noise contribution must be negligible with respect to the one of the readout channel to be measured. The noise of the Injection Circuit developed in this work has been evaluated by measuring the power spectral density of the current provided in Current Injection mode and of the voltage in Charge Injection mode. In the former circuit the noise in the output current is converted into a voltage by a low-noise transimpedance amplifier and then detected by an Agilent 4395A Network/Spectrum Analyzer [12], while in the latter case the noise in the output voltage is amplified by a non-inverting voltage amplifier, AC coupled with the Pulser, and then detected by the Analyzer. Noise measurements have been performed in the 100 Hz-1 MHz range for different values of the DAC input code, that is of the injected signal, ranging from 1 up to 20. This limited range has been chosen since it is of prominent interest in view of the application of the circuit in the DSSC chip as will be shown in the next Section. Fig. 1.27 and Fig. 1.28 show noise current spectra for the Current Injection pulser and noise voltage spectra for the Charge Injection pulser respectively. In the investigated frequency range, both exhibit $1/f$-like noise at low frequencies and white noise in the high frequency portion of the spectra. Therefore, they can be modeled by means of equation (1.12) and (1.13) for the current and noise respectively.

$$S_i^2(f) = a_{i,w} + \frac{a_{i,f}}{f} \tag{1.12}$$

$$S_v^2(f) = a_{v,w} + \frac{a_{v,f}}{f} \tag{1.13}$$

In both equations, the first terms, $a_{i,w}$ and $a_{v,w}$, account for the frequency independent contribution while the second ones represents the $1/f$-like noise and depends on the intensity coefficients $a_{i,f}$ and $a_{v,f}$. Noise measurement results of Fig. 1.27 and Fig. 1.28 show that white and $1/f$-like contributions increase with the increase of the injected signal in both the Current and the

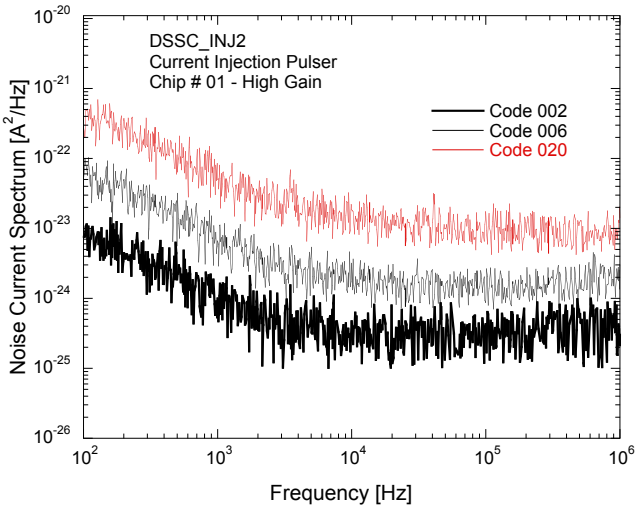

Figure 1.27: Noise current spectra for the Current Injection Pulser measured at different values of the DAC input code (Code 2, 6 and 20).

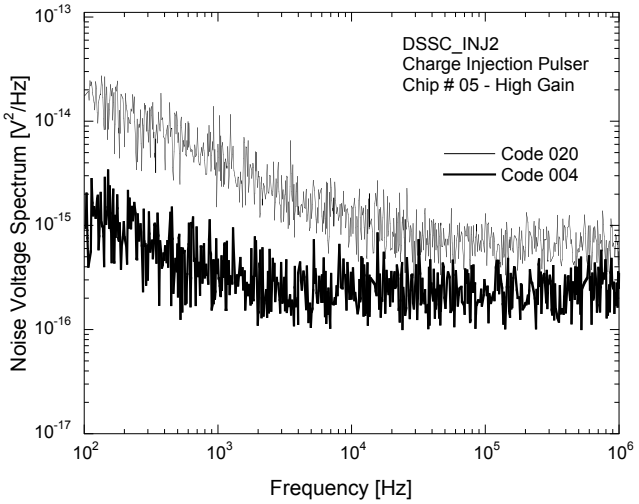

Figure 1.28: Noise voltage spectra for the Charge Injection Pulser measured at different values of the DAC input code (Code 4 and 20).

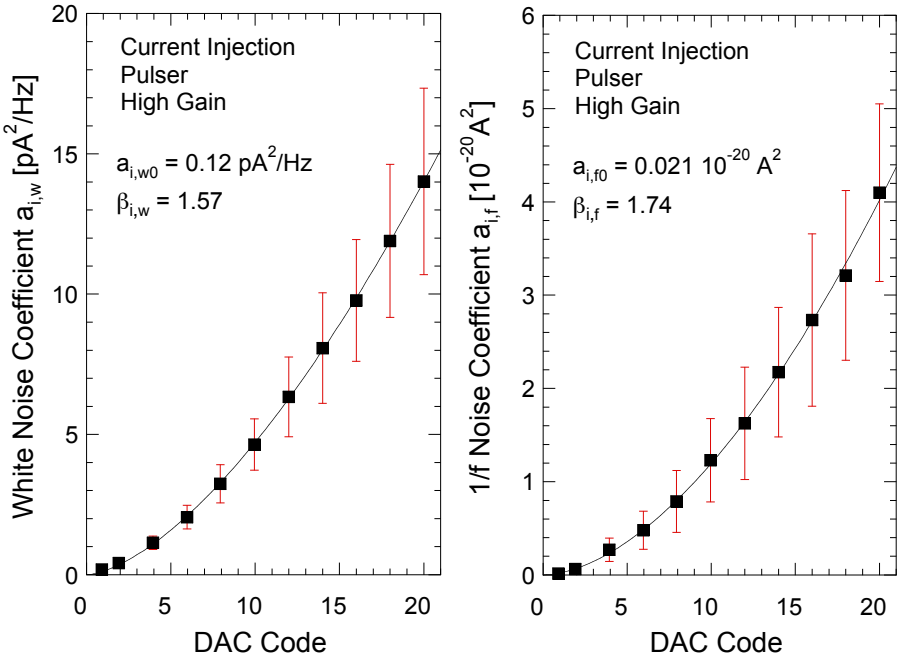

Figure 1.29: White ($a_{i,w}$) and $1/f$-like ($a_{i,f}$) current noise parameters as a function of the input DAC code.

Charge Injection pulser. It can be simply explained with the fact that the noise drain current in a MOSFET is directly proportional to its transconductance (g_m). This increases increasing the value of the I_D, so for higher input DAC codes there is an increase of the noise current in most devices of the pulser, wi which generates an increase of the total output noise. Simulation results have shown that many devices contribute to the total output noise and in a way that is strongly related with the DAC code. Therefore, it is difficult to find a simple device-based model describing the noise. Nonetheless, the behaviour of the noise coefficients can be studied as a function of the DAC input code and modeled by means of semi-empirical laws. Up to 10 samples of the Current Injection Pulser have been measured and the relevant white $a_{i,w}$ and $1/f$-like $a_{i,f}$ current noise parameters have been extracted. Fig. 1.29 shows the mean value obtained for these parameters as a function of the DAC code, together

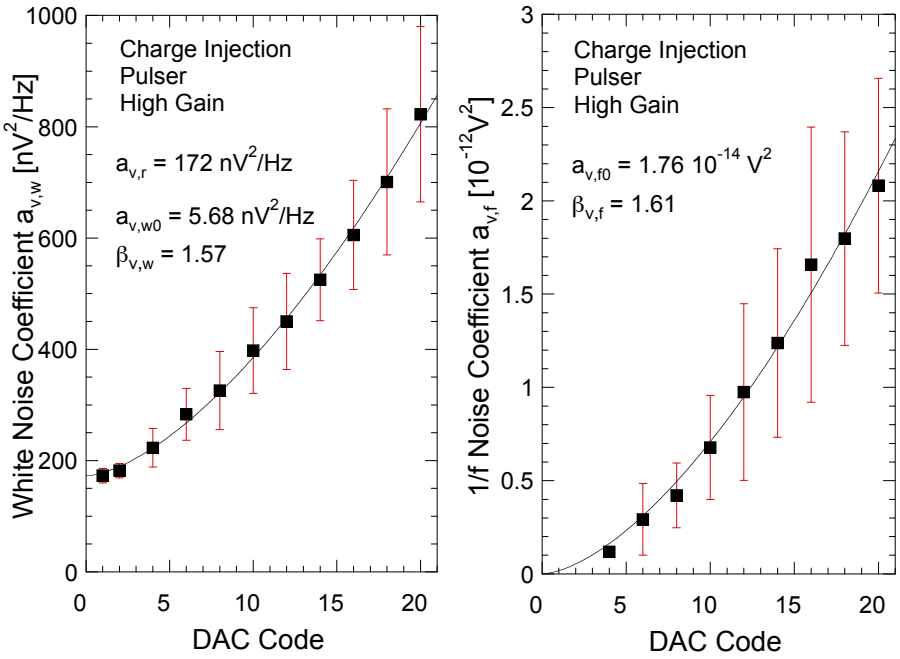

Figure 1.30: White ($a_{v,w}$) and $1/f$-like ($a_{v,f}$) voltage noise parameters as a function of the input DAC code.

with the spread across different samples expressed in terms of ± the relevant standard deviation. As expected, both coefficients increase with the DAC code and the following empirical law can be used to model this behavior:

$$a_{i,w} = a_{i,w0} \cdot k^{\beta_{i,w}}, \tag{1.14}$$

$$a_{i,f} = a_{i,f0} \cdot k^{\beta_{i,f}}, \tag{1.15}$$

where $1 \leq k \leq 20$ is the DAC code, $a_{i,w0}$ and $a_{i,f0}$ are the white and $1/f$ noise coefficients extracted for $k=1$ and $\beta_{i,w}$ and $\beta_{i,f}$ are the exponents of the power law. By fitting the plots of Fig. 1.29 with the above mentioned laws the values of noise coefficients reported in Table 1.7 are obtained. Same procedure can be followed to study the noise coefficients $a_{v,w}$ and $a_{v,f}$ extracted from the voltage spectra of the Charge Injection pulser. These values are reported as a

Table 1.7: Coefficients for noise current and voltage spectra of Current Injection and Charge Injection Pulser.

	Current Injection		Charge Injection	
White	$a_{i,w0}$ [pA^2/Hz]	0.12±0.004	$a_{v,w0}$ [nV^2/Hz]	5.68±1.23
noise	$\beta_{i,w}$	1.57±0.011	$\beta_{v,w}$	1.57±0.07
			$a_{v,r0}$ [nV^2/Hz]	172±9
$1/f$	$a_{i,f0}$ [10^{-20}A^2]	0.021±0.002	$a_{v,f}$ [10^{-11}V^2]	1.76±0.04
noise	$\beta_{i,f}$	1.74±0.04	$\beta_{v,f}$	1.61±0.09

function of the DAC code in Fig. 1.30. It can be noticed that the white noise coefficient does not drop to zero for low values of the DAC code as for the Current Injection Pulser. The behavior of the noise coefficients can be modeled by means of the following empirical law for the Charge Injection Pulser:

$$a_{v,w} = a_{v,r0} + a_{v,w0} \cdot k^{\beta_{v,w}}, \tag{1.16}$$

$$a_{v,f} = a_{v,f0} \cdot k^{\beta_{v,f}}. \tag{1.17}$$

where the $a_{v,r0}$ term in equation (1.16) accounts for the DAC-code independent contribution which dominates for low values of the injected charge. This contribution can be ascribed to the thermal noise of the R_B resistor shown in Fig. 1.9. Therefore $a_{v,r0}$=$4k_BTR_B$, where k_B is the Boltzmann's Constant and T is the absolute temperature. The value extracted for voltage noise coefficients are reported in Table 1.7. It can be noticed that, neglecting the DAC-code independent contribution $a_{v,r0}$, the other noise coefficients of current and charge injection pulser are strongly related by a resistor whose value is close to the one of the R_B resistor.

$$\sqrt{\frac{a_{v,w0} \cdot k^{\beta_{v,w}}}{a_{i,w0} \cdot k^{\beta_{i,w}}}} \approx 7\ k\Omega \tag{1.18}$$

$$\sqrt{\frac{a_{v,f0} \cdot k^{\beta_{v,f}}}{a_{i,f0} \cdot k^{\beta_{i,f}}}} \approx 8\ k\Omega \tag{1.19}$$

According to simulation results, the main contributions to the output noise come from the M_1 transistor in Fig. 1.9 and Fig. 1.10 and from the amplifier of the Voltage Drop Compensation circuit. Since these components are included in both Charge and Current Injection Pulser we can assume that the noise in the latter circuit has the same amount of the one in the Current Injection Pulser converted in a voltage by the R_B resistor. Therefore, we can derive the following relationship between the noise in the two pulsers.

$$S_v^2(f) = 4k_BTR_B + R_B^2 S_i^2(f) \tag{1.20}$$

This noise model, together with the one for the Current Injection Pulser expressed in equation (1.12) and the relevant noise coefficient reported in Table 1.7, can be used to evaluate the noise contribution of the circuit as a function of the specific application, as will be shown in Section 2.1 for the DSSC chip.

Chapter 2

Injection Circuit and DSSC

2.1 Circuit Application in the DSSC chip

The Injection circuit presented in the first chapter is used as a part of the DSSC chip. Because of this the main circuit parameters, such as linearity and noise performance, have been evaluated by referring to the specific application in the frame of the DSSC chip.

2.1.1 Linearity

Since the characteristic of the sensor adopted in the DSSC project is non linear, the linearity of the Injection Circuit can be evaluated paying particular attention to the first region of the dynamic range where, considering a standard linear DEPFET with a typical detector gain of 360 pA/e- for the DCR and of 2.8 μV/e- for the SFR readout [7], a one-to-one correspondence holds between the number of input photons at 1 keV and the DAC code in high gain. To this end the linear fit of the Injection Circuit transfer functions evaluated in Chapter 1, is now performed only on the first part of the dynamic range, corresponding to an incoming signal of about 20 photons at 1 keV. The linearity error has been expressed in terms of photons at 1 keV by considering the above mentioned detector gain factors.

In Fig. 2.1 results concerning both the Current and the Charge Injection Pulser are shown for one of the tested samples. The non-linearity error is

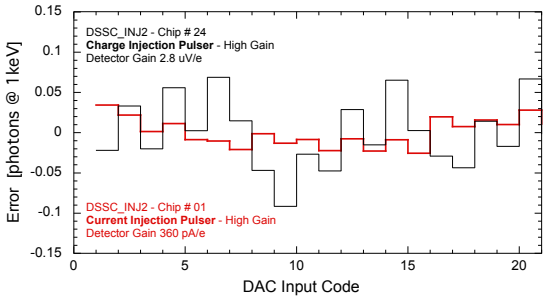

Figure 2.1: Linearity error, expressed in terms of photons at 1 keV, as a function of the input DAC code. The linear fit is done only on the first part of the dynamic range, corresponding to a detector incoming signal of about 20 photons at 1 keV.

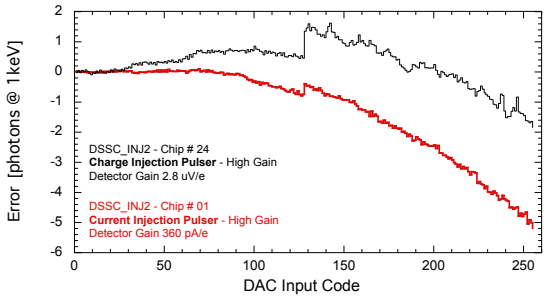

Figure 2.2: Linearity error, expressed in terms of photons at 1 keV, as a function of the input DAC code. The linearization is performed on the initial part of the range and the error is evaluated on the entire dynamic range.

below 0.04 photons at 1 keV for the Current Injection sample and below 0.09 photons at 1 keV for the Charge Injection sample. The statistical analysis performed on all the investigated samples provides a mean value of the error of 0.05±0.02 photons at 1 keV for the Current Injection Pulser and of 0.08±0.03 photons at 1 keV for the Charge Injection Pulser as reported in Table 2.1. Since the linearity of the circuit can be better evaluated by referring to the specific application, the performance of the Current Injection Pulser must be compared to the linearity of the front-end used in the DCR mode in the DSSC chip, which is about 0.05 photons at 1 keV [18]. The front-end linearity information is not available for the SFR mode. Starting from the fitting curve obtained in the first

Table 2.1: Maximum linearity error in photons at 1 keV.

DAC Code	Max linearity error [photons at 1 keV]	
range	Source Follower Readout	Drain Current Readout
1-20	0.08±0.03	0.05±0.02
1-255	7±4	8±4

part of the range, the error over the complete dynamic range can be evaluated as shown in Fig. 2.2. As expected the error increases when moving away from the initial range where the linearization is performed. A mean value of the maximum error of about 8±4 photons at 1 keV for the Current Injection Pulser and of 7±4 photons at 1 keV for the Charge Injection Pulser is obtained for all the tested samples as reported in Table 2.1. For what concerns the Current Injection Pulser the non linearity error is lower than the value of 10 photons obtained for the front-end [18].

2.1.2 Noise Performance

The noise performance of the injection circuit can also be better evaluated in view of the application in the DSSC chip. In this project both readout strategies include an analog filter implementing a trapezoidal weighting function to minimize the noise. The noise contribution of the injection circuit to the overall noise of the readout system can be evaluated in terms of Equivalent Noise Charge (ENC) as expressed in [19]. To this end, the output noise of the pulser must be referred at the external gate of the DEPFET by dividing the measured noise spectra for the detector gain which is assumed constant over the bandwidth of interest In the case of the SFR mode it is equal to one, instead it is given by the external gate transconductance g_{mE}=68 μA/V for the DCR mode. According to this, the ENC at the input of the system due to the Injection circuit for the Charge Injection and the Current Injection pulser respectively, is given by:

Table 2.2: ENC expressed in electrons rms for different readout speed and readout strategies.

Speed [MHz]	Source Follower Readout			Drain Current Readout		
	DEPFET [e-]	ASIC [e-]	INJ [e-]	DEPFET [e-]	ASIC [e-]	INJ [e-]
5.0	46	52.4	50.3	35	27.6	14.4
2.5	18.9	20.5	20.5	18	8.7	7.3
1.0	10.3	11.3	10.9	10	4.6	4.1

$$ENC_v^2 = C_{eq}^2 \left(\frac{a_{v,w}}{\tau} A_1 + 2\pi a_{v,f} A_2 \right) \tag{2.1}$$

$$ENC_i^2 = \frac{C_{eq}^2}{g_{mE}^2} \left(\frac{a_{i,w}}{\tau} A_1 + 2\pi a_{i,f} A_2 \right) \tag{2.2}$$

where C_{eq}=60 fF is the equivalent input capacitance of the system (since C_{eq} depends on the input charge this value holds only for a few photons collected by the detector) [4], A_1 and A_2 are the filter parameters depending on the shape of the weighting function performed by the readout electronics (A_1=2 and A_2=1.38 for the trapezoidal weighting function), and τ is the shaping time of the readout filter. In the frame of the DSSC operation the system can be operated at different frame rates (0.9-4.5 MHz) and τ has been defined as half of the time available to process the signal. So the values for the shaping time are 35, 135 and 435 ns for the DCR mode and 20, 120 and 420 ns for the SFR mode. The ENC has been evaluated considering the noise parameters of Table 1.7. Since both Pulsers exhibit a dependence of the noise on the amplitude of the injected signal, the ENC has been extracted for an injected signal corresponding to 1 photon at 1 keV, that is, for a DAC code of 1 in the high gain configuration. Results are reported in Table 2.2, together with the contributions belonging to the detector and the front-end as reported in [4].

The noise contribution due to the Injection Circuit is slightly lower with respect to the one of the front-end in both SFR mode and DCR mode. Same consideration holds for the noise coming from the DEPFET in DCR mode. In SFR mode, instead, the noise of the Injection Circuit is slightly higher than the noise due to the DEPFET. Though it is always lower than the front-end, the noise due to the Injection Circuit is not negligible. Simulation results have identified in the amplifier of the Voltage Drop Compensation circuit the main source of noise. Therefore, better performance can be achieved by working on this block which has not been optimized from the stand point of the noise.

2.2 Improved Current Injection

An improved version of the injection circuit, `DSSC_INJ3`, has been merged into a second 8 × 8 mini-matrix pixel of the DSSC chip and submitted to the foundry in May 2012. The new design differs from the previous one for a different value of the LSB in the two working modes. The new version also has optimized performance in terms of settling time and noise as well as linearity, with respect to the previous version. The `DSSC_INJ3` includes only the pulser for the current injection, because the drain current readout mode was chosen for the final version of the DSSC chip.

2.2.1 Architecture

In the improved version of the injection circuit, the ratio between the current provided in high and low gain configuration has been moved from 1:2 to 1:10 to comply with the requirements coming from the first calibration specification of the DSSC chip. In both working modes lower noise, faster settling time together with higher linearity have to be guaranteed. To fulfill all these requirements some changes have been included in the circuit topology.

As shown in Fig. 2.3 the conceptual scheme of the injection circuit is similar to the one of the old version. The main difference is the High Gain (HG) control signal which in this version is routed inside the pixel. In this way it is possible to have two different configurations of the devices hosted in the pixel, one

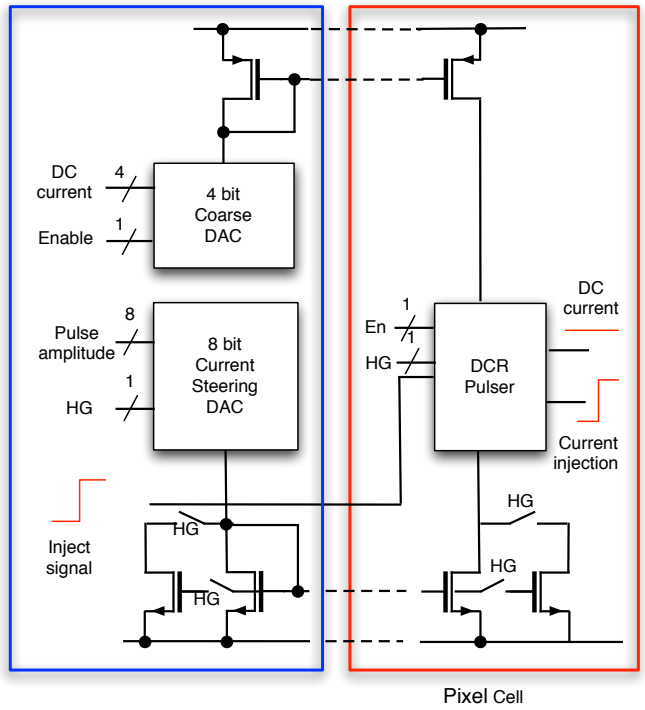

Figure 2.3: Conceptual block diagram of the new version of injection circuits.

optimized for the high gain and another for the low gain mode, and is possible to select the correct one by the HG signal. In this way it is possible to match the new tuning range specification together with all the other constraints listed before.

Periphery

The part of the circuit hosted in the chip periphery is similar to the one of the previous version: the DAC's schematic is unchanged with the exception of the current reference which, instead, has been changed to match the new dynamic range requirements. The two current reference levels are now: 1uA and 100 nA, so the DAC output current ranges from 100nA to 255 uA. Due to the wide difference in the current range and in the step, the resistive voltage reference

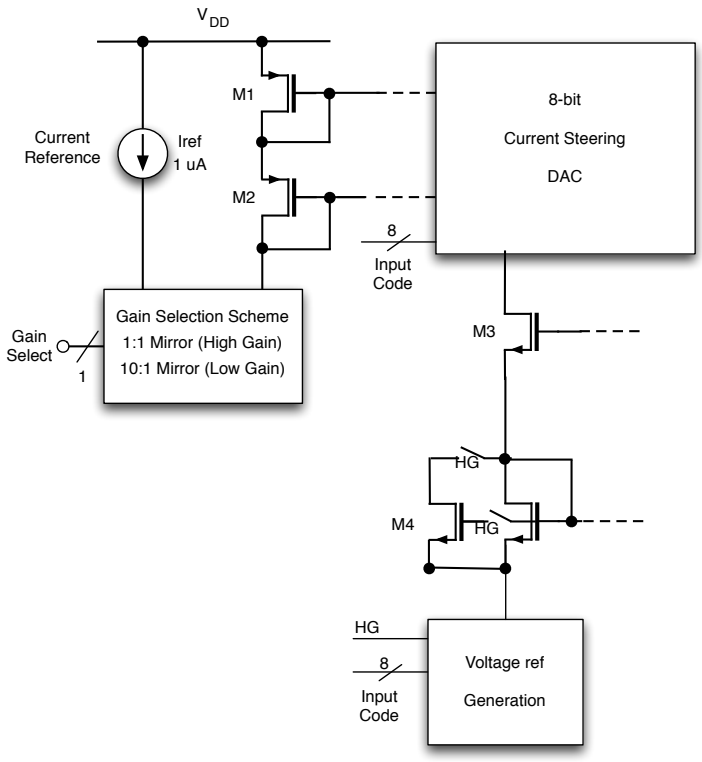

Figure 2.4: Schematics of the new version of periphery circuits.

has been changed, maintaining the same topology. The part of cascode current mirror hosted in the periphery is now controlled by the HG control signal as shown in Fig. 2.4. With some simple switches it is possible to change the dimension of the transistor of the current mirror. The same bit controls the part of the current mirror in the pixel, in this way the mirror ratio is fixed in both working modes, and it is equal to 10:1 as in the previous version (the current is reduced by a factor of 10 in the pixel). Concerning the coarse DAC the scheme shown in Fig. 1.14 is maintained. The transistors dimension was optimized for noise performance, and a capacitor C was added as indicated in Fig. 2.5.

The capacitor C introduces a very low cutoff frequency f_c. This low-pass

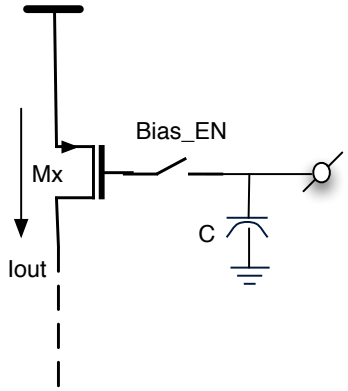

Figure 2.5: Schematics of the in-pixel part of the coarse DAC. Capacitor C, added in this new version, is shown.

filtering was added in order to minimize the noise contribution coming from the periphery. The f_c of the filter could be obtained using:

$$f_c = \frac{1}{2\pi \frac{1}{g_m} C_{TOT}} \tag{2.3}$$

where $C_{TOT} = 2^N C$, and N is the number of capacitors connected in parallel, which is equal at the number of the pixels in the matrix. Because the dimension of the matrix is 64×64 there are 4096 capacitors connected together in parallel, in this way a very low f_C was obtained and noise is effectively filtered. After mounting the ASIC onto the sensor, it is possible to disable the bias current opening the switch controlled by the Bias_EN control bit. It is possible to see that the capacitors are connected together even if the switch is open, so the value of the f_C does not change varying the number of enabled pixels.

In-Pixel Circuits

As already mentioned, the new version of the injection circuit requires the HG control bit to be routed inside the pixel. This could be a problem: an additional control bit in the pixel means an additional line to be routed through the

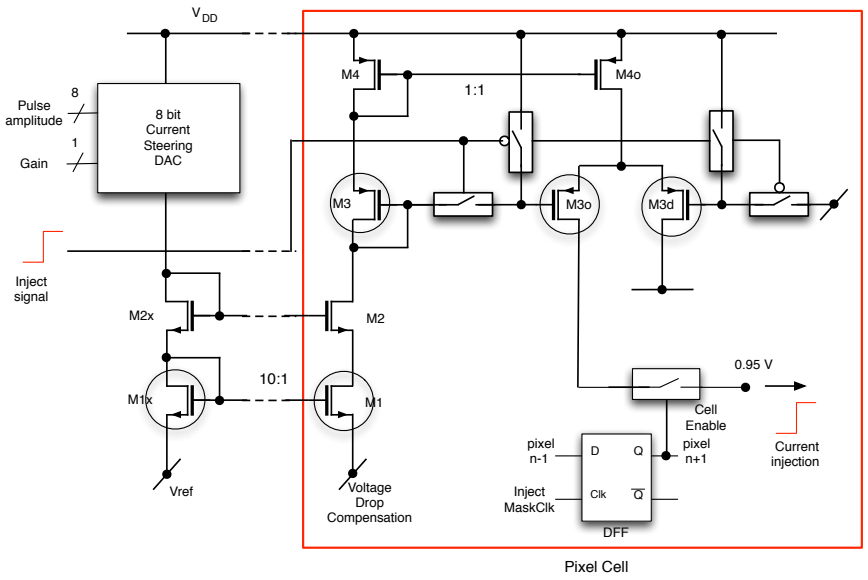

Figure 2.6: Schematics of the new version of pixel circuits.

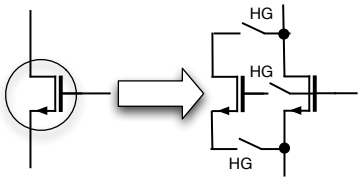

Figure 2.7: In the schematics reported in this chapter, this graphical representation is used.

matrix, which may generate routing problems and parasitic coupling along the line. To prevent such problems HG signal is controlled as a static bit, so it does not need a dedicated line. This bit is stored into the In-Pixel' shift-register which contains all the static bits used into the pixel, and it is loaded during the initialization phase (when the DAC input code, and so the injected current or charge, is loaded). As shown in Fig. 2.6 the right part of the current mirror is controlled by the HG bit, so that the dimensions of those transistors change together with the ones of the current mirror hosted in the periphery. The current ratio is 10:1, and the linearity performance are optimized. The

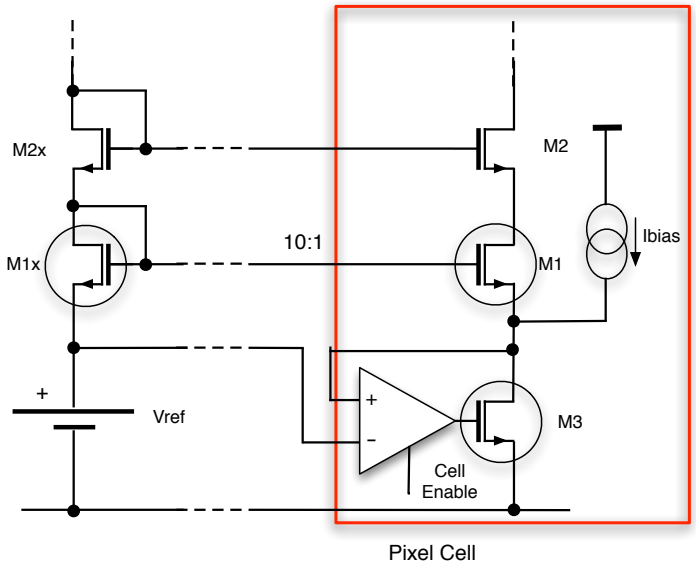

Figure 2.8: Schematics of the new version of voltage drop compensation circuit.

in-Pixel part of the voltage drop compensation circuit has been changed. The MOS connected at the output of the amplifier (M_3) is controlled by the HG signal, and it is biased by an additional bias current (I_{bias}). In this way M_3 is biased in saturation region in all the combinations of DAC input code and pulser working mode. So it is possible to achieve a very good phase margin of the system together with a small bandwidth of the amplifier. A narrow band together with a good phase margin is important because the amplifier in Fig. 2.8 has ideally to work only in DC. Its output has to be constant when the inject signal (show in Fig. 2.6) changes. If so the drain current of $M_1 \sim M_4$ in Fig. 2.6 remains constant, so the settling time is fast. The narrow band of the amplifier also filters noise contributions coming from amplifier and periphery circuits, and it reduces the white output noise.

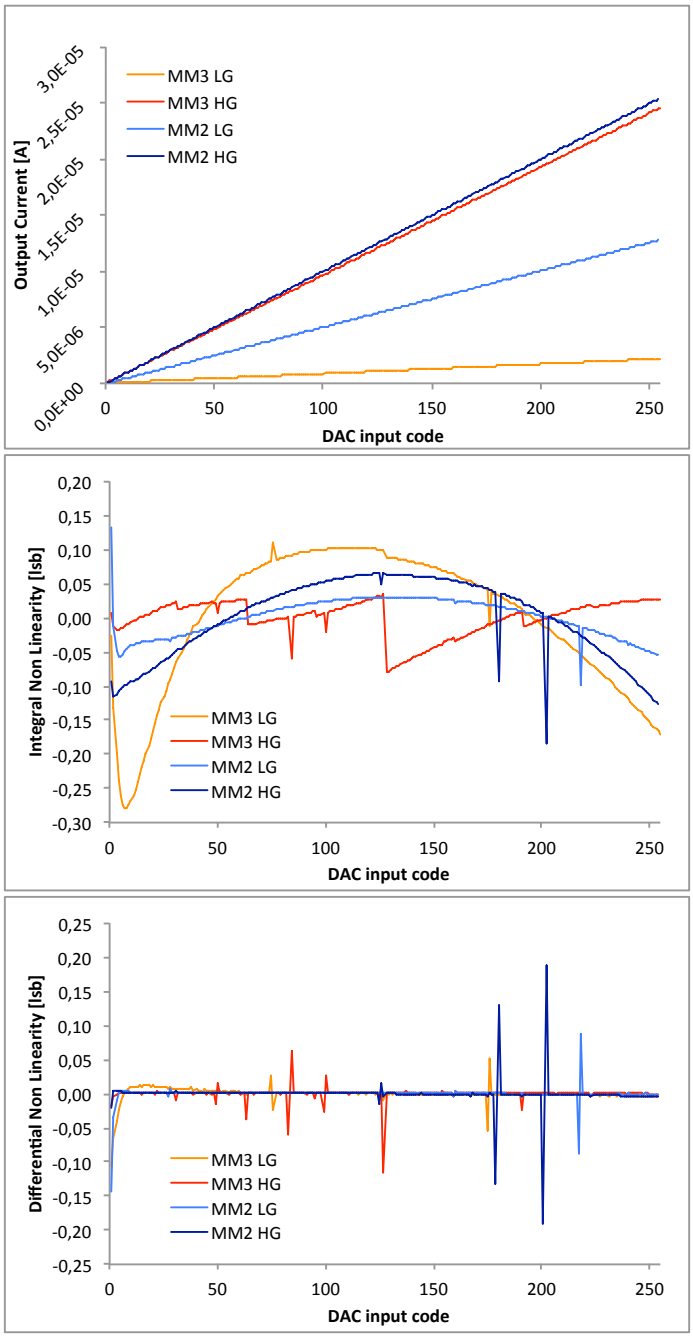

Figure 2.9: Comparison of output current in `DSSC_INJ3` and the current pulser of `DSSC_INJ2` as a function of input DAC code both in High and Low gain configurations (upper plot). Integral and Differential non linearity of both `DSSC_INJ2` and `DSSC_INJ3` as a function of DAC input code. Both in high and low gain configuration (lower plot).

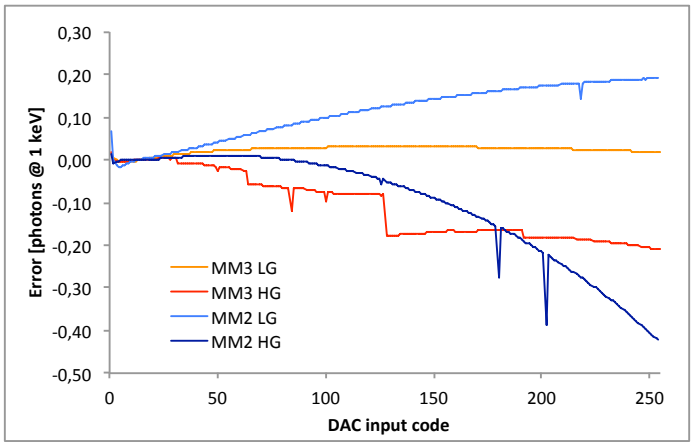

Figure 2.10: Linearity error simulated in numbers of photon @ 1 keV for both `DSSC_INJ2` and `DSSC_INJ3` as a function of DAC input code. Both high and low gain are shown.

2.2.2 Simulation results

The new version of the injection circuits was integrated in the prototype matrix MM3. At the moment measurements results are not available,so in the following sections only simulation results will be shown . The circuit has been evaluated in terms of linearity and noise as the previous version. The `DSSC_INJ3` has been simulated also in transient mode in order to evaluate the timing performance. All the simulations results will be shown in the following, compared with the simulations done on the `DSSC_INJ2` injection circuit.

Linearity

In order to evaluate the linearity of the system its output current was simulated as a function of the input DAC code. The linearity was evaluated in terms of differential and integral non linearity using equations 1.11 and 1.10. In Fig. 2.9 the results of simulation are shown compared with the ones for `DSSC_INJ2` version.

Looking at Fig. 2.9 it is possible to see that in high gain the output current range in the new pulser version is really close to the range in the old one. In

low gain, instead, the output range is smallest then in DSSC_INJ2 because the specifications regarding the output range for the low gain configuration are changed, and that range was reduced. Good results was obtained in terms of both integral and differential non linearity. The maximum value simulated for DSSC_INJ3 is really close to the one simulated in the previous version. In order to have a better comparison between the two different injection circuit versions, the INL shown in 2.9 was recalculated and expressed in number of photons @ 1 keV. The linear fitting was done only on the current corresponding to the first 20 DAC input codes. In 2.10 the results of that elaboration are shown. By evaluating the error in term of number of photons @ 1keV with the new injection circuit version it is possible to observe that the error in low gain for the DSSC_INJ3 is close to 0. This is expected due to the small dynamic range with this configuration. Concerning the high gain mode, the error is smaller in the new injection circuit version with respect to the previous one by a factor of two. The improvements in term of linearity in the new version have been obtained by the possibility to use the HG control signal (as shown in Fig. 2.7) at pixel level. In this way it was possible to optimize the dimension of transistors, and so, the performances of the injection circuit, for each gain mode.

Timing

The DSSC_INJ3 injection circuit was simulated in transient mode in order to evaluate its time domain response, and it was compared with the time domain simulations of the DSSC_INJ2. Time performance of the injection circuit has been taken into account by simulating the output of both high and low gain mode during a transition from low to high logical level of the injection signal and with different DAC input codes in both gain mode. In Fig. 2.11 the transient response of the output current has been shown as an example. In all the configurations shown in the picture, the response of the output of the new version is faster than the previous one. In order to evaluate the timing performance of both the injection circuit versions the settling time parameter is taken into account. The settling time ($t_{SETTLING}$) is the time needed by the output signal to settle within a value lesser or equal to the 10% of the steady

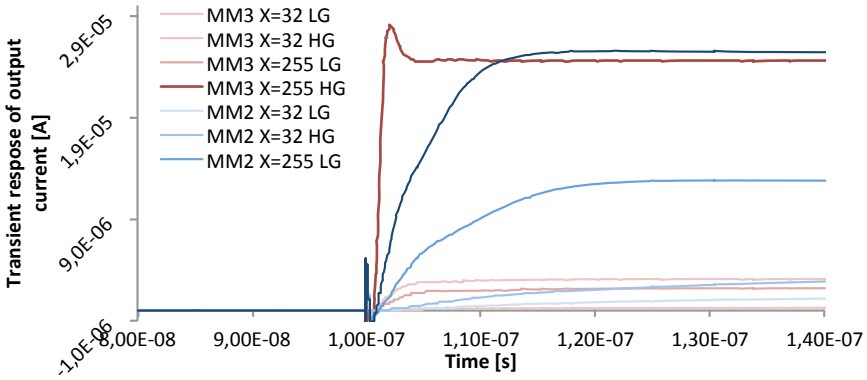

Figure 2.11: Transient output for both `DSSC_INJ2` and `DSSC_INJ3` for different DAC input code, in high and low gain. The input injection signal change at Time = 100 ns.

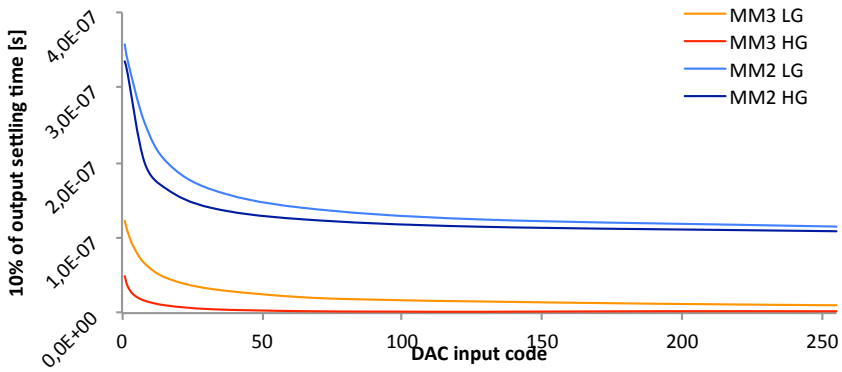

Figure 2.12: Settling time of the output at the 10% of the final current.It is possible to see a significant improvement in the time performances of `DSSC_INJ3` respect to `DSSC_INJ2`

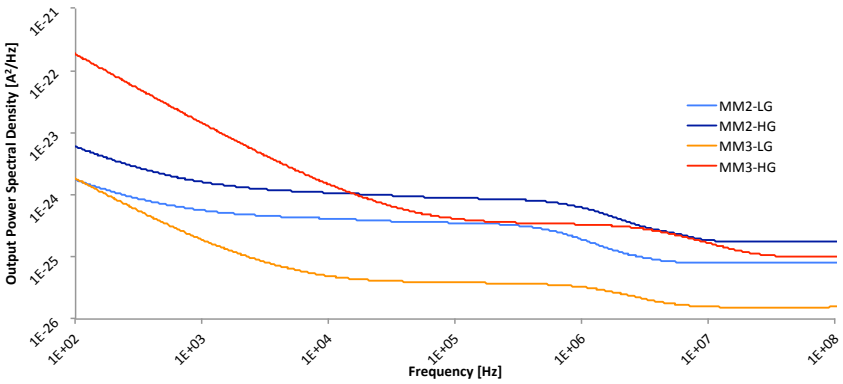

Figure 2.13: Output power spectral density in bot High and Low gain for `DSSC_INJ2` and `DSSC_INJ3`

value, in order to take into account possible overshoots. The simulated value of $t_{SETTLING}$ were reported in Fig. 2.12, where improvement in term of speed of the new version is more evident. These improvements become possible due to the use of the HG signal in the pixel circuits, and also thanks to the new voltage drop compensation circuit shown in Fig. 2.8. Adding the current generator I_{bias} the output transistor M_3 is correctly biased for all the gain mode and DAC input code. In this way it is possible to achieve a better phase margin of the amplifier, and so a faster settling time of the output current. Fig. 2.12 show that for both `DSSC_INJ2` and `DSSC_INJ3` version the high gain mode is faster then the low gain, and the settling time decreases, increasing the DAC input code. The reason is that, looking at Fig. 2.6, the settling time is inversely proportional at the value of the current which charge the gate capacitance of $M_{3,o}$, and that current is equal to I_{out}, so for low value of output current, corresponding at the first DAC codes the settling time performance are the worst.

Noise

A characterization in terms of noise performance of `DSSC_INJ3` has been done simulating the output power spectral noise density for both the output of the

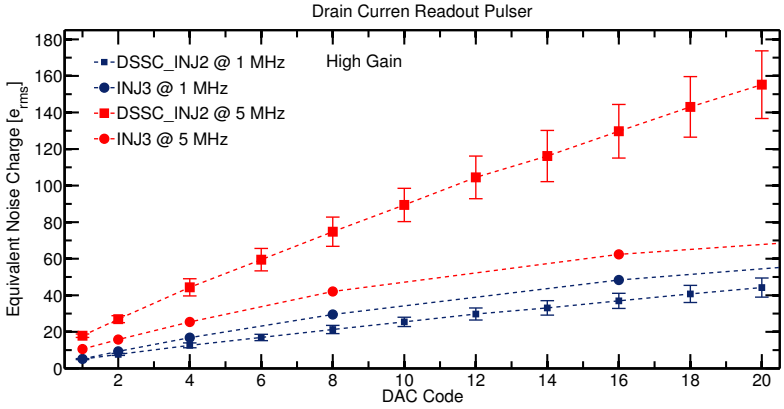

Figure 2.14: Comparison between The ENC simulated for `DSSC_INJ2` and `DSSC_INJ3` in High gain at minimum injected current at difference integration time.

`DSSC_INJ3`. The simulation was performed in the same frequency range used for the measurement of the `DSSC_INJ2` (from 100 Hz to 100 MHz). `DSSC_INJ3` as `DSSC_INJ2` is not optimized for noise performance at the output of the pulser. In fact for low input DAC code the dominant noise contribution is the one coming from the coarse DAC, so, as it is possible to see by the simulation, in the new version of the injection circuit the noise from the pulser is approximately equal to that in the previous version. Instead, an improvement in the noise coming from coarse DAC was achieved. As an example of the noise at the output of the pulser in Fig. 2.13 the output noise power spectral density is shown.

In Fig. 2.13 it is possible to see that in the new version the $1/f$ noise contribution is bigger than in the previous one, instead the white noise is smaller in the new version. From the output noise spectrum it is possible to extract the white and $1/f$ noise coefficients, and using equation 2.2 it is possible to calculate the equivalent noise charge rellevant to the current at the output of the pulser. The result is shown in Fig. 2.14 at different integration times for both versions of the injection pulser. For short integration times (τ), the dominant term in equation 2.2 is the white noise, instead, for long integration

times, the second term, proportional at the flicker noise, becomes dominant. So the new version of the injection circuit has better performance in terms of ENC for the high frequency operation, but, due to the smallest $1/f$ noise, the `DSSC_INJ2` has better performance in the low frequency operation.

As described in this chapter, in the new version of the injection circuit the coarse DAC was optimized for noise performance. The simulation of the power spectral density of the output current of the coarse DAC is reported in Fig. 2.15 for both `DSSC_INJ2` and `DSSC_INJ3`. The spectrum related to the new version is under the old one in the entire frequency range. Using equation 2.2 ENC data were extracted and reported in Tab. 2.3 together with the ENC results for the pulser output. Due to the optimization done in the new version for the noise performance of the coarse DAC, the ENC values are better than in the previous version by a factor of 7 for all the integration times. The results for the pulser are similar to the previous version with an improvement for the higher frequency of operation.

Table 2.3: ENC expressed in numbers of electrons for different readout speed .

	ENC [e^-]			
	DCR Pulser		Coarse DAC	
Speed [MHz]	`INJ2`	`INJ3`	`INJ2`	`INJ3`
5.0	14.4	10.6	685	91
2.5	7.3	6.6	350	53
1.0	4.1	5.2	196	39

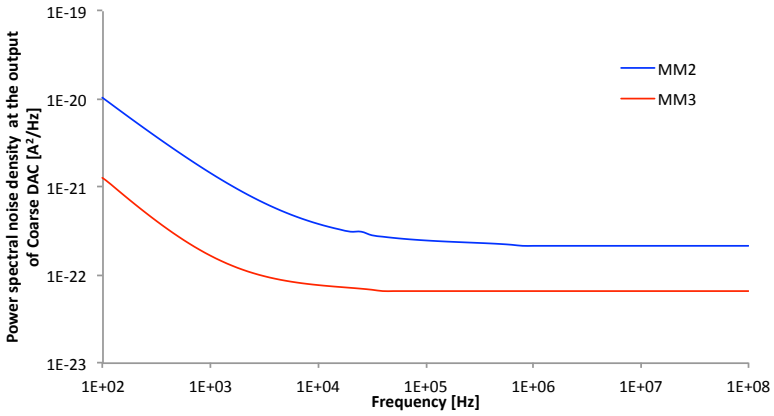

Figure 2.15: Output noise current spectrum of the coarse DAC for `DSSC_INJ2` and `DSSC_INJ3` compared with the output noise of the DEPFET

Chapter 3

Serial data link in LVDS standard

The DSSC chip will be controlled by fast (up to 800 MHz) differential LVDS signals which are generated in a discrete clock driver chip operated at 3.3 V and in an FPGA as shown in Fig. 3.1. Therefore, the dc levels of these LVDS signals will be larger than the supply voltage of the DSSC ASIC of nominally 1.2 V. In order to nevertheless receive the signals without further coupling networks (for space and performance reasons), an LVDS receiver has been developed which can cope with signals above the supply (common mode voltage of up to 1.4 V). To send data off chip, a corresponding LVDS transmitter has been designed. It is based on a full bridge configuration with common mode feedback to keep dc levels stable over process, voltage and temperature variations. The design operates at up to 1.6 Gbps, leaving a large safety margin and providing fast edges for safe signal sampling. In this chapter a complete description of the LVDS link will be shown.

3.1 Link architecture and specifications

The output of an LVDS driver is a current supplied by a generator (nominal 3.5 mA) that drives a matched pair of cables. The current passes through a resistance of 100Ω (matched to the characteristic impedance of the cable),

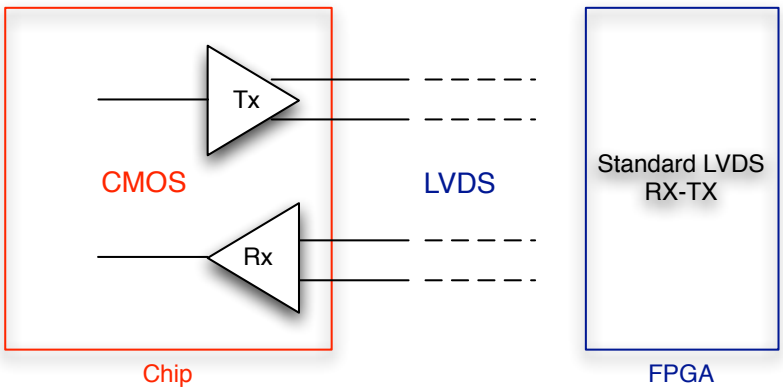

Figure 3.1: Conceptual block of an LVDS link between the DSSC chip and the FPGA.

located in the receiver, then back in the opposite direction, along the other cable. Therefore, there is a voltage drop of 350 mV across the resistor. The receiver, having a high input impedance, detects the polarity of this voltage in order to determine a logical level. This type of signalling is called the current loop. The small amplitude of the signal and the paired cables reduce the amount of radiated electromagnetic noise; in addition, the low common mode voltage of about 1.25 V (as defined in the standard below) LVDS technology can be used with a wide range of integrated circuits with power supply voltages of about 2.5 V. Because of the small differential voltage, about 350 mV, the static power dissipation in the resistor LVDS load is only 1.2 mW. A typical LVDS transmitter-receiver is shown in Fig: 3.2 where we can identify three main components: the transmitter, the receiver and the transmission line.
The benefits of LVDS technology are:

- Elimination of the spike: the current source in the transmitter is always turned on, but changes direction using an H-bridge, according to the logic level to be transmitted. In this way the spikes generated by switching of transistors are reduced.

- Immunity to interference: the cables where information travels are paired,

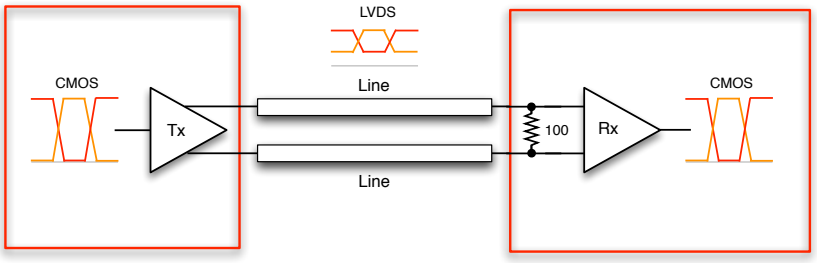

Figure 3.2: Conceptual block diagram of a typical LVDS link.

moreover the information is intrinsically differential: in this way the noise contribution is considerably reduced.

- Low power dissipation: the power dissipation on the receiver load is given by a 3.5 mA current on a resistance load of 100 ohm, so the power dissipation is 1.125 mW. This is a very low value if compared with other transmission standards.

In Tab. 3.1 the specifications of a commercial LVDS link are summarized. With the technology used for this work it is impossible to meet the commercial LVDS requirements in terms of maximum value of common mode and differential mode voltage. In fact, in the worst case the transmitter has to drive an output voltage of about 1.8 V, which is impossible for a technology with a supply voltage of 1.2V. Because of this a new transceiver with different operational parameters has been designed. The redefined parameters are summarized in Tab. 3.2. A transceiver using the specification summarized in Tab. 3.2 can communicate with another another one the specification summarized in Tab. 3.1. So the transceiver described in this chapter can be used in a link like Fig. 3.1.

3.2 Link Receiver

The LVDS receiver is based on the circuit shown in Fig. 3.3. Since the LVDS input signal provided by the FPGA complies with the commercial LVDS stan-

Table 3.1: Commercial LVDS Standard specifications

Parameter	Description	Min	Max	Unit
V_{DM}	Differential output voltage	247	454	mV
V_{CM}	Common Mode output Voltage	1.125	1.375	V
ΔV_{OD}	|Change to V_{OD}|		50	mV
ΔV_{OS}	|Change to V_{OS}|		50	mV
I_{SA}, I_{SB}	Short circuit current		24	mV
tr/tf	Output rise/fall times (200 Mbps)	0.26	1.5	ns
	Output rise/fall times (<200 Mbps)	0.26	1.5	ns
I_{SA}	Input current		20	μA
I_{NOM}	Output driver current		3	mA
V_{TH}	Receive threshold voltage		+100	mV
V_{IN}	input voltage range	0	2.4	V

Table 3.2: Redefined LVDS Parameter

Parameter	Description	Value	Unit
V_{DM}	Differential Mode output Voltage	200	mV
V_{CM}	Common Mode output Voltage	600	mV
I_{NOM}	Output driver current	2	mA

dard (see Tab. 3.1), the input voltage has a maximum value over the supply voltage and the maximum allowed voltage of the transistors of the receiver. The circuit used to convert the input LVDS signal to a CMOS signal is divided into two parts: the first is an input matching resistor net, the second is a voltage comparator. The input resistive net is used to reduce the amplitude of the input signal. The input impedance of that net is given by

$$R_{in} = 2(R_{diff}/2 \parallel 4R_0) \tag{3.1}$$

and the comparator input voltage is given by

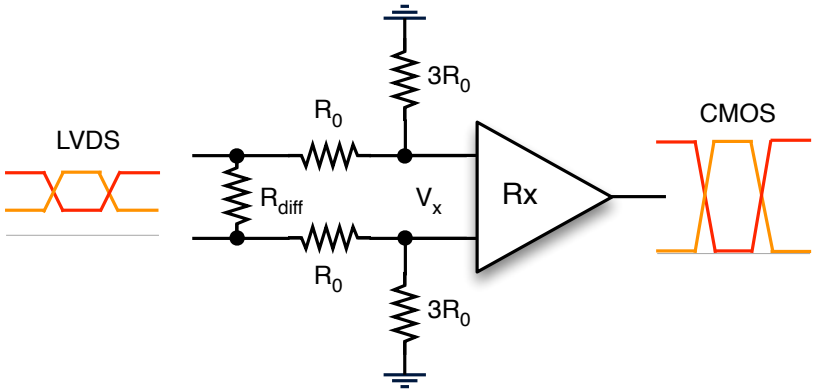

Figure 3.3: Schematic of the designed LVDS receiver. It is possible to observe the resistive input matching net, and the voltage comparator.

$$V_x = \frac{3}{4} V_{LVDS} \tag{3.2}$$

if $R_{diff} \ll R_0$ and $R_{diff} = 100\Omega$ the input resistance of the receiver is $R_{in} \approx 100\Omega$, and could be correctly driven by the LVDS transmitter on the FPGA. In order to detect the polarity of the input current, so the value of the correspondent CMOS bit, the comparator in Fig. 3.4 is used to detect the differential voltage on the input impedance. It is a typical voltage comparator. The transistors $M_1 \sim M_5$ are an open loop voltage amplifier for the V_{LVDS} input voltage. In cascade with the amplifier output there are two high gain CMOS inverters in order to have a clean CMOS output signal.

3.3 Link Transmitter

The transmitter as shown in Fig 3.5 includes a current driver and a Common-Mode FeedBack circuit (CMFB). The current driver comprises a current source transistor M_1, a current sink transistor M_2, and four MOS current switches $M_3 \sim M_6$ in "H" bridge configuration controlled by the signals D and DB, as follows:

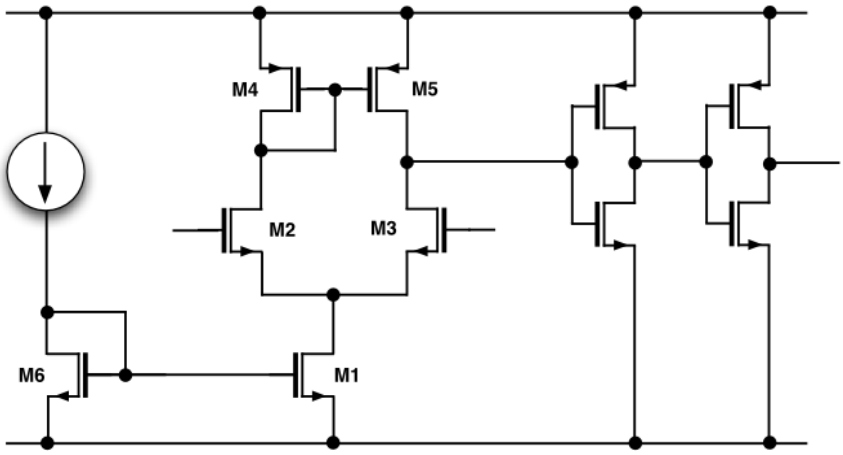

Figure 3.4: Circuit schematic of the voltage comparator. It is composed by an open-loop amplifier in series with a digital buffer.

- Transmission of 1: the switches M3 and M6 are turned on (D = high) while M4 and M6 are turned off (DB = low), the current crosses the R 100 ohm generating a positive voltage drop at the receiver input, so its output goes to the level high.

- Transmission of 0: the switches M4 and M5 are turned on (DB = high) and M3 and M6 are turned off (D = low), in this case the polarity of the current through the resistance is reversed and then generates a voltage drop negative input to the receiver, so its output goes to the level low.

With a nominal 100Ω termination resistor at the receiver, both the common-mode voltage V_{OCM} at the transmitter output and the differential voltage V_{OCM} at the receiver input should fall within the LVDS standard specification over the full range of process, supply voltage and temperature (PVT) variations. As other differential output circuits such as a fully differential operational amplifier, a main problem associated with the differential approach is the shifting of V_{OCM} from the design value which may push the transistors in transmitter and receiver out of the proper operating regions.

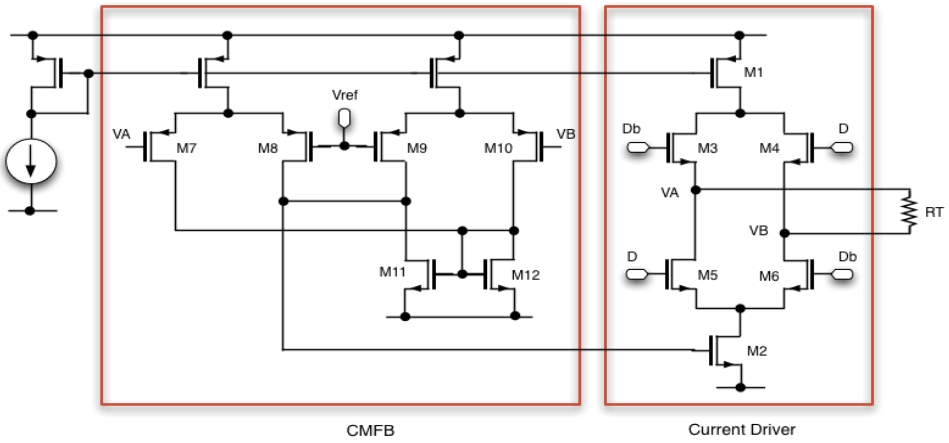

Figure 3.5: Circuit schematic of the LVDS transmitter.It is possible to see the common mode feedback amplifier and the transmission current driver controlled by the input CMOS signal.

The feature of the transmitter shown in this chapter is the CMFB scheme which consists of no resistors as shown in Fig. 3.5 (frequency compensation is not shown for simplicity). The operating principle is the following. As soon as the drops of V_A and V_B cause V_{OCM} lower than V_{REF} , the output voltage of CMFB circuitry V_{FB} decreases which in turn reduces the current of M_2. Thus, V_{OCM} will be increased. The reverse process is also true when V_A and V_B cause a V_{OCM} higher than V_{REF}. By some simple algebraic manipulation, the analytic relation between V_{OCM} and V_{REF} can also be derived. Referring to Fig. 3.5, the currents of $M_7 \sim M_{10}$ are:

$$I_{M_7} = \left(\frac{V_A - V_{REF}}{2}\right) g_m \tag{3.3}$$

$$I_{M_8} = \left(\frac{V_{REF} - V_A}{2}\right) g_m \tag{3.4}$$

$$I_{M_9} = \left(\frac{V_{REF} - V_B}{2}\right) g_m \tag{3.5}$$

$$I_{M_{10}} = \left(\frac{V_B - V_{REF}}{2}\right) g_m \tag{3.6}$$

Where g_m is the transconductance of $M_7 \sim M_{10}$ With the same gate-source terminal voltage, the currents of M11 and M12 are equal:

$$I_{M_{11}} = I_{M_8} + I_{M_9} = I_{M_{12}} = I_{M_7} + I_{M_{10}} \tag{3.7}$$

After substituting the $I_{M_7} \sim I_{M_{10}}$ terms in Eq. 3.7 with Eq. 3.3 to Eq. 3.8, the following desired result is obtained:

$$V_{OCM} = \frac{V_A + V_B}{2} \tag{3.8}$$

In a transmission LVDS standard, at the receiver input a voltage differential $V_{ODM} = V_A - V_B$ is applied corresponding to the voltage drop generated across the resistor $R_T = 100\Omega$ by a current of 3.5mA. The common mode voltage is given by $V_{IN,MAX}/2$. As indicated in the previous paragraph, in this work the LVDS standard has been redefined, so the current delivered by the generator is nominally equal to 2 mA, while the design value for the common mode voltage is 600 mV.

3.4 Measurements

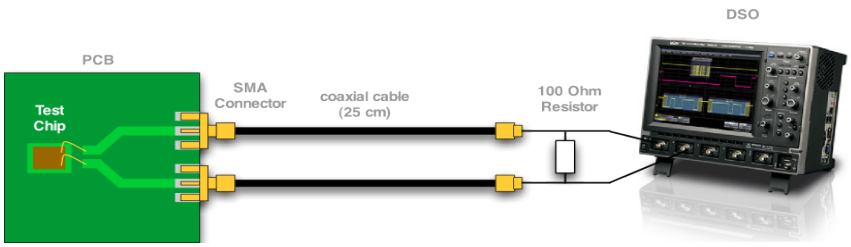

Figure 3.6: Set up.

In order to test the designed LVDS transceiver a dedicated set-up has been developed. The set-up consist of a PCB board designed properly for high fre-

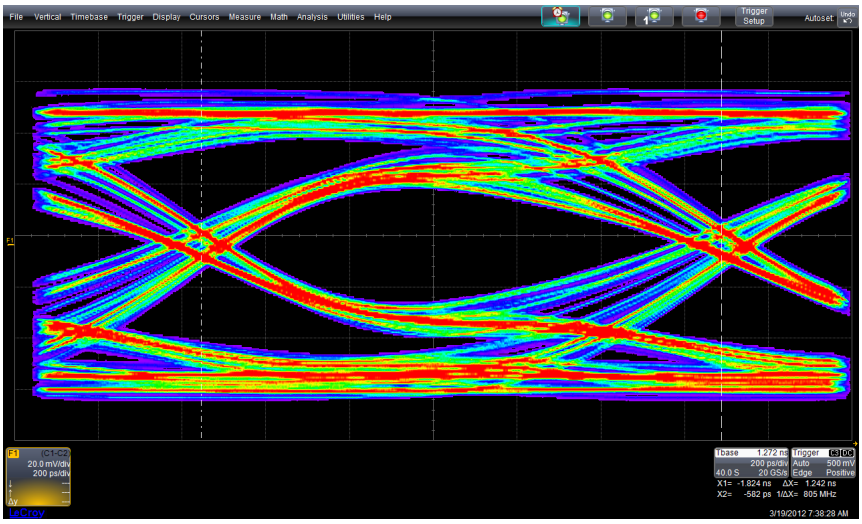

Figure 3.7: eye.

quency operation. The chip is directly connected by wire bonding to the PCB in order to reduce the capacitive parasitics. The input signal is provided by a pattern generator Tektronix DTG 5334 and the output signal was measured by an oscilloscope Le Croy wave-pro 735 ZI.

Transmitter

Fig. 3.6 shows a simplified version of the set-up used for the transmitter measurements. By the pattern generator (not shown in the picture) a 800 MHz CMOS signal (0 - 1.2V) is provided at the input of the transmitter with a random pattern. Its outputs are connected to the 100Ω R_T resistor. By a differential probe, the differential voltage on the resistor is measured on the oscilloscope. The eye diagram reported in Fig. 3.7 represents the output of the transmitter. Looking at the diagram is possible to see that the output meets the specification shown in Tab. 3.1 and Tab. 3.2, so the LVDS signal provided by the designed transmitter can be detected by a commercial LVDS receiver.

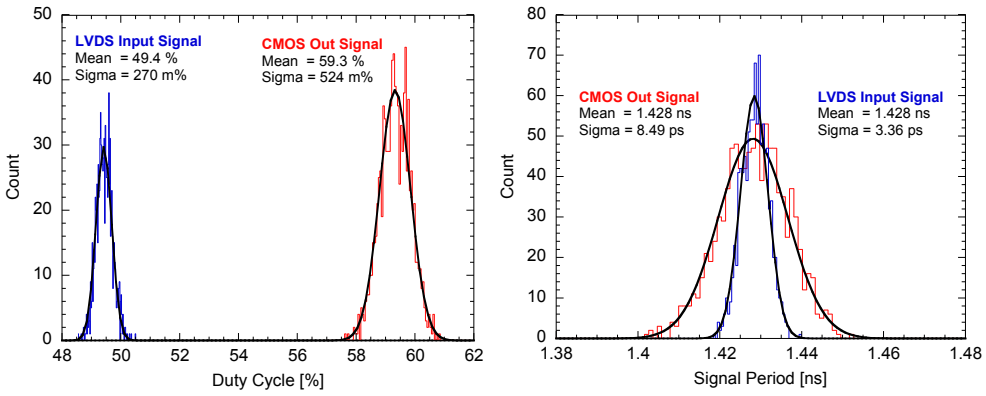

Figure 3.8: jitter.

Receiver

On the DSSC chip the reference signal for the in-pixel ADC is generated off chip and transmitted using an LVDS signal. Since the performances of the ADC are degraded by the jitter of the reference signal the LVDS receiver has to introduce a low degradation of this parameter of the received signal. An LVDS input signal (0.95V - 1.4V) is provided at the input of the receiver. In this case, to reduce the capacitance of the probe, an active micro probe was used, and the output signal was sensed directly on the output pad on the chip. The input signal was a 50% duty cycle square wave with a 700 MHz frequency. In Fig. 3.8 the output frequency and duty cycle are shown. Is possible to observe a shift of the duty cycle of the output signal of the order of 10%, but it will be corrected by a duty cycle correction block which will be integrated in the DSSC chip. The jitter of the output has a value of about 0.5% for the duty cycle and 8.5 ps (0.5%) for the period. These values are compatible with the specification foreseen for the ADC, so the receiver can be used in the DSSC chip.

Conclusion

This thesis discussed the design of a high-linearity, low dispersion, low noise injection circuit to be used for pixel-level calibration of detector readout electronics. The proposed circuit is implemented in a 130 nm CMOS technology and will be part of the 64×64 pixel DSSC readout chip which is currently under development for applications at the European XFEL facility. The injection circuit is comprised of two main parts: the high-accuracy 8-bit DAC located in the chip periphery and a pulser hosted by each pixel cell. Since two options for the detector readout are currently under investigation, two pulser circuit architectures have been designed. Simulation results have shown that in both solutions the pulser is able to emulate the signal delivered by the DSSC sensor in the whole dynamic range and with the required resolution. The request of linearity and noise has been respected for both the pulsers options. Chapter 2 discussed the performances of the injection circuit as a part of DSSC chip. It has been verified that the circuit is able to cover the full dynamic range of the signals delivered by the sensor with the required resolution. The same chapter described an improved version of the current option of the injection circuit. This new version ensured a better performance in term of linearity noise and speed. The results of the simulation done on this version of the injection circuit were shown to be consistent with the results of the simulation done on

the previous version. Finally, chapter 3 described an LVDS transceiver used in the DSSC chip as an interface between the chip and the FPGA used for the output data readout. The functionality of the lock together with 800 MHz measurement has been shown in the chapter.
The activity described in this thesis will continue with the characterization of the circuits in a complete readout channel. After the characterization, a complete 64×64 readout test matrix will be integrated and tested together with the DEPFET sensors matrix.

Appendix A

X-ray Free Electron Lasers (XFEL) will provide full coherent light of hard X-rays in short pulses of few femtoseconds (fs). This time scale is of particular importance because atoms in molecules or solids oscillate around their equilibrium positions with periods of a few hundreds of fs. Using such a source it will be possible to probe atomic arrangements like snapshots after an external perturbation or as a function of an intrinsic excitation and to study intermediate states and pathways of chemical reactions and phase transitions on a fs-time scale. Moreover, due to the full coherence of the FEL pulses and its high intensity scientists have the dream to solve the complicated structure of molecules, clusters or large bio-molecules quasi by a single shot experiment before the object becomes destroyed due to the high laser excitation. Typical sets of experiments will be of spectroscopic nature where the emission lines of a highly excited state of specimen must be recorded as a function of energy. Another set of experiments consists of the detection of elastic or inelastic scattering from a sample where a set of diffraction lines must be recorded as a function of position in space. The realization of these experiments has a high demand for appropriate detectors. All scattering events have to be detected in space and time and energy. Considering the particular time structure of XFEL the detector must be able to "record" a single shot or a series of shots and must

be ready to "record" a second shot or shot series after a certain delay time. The DSSC is offered to serve several of the experiments. The detector will be able to detect up to $10^4 1keV$ photons in one single pixel. The final detector module will have a total sensitive area of 400 cm^2, composed of 16 monolithic detectors comprising 512x128 pixels each. It is capable to operate within the XFEL bunch structure and complies with the anticipated number of photons per frame per pixel. The insensitive area between the individual detector modules is less than 15 %. The detector system is based on an active pixel sensor with a DEPFET as a central detector amplifier structure. The detector chip is bump bonded to an ASIC which comprises amplification, shaping, analog to digital conversion, signal storage and data transfer. The silicon sensor (DSSC) will be fabricated in a format of 128×512, while the analog/digital ASICs will have a format of 64×64. The sensor has been designed so as to combine high energy resolution at low signal charge with high dynamic range. This has been motivated by the desire to be able to be sensitive to single low energy photons and at the same time to measure detector signals corresponding to up to 1000 photons of 10keV or 10000 photons of 1keV. In order to fit this dynamic range into a reasonable output signal range, achieving at the same time single photon resolution, a strongly non linear characteristics is required. At low signals the required sensitivity is determined by the noise of the system while at high signals the Poisson fluctuations in the number of produced photons dominate. The standard way to obtain a non linear response (for example logarithmic) is the coupling of a detector with linear response to an electronic circuit with non-linear characteristics. This is needed especially when using integrated circuits with low power supply voltage as is the case in submicron technology. Nevertheless a non linear characteristic of the readout electronics increases the complexity of the circuit design. The new proposed DEPFET solution shifts quite naturally the non-linearity into the detector thereby facilitating considerably the task of the electronics. At the same time the DEPFET charge handling capability is enormously increased with respect to standard DEFFETs. We will describe the basic DEPFET structure, operation principle and properties and its natural application as a building block of a pixel detector before concentrating on the specific solution foreseen for XFEL.

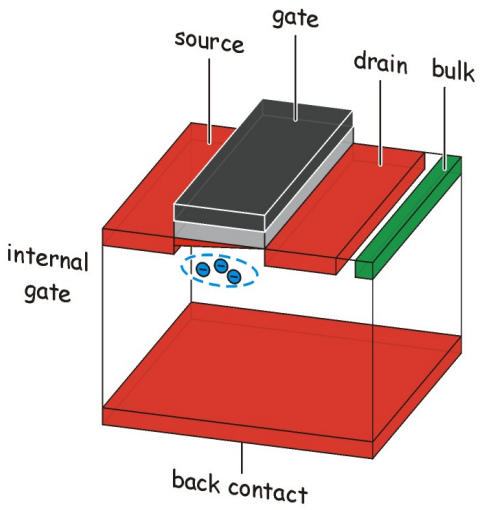

Figure 3.9: The concept of a DEPFET. The signal electrons are collected in a potential minimum (internal gate) located below the channel of a FET located on top of the fully depleted bulk.

Fig. 3.9 shows the principle of a DEPFET [21]. A Field Effect Transistor is located on one surface of a silicon wafer and a large area diode on the opposite surface. The n-type bulk is fully depleted with the help of a sideward located n+ doped clear contact. Suitable doping and choice of bias voltages creates a potential maximum right below the channel of the transistor. This is call Internal Gate IG. Electrons generated by radiation are collected in the internal gate. They create mirror charges in the channel, thereby increasing channel conductivity. For fixed source and external gate voltages the transistor current is increased. Alternatively for fixed transistor current (source follower) the source voltage will change. Applying a sufficiently strong positive voltage pulse to the clear (bulk) contact removes all charge from the internal gate. Therefore there is no statistical variation in the amount of leftover charge and the reset noise is zero. The charge can be measured by the current increase after charge collection or by the current difference before and after clearing of the IG. The device has combined properties of detector, amplifier and charge

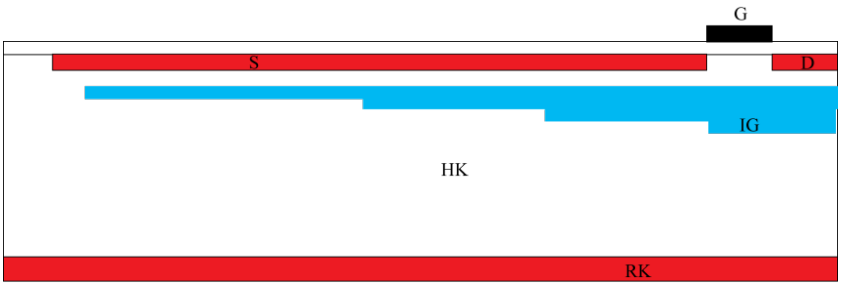

Figure 3.10: The first signal electrons are collected in the potential well exactly below the gate (IG) due to its most positive potential. If that area is filled up with electrons the next (blue) disk -extending below the source and the gate- collects electrons and so forth. Only the fraction of the additional charge that arrives below the internal gate (IG) is effective in modulating the transistor current. This leads to the non-linear amplification behavior of the DSSC.

storage (memory) cell. The bulk of the device is fully depleted and therefore sensitive to radiation and the backside diode can be used as a homogeneous non obstructed thin entrance window. Full depletion of the device extends the sensitivity to higher X-ray energies and the backside entrance window may be optimized for low energy X-ray sensitivity or, using anti reflective coating, for high quantum efficiency in the optical regime. The DEPFET is a natural building block for a pixel detector as it combines the properties of detector, amplifier and storage cell in a simple structure [22]. For XFEL the high repetition rate requires parallel readout of all pixels. Therefore a separate readout channel is required for each pixel and all pixels have to be powered during the pulse train. Nevertheless a new type of DEPFET solves the challenge of providing excellent charge resolution for low signals as required for single photon detection with very large charge handling capacity for pixels containing the overlap of very many photons. This is accomplished by providing a strongly non-linear current-charge characteristics.

The basic concept is shown in Fig. 3.10. The internal gate extends into the region below the large area source. Small signal charges assemble below the channel only, being fully effective in steering the transistor current. Large signal

charges will spill over into the region below the source and correspondingly be less effective in steering the transistor current.

The DEPFET is surrounded by a small drift chamber and a clear electrode has been added to the DEPFET. This concept can be applied with very similar properties to DEPFET pixels with areas from $75 \times 75 \mu m^2$ up to $300 \times 300 \mu m^2$. The final size will mainly be given by the area of the ASIC and the anticipated properties of the interconnection technology.

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