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LINEARIZATION TECHNIQUES OF DVB-H TUNERS IN CMOS TECHNOLOGY

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Index

Introduction

The evolution of cellular phones involves both new solutions for chips used and the definition of new standards. The DVB-H (Digital Video Broadcasting–Handheld) standard indeed is an evolution of the DVB-T (Digital Video Broadcasting-Terrestrial) as response of specific industry requests for TV signals on portable devices. This new broadcast technology is totally backward compatible with the terrestrial digital television standards but it allows, with new features, to receive signals with high quality and a lower power consumption that are key points in a handheld device. Different architectures of

chipsets have been considered to satisfy this growing request of transmitting broadband services to mobile radio terminals and comparable pocket sized portable devices. In fact, an important end point in this kind of wireless communication design consists in cover the wideband of the DVB-H (VHF III-UHF IV-V), increasing portability and performances, reducing costs and dimensions. The possibility to share different resources and to enhance the degree of reconfigurability in function of the scenario dependent on the channel conditions is a outset for the implementation of a more efficient chipset.

This PhD thesis is centered on the reduction of power and system costs of a broadband DVB-H TV tuner implementing a new kind of single to differential LNA and a multimode downconverter stage. Indeed, the application of an IM2 linearization technique permits to implement a single to differential front-end with performances comparable with a fully differential one, eliminating the off-chip baluns.

The first two chapters show an introduction of the standard peculiarity, the derivation of the system requirements and a description of the state of the art of wideband amplifiers.

In particular, the *first chapter* describes, after a brief historical overview of the DVB-H standard, the main technology elements introduced: the power saving algorithm based on time multiplexed transmission of different services (time slicing), the use of an enhanced error protection scheme (MPE-FEC), an additional network mode (4k-mode) assuring more flexibility in designing single frequency networks. The specifications in terms of linearity (IIP2 and IIP3) and noise (NF) for the design of a DVB-H TV tuner are derived.

In the *second chapter*, the choices of a single to differential architecture and of a single wideband LNA are motivated. The different broadband LNA solutions are compared and in particular the CG-CS (or noise cancelling) topology is studied in terms of noise and linearity. Analytical expressions for the in band noise and second and third order distortion are summarized.

The last two chapters illustrate the theory of a linearization technique to improve the IIP2 performance of a single to differential wideband LNA and the circuital blocks designed and integrated in this PhD. Consequently, the circuital solution designed to realize an LNA with IM2 cancellation using a feedback is implemented and integrated in a test chip in 90nm TSMC technology. The application of the circuital solution is extended to a complete front-end that is integrated in a test chip in 90nm TSMC technology with a multimode passive mixer.

Specifically the *third chapter* presents a solution to achieve for a single to differential LNA a similar IM2 than a fully differential topology. The theory of this technique and circuital solution proposed in literature is exposed. A new low noise solution with analytical expressions for IM2, IM3 and noise figure is studied and designed.

The experimental results obtained from measurements of a wideband LNA test chip with simultaneous minimum noise and IM2 cancellation are presented.

Finally, in *chapter four* , the additional problems in terms of non linearity for a wideband TV tuner are discussed. This part shows the choice of the front-end architecture and the design of the downconverter stage. The multimode approach is applied to different blocks to get different configurations depending on the different scenarios. A Test chip of the designed solution of the single to differential multiband multimode front end has been integrated and measured. The front end performances are comparable with the fully differential ones published in literature.

1

DVB-H: Digital Broadcast Services to Handheld Devices

The system for fixed and portable reception of digital terrestrial television, known as digital video broadcasting-terrestrial (DVB-T), has been available for several years. Making this available for handheld devices is an obvious next step, along with integration into global system for mobile communications (GSM) convergence terminals. In order to support these new applications, the existing DVB-T standard was argumented to include digital video broadcasting-handheld (DVB-H).The new extension brings features that make it possible to receive digital video broadcast type services in handheld, mobile terminals. After an historical introduction in this chapter an overview of the DVB-H standard is presented and the derivation of the key specifications is shown.

1.1 History and Background.

DVB-T

The Digital Video Broadcast (DVB) Project started research work related to mobile reception of DVB-Terrestrial (DVB-T) signals as early as 1998, accompanying the introduction of commercial terrestrial digital TV services in Europe.

In 2000, the UE-sponsored Motivate (Mobile Television and Innovative Receivers) project concluded that mobile reception of DVB-T is possible but it implies dedicated broadcast networks, as such mobile services are more demanding in robustness than broadcast networks planned for fixed DVB-T reception.

Later in 2002, the EU-sponsored Multimedia Car Platform (MCP) project explored the excellent behavior of antenna diversity reception which, introducing spatial diversity in addition to the frequency and time diversities provided by the DVB-T transmission layer, improved sufficiently reception performance to allow a mobile receiver to access DVB-T signals broadcast for fixed receivers. Five years after its inception, DVB-T shows sufficient flexibility to permit mobile broadcast services deployment in cities like Singapore or in Germany.

But, during these five years, consumer habits have evolved, and in early 2002, the DVB community was asked to provide technical specifications to allow delivery of rich multimedia contents to handheld terminals, a property that has been missing in the original DVB-T. This would make it possible to receive TV-type services in a small, handheld device like a mobile phone.

Beyond DVB-T

This approach requires specific features from the transmission system serving such devices:

- as these devices are battery powered, the transmission system shall offer them the possibility to repeatedly power off some part of the reception chain to increase the battery usage duration.
- as the technology is targeting mobile users, the transmission system shall ease access to the services when receivers leave a given transmission cell and enter a new one.
- as services are expected to be delivered in an environment suffering severe mobile multipath channels and high levels of man-made noise, the transmission system shall offer additional means to mitigate these effects on the receiving capabilities.
- the system should be capable to handle a number of reception scenarios; indoor, outdoor, pedestrian and inside a moving vehicle; and, consequently, the transmission system shall offer sufficient flexibility and scalability to allow the reception of

the services at various speeds, while optimizing transmitter coverage. Also, the system should be usable in various parts of the world and should offer the flexibility to be used in various transmission bands and channel bandwidths.

- All this should be achieved with a system based on DVB-T in order to have maximal compatibility with the existing DVB-T networks and implementations.

DVB-H

The work to define such a system within the DVB Project started in the beginning of year 2002 first by defining a set of commercial requirements for a system supporting handheld devices. The technical work then led to a system called Digital Video Broadcasting—Handheld (DVB-H), which was published as European Telecommunications Standards Institute (ETSI) Standard EN 302 304 in November 2004 . This standard is an umbrella standard defining in which way to combine the earlier existing—now updated—ETSI standards to form the DVB-H system.

1.2 System and Standards

DVB-H shall offer broadcast services for portable and mobile usage, including audio and video streaming in acceptable quality. The data rates feasible in practice have to be sufficient for this purpose. For the DVB-H system a useful data rate of up to 10 Mbit/s per channel is envisaged. Transmission channels are planned in the VHF band III [174-240 MHz] and in the UHF III and IV broadcasting bands [470-890 MHz].

DVB-H extensions

DVB-H comprises a bundle of technology elements. The standard uses a power saving algorithm based on time multiplexed transmission of different services. The technique, called *time slicing*, allows for selective access to the desired data and results in a large battery power saving effect. Additionally, time slicing allows soft handover with only one receiver unit. The poor signal reception conditions are thwarted with an enhanced error protection scheme on the link layer. This scheme is called *MPE-FEC* (Multi-Protocol Encapsulation Forward Error Correction). MPE-FEC employs powerful channel coding and time interleaving. Furthermore, the DVB-H standard introduces an additional network mode, the '*4K mode*', assuring more flexibility in designing single frequency networks for mobile reception, and also an enhanced signalling channel for improving access to the services. It should be emphasized that neither time slicing nor MPE-FEC technology elements, as they are implemented on the link layer, touch the DVB-T physical layer in any way. This

means that the existing receivers for DVB-T are not disturbed by DVB-H signals. DVB-H is totally backward compatible to DVB-T.

DVB-H physical layer

About the physical layer, it has four extensions to the existing DVB-T physical layer:

- the bits in transmitter parameter signalling (TPS) have been upgraded to include two additional bits to indicate presence of DVB-H services and possible use of MPE-FEC to enhance and speed up the service discovery.
- a new 4K mode orthogonal frequency division multiplexing (OFDM) mode is adopted for trading off mobility and single-frequency network (SFN) cell size, allowing single-antenna reception in medium SFNs at very high speeds. This gives additional flexibility for the network design. 4K mode is an option for DVB-H complementing the 2K and 8K modes that are as well available. Also all the modulation formats, QPSK, 16QAM and 64QAM with nonhierarchical or hierarchical modes, are possible to use for DVB-H.
- a new way of using the symbol interleaver of DVB-T has been defined. For 2K and 4K modes, the operator may select (instead of native interleaver that interleaves the bits over one OFDM symbol) the option of an in-depth interleaver that interleaves the bits over four or two OFDM symbols, respectively. This approach brings the basic tolerance to impulse noise of these modes up to the level attainable with the 8K mode and also improves the robustness in mobile environment.
- the fourth addition to DVB-T physical layer is the 5-MHz channel bandwidth to be used in nonbroadcast bands. This is of interest, e.g., in the United States, where a network at about 1.7 GHz is running using DVB-H with a 5-MHz channel.

DVB-H user equipment

The conceptual structure of DVB-H user equipment is depicted in Figure 1.1

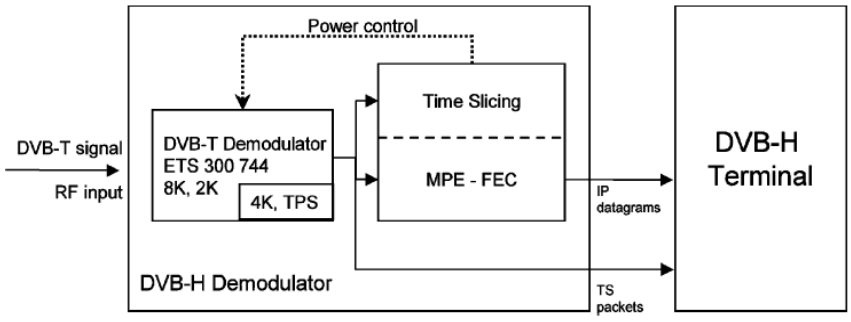

Figure 1.1 :Conceptual structure of a DVB-H receiver.

It includes a DVB-H receiver (a DVB-T demodulator, a time-slicing module, and an optional MPE-FEC module) and a DVB-H terminal. The DVB-T demodulator recovers the transport stream (TS) packets from the received DVB-T RF signal. It offers three transmission modes: 8K, 4K, and 2K with the corresponding signalling. The time-slicing module controls the receiver to decode the wanted service and shut off during the other service bits. It aims to reduce receiver power consumption while also enabling a smooth and seamless frequency handover. The MPE-FEC module, provided by DVB-H, offers in addition to the error correction in the physical layer transmission, a complementary FEC function that allows the receiver to cope with particularly difficult reception situations.

1.2.1 Time Slicing

A particular difficulty of the terminals is the limited battery capacity and the necessity to handle this capacity economically. In a way, being compatible with DVB-T is opposed to this requirement because demodulating and decoding a broadband, high data rate stream like the DVB-T stream involves inevitably a higher power dissipation in the tuner and the demodulator part. An investigation at the beginning of the development of DVB-H showed that the total power consumption of a DVB-T front end was quite above 1 Watt at the time of the examination and was expected not to decrease below 600 mW until 2006; meanwhile a somewhat more optimistic value seems realistic but the envisaged target of 100 mW as a maximum threshold for the entire front end is still inaccessible for a DVB-T receiver. A considerable drawback for the battery-operated terminals is the fact that with DVB-T the whole data stream has to be decoded before one of the services of the multiplex can be accessed. The power saving potential used in DVB-H is derived from the fact that essentially only those parts of the stream have to be received which carry data of the service currently selected. However, the data stream needs to be reorganized in a suitable way for that purpose. With DVB-H, service multiplexing is performed in a pure time division multiplex. The data of one particular service are therefore not transmitted continuously but in compact periodical bursts with interruptions in between.

DVB-T:costant bit rate, high power consumption

This kind of signal can be received time-selectively by the terminals synchronizing to the bursts of the wanted service and switching off during the intermediate time when other services are transmitted. The off-time between bursts gives the power saving. This technique is called *time slicing*. Bursts entering the receiver have to be buffered

DVB-H time slicing :power saving with time selectivity

and read out with a constant data rate, the service data rate, in case of a streaming service.

The standard DVB way of carrying IP datagrams in an MPEG-2 TS is to use multiprotocol encapsulation (MPE). With MPE each IP datagram is encapsulated into one MPE section. A stream of MPE sections are then put into an elementary stream (ES), i.e., a stream of MPEG-2 TS packets with a particular program identifier (PID). Each MPE section has a 12-B header, a 4-B cyclic redundancy check (CRC-32) tail and a payload length, which is identical to the length of the IP datagram, which is carried by the MPE section.

A typical situation for future handheld DVB-H devices may be to receive audio/video services transmitted over IP on ESs having a fairly low bit rate, probably in the order of 250 kb/s. The MPEG-2 TS may, however, have a bit rate of e.g., 10 Mb/s. The particular ES of interest thus occupies only a fraction (in this example, 2.5%) of the total MPEG-2 TS bit rate. In order to drastically reduce power consumption, one would ideally like the receiver to demodulate and decode only the 2.5% portion of interest, and not the full MPEG-2 TS.

High bit rate bursts

With time slicing this is possible, since the MPE sections of a particular ES are sent in high bit rate bursts instead of with a constant low bit rate. During the time between the bursts—the off-time—no sections of the particular ES are transmitted. This allows the receiver to power off completely during off-time; see Figure 1.2. The receiver will, however, have to know when to power on again to receive the next burst. In a particular burst the start time of the following burst of the same ES is signaled via a Δt parameter in the header of all sections of the burst, which makes the signalling very robust against transmission errors. During off time bursts from other time sliced ESs are typically transmitted.

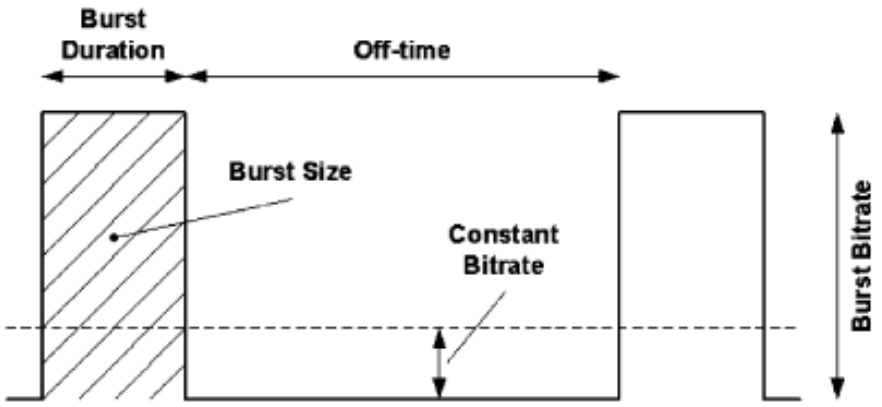

Figure 1.2: Principle of time slicing

Bursts interleaving

The peak bitrate of the bursts may potentially be the full MPEG-2 TS bitrate, but could also be any lower peak value allocated for the ES. If the value is lower than the peak bitrate, the MPEG-2 TS packets of a particular burst may be interleaved with MPEG-2 TS packets belonging to other ESs (DVB-H or other, e.g., SI or MPEG-2 audio/video).Thanks to the flexible Δt signalling there are no requirements to have fixed burst sizes or fixed time between bursts. A variable-bit-rate coded video stream could therefore use a variable burst size and/or a variable time between bursts. It should be noted that one burst could contain several services, which would then share PID but could e.g., be discriminated by different IP addresses. If the average bitrate of the ES is 500 kb/s, the peak bitrate is 10 Mb/s and the burst size is 2 Mb (maximum allowed value), the burst time becomes 200 ms, and the burst cycle time 4 s. The receiver, however, has to wake up a little bit before the burst to synchronize and be prepared to receive the sections. Assuming a figure of 200 ms for the total preparation time, including some margin for Δt jitter, the power saving in the example becomes 90%. It is probable that the actual parameters used for time slicing will be a compromise between power consumption and other factors, such as service access time and RF performance.

90% power saving

1.2.2 MPE-FEC (Multi-Protocol Encapsulation Forward Error Correction)

The MPE-FEC is and additional forward correction in the MPE level. In contrast to other DVB transmission systems which are based on the DVB transport stream adopted from the MPEG2 standard. the DVB-H system is IP (Internet Protocol)-based. therefore the outer DVB-H interface is the IP interface. This determination allows simple combination with other networks as currently in the process of being defined in the *IP Datacast system*. Nevertheless, the MPEG2 transport stream is still used as a physical carrier method. The IP data are embedded into the transport stream by means of the Multi Protocol Encapsulation (MPE), an adaptation protocol defined in the DVB Data Broadcast Specification. On the level of the MPE an additional stage of forward error correction (FEC) is added. This technique, called MPE-FEC, is the second main innovation of DVB-H besides the time slicing. MPE-FEC complements the physical layer FEC of the underlying DVB-T standard. It is intended to enhance the reliable reception especially with handheld devices which make the reception of high data rate streams in a mobile environment difficult.

MPE

FEC

With MPE-FEC the IP datagrams of each time sliced burst are protected by Reed–Solomon parity data (RS data), calculated from the IP datagrams of the burst. The RS data are encapsulated into MPE-FEC sections, which are also part of the burst and are sent immediately after the last MPE section of the burst, in the same ES, but with different table_id than the MPE sections, which enables the receiver to discriminate between the two types of sections in the ES. For the calculation of the RS data an MPE-FEC frame is used. The MPE-FEC frame consists of an application data table (ADT), which hosts the IP datagrams (and possible padding), and an RS data table, which hosts the RS data; see Figure 1.3.

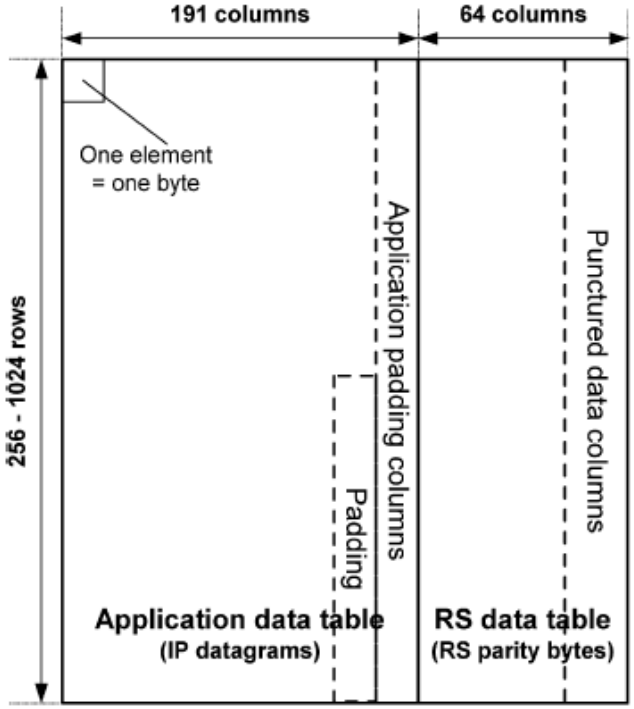

Figure 1.3: MPE-FEC frame.

The number of rows in the MPE-FEC frame is signaled in the service information (SI) and may take any of the values 256, 512, 768, or 1024. The number of columns is 191 for the ADT and 64 for the RS data table. The IP datagrams of a particular burst are introduced vertically column-by-column in the ADT, starting in the upper left corner. If an IP datagram does not end exactly at the bottom of a column, the remaining bytes continue from the top of the next column. If the IP datagrams do not exactly fill the ADT, the remaining byte positions are padded with zeros. On each row the 64 parity bytes of the RS data table are then calculated from the 191 IP datagram bytes (and padding bytes, if applicable) of the same row, using the Reed–

Solomon code RS(255 191). This provides a large virtual time interleaving, since all RS data bytes are calculated from IP datagrams distributed all over the burst. Each IP datagram is transmitted in an MPE section and each column of the RS data table is transmitted in an MPE-FEC section. All headers of the MPE and MPE-FEC sections contain a 4-B real time parameters field, which include a 12-b start address, which indicates the byte number (counted from the start of the table) of the start position of the corresponding IP datagram or RS data column, as well as the 18-b Δt parameter and 1-bit flags to signal end-of-table and end-of-frame. The resulting protocol stack for DVB-H (when MPE-FEC is used) is depicted in Figure 1.4.

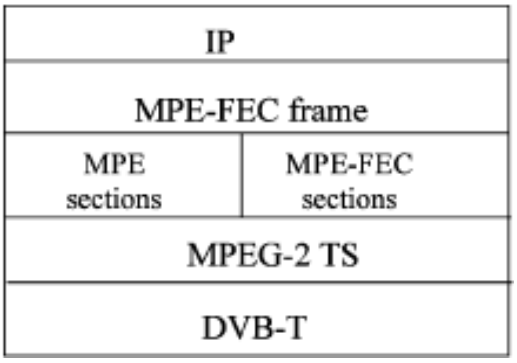

Figure 1.4: Protocol stack for DVB-H.

1.2.3 4K Mode and Interleaving

The objective of the 4K mode is to improve network planning flexibility by trading off mobility and single frequency network (SFN) size. To further improve robustness of the DVB-H 2K and 4K modes in a mobile environment and impulse noise reception conditions, an in-depth symbol interleaver has also been added to the standard. It aims to offer an additional trade off between SFN cell size and mobile reception performance, providing an additional degree of flexibility for network planning. The operator of a dedicated DVB-H network can then select one of the three FFT sizes that best responds to the actual needs. For 2K and 4K modes, the in-depth interleavers increase the flexibility of the symbol interleaving, by decoupling the choice of the inner interleaver from the transmission mode used. This flexibility allows a 2K or 4K signal to take benefit of the memory of the 8K symbol interleaver to effectively quadruple (for 2K) or double (for 4K) the symbol interleaver depth to improve reception in fading channels. This provides also an extra level of protection against short noise impulses caused by, e.g., ignition interference and interference from various electrical appliances. The conceptual principle of the in-

SFN cell size vs reception performance

depth interleaver is depicted in Figure 1.5, where the situation for 4K mode with 8K interleaver is sketched.

Figure 1.5 represents the OFDM symbols in the time and frequency domain. Each OFDM symbol at time *i* has a collection of carriers *j*, each carrier having phase and amplitude determined by *n*-tuples of bits $S_{i,j}$. The *n*-tuple size *n* is determined by the carrier modulation: *n* is 2 for QPSK, 4 for 16QAM, and 6 for 64QAM. Note that for simplicity reasons only eight carriers are shown per each OFDM symbol. With the "normal" native interleaver these *n*-tuples would be reallocated along the carriers within one OFDM symbol. For the in-depth interleaver *n*-tuples of two consecutive OFDM symbols, at time *i* and *i+1*, are taken and reallocated as shown in the lower part of the picture (Figure 1.5b).

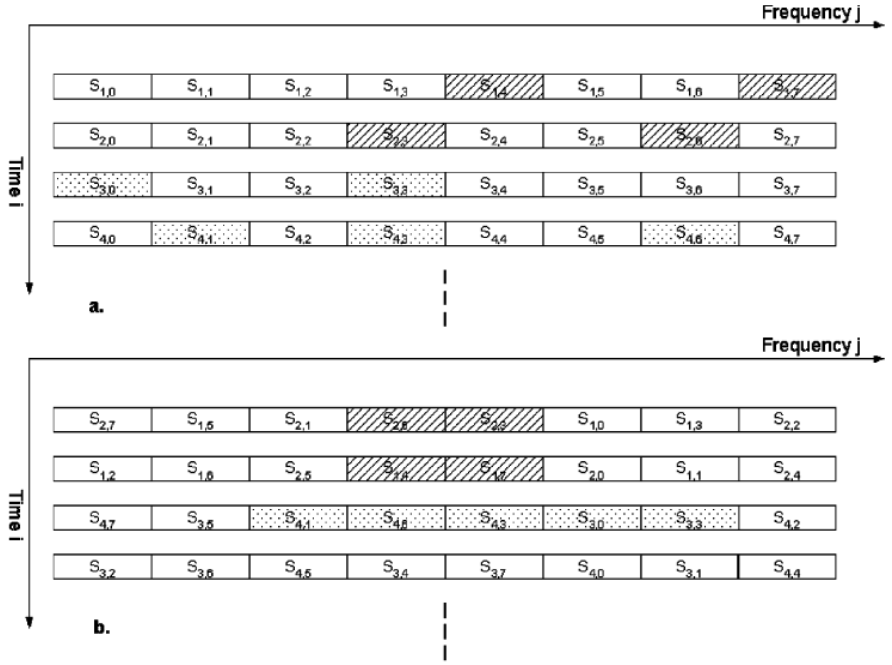

Figure 1.5: a) The symbol order before in-depth interleaving and after deinterleaving.b) The symbol order after interleaving in the channel.

Errors distributed either in time and frequency domain

In this way an error event in the channel, concentrated either in the time domain or in the frequency domain, is more uniformly distributed and enhances the convolutional code possibilities to decode the original bits correctly. The 2K mode behaves similarly, having interleaving over four OFDM symbols instead of two. 4K mode and in-depth interleavers affect the physical layer; however, their implementations do not imply large increase in equipment complexity (i.e., logic gates and memory) over the earlier version of DVB-T standard EN 300 744 for either transmitters or receivers.

1.2.4 DVB-H network

DVB-H is intended to use the same broadcasting spectrum, which DVB-T is currently using. The physical layer of DVB-H is in fact DVB-T and therefore there is a full spectrum compatibility with other terrestrial services. DVB-H can be introduced either in a dedicated DVB-H network or by sharing an existing DVB-T multiplex between the services of the two standard. When the final selection of the DVB-H concept was made, the capability to share a multiplex with DVB-T was indeed one of the decisive factors, as it was seen that this would enhance the commercial introduction possibilities of the service in the crowded UHF broadcasting spectrum. Technically almost any DVB-T frequency allotment or assignment can be used also for DVB-H; the only limitations come from interoperability with GSM900 cellular transmitter in the DVB-H terminal. If simultaneous operation is required, the frequencies below about 700–750 MHz are favored. For broadcasters DVB-H can be seen just as a new means to provide broadcast services for a new, interesting group of customers, namely, the mobile phone users. If this is seen as interesting enough, spectrum will be available. It is in any case expected that the situation will be more relaxed after the analog TV services will start to close. It should also be noted that DVB-H is very spectrum efficient when compared with the traditional TV-services. One 8-MHz channel can deliver 30–50 video streaming services to the small screen terminals. This is ten times more than standard-definition TV (SDTV) with MPEG-2 or 20 times more than high-definition TV (HDTV).

1.3 Derivation of specifications for a DVB-H tuner.

1.3.1 System bandwidth

The receivers shall be able to receive all channels in in the VHF band III and UHF band IV and V. The receiver should support the 6 MHz, 7 MHz, and 8 MHz bandwidths according to the market area needs. Transmission channels are planned in the VHF band III [174-240 MHz] and in the UHF III and IV broadcasting bands [470-890 MHz].The centre frequencies *fc* of the incoming DVB-H RF signals are:

VHF III

- For countries using 8 MHz channel raster:

fc = 178 MHz +(N-6) x 8 MHz +f_{offset}
N = {6, …,12} (VHF channel number)

- For countries using 7 MHz channel raster:

fc = 177,5 MHz +(N-5) x 7 MHz +f_{offset}
N = {5, …,12} (VHF channel number)

- For countries using 6 MHz channel raster:

fc = 177,0 MHz + (N-7) x 6 MHz +f_{offset}
N = {7, …,13} (VHF channel number)

In some countries offsets may be used:
Preferred offset is ± n x 1/6 MHz. n = { 1, 2,…}

UHF IV and V

- For countries using 8 MHz channel raster:

fc = 474 MHz + (N-21) x 8 MHz +f_{offset}
n = {21, …,69} (UHF channel number)

- For countries using 7 MHz channel raster:

fc = 529,5 MHz +(N-28) x 7 MHz +f_{offset}
n = {28, …,67} (UHF channel number)

- For countries using 6 MHz channel raster:

fc = 473,0 MHz +(N-14) x 6 MHz +f_{offset}
n = {14, …,83} (UHF channel number)

In some countries offsets may be used:
Preferred offset is ± n x 1/6 MHz. n = { 1, 2,…} In the UK n=1.

In the following specification we just consider the case of 8 MHz channels.

1.3.2 System requirements

The receiver shall be capable of correctly demodulating all modes specified in ETSI EN 300 744, except the code rates 5/6 and 7/8. The front end shall therefore be able to work with any combination of:

- Constellation (QPSK, 16-QAM, 64-QAM, hierarchical 16 QAM, hierarchical 64-QAM),
- Code rate (1/2,2/3,3/4),
- Guard interval (1/4,1/8,1/16 or 1/32),
- Transmission mode (2k or 8k),
- Where applicable α (1, 2 or 4).

The receiver performance is defined according to the reference model shown in Figure 1.6.

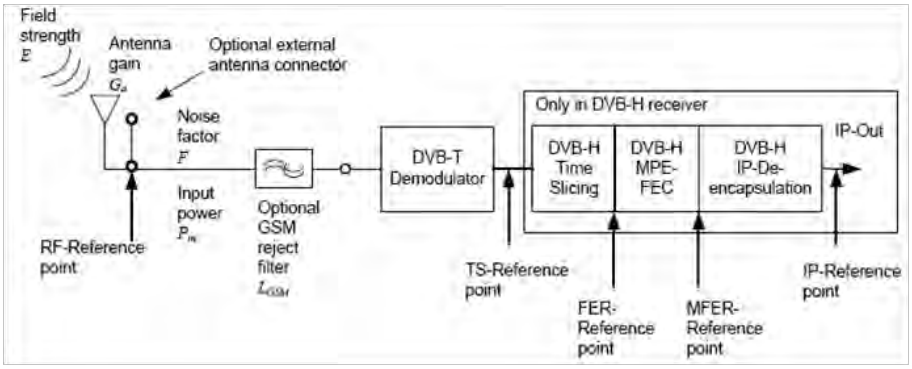

Figure 1.6: Reference model.

The used reference receiver model describes the DVB-H receiver performance in an idealised way [1.6]. In terms of *C/N* the DVB-H receiver shall have the performance given in Table 1.1 [1.6], when noise (N) is applied together with the wanted carrier (C) integrated in a signal bandwidth of 7,61 MHz. The values are calculated using the theoretical C/N figures given in ETSI EN 300 744 V1.5.2 added by an implementation margin of 1,1 dB for QPSK, 1,3 dB for 16-QAM and 1,5 dB for 64-QAM modes.

Modulation	Code rate	Gaussian C/N [dB]
QPSK	1/2	3,6
QPSK	2/3	5,4
16-QAM	1/2	9,6
16-QAM	2/3	11,7
64-QAM	1/2	14,4
64-QAM	2/3	17,3

Table 1.1

At the sensitivity level for DVB-H mode the portable terminal should have a system noise figure (NF) of 5 dB [1.6] or less at the RF-reference point. A system noise figure of 5dB corresponds to the following noise floor power level (P_{nf}):

$$P_{nf} = P_{anf} + NF = 105{,}2[\text{dBm}] + 5[\text{dB}] = -100{,}2\ \text{dBm} \quad (1.1)$$

Noise floor

with P_{anf} =kTB the noise floor referred to the antenna. So the receiver's minimum signal input level (or sensitivity) is given by:

Sensitivity

$$P_{min} = P_{nf} + C/N = -100{,}2\ [dBm] + 17{,}3\ [dB] = -82{,}9\ dBm \quad (1.2)$$

with C/N of 64-QAM 2/3 code rate (Table 1.1). We consider this value of C/N for the specification because it is the worst case.

1.3.3 Interference immunity: Linearity

Traditionally immunity to analogue and digital signals has been defined with simple single interferer patterns. Either one digital or one analogue interfering adjacent signal has been introduced by the standard and protection ratio to the wanted digital signal has then been defined. This assumes that the receiver would have some degree of preselection to remove other interfering signals that are also present. From a linearity point of view, the single interferer scenario is most probably not challenging enough for some types of circuit topology. Therefore, in addition to the single interferer approach, a more complete ensemble of interfering patterns is proposed for the testing.

Selectivity and Linearity pattern

Two different interference pattern sets have been defined. The first one is testing mainly receiver selectivity and includes two classical single interferer patterns. The second one is testing receiver linearity with two interferers. No additional noise is added and the channel profile is Gaussian.

In a wideband system a single tone can generate distortion because the harmonic products of the interferer are again in the signal band. Indeed the intermodulation product generated in band can fall into the desired channel (Figure 1.7). This is not a problem in a narrowband system .

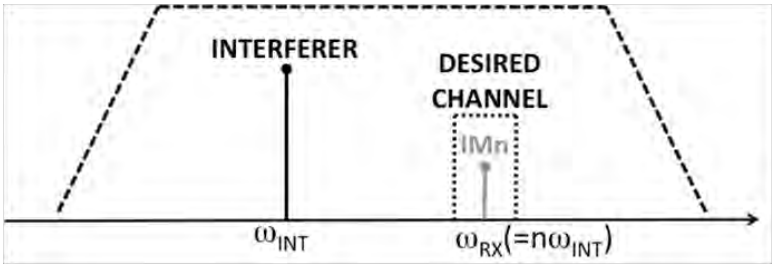

Figure 1.7: Non-linearity in wideband system.

One tone test

This kind of linearity has been considered in the selectivity pattern (Figure 1.8). In a selectivity pattern the unwanted channel can be any of the analog or digital television channels within the whole band. The following two patterns are used for receiver selectivity testing:

- Pattern S1, one adjacent analogue signal on N±m or image.
- Pattern S2, one adjacent digital DVB-T signal on N±m or image

with N the channel in which there is the wanted signal. P_{sign} is the wanted signal power and P_{int} is the unwanted signal power. The minimum P_{sign}/P_{int} for 64-QAM 2/3 cod rate for S1 and S2 pattern is shown in Table 1.2 [1.6].

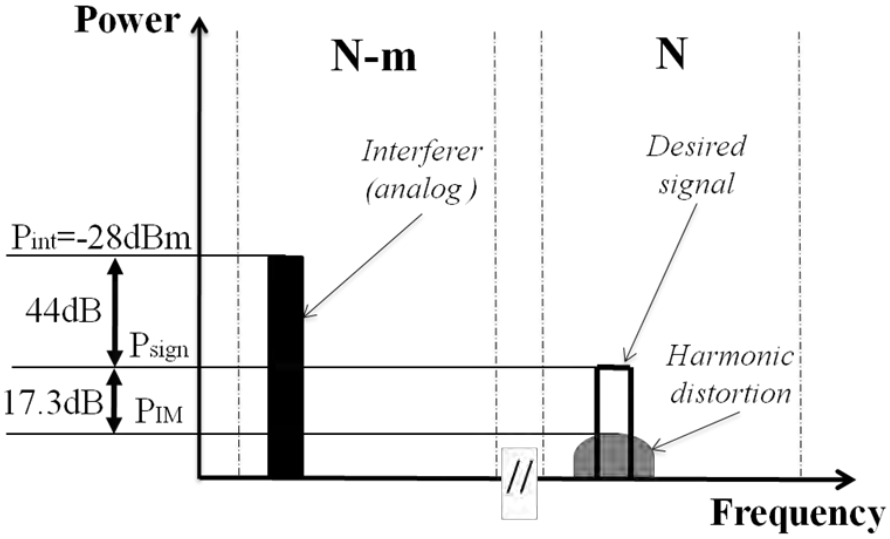

Figure 1.8:Selectivity Pattern S1

Selectivity Pattern	P_{sign}/P_{int} [dB]
S1(analog interferer)	44
S2(digital interferer)	42

Table 1.2

The IIP2 and IIP3 requirements related to the worst case of selectivity patterns S1with a constant NF of 5dB can be now calculated.

$$P_{IM}=P_{int}-P_{sign}/P_{int}-C/N \quad (1.3)$$
$$P_{IM2}=2P_{int}-IIP2 \quad (1.4)$$
$$P_{IM3}=3P_{int}-IIP3 \quad (1.5)$$

IIP2 and IIP3 for one tone test

with P_{IM} the input referred level of the IM product. If we want to calculate the IIP2 requirement we consider $P_{IM}=P_{IM2}$ with $\omega_{IM2}=2\omega_{INT}$. In the same way for the IIP3 we consider $P_{IM}=P_{IM3}$ with $\omega_{IM3}=3\omega_{INT}$. Therefore the IIP2 and IIP3 requirements, in the worst case of selectivity patterns S1, are shown in the following Table. The interferer power is -28dBm.

	IIP2[dBm]	IIP3[dBm]
Selectivity Pattern S1	33	2,5

Table 1.3

Two tones test

For the linearity pattern the two unwanted channels are located at N+2 and N+4 or N-2 and N-4. Due to the nonlinearity in the tuner IC, the second and third order intermodulation products will fall into the wanted (N) channel. The unwanted channels can be analog or digital

TV signals (Table 1.4 [1.6]). The following four patterns are used for receiver linearity testing:

- Pattern L1, N+2 digital channel and N+4 analogue channel
- Pattern L2, N+2 and N+4 analogue channel
- Pattern L3, N+2 and N+4 digital
- Pattern L4, analogue in VHF III and digital in UHF

Linearity Pattern	$P_{sign}/P_{int\ 1}$dB]	$P_{sign}/P_{int\ 2}$[dB]
L1(Digital-Analog)	42	47
L2(Analog-Analog)	47	47
L3(Digital-Digital)	42	42
L4(Analog in VHF-Digital in UHF)	47	47

Table 1.4

In the linearity patterns testing the minimum P_{sign}/ P_{int} for 64-QAM 2/3 cod rate is 47dB (Figure 1.9), so it's possible to calculate the IIP2 and IIP3 requirement for this worst case. The interferer power is -35dBm.

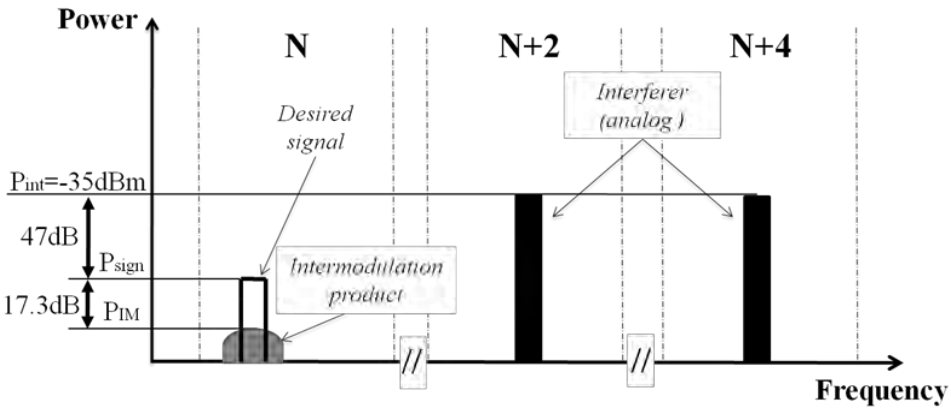

Figure 1.9:Linearity pattern L2

IIP2 and IIP3 for two tone test

Using the equations 1.3-1.5 we obtain the requirements for IIP2 and IIP3 shown in the following Table.

	IIP2[dBm]	IIP3[dBm]
Linearity Pattern L2	29,3	-3

Table 1.5

1.4 Conclusions

In the first two paragraphs of this chapter we introduce the standard DVB-H.DVB-H is a digital broadcast standard offering high data rate audio/video content delivery to handheld terminals, taking into

consideration the terminal specific features. The new DVB-H standard, while in no way changing the current digital TV business models for fixed reception, could provide new business possibilities for a variety of players from broadcast and cellular operators to chip and equipment manufacturers. The power saving given by time slicing makes digital broadcast reception in handheld terminals practical reality. The new system has been well received by various operators, both broadcast and telecom. Several pilot networks are running in various parts of the world and commercialization in the form of chips and user terminals takes place by several manufacturers.
In the third paragraph we show the derivation of the key specifications and a summary of those is shown in the Table 1.6.

Key specifications for a DVB-H TV Tuner

	IIP2[dBm]	IIP3[dBm]	NF[dB]
Selectivity Pattern S1 (one tone test)	33	2,5	5
Linearity Pattern L2 (two tones test)	29,3	-3	5

Table 1.6

References

[1.1] U. Reimers, *DVB-The family of international standards for digital video broadcasting*, Proc. IEEE vol. 94, no. 1, pp. 173-182, Jan. 2006.

[1.2] U. Ladebusch and C. Liss, *Terrestrial DVB (DVB-T): A broadcast technology or stationary portable and mobile use*, Proc. IEEE vol. 94, no. 1, pp. 183-193, Jan. 2006.

[1.3] M. Dawkins, A. Burdett, and N. Cowley, *A single-chip tuner for DVB-T*, IEEE J. Solid-State
Circuits, vol. 38, no. 8, pp. 1307-1317, Aug. 2003.

[1.4] G. Faria, J. A. Henriksson, E. Stare, and P. Talmola, *DVB-H: Digital Broadcast Services to Handheld Devices*, Proc. IEEE, vol. 94, no. 1, pp. 194-209, January 2006.

[1.5] P. Antoine, P. Bauser, H. Beaulaton, M. Buchholz, D. Carey, T. Cassagnes, T. K. Chan, S. Colomines, F. Hurley, D. T. Jobling, N. Kearney, A. C. Murphy, J. Rock, D. Salle, and T. Cao-Thong, *A direct-conversion receiver for DVB-H*, IEEE J. Solid-State Circuits, vol. 40, pp. 2536-2546, Dec. 2005.

[1.6] EICTA MBRAI 2.0, *Mobile and portable DVB-T/H radio access*.

2

Wideband Balun LNA with Noise Cancelling

Low-cost, low-power and small physical size required by cellular phones and other mobile terminals necessitates moving into smaller geometries and integrating more functionality into a single piece of silicon. Building high performance radios in nanometer digital CMOS processes, is a critical step towards single-die implementations of complex communication and broadcast standards. For competitive, low-cost solutions in the emerging market of mobile TV, it is desirable to support multiple standards deployed world-wide that use different RF bands. In this chapter a wideband balun LNA who combines the balun and the LNA functionality is described. The possibility to use this LNA in a wideband low-noise receiver for DVB-H is shown. The limitations of this choice are presented.

2.1 TV Tuners.

In recent years, TV tuners have become increasingly integrated. Solid-state technology advances are allowing monolithic same-chip implementations of IOW noise broadband amplifiers, low phase noise voltage controlled oscillators (VCO), and low distortion mixers, all with reasonable power consumption. However, modern TV receivers and set-top boxes require universal tuners capable of processing different standards of analog and digital, terrestrial and cable broadcast. The use of passive components as channel and image filters can significantly simplify the receiver design given the aforementioned impairments. However, these components are difficult to implement in silicon, even with recent advances. A significant problem is also the implementation of wideband balun for the conversion single (from the antenna) to differential (to the front end) with low losses.

Narrowband paths or wideband path

Moreover the broadband nature of the TV band introduces many technical challenges in the design of silicon tuners. These design challenges include harmonic reject mixing, image rejection, low noise and linearity over wide bandwidth, and high dynamic range. The straight solution for multistandard multimode front-ends employs parallel narrowband receiving paths (Figure 2.1) [2.1] at cost of die and board area, high pin count, and lack of reconfigurability. A possible alternative is a single receiver with a wideband LNA to cover the whole band of interest (Figure 2.2).

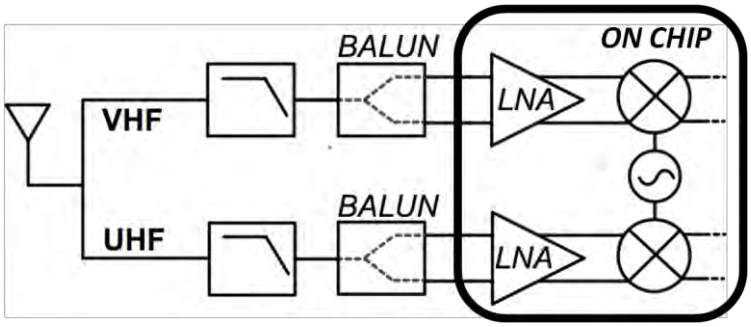

Figure 2.1: Multy-path Tuner

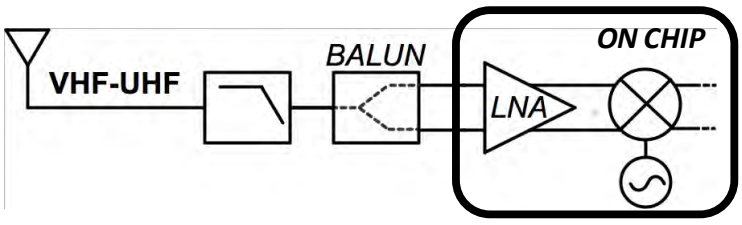

Figure 2.2: Single path Tuner

However high sensitivity integrated receivers require LNAs with sufficient large gain, noise figure well below 3 dB, adequate linearity and source impedance matching. This requirements, in the second topology of receiver, must be achieved over a wide range of frequency.

2.2 Wideband LNAs

In this section several wideband CMOS techniques are presented.
In Figure 2.3 well known topologies of wideband amplifiers are shown. In Table 2.1 the noise factor and the matching condition are reported. Just thermal noise is considered.

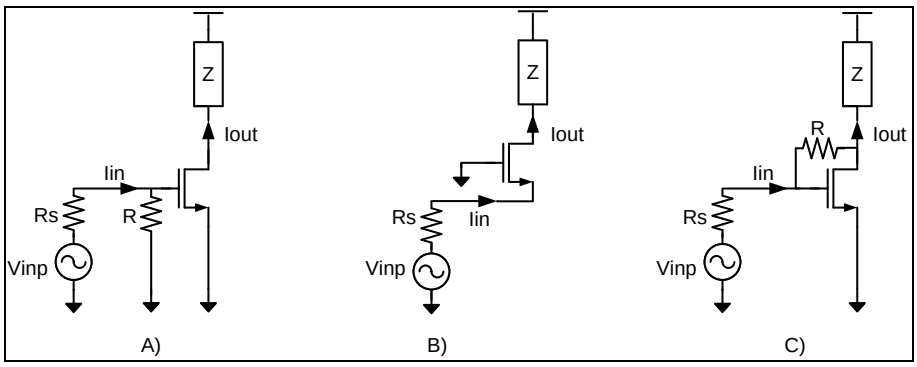

Figure 2.3 :Wideband LNAs

Common source

The first one (Figure 2.3 A) uses a simply resistive termination of the input port of a common source stage to provide a 50 Ω impedance. This topology it's too noisy for two main reasons. First of all we have 3 dB of NF only introducing the resistive termination (the first term of 2.1 is 2 for this reason). Then we have a 6dB attenuation of the signal at the input and so the contribution of the MOS is 4 times higher (the second term of 2.1).The last term of 2.1 is the contributor of the load.

$$F = \mathbf{2} + \frac{\mathbf{4}\gamma}{gmRs} + \frac{\mathbf{4}}{gm^{\mathbf{2}}RsZ} \qquad (2.1)$$

Common gate

The second LNA (Figure 2.3 B) is a common gate. This architectural approach uses the source of the common gate stage as the input termination. The NF, applying the matching condition $R_S=1/g_m$, in this case is round 3dB (2.2), but fixed the input matching condition, no more degrees of freedom are available in the design. The second and third term of the (2.2), are the contributions of the MOS and of the load

$$F = \mathbf{1} + \frac{\gamma}{gmRs} + \frac{Rs}{Z}\left(\mathbf{1} + \frac{\mathbf{1}}{gmRs}\right)^{\mathbf{2}}\Bigg|_{gm=\mathbf{1}/Rs} = \mathbf{1} + \gamma + \frac{\mathbf{4}Rs}{Z} \qquad (2.2)$$

Common source with shunt series feedback

The last LNA (Figure 2.3 C) uses resistive shunt-series feedback to set the input and output impedances. To reduce the noise of this topology it is possible to increase the transcondactance (Equation 2.3). This approach is critical because if we realize a greater MOS to increase the g_m we reduce the cut off frequency of the wideband amplifier. On the other hand it's possible to increase the current, for fixed dimensions, but to obtain an enough low noise factor we need a very high power dissipation compared to others amplifiers with similar noise performances. To improve the noise performance of this topology a PN stage can be implemented. In the following equation, the second term is the noise contributor of the MOS, the second of the feedback resistor R and the third of the load.

$$F = 1 + \frac{\gamma}{gmRs} + \frac{1}{gmZ + 1} + \frac{1}{gm^2 RsZ} \tag{2.3}$$

These topologies suffer from a fundamental trade off between their noise factor F and impedance matching, $Z_{IN}=R_s$. For a sufficiently large gain, low F requires a large g_m or R. Conversely, impedance matching demands a fixed $g_m=1/R_s$ or $R=R_s$. Therefore in this topologies F is equal or higher than 3dB, with a reasonable power consumption.

Common gate with multiple feedbacks

The trade off between F and source impedance can be broken exploiting feedbacks round the common gate stage. In literature this kind of solution is proposed for narrow band amplifiers [2.4], but in principle it can be realized for a wideband LNA too (Figure 2.4). The new degrees of freedom provided by the use of feedbacks not only can improve the amplifier's performance, but also offers a high level of reconfigurability that allows to exchange gain, noise and/or linearity with power consumption.

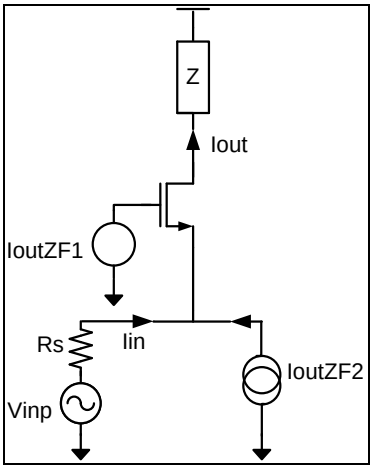

Figure 2.4:Multiple feedbacks round the common gate.

This new approach, called adaptive optimization, uses the ability to reconfigure the feedback network to match the amplifier

characteristics to the changing working conditions. In equation 2.4 the noise factor of the common gate stage depending on the feedbacks values F1 and F2 is shown. The second term in 2.4 is the contributor of the MOS, the third one of the load. For a detailed analysis see Appendix A.

$$F = 1 + \gamma\left(1 - \frac{ZF_1}{Rs} - F_2 Z\right) + \frac{Rs}{Z}\left(2 - \frac{ZF_1}{Rs} - F_2 Z\right)^2 \qquad (2.4)$$

A possible drawback of an implementation with feedbacks can be the stability of the system and the sensitivity to process variations.
The factors of noise and the matching conditions of all the topologies presented in this paragraph are summarized in the Table 2.1.

Topologies	Noise Factor	Matching condition
Resistive termination	$F = 2 + \frac{4\gamma}{gmRs} + \frac{4}{gm^2 RsZ}$	$R = Rs$
Common Gate	$F = 1 + \gamma + \frac{4Rs}{Z}$	$gm = \frac{1}{Rs}$
Shunt Series Feedback	$F = 1 + \frac{\gamma}{gmRs} + \frac{1}{gmZ + 1} + \frac{1}{gm^2 RsZ}$	$R = Rs(1 + gmZ)$
CG With Multiple Feedbacks	$F = 1 + \gamma\left(1 - \frac{ZF_1}{Rs} - F_2 Z\right) + \frac{Rs}{Z}\left(2 - \frac{ZF_1}{Rs} - F_2 Z\right)^2$	$gm = \frac{1}{Rs - (F_1 + F_2 Rs)Z}$

Table 2.1

2.3 Wideband balun LNA with noise cancelling

All the wideband LNAs presented in the previous section are supposed to be implemented like differential LNAs. That means, according with Figure 2.2, that we need a wideband off chip passive balun too. It's possible to circumvent this problem using a balun-LNA on chip (Figure 2.5).

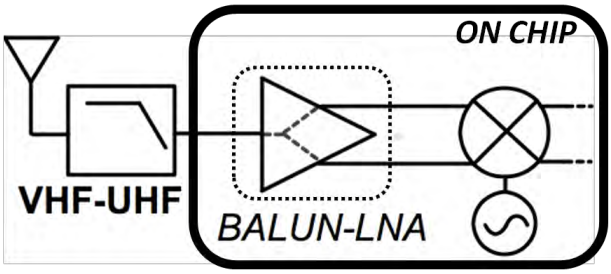

Figure 2.5: Tuner with a wideband balun-LNA.

Wideband balun LNA

Like we said before, in contrast to a multi-LNA solution, the single wideband LNA is flexible and efficient in terms of area, power and costs. Single-ended input LNAs are preferred to save I/O pins and because antennas and RF filters usually produce single ended signals. On the other hand, differential signalling in the receive chain is

preferred in order to reduce second-order distortion and to reject power supply and substrate noise. Thus, at some point in the receive chain a balun is needed to convert the single-ended RF signal into a differential signal. Off-chip baluns with low losses are typically narrowband so that several baluns would be required in case of wideband operation. On the other hand, wideband passive baluns typically have high loss, degrading the overall NF of a receiver significantly. So we can have an advantage in terms of costs and noise because the balun and its losses are eliminated.

2.3.1 Noise cancelling

Noise cancelling principle

In this paragraph, a wide-band low-noise technique is presented, which is able to decouple F from $Z_{in}=R_S$ without needing global feedbacks or compromising the source match. This is achieved by cancelling the output noise of the matching device without degrading the signal transfer [2.2].
To better understand this last concept we can use a block diagram shown in Figure 2.6.

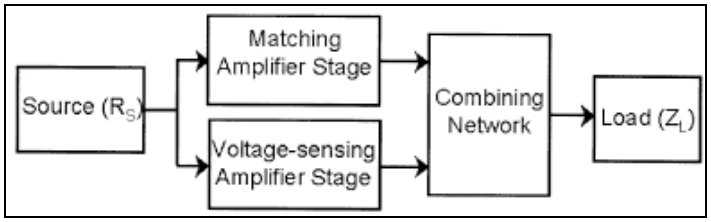

Figure 2.6: Block diagram of the LNA exploiting the noise cancellation [2.2].

It consists of the following functional blocks:

- Amplifier stage providing the source impedance matching, Zin=Rs.
- An auxiliary amplifier sensing the voltage (signal and noise) across the real input source
- A network combining the output of the two amplifiers, such that noise from the matching device cancels while signal contributions add.

Noise cancelling implementation

An implementation of noise cancelling can be realized using the resistive shunt-series feedback (Figure 2.3 C) as matching amplifier stage. Figure 2.7 (A) shows a straightforward functioning using an ideal feedforward voltage amplifier. The input impedance of the matching amplifier stage, without the load, is $Z_{IN}=R_S$ and its voltage gain is $A_{V,MS}=V_Y/V_X=1-g_{mi}R$. For the matching condition, the F of this stage is larger than 3dB, as discussed in the previous paragraph. Let us now analyze the signal and the noise voltages at the input node

X and output node Y, both with respect to ground, due to the noise current $I_{n,i}$ of the impedance-matching MOSFET.

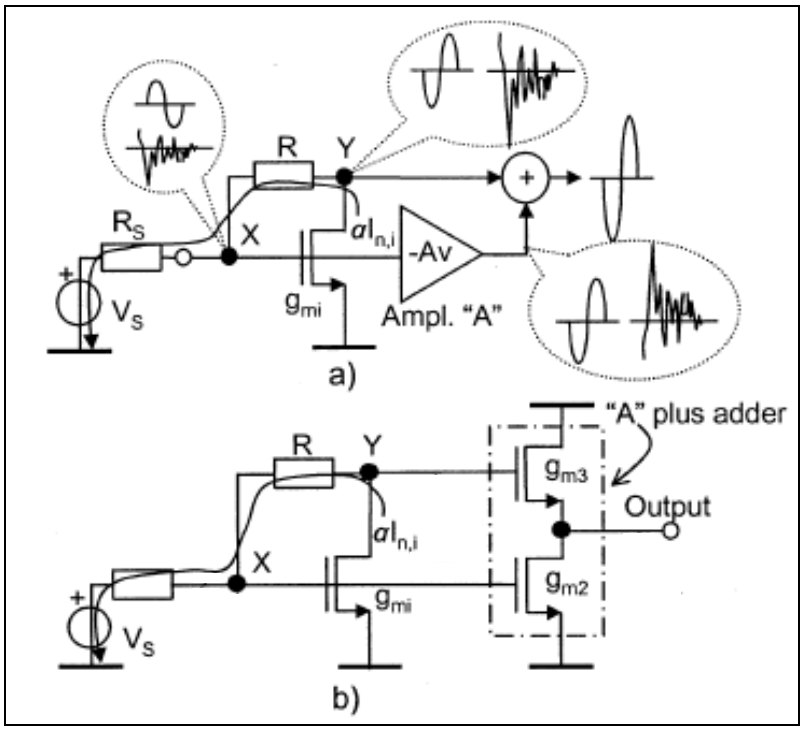

Figure 2.7: Ideal (A) and circuital (B) implementation of the noise cancelling[2.2].

Depending on the relation between $Z_{IN}=1/g_{mi}$ and R_S, a noise current $\alpha(R_S, g_{mi})\cdot I_{n,i}$ flows out of the matching MOSFET through R and R_S , with $0 < \alpha < 1$. This current causes two instantaneous noise voltages at nodes X and Y, which have equal sign. On the other hand, the signal voltages at nodes X and Y have opposite sign, because the gain $A_{V,MS}$ is negative, assuming $g_{mi}R>1$. This difference in sign for noise and signal makes it possible to cancel the noise of the matching device, while simultaneously adding the signal contributions constructively. In other words the noise cancelling technique is the cancellation of the noise of the matching amplifier stage at the output. This is done by creating a new output, where the voltage at node Y is added to a scaled negative replica of the voltage at node X. A proper value for this scaling factor renders noise cancelling at the output node, for the thermal noise originating from the matching device. With simple calculations [2.2] it's possible to extrapolate a value of the ideal voltage gain for the noise cancellation; $A_{V,C}=1+ R/R_S$. From this value two characteristics are evident:

- Noise cancelling depends on the absolute value of the real impedance of the source, R_S.

- The cancellation is independent on $\alpha(R_S,g_{mi})$·and on the quality of the source impedance match. This is because any change of g_{mi} equally affects the noise voltages at X and Y.

The Figure 2.7 (B) shows an elementary circuital realization of the noise cancelling LNA. Amplifier A and the adder are replaced with the common-source stage M2–M3, rendering an output voltage equal to the voltage at node X times the gain $A_V = g_{m2}/ g_{m3}$. Transistor M3 also acts as a source follower, copying the voltage at node Y to the output. Note that any small signal that can be modelled by a current source between the drain and source of the matching device is cancelled as well (e.g., 1/f noise, thermal noise of the distributed gate resistance, and the bias noise current injected into node Y). However, the noise of R is not cancelled. This can be seen splitting its noise current $I_{n,Ri}$ in two correlated sources to ground, at the output node Y and the input node X. The former is cancelled for $A_V = A_{V,C}$, the latter is not.

No cancellation of feedback resistance noise and single ended output

This LNA so exploiting the noise cancellation, but it isn't a balun-LNA because we have one input and one output. The next step presented in the following paragraph is the noise cancelling technique realized with the single to differential conversion.

2.3.2 Wideband balun LNA: CG-CS topology

CG-CS noise cancelling implementation

Described the noise cancelling technique in a wideband-LNA, the analysis of the common gate (CG) common source (CS) topology (Figure 2.8) is presented.

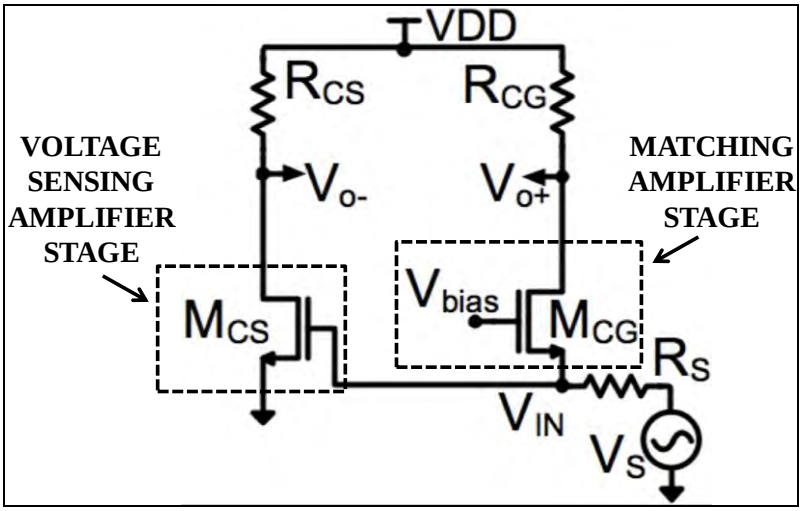

Figure 2.8: CG-CS topology.

Using the definitions introduced in the previous paragraph, the CG is the matching amplifier stage and the CS is the sensing amplifier stage. In other words we can consider (Figure 2.9) the two stages like an inverting amplifier (CS) and a non-inverting one (CG) with equal but

Single input to differential output

opposite sign gain G. The main difference compared to the Figure 2.6 is the absence of an adder and so the differential output and not the single ended one. In this way the cancellation is realized after the recombination of the differential output in base band, and not at the output of the LNA.

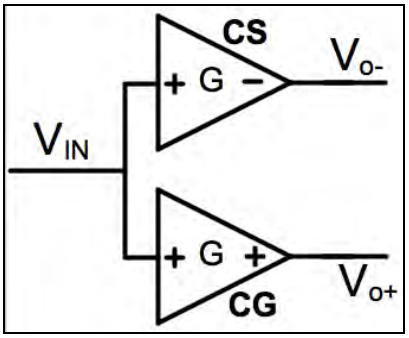

Figure 2.9: Block diagram of the CG-CS scheme

Input matching and output balancing

For a proper design of this kind of LNA two fundamental conditions has to be realized, the input matching ($R_{in,CG}=1/g_{mCG}$) and the output balancing. The gain of the two amplifiers has to be equal to guarantee the balance of the outputs. The two outputs have to be considered equal not only in terms of small signal gain, but also from a bias point of view. Assuming $A_{V,CG}=g_{mCG}R_{CG}$ the voltage gain of the CG, $A_{V,CS}=-g_{mCS}R_{CS}$ the voltage gain of the CS, $I_{bias,CG}$ and $I_{bias,CS}$ the bias currents of CG and CS respectively, for the output balance both of the following expressions has to be considered:

$$G = \left|gm_{CS}R_{CS}\right| = \left|gm_{CG}R_{CG}\right| \tag{2.5}$$

$$I_{biasCS}R_{CS} = I_{biasCG}R_{CG} \tag{2.6}$$

Noise cancellation

The equation 2.5 it's necessary for the noise cancelling at the differential output too, indeed:

$$v_{n,CS} = v_{n,in}A_{V,CS} = v_{n,CG} = v_{n,in}A_{V,CG} \tag{2.7}$$

where $v_{n,CS}$ and $v_{n,CG}$ are the voltage noise at the CS and CG output and $v_{n,in}$ the voltage noise at the input node. It's clear from the equation 2.6 that the output balance is a primary condition also for the noise cancellation.
Until now, we considered only the noise point of view in the analysis presented, but in a wideband LNA the linearity requirements are also really important. About this , considering in the expression of the gain the matching condition $R_{in,CG}=1/g_{mCG}$ from [2.3] it's also possible to write the gain in this way:

$$A_{V,CS} = -A_{V,CG} = -\frac{R_{CG}}{R_S} \tag{2.8}$$

Distortion cancellation

Now the non-linear input voltage v_{in} can be written as a Taylor expansion of the signal source voltage v_S:

$$v_{in} = \alpha_1 v_S + \alpha_2 v_S^2 + \alpha_3 v_S^3 + \ldots = \alpha_1 v_S - v_{NL} \tag{2.9}$$

where v_{NL} contains all the unwanted nonlinear terms and the coefficient α_1 is 0.5 in the matching condition. The output voltage of the CG and CS can be written as [2.3]:

$$v_{o,CG} = i_{in} R_{CG} = \frac{v_S - v_{in}}{R_S} R_{CG} = ((1-\alpha_1)v_S - v_{NL})\frac{R_{CG}}{R_S} \tag{2.10}$$

$$v_{o,CS} = -v_{in}\frac{R_{CG}}{R_S} = -(\alpha_1 v_S + v_{NL})\frac{R_{CG}}{R_S} \tag{2.11}$$

and so from the previous expressions the differential voltage output is:

$$v_{o,diff} = v_{o,CG} - v_{o,CS} = v_s \frac{R_{CG}}{R_S} \tag{2.12}$$

Again the gain required in the CS stage to cancel the distortion products of the CG equals the gain required to obtain the output balancing.

CG CS stages design

In literature two design options allow to realize the output balancing [2.3]:

- $g_{m,CS} = g_{m,CG}$ and $R_{CS} = R_{CG}$
- $g_{m,CS} = n g_{m,CG}$ and $R_{CS} = \frac{R_{CG}}{n}$

In both cases the output imbalance is zero but the noise of the first design option is higher. The difference is the noise of the CS. In the first case the $g_{m,CS} = 1/R_S$ is low, and the noise generated is high. In the second design alternative instead the noise of the CS is proportional to 1/n so as grater is $g_{m,CS}$ as lower is the noise.
In conclusion a simultaneous balancing and cancellation of unwanted noise and distortion currents of the CG transistor is possible under equal gain for the two amplifiers and input matching condition. In the next paragraphs a more detailed analysis of noise and distortion is presented.

2.3.3 CG-CS topology: Noise analysis

In this section an analysis of the CG-CS topology is done. In the Figure 2.10 the circuit with the noise generators is shown.

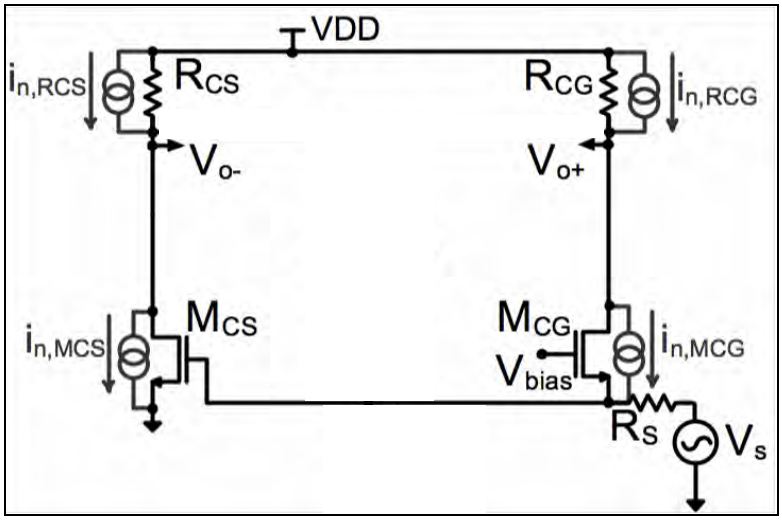

Figure 2.10: Noise analysis of the CG-CS stage.

The equivalent generators of thermal noise of the CS and CG stages and of their load R_{CG} and R_{CS} are:

$$\begin{aligned} i_{n,MCS} &= \sqrt{4kT\gamma g_{m,CS}} \\ i_{n,MCG} &= \sqrt{4kT\gamma g_{m,CG}} \\ i_{n,RCS} &= \sqrt{\frac{4kT}{R_{CS}}} \\ i_{n,RCG} &= \sqrt{\frac{4kT}{R_{CG}}} \\ v_{n,RS} &= \sqrt{4kTR_S} \end{aligned} \tag{2.13}$$

The transfer functions of noise from the input to the differential output are :

$$\begin{cases} \left|T_{n,MCS}\right| = R_{CS} \\ \left|T_{n,MCG}\right| = \dfrac{R_{CG}}{2} + \dfrac{g_{m,CS}}{2g_{m,CG}} R_{CS} \\ \left|T_{n,RCG}\right| = R_{CG} \\ \left|T_{n,RCS}\right| = R_{CS} \\ \left|T_{n,RS}\right| = \dfrac{1}{2}(g_{m,CS}R_{CS} + g_{m,CG}R_{CG}) \end{cases} \tag{2.14}$$

If we consider in particular the transfer function of noise $i_{n,MCG}$:

$$\left|T_{N,MCG}\right| = \frac{R_{CG}}{2} + \frac{g_{m,CS}}{2g_{m,CG}} R_{CS} \tag{2.15}$$

Noise cancelling condition

a condition to cancel the noise at the differential output of the CG stage can be simply extrapolated. From the previous expression the cancellation of noise of the CG (noise cancelling condition) can be extrapolated assuming :

$$\frac{R_{CG}}{2} + \frac{g_{m,CS}}{2g_{m,CG}} R_{CS} = 0 \tag{2.16}$$

and, as described before, this condition is the output balance:

$$g_{m,CG} R_{CG} = -g_{m,CS} R_{CS} \tag{2.17}$$

At this point the noise factor is:

$$F = 1 + \frac{i_{n,RCG}^2 \left|T_{n,RCG}\right|^2 + i_{n,RCS}^2 \left|T_{n,RCS}\right|^2 + i_{n,MCS}^2 \left|T_{n,MCS}\right|^2}{v_{n,RS}^2 \left|T_{n,RS}\right|^2} \tag{2.18}$$

that using the 2.13-2.18 and with the differential gain $A_{V,diff}=2g_{m,CS}R_{CS}$ can be rewrite as:

Noise factor

$$F = 1 + \frac{g_{m,CG}}{g_{m,CS}} \gamma + \frac{2}{A_{V,diff}} + \frac{2g_{m,CG}}{A_{V,diff} g_{m,CS}} \tag{2.19}$$

Definition of β

The second term is the contributor of noise of the CS, the third of the R_{CG} and the fourth of the R_{CS}. Looking the 2.18, it's clear the reduction of F if the $g_{m,CS}$ is chosen n times bigger than the $g_{m,CG}$. Also as the $A_{V,diff}$ is higher as the contributors of noise of the loads are lower. Introducing the factor $\beta=g_{m,CS}/g_{m,CG}$ the expression of F becomes:

$$F = 1 + \frac{\gamma}{\beta} + \frac{2}{A_{V,diff}} + \frac{2}{A_{V,diff}\beta} \tag{2.20}$$

The 2.20 in function of β and for different values of the differential gain in Figure 2.11 is plotted.

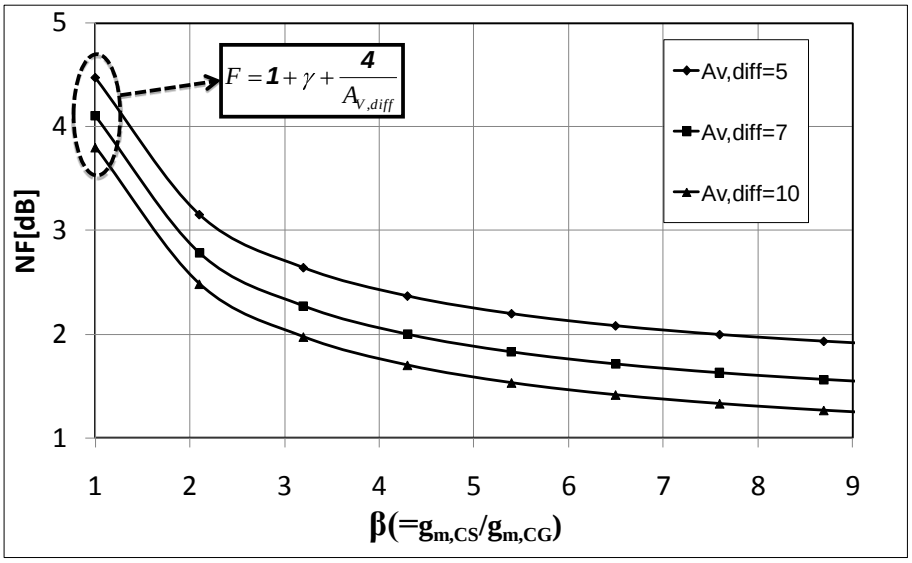

Figure 2.11: Variation of $\beta = g_{m,CS}/g_{m,CG}$ for different values of the differential gain $A_{V,diff}$

The higher is $A_{V,diff}$ the lower is the noise, but the most significant improvement is due to a $\beta>1$. In the graph the expression of the noise factor for $\beta=1$ is reported.

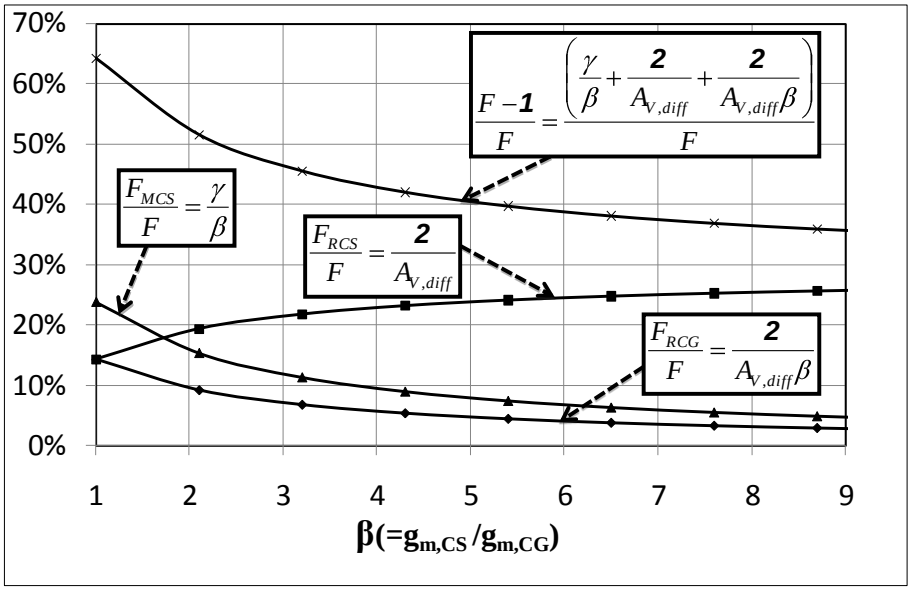

Figure 2.12:Noise contributors normalized to the total noise F.

It's interesting to notice that it's possible to obtain the same noise using different values of differential gain and β. For a higher gain we need a lower β and vice versa. In Figure 2.12 the variation of the noise contributors of CS stage, R_{CG} and R_{CS}, normalized to F, is plotted. For $\beta=1$ the main contributor of noise is the common source stage. For $\beta>2$ the main contributor start to be the R_{CS} one and there's a reduction of 20% in the total noise for $\beta=3$. This is because either the noise of the MOS either the noise of the R_{CG} are lower. In other words

the CS stage is the noisier part of the circuit and using a β>1 this one is reduced even if we use the same differential gain.

2.3.4 CG-CS topology: Linearity analysis

In this paragraph the non-linearity of the balun-LNA in the CG-CS topology is analyzed. The contribution of the distortion of the two MOS with power series are considered like shown in Figure 2.13.

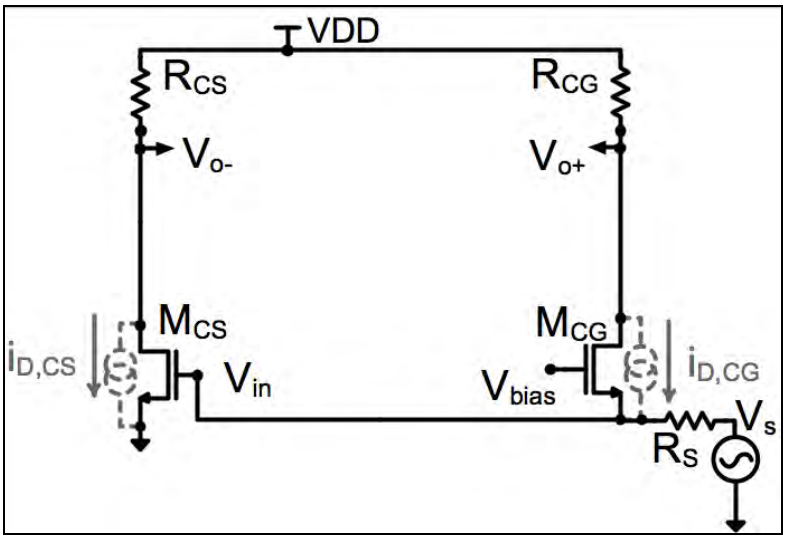

Figure 2.13:Linearity analysis of the CG-CS topology.

To determinate the distortion of this circuit, the following system has to be solved:

$$\begin{cases} \dfrac{V_{in}-V_S}{R_S} = i_{D,CG} \\ V_{o+} = -i_{D,CG}R_{CG} \\ V_{o-} = -i_{D,CS}R_{CS} \\ i_{D,CG} = g_{m,CG}(-V_{in}) + g_{2,CG}(-V_{in})^2 + g_{3,CG}(-V_{in})^3 \\ i_{D,CS} = g_{m,CS}(-V_{in}) + g_{2,CS}(-V_{in})^2 + g_{3,CS}(-V_{in})^3 \\ V_{in} = A_1V_S + A_2V_S^2 + A_3V_S^3 \end{cases} \tag{2.21}$$

At the differential output, imposing the conditions of input matching ($g_{m,CG}=1/R_S$) and output balancing ($g_{m,CG}R_{CG}= g_{m,CS}R_{CS}$) the second and third order intermodulation products are the following:

IM2 and IM3 expressions

$$V_{O,IM2} = \frac{g_{2,CS}R_{CS}}{4}V_S \tag{2.22}$$

$$V_{O,IM3} = \left[\frac{g_{2,CG}g_{2,CS}R_SR_{CS}}{8} + \frac{g_{3,CS}R_{CS}}{8}\right]V_S \tag{2.23}$$

In each of the previous expressions the distortion at the output it's not proportional to coefficient of the CG. This is because at the two single ended outputs the coefficient of distortion of the CG of second (in 2.22) and third (in 2.23) distortion $g_{2,CG}$ and $g_{3,CG}$ have the same sign, so they are cancelled at the differential output. In other words the distortion of the common gate at the two outputs is a common mode contributor, like the noise, and so it's cancelled at the differential output. Therefore, as introduced before, with a wideband balun-LNA noise and distortion cancelling of the CG stage are obtained.

2.4 Conclusions

Today's implementations of multi-band receivers usually stack several individually tuned and optimized RF front-end, and when possible share the IF circuit blocks. The first step towards a multi-band front-end is a linear, wide-band low noise amplifier (LNA). Narrowband LNA design benefits significantly from resonant input circuits and loads to achieve high gain, low noise figure and impedance matching. Anyway, even a wideband LNA must provide high gain, low noise figure and also acceptable 50 Ω input matching over many decades. This requires new design techniques and circuit configurations.
In this paragraph the noise cancelling technique to low the noise of broadband LNA is presented. First this technique on a single ended amplifier is described. After the implementation of the noise cancelling on a single to differential LNA is shown. The CG-CS topology is used and an intuitive and detailed analysis of noise and distortion is done. Therefore in this paragraph the CG-CS topology as wideband balun LNA with input matching, output balancing and simultaneous noise and distortion cancelling is investigated. In the next chapter an improvement of this architecture is proposed.

References

[2.1] K. Vavelidis, I. Vassiliou, N. Haralabidis, A. Kyranas, Y. Kokolokis, S. Bouras, G. Kamoulakos, C. Kapnistis, S. Kavadias, N. Kanakaris, E. Metaxakis, C. Kakozidis, H. Peyravi, *A 65nm CMOS Multi-Standard, Multi-Band*, Proc. IEEE, 2007.

[2.2] F. Bruccoleri, Eric A.M. Klumperink and Bram Nauta, *Wide-Band CMOS Low-Noise Amplifier Exploiting Thermal Noise Cancelling*, Proc. IEEE vol. 39, no. 2, Feb. 2004.

[2.3] Stephan C. Blaakmeer, Eric A.M. Klumperink , Domine M. W. Leenaerts and Bram Nauta *Wideband Balun-LNA With Simultaneous Output Balancing, Noise-Cancelling and Distortion-Cancelling* , Proc. IEEE vol. 43, no. 6, pp. 183-193, June. 2008.

[2.4] A. Liscidini, G. Martini D. Mastantuono, and R. Castello " *Analysis and Design of Configurable LNAs in Feedback Common Gate Topologies*" on Volume 55, Issue 8, Aug. 2008 Page(s):733-737, IEEE Transaction on Circuits and Systems Part II: Express Briefs (TCAS2).

3

Wideband Balun LNA with Noise Cancelling and IM2 cancellation feedback

In true multi-standard and wideband operation, intermodulation and harmonics of interferers at distant frequencies can generate in band interference. For this reason the RF front-end must have high linearity, i.e. high second and third order distortion intercept points (IIP2 and IIP3). It is not trivial to build a wideband active balun with an low enough IM2, indeed, state-of-the-art wideband receivers [3.1-3.2] typically have single-ended inputs, leading to a lower IIP2 compared to fully differential topologies. In this chapter a technique to improve the IM2 of a single to differential amplifier is described. A new low noise circuital implementation of a wideband balun LNA is analyzed and the measurements of NF, IIP2 and IIP3 of a test chip are presented.

3.1 Second order distortion cancellation

IM2 generation in a single to differential amplifier

To show how, in principle, the even order distortion of a single-ended input, differential output amplifier can be effectively cancelled let us first investigate how this distortion is generated using the simplified block diagram in Figure 3.1 [3.3]. Single-ended to differential conversion is achieved using two separate amplifiers (as presented in chapter 2 for the CG-CS topology): one inverting and one non-inverting.

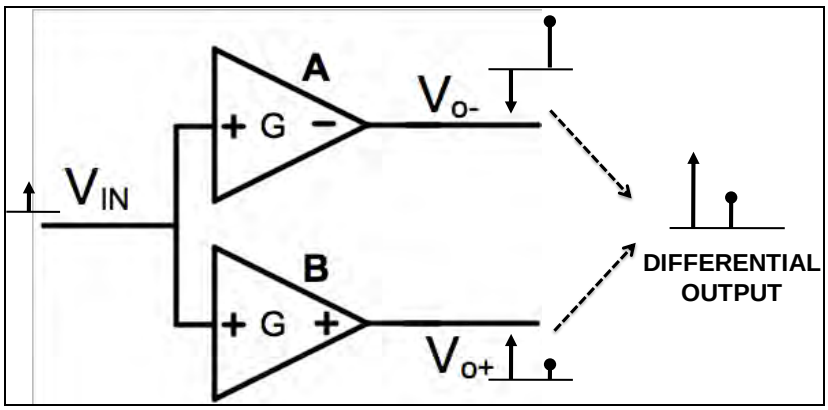

Figure 3.1:Block diagram of a single to differential amplifier.

In order to convert the input signal to a pair of balanced output signals the two amplifiers need to have the same gain but opposite phases (black arrows in Figure 3.1). Second order distortion, arising from the non-linearity of the active devices in the two amplifiers, will produce two fully correlated distortion components in the output terminals (black arrows with circular top). The two components will not necessarily have the same magnitude in a wideband amplifier (in fact this is generally not the case); however they generally have the same phase. As a result, considering the differential output, a finite second order distortion will corrupt the desired signal.

IM2 cancellation with feedback

If now the common mode in the outputs (Figure 3.2) is measured, the linear signal will be ideally zero (assuming perfectly balanced output) while the even order distortion will be equal to the addition of the distortion components produced by the two amplifiers. By feeding back the common mode output to the amplifier input with the proper amplitude and phase, the even order distortion in the differential output can be fully cancelled. Notice that, since the amplitude of the linear signal in the common mode output is zero (no black arrow, but only the gray one appears, the common mode (CM) IM2 distortion), any second order nonlinearity in the feedback path will not result in second order distortion. The amount of feedback (α) needed to perform the distortion cancellation depends on the relative distortion produced by the two amplifiers. The feedback is a particular kind of 'common mode' feedback: the loop gain is zero and there is a single

'Common mode' feedback with $G_{LOOP}=0$

input so the usual consideration for common mode feedback loops here do not apply.

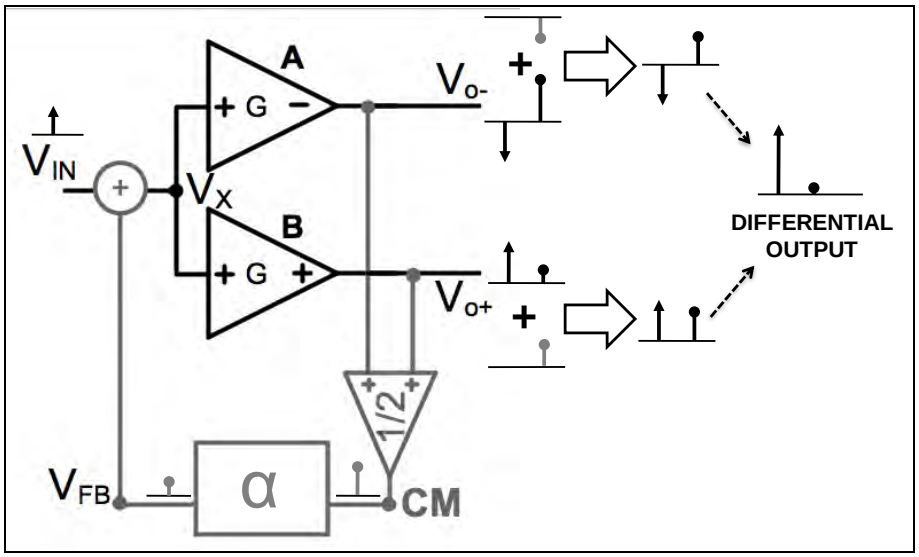

Figure 3.2:Block diagram of a single to differential amplifier with IM2 distortion cancellation feedback.

In other words, applying a signal at the input of the amplifiers we generate to opposite in phase signals (black arrows) at the output and two in phase IM2 distortions (black arrows with circular top). Adding a common mode feedback only the common mode is sensed and so no signal is in the feedback path, but only IM2 distortion (gray arrow with circular top). At this point, just the distortion is re-injected to the input, with a proper feedback factor α. No distortion in the feedback path is generated, because there is no signal in the feedback path. Due to feeding back the common mode of the distortion, at the two outputs the signal is always the same, but the distortion is equalized (gray plus black arrows with circular top). Finally, the distortion at the differential output is ideally cancelled. If the distortion amplitudes are equal, no feedback is necessary, but as shown in the previous chapter, in this scheme the two amplifiers are different and so different distortions appear at the two outputs. This is a key point: the IM2 considered in this kind of architecture is not generated by mismatches in two identical blocks like in the fully differential amplifiers, but by different blocks. The main contribution of this kind of IM2 is systematic and not statistic.

IM2 cancellation with feedforward

Notice that the introduction of the feedback path from the common mode output to the single-ended input does not alter the signal transfer function since the loop gain is ideally zero. As a result the cancellation can be carried out similarly to the feed-forward cancellation suggested in [3.4] and shown in Figure 3.3. In this case the effect on the IM2 is the same but the input matching is not perturbed by the cancellation feedback (e.g. the loading effect of the feedback). The disadvantage is the challenging design of the block that generates the common mode and the duplication of the number of blocks used for the distortion

cancelling. It's important to underline that no signal passes through feedforward blocks, because the CM in only a distortion common mode, otherwise distortion in the feedforwaard path is generated.

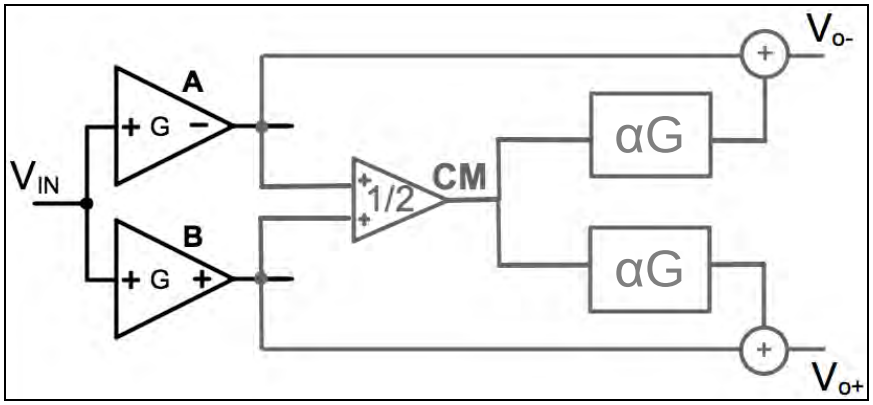

Figure 3.3:Block diagram of a single to differential amplifier with IM2 distortion cancellation feedforward.

IM2 cancellation after the mixer

Another possible implementation of the feedforward uses the downconverter stage too (Figure 3.4). The feedforward path is closed after the mixer stage, with an addition in current. This kind of solution is more efficient than the previous and the stage of transconductance of the feedforward is a simpler solution to realize the common mode of the distortion removing the signal. A solution can be for example a differential PN transconductance stage with the outputs short-circuited.

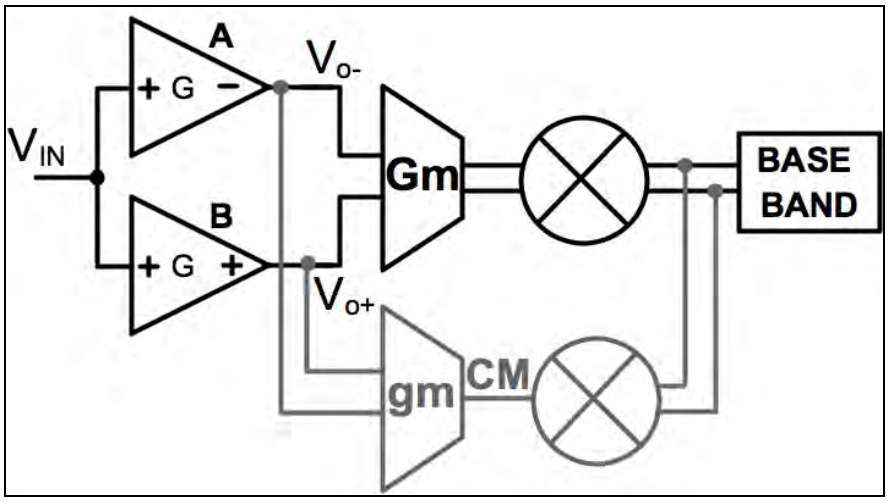

Figure 3.4:Block diagram of a single to differential amplifier with IM2 distortion cancellation feedforward using mixers.

3.1.1 IM2 feedback solution

After an intuitive description of the IM2 cancellation, a more detailed analysis of linearity of second and third order distortion in the case with feedback is done. In the following system the equations to find the non-linear coefficients are summarized:

Non linear analysis of feedback solution

$$\begin{cases} V_{out+} = a_1 v_x + a_2 v_x^2 + a_3 v_x^3 \\ V_{out-} = b_1 v_x + b_2 v_x^2 + b_3 v_x^3 \\ V_{FB} = \left(\frac{V_{out+} + V_{out-}}{2} \right) \alpha \\ V_X = V_{IN} - V_{FB} \end{cases} \quad (3.1)$$

with a_i and b_i the Taylor coefficients of the non-linear transfer function of the inverting amplifier A and the non-inverting amplifier B in Figure 3.2. Considering $a_1=G/2=-b_1$, the second and the third intemodulation products at the differential output are the following:

IM2 and IM3 closed loop coefficients

$$V_{O,IM2} = c_{2,CL} V_{IN}^2 = \left(b_2 - a_2 - G \frac{a_2 + b_2}{2} \alpha \right) V_{IN}^2 \quad (3.2)$$

$$V_{O,IM3} = c_{3,CL} V_{IN}^3 = \left(2G \left(\frac{a_2 + b_2}{2} \alpha \right)^2 - G \frac{b_3 - a_3}{2} \alpha - 2 \left(\frac{a_2 + b_2}{2} \alpha \right) (b_2 - a_2) + a_3 + b_3 \right) V_{IN}^3 \quad (3.3)$$

with $c_{2,CL}$ and $c_{3,CL}$ the IM2 and IM3 close loop coefficients. In the (3.2) and (3.3) with $\alpha=0$ the open loop coefficients ($c_{2,OL}$ and $c_{3,OL}$) are gotten. In particular $c_{2,OL}=(b_2-a_2)$ and $c_{3,OL}=(b_3+a_3)$. From the (3.2) it's possible to extrapolate the value of α to obtain the perfect cancellation (α_{CANC}) of the IM2 ($c_{2,CL}=0$):

General expression of α_{CANC}

$$\alpha_{CANC} = \frac{2}{G} \frac{b_2 - a_2}{a_2 + b_2} \quad (3.4)$$

It's interesting to notice that the higher is the gain G and the total IM2 distortion (a_2+b_2) generated by the two amplifier the lower is the value of α_{CANC}. At the same time, as said before, the lower is the difference of the two distortions the lower feedback factor is needed. Assuming now $\alpha= \alpha_{CANC}$ in the (3.3) the third order coefficient of the differential output becomes:

IM3 coefficient c_3 for $\alpha=\alpha_{CANC}$

$$V_{O,IM3} = (a_3 + b_3) \left(1 - \frac{b_3 - a_3}{a_3 + b_3} \frac{G \alpha_{CANC}}{2} \right) V_{IN}^3 \quad (3.5)$$

Defining now c_3, c_3^* and c_2 as in the following expressions:

$$c_3 = (a_3 + b_3) \left(1 - \frac{b_3 - a_3}{a_3 + b_3} \frac{G \alpha_{CANC}}{2} \right) \quad (3.6)$$

$$c_3^* = \frac{b_3 - a_3}{a_3 + b_3} \tag{3.7}$$

$$c_2 = \frac{G}{2}\alpha_{CANC} = \frac{b_2 - a_2}{a_2 + b_2} \tag{3.8}$$

To better understand the effects of the feedback on the IM3 in a general case can be done (Figure 3.5). Some assumptions on this coefficients has to be done:

- c_2 and c_3^* are between -1 and +1.
- $c_2 \approx 1$ if $b_2 >> a_2$, $c_3^* \approx 1$ if $b_3 >> a_3$. These are limit conditions.
- c_2 and c_3^* are equal to zero only if the two amplifiers in Figure 3.2 have exactly the same second and third order distortion.

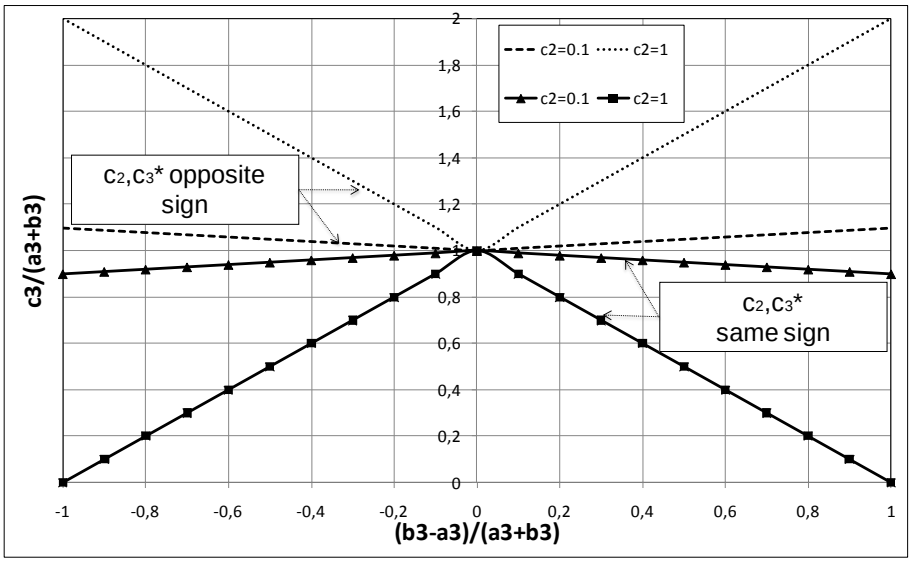

Figure 3.5:Third order intermodulation product.

In Figure 3.5 on the vertical axis is reported the c_3 coefficient normalized to the open loop coefficient ($c_3/c_{3,OL}$), on the horizontal axis c_3*. Four graphs are plotted for two values of c_2: the two dashed ones considering $c_2c_3^*<0$ and the other ones considering $c_2c_3^*>0$. In the first case ($c_2c_3^*<0$) the higher is the difference of the second order distortion of the two amplifiers ($|b_2-a_2|$) the higher is the third order distortion (c_3) too. Instead, if $c_2c_3^*>0$, the higher is $|b_2-a_2|$, the lower is c_3 and so the third order distortion. In the same way, the higher is $|b_3-a_3|$ the higher is IM3 if $c_2c_3^*<0$, but, if $c_2c_3^*>0$, the lower is the third order distortion. In other words, if the two coefficients c_2 and c_3^* have the same sign, the higher is the difference of the second or third order distortion in the two amplifiers the higher is the IM3 improvement. Vice versa if c_2 and c_3^* have opposite sign the best condition is when $c_2=0$ (and so when no feedback is applied) or when the third order distortions are exactly equal in the two amplifiers ($c_3^*=0$). It's possible

to summarize the previous considerations on the IM3 in a balun LNA with feedback for IM2 cancellation in this way:

General conditions for IM3 improvement

- $\frac{c_3}{a_3+b_3} = 1 - c_3^* c_2, c_3^* = \frac{b_3 - a_3}{a_3 + b_3}, c_2 = \frac{b_2 - a_2}{a_2 + b_2}$
- If $c_2 c_3^* < 0$ and $|c_2|$ or $|c_3^*|$ increase, the IM3 increases (dashed curves).
- If $c_2 c_3^* > 0$ and $|c_2|$ or $|c_3^*|$ increase, the IM3 decreases (continuous curves).

No cancellation of IM3 can be obtained in reality using the IM2 cancellation feedback, because only if one of the two amplifiers has no IM2 distortion an IM3 cancellation is realized. Nevertheless considering the conditions expressed before and using the common mode feedback presented, it is possible to reduce the IM3 compared to the case without feedback.
Not only the IM2 and IM3, but also the noise transfer function of the two amplifiers is affected by the feedback. The noise of one amplifier is magnified while the noise of the other is partially suppressed. Consequently, an analysis of the effect of this feedback on the noise cancelling topology is proposed. A noise analysis and linearity analysis are carried out in the next sections for the common-gate, common-source amplifier for different types of feedback.

3.2 IM2 feedback implementation

CG-CS with IM2 cancellation feedback

In order to study the influence of the feedback path on the noise performance, the CG-CS topology is studied and the simplified schematic with ideal feedback is shown in Figure 3.6. The key property of this amplifier is that, by simply imposing impedance matching ($g_{m,CG}=1/R_S$) and balanced outputs ($g_{m,CG}R_{CG} = g_{m,CS}R_{CS} = A_{V,diff}/2$), the noise and distortion generated by the common-gate stage appear at the output as common-mode signals and can therefore be suppressed by the following differential stages.

3.2.1 Noise Analysis

The equivalent generators of thermal noise of the CS ($i_{n,MCS}$) and CG ($i_{n,MCG}$) stages , of their load R_{CG} ($i_{n,RCG}$) and R_{CS} ($i_{n,RCS}$), of the feedback ($i_{n,FB}$) and of the input source($v_{n,RS}$) are:

$$\begin{cases} i_{n,MCS} = \sqrt{4kT\gamma g_{m,CS}} \\ i_{n,FB} = \sqrt{4kT\gamma g_{m,FB}} \\ i_{n,MCG} = \sqrt{4kT\gamma g_{m,CG}} \\ i_{n,RCS} = \sqrt{\frac{4kT}{R_{CS}}} \\ i_{n,RCG} = \sqrt{\frac{4kT}{R_{CG}}} \\ v_{n,RS} = \sqrt{4kTR_S} \end{cases} \quad (3.9)$$

The feedback noise is modelled like a current generator of an equivalent single transistor.

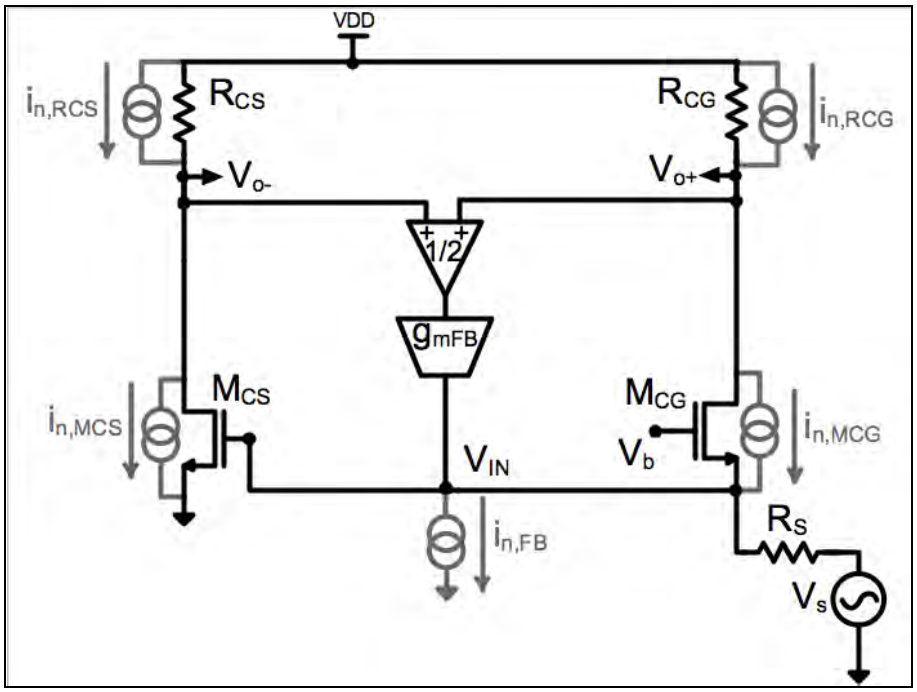

Figure 3.6:Noise sources of CG-CS topology with ideal cancellation feedback.

The transfer functions of noise from the input to the differential output are :

$$\begin{cases} |T_{n,RCG}| = \dfrac{2R_{CG}(1+g_{m,CG}R_S+g_{m,CS}R_{CS}R_Sg_{m,FB})}{-2(1+g_{m,CG}R_S)+(g_{m,CG}R_{CG}-g_{m,CS}R_{CS})R_Sg_{m,FB}} \\ |T_{n,FB}| = \dfrac{2(g_{m,CG}R_{CG}+g_{m,CS}R_{CS})R_S}{-2(1+g_{m,CG}R_S)+(g_{m,CG}R_{CG}-g_{m,CS}R_{CS})R_Sg_{m,FB}} \\ |T_{n,RCS}| = \dfrac{2R_{CS}(-1-g_{m,CG}R_S+g_{m,CG}R_{CG}R_Sg_{m,FB})}{2(1+g_{m,CG}R_S)+(-g_{m,CG}R_{CG}+g_{m,CS}R_{CS})R_Sg_{m,FB}} \\ |T_{n,MCG}| = \dfrac{2(R_{CG}-g_{m,CS}R_{CS}R_S+g_{m,CS}R_{CG}R_{CS}R_Sg_{m,FB})}{-2(1+g_{m,CG}R_S)+(g_{m,CG}R_{CG}-g_{m,CS}R_{CS})R_Sg_{m,FB}} \\ |T_{n,MCS}| = \dfrac{2R_{CS}(1+g_{m,CG}R_S-g_{m,CG}R_{CG}R_Sg_{m,FB})}{2(1+g_{m,CG}R_S)+(-g_{m,CG}R_{CG}+g_{m,CS}R_{CS})R_Sg_{m,FB}} \\ |T_{n,RS}| = \dfrac{2(g_{m,CG}R_{CG}+g_{m,CS}R_{CS})R_S}{-2(1+g_{m,CG}R_S)+(g_{m,CG}R_{CG}-g_{m,CS}R_{CS})R_Sg_{m,FB}} \end{cases} \quad (3.10)$$

It's interesting to notice that the transfer function of the signal is the same of the feedback one. As usual the noise factor can be written as:

$$F = 1+\frac{i_{n,RCG}^2|T_{n,RCG}|^2+i_{n,RCS}^2|T_{n,RCS}|^2+i_{n,MCS}^2|T_{n,MCS}|^2+i_{n,MCG}^2|T_{n,MCG}|^2+i_{n,FB}^2|T_{n,FB}|^2}{v_{n,RS}^2|T_{n,RS}|^2} \quad (3.11)$$

Comparing the (3.12) with the (2.19) not only the noise of the feedback appears in the formula but also the noise of the CG. So at first sight, it seems that there is no more noise cancellation if we introduce this kind of feedback. Substituting the (3.9-1.10) in the (3.11) the final expression of the noise factor is:

$$F = 1+\left(\frac{\alpha}{2}\right)^2\gamma+\frac{\gamma}{\beta}\left(1-\frac{\alpha}{2}\right)^2+\frac{2}{A_{V,diff}}\left(1+\frac{\alpha}{2}\right)^2+\frac{2}{\beta A_{V,diff}}\left(1-\frac{\alpha}{2}\right)^2+\frac{2\gamma\alpha}{A_{V,diff}} \quad (3.12)$$

Noise Factor with feedback α

with $\alpha=g_{m,FB}R_{CG}$ the feedback factor (as shown in Figure 3.2) and $\beta=g_{mCS}/g_{mCG}$, introduced in (2.20). If the (2.20) is rewritten here :

$$F = 1+\frac{\gamma}{\beta}+\frac{2}{A_{V,diff}}+\frac{2}{A_{V,diff}\beta} \quad (3.13)$$

and is compared with the (3.12) these considerations can be done:

- In the noise factor with feedback compare the contribution of noise of the common gate (second term of (3.12)).This one is zero with $\alpha=0$

- The contribution of noise of the common source (third term of (3.12)) is reduced by the increasing of α (when $\alpha<2$, but this is a reasonable condition for a real feedback).
- The fourth contribution is the noise introduced by R_{CG} and it is increased by the feedback factor α.
- The fifth contribution is the noise of the R_{CS} and it's reduced by the feedback factor α.
- The contribution of noise of the feedback is the last term in (3.12) and it's proportional to α.

So, the feedback factor α increases the noise factor of the simple CG-CS stage introducing the noise of the feedback, the noise of the common gate stage and increasing the noise contribution of the R_{CG}. On the other hand the noise of the CS and the noise of the R_{CS} are reduced if the α increase. Therefore it's not clear if the common mode feedback increase or decrease the total noise.
To understand this and to find a design rule, the following plot in Figure 3.7 is done. Curves a), b) and c) are drawn for a constant voltage gain of 5 and different values of β. For low power designs $\beta=1$ ($g_{m,CS}=g_{m,CG}$), the noise is found to be slightly improving when feedback is increased. For lower noise, $g_{m,CS}$ must be increased. If $g_{m,CS}$ is increased but R_{CS} is lowered to keep a constant gain, noise lowers more quickly if the feedback path is not enabled ($\alpha=0$). This is due to the fact that, when the feedback is enabled, a greater part of the noise is due to the load resistors. If, on the other hand, the gain is increased together with $g_{m,CS}$ (e.g. keeping the load resistance constant) as in curves d), e), it becomes possible to decrease the noise figure in the IM2 cancelling configuration approximately in the same way as in the noise cancelling configuration. The optimal choice of $A_{V,diff}$ and β depends on the specific design target.

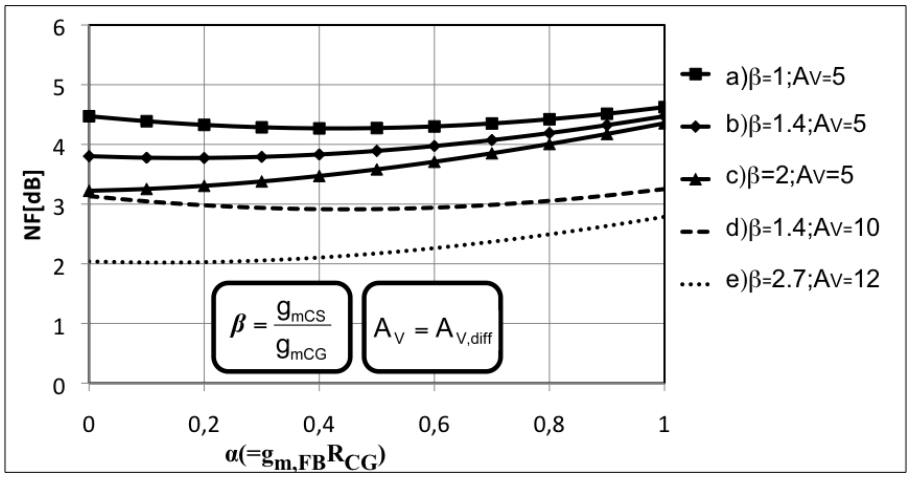

Figure 3.7:Calculated noise figure for different values of β and $A_{V,diff}$, with a variation of the feedback factor α.

3.2.2 Distortion Analysis: IM2 and IM3

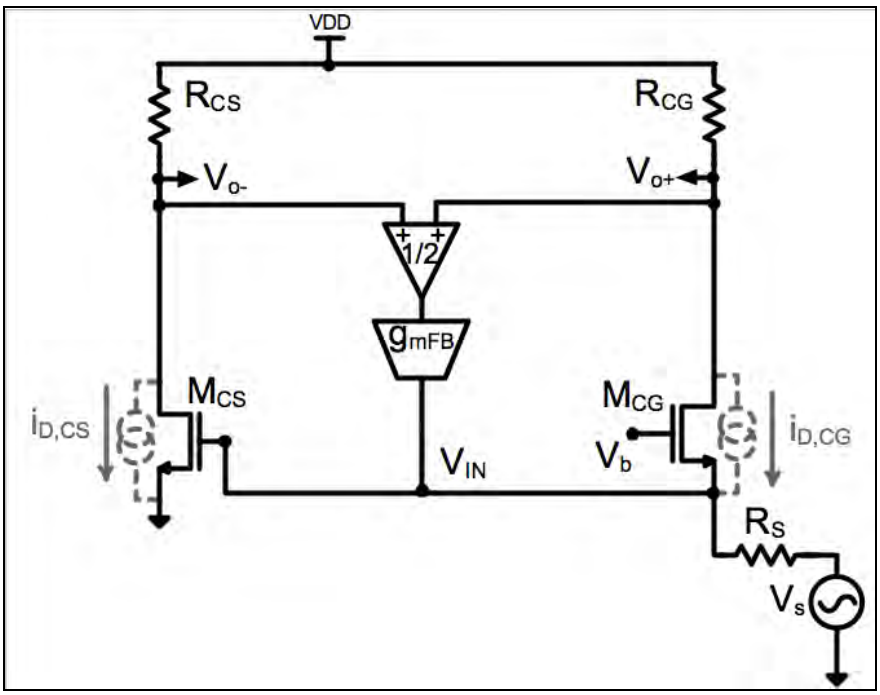

Figure 3.8: Non-linear sources of CG-CS topology with ideal cancellation feedback.

After the description of the influence of feedback on noise, the linearity analysis (as done in the ideal case, Figure 3.2) can be extended to the CG-CS topology with ideal feedback (Figure 3.8).
To determinate the distortion of this circuit, the following system has to be solved:

$$\begin{cases} \dfrac{V_{in}-V_S}{R_S} = i_{D,CG} + i_{FB} \\ V_{o+} = -i_{D,CG}R_{CG} \\ V_{o-} = -i_{D,CS}R_{CS} \\ i_{D,CG} = g_{m,CG}(-V_{in}) + g_{2,CG}(-V_{in})^2 + g_{3,CG}(-V_{in})^3 \\ i_{D,CS} = g_{m,CS}(-V_{in}) + g_{2,CS}(-V_{in})^2 + g_{3,CS}(-V_{in})^3 \\ V_{in} = A_1V_S + A_2V_S^2 + A_3V_S^3 \\ i_{FB} = \dfrac{V_{o+}+V_{o-}}{2} g_{m,FB} \end{cases} \qquad (3.14)$$

IM2 coefficient for CG-CS with feedback

At the differential output, imposing the conditions of input matching ($g_{m,CG}=1/R_S$) and output balancing ($g_{m,CG}R_{CG}= g_{m,CS}R_{CS}$) the second order intermodulation product is the following:

$$V_{O,IM2FB} = \left(g_{2,CS}R_{CS} - R_{CG}g_{m,FB}\frac{g_{2,CS}R_{CS} + g_{2,CG}R_{CG}}{2} \right)\left(\frac{V_S}{2}\right)^2 \quad (3.15)$$

From the (3.15) the transcoductance that gives a perfect cancellation of $V_{O,IM2FB}$ is:

Feedback transconductance for IM2 cancellation

$$g^*_{m,FB} = \frac{2}{R_{CG}}\left(\frac{g_{2,CS}R_{CS}}{g_{2,CS}R_{CS} + g_{2,CG}R_{CG}}\right) = \frac{2}{R_{CG}}\left(\frac{1}{1 + \frac{g_{2,CG}}{g_{m,CG}}\frac{g_{m,CS}}{g_{2,CS}}}\right) \quad (3.16)$$

Moreover the expression of third order intermodulation product with input matching ($g_{m,CG}=1/R_S$) , output balancing ($g_{m,CG}R_{CG}= g_{m,CS}R_{CS}$) and $g_{m,FB}=g^*_{m,FB}$ is:

IM3 coefficient for CG-CS stage with feedback

$$V_{O,IM3FB} = \left[\frac{g_{3,CS}R_{CS}}{8} + \frac{g_{2,CS}R_{CS}}{8}\frac{g_{3,CS}R_{CS} - g_{3,CG}R_{CG}}{(g_{2,CG}R_{CG} + g_{2,CS}R_{CS})}\right]V_S^3 \quad (3.17)$$

Comparing the (3.17) with the (2.23) a consideration on the IM3 can be done. With feedback it's possible to obtain an improvement of the third order linearity, as described in the analysis of the block diagram (Figure 3.2). Indeed, with $g_{2,CS}$,$g_{2,CG}$>0 the IM3 without feedback increases, instead the IM3 with feedback decreases, if the second term of (3.17) is positive. Rewriting the (3.17) considering $g_{m,CG}R_{CG}= g_{m,CS}R_{CS}$ the following expression for the IM3 closed loop ($IM3_{CL}$) coefficient can be written:

$$IM3_{CL} = \left|\frac{g_{3,CS}R_{CS}}{8}\left(1 - \frac{\frac{g_{3,CG}}{g_{m,CG}}\frac{g_{m,CS}}{g_{3,CS}} - 1}{1 + \frac{g_{2,CG}}{g_{m,CG}}\frac{g_{m,CS}}{g_{2,CS}}}\right)\right| \quad (3.18)$$

with $IM3_{OL}$ equal to:

$$IM3_{OL} = \left|\frac{g_{3,CS}R_{CS}}{8}\left(1 + \frac{g_{2,CS}g_{2,CG}}{g_{3,CS}g_{m,CG}}\right)\right| \quad (3.19)$$

from the (2.23). In Figure 3.9 the ratio $IM3_{CL}/IM3_{OL}$ is plotted. In this case the coefficients of two simulated transistors are substituted in the equations. In this way a description of different cases can be evaluated. Different bias voltages for the CS gate, sweeping the bias voltage of the CG are used. The ratio $IM3_{CL}/IM3_{OL}$, for the coefficients considered, it's often under one. Consequently it seems

Simulations to verify the theoretical IIP3 improvement

that the feedback realize an improvement of the IIP3 of the LNA enough easily. In This simulations the β factor is considered constant (β=2.5) and the two transconductances are $g_{m,CG}=1/R_S=20mS$ and $g_{m,CS}=50mS$. In this way the input matching condition is guaranteed.

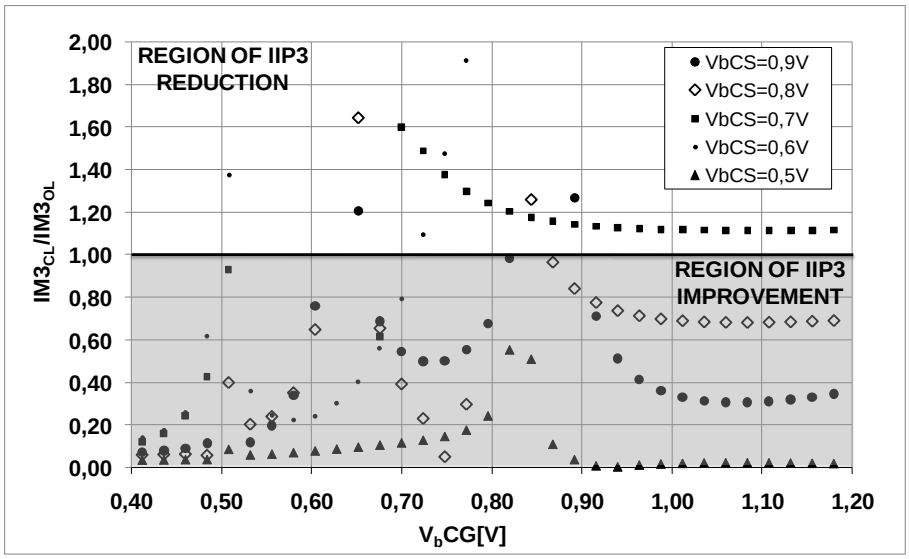

Figure 3.9:Theoretical expression of $IM3_{CL}/IM3_{OL}$ considering simulated coefficients for different bias voltages of CG and CS.

Anyway this analysis is a simplification of the problem. Indeed, the two stages are considered as one transistor stage and the non-linearity is considered just in band. The effects of the limitation of bandwidth are not considered. In other words, introducing the feedback for the IM2 cancellation the IIP3 can be improved for particular bias conditions of the CG and of the CS stage. This improvement is confirmed through the equations (3.18) and (3.19), using the coefficients obtained by simulations. Hence, the IIP3 improvement doesn't seem to be difficult to achieve, for a given bias for the CG, with real non-linear coefficients too.

As a result, applying the common mode feedback to the CG-CS topology an ideal cancellation of IM2 for a particular value of feedback transconductance is obtained. Then an improvement of third order distortion can be achieved. These results follow the ones introduced in the previous paragraph using just block diagrams.

Circuital implementation of feedback

A circuital implementation of the feedback is presented in [3.3]. The schematic of the feedback is reported in Figure 3.10. The ideal block to sense the common mode of the outputs is simply a resistive divider. The $g_{m,FB}$ is realized with a single MOS (M_{FB}) and M_{FBEN} is used only to enable or disable the feedback. In other words, it connects the feedback to the input acting as a variable degeneration. All the considerations done before for the ideal feedback are valid also with this topology. The main disadvantage of this choice is the high noise introduced by the feedback. A noise figure higher than 5dB for the whole LNA with a buffer at the output is measured [3.3]. So, using the

topology of Figure 3.10 an IM2 cancellation is obtained, but the advantage of noise introduced by the noise cancelling is missed. In the next paragraph a less noisy architecture is presented.

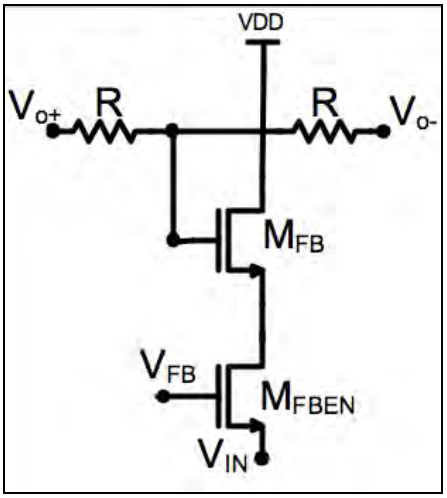

Figure 3.10: Circuital implementation of the common mode feedback.

3.3 Low noise feedback implementation

New low noise feedback implementation

The idea behind the solution proposed in this paragraph is to exploit the noise and distortion in the common mode output, dominated by the common-gate stage, to simultaneously cancel out the IM2 distortion in the differential output and improve noise. A feedback transconductor with low output noise is implemented in this design. Before to describe the circuital implementation, it's necessary to analyze the feedback topology using ideal blocks. In particular the functionality of the new kind of feedback is proposed in Figure 3.11.

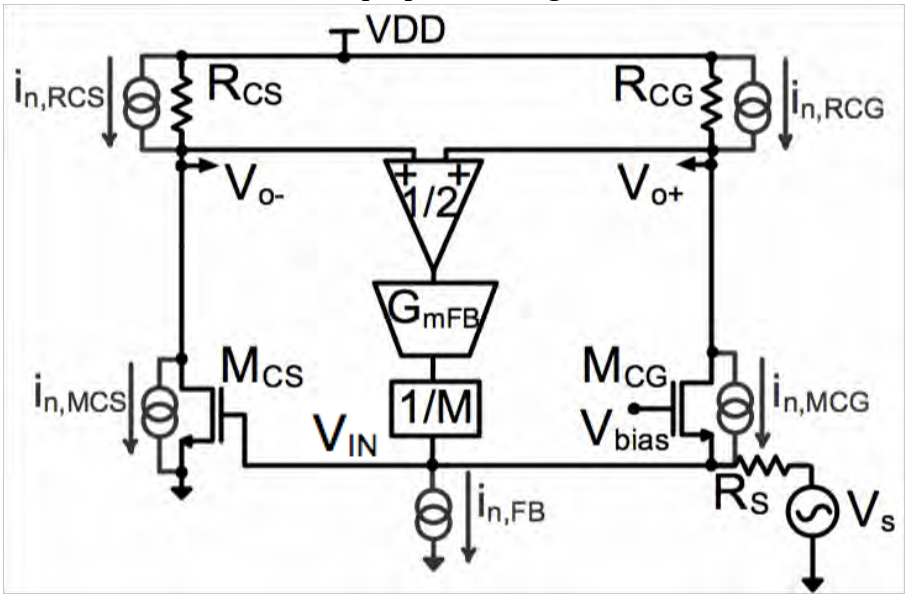

Figure 3.11: Bolck diagram of the IM2 cancelling low noise common mode feedback.

The difference between this feedback and the one introduced in Figure 3.6 is the block for the 1/M division. So, the feedback transconductance $g_{m,FB}$ is :

$$g_{m,FB} = \frac{G_{m,FB}}{M} \tag{3.20}$$

From a linearity point of view the analysis proposed in the previous paragraph remains valid. The expression for the $g_{m,FB}^{*}$ is again the (3.16) and the coefficient for the third order intermodulation product is the (3.17).
From the noise analysis point of view, a significant improvement is made.. All the contributions of noise are the same, the only difference is the transfer function of the feedback and so only the contributions of the feedback is changed. As a result, all the contributions are the same except for the feedback one, that is divided by M. Substituting in the (3.9) the (3.19) and then using the (3.10) the noise factor for this new kind of feedback is:

Noise Factor with new feedback

$$F = 1+\left(\frac{\alpha}{2}\right)^2\gamma+\frac{\gamma}{\beta}\left(1-\frac{\alpha}{2}\right)^2+\frac{2}{A_{V,diff}}\left(1+\frac{\alpha}{2}\right)^2+\frac{2}{\beta A_{V,diff}}\left(1-\frac{\alpha}{2}\right)^2+\frac{2\gamma\alpha}{MA_{V,diff}} \tag{3.21}$$

As described before, some terms are increased by the feedback α (the second, the fourth and last respectively the CG, the R_{CG} and the feedback term) and some others are decreased (the third and the fifth respectively the CS and the R_{CS} term). In conclusion, from the (3.21), introducing the 1/M divider, the contribution of noise introduced directly by the feedback, is divided by M compared with the (3.12). No changes are done for the 'signal'(in this case the signal is only the second order distortion) in the feedback path, indeed the IM2 cancellation can be realized with the same value of $g_{m,FB}$ than in the previous paragraph. Vice versa the noise is reduced because the signal is divided by M but the noise is divided by M^2. Consequently the signal to noise ratio of this contribution is multiplied by M or in other words the noise is reduced of M times.

M divider: Quantitative analysis

After a qualitative analysis of this new kind of feedback, a quantitative consideration for a design can be done. First of all, the amount of the reduction of noise due to the M factor has to be analyzed. In Figure 3.12 the total noise and the contribution of the feedback, normalized to the total noise with M=1 are plotted.
The circuit is supposed to be with an α=1 and a constant gain. Looking to the picture, the reduction of the feedback contribution and, as a consequence, the reduction of the total noise increasing M is shown. In particular, for M≥4 the total noise is constant, even if the contribution of the feedback continues to be reduced.

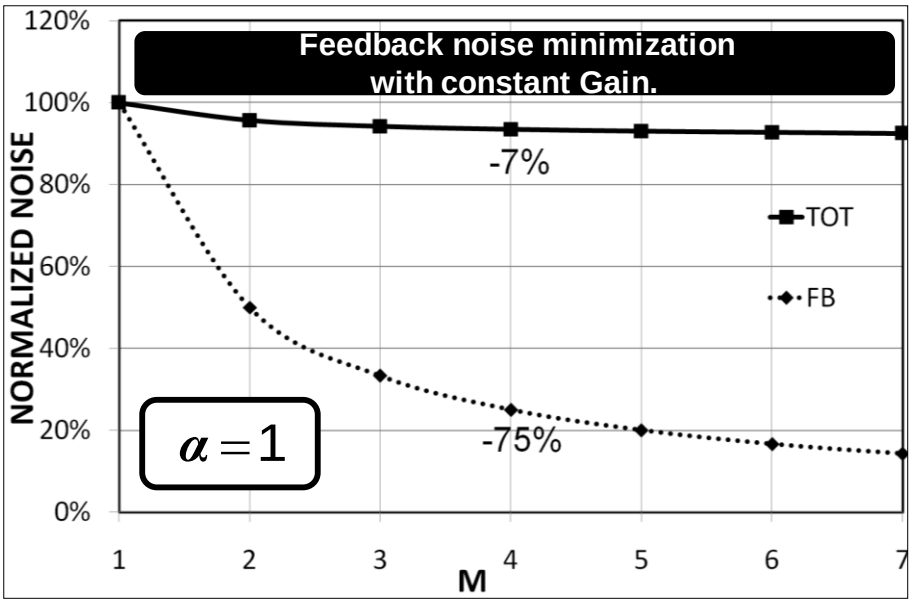

Figure 3.12:Variation of total and the feedback noise using the M divider.

Value of M: Power vs Noise

This is due to the fact that the maximum reduction of the total noise is 7% and after the reduction of 75% of the feedback contribution this one is negligible. So it isn't useful to have M≥4 and, as will be clearer after, a higher M implies a higher power dissipation.

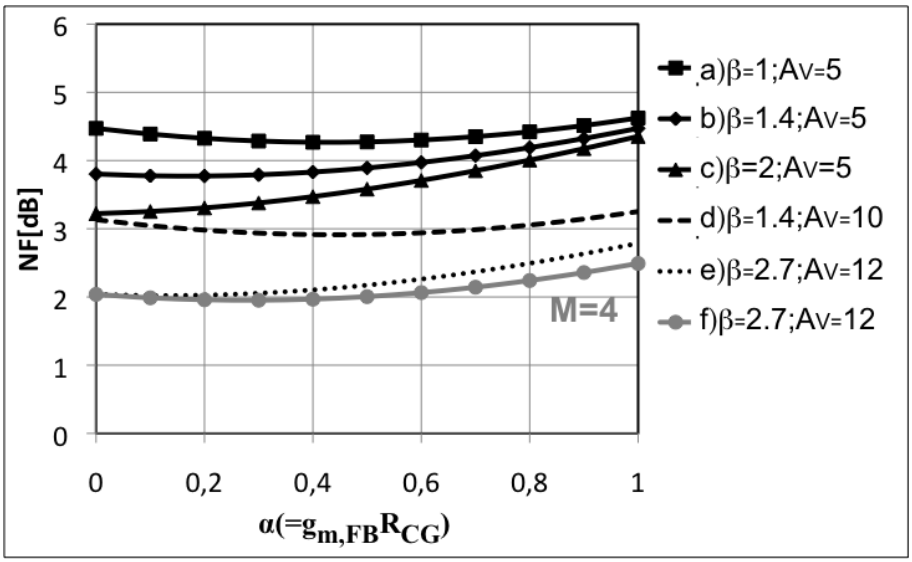

Figure 3.13: Calculated noise figure for different values of β and $A_{V,diff}$, with a variation of the feedback factor α and introducing M>1.

In any case the Figure 3.12 is the proof that, even if the gain, the feedback factor (α) and the ratio between the transconductances of the CS and of the CG (β) are constant, with this typology of feedback is possible to reduce the noise.

Effects of 1/M block on noise

The Figure 3.13 is the plot of different curves for different values of β and differential gain in function of the α factor. The curves from a) to e) are already shown in Figure 3.7. As already said, for α=0 there's a

reduction of the NF increasing β for a fixed gain(a)-c)).The reduction is substantially null if the α factor increases (α=1). In other words there's a high dependence on α of the NF. To reduce this dependence a higher gain is necessary. Indeed, comparing the curves b) and d), with the same β, but with a double gain, a lower NF and a flatter curve in the plot is obtained. That means that to reduce the dependence on α a higher gain has to be realized. In particular, in curve e) for a gain and β shown in the graph, a NF round 2dB and an enough low dependence on α is obtained. The problem of this choice of parameters is that the α factor optimum (α_{OPT}) to obtain the lowest NF is essentially equal to zero. In other words, the best configuration of noise is the one without feedback and so without IM2 cancellation. Vice versa to obtain an IM2 cancellation a disadvantage in noise is needed. To overcome this problem, the 1/M divider is used. Indeed, not only a reduction of noise and a less dependence on α is realized with the divider, but an optimum value of the feedback factor in term of noise can be implemented ($\alpha_{OPT} \neq 0$). So, in principle, it's possible to comprehend that an LNA with particular value of feedback factor ($\alpha=\alpha_{OPT}$) can be designed with a lower noise than an LNA without feedback (α=0). In Figure 3.14 the NF in function of β is plotted. With a $\alpha=\alpha_{OPT}$ is possible to get a NF lower than α=0. In a real implementation the β factor is enough higher than 1 and, as plotted in the picture, for enough high values of β the noise figures with and without feedback are essentially the same.

α optimum for noise (α_{OPT})

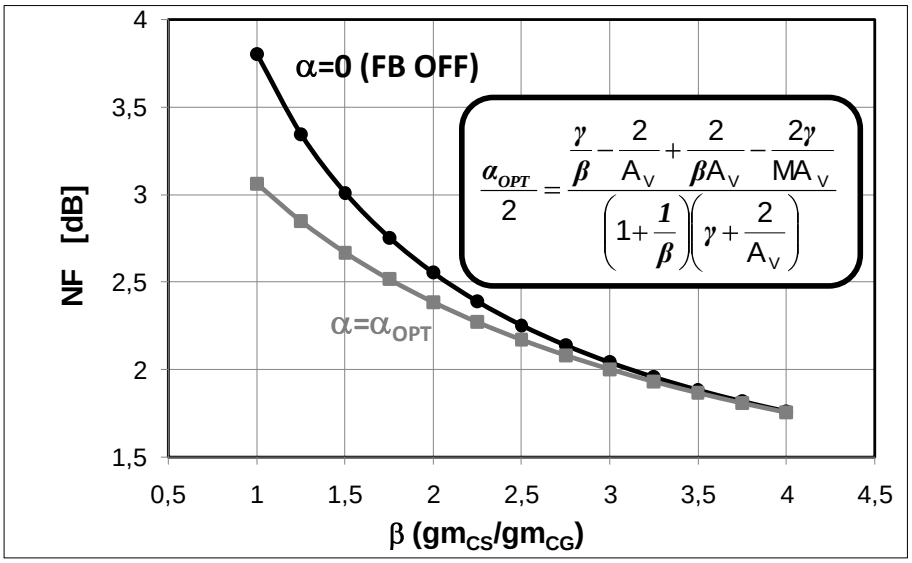

Figure 3.14: Design flow for an optimum feedback for minimum noise.

The expression for α_{OPT} derived by the (3.21) is:

$$\frac{\alpha_{OPT}}{2} = \frac{\frac{\gamma}{\beta} - \frac{2}{A_V} + \frac{2}{\beta A_V} - \frac{2\gamma}{MA_V}}{\left(1+\frac{1}{\beta}\right)\left(\gamma+\frac{2}{A_V}\right)} \tag{3.22}$$

Now re-writing the (3.16) as:

α for IM2 cancellation (α_{CANC})

$$\alpha_{CANC} = g^{*}_{m,FB} R_{CG} = \left(\frac{2}{1+\frac{g_{2,CG}}{g_{m,CG}}\frac{g_{m,CS}}{g_{2,CS}}} \right) \tag{3.23}$$

the value of the feedback factor for the IM2 cancellation is derived. From the (3.22) and (3.23) a design methodology for an LNA with this feedback can be done:

Design optimization: $\alpha_{CANC}=\alpha_{OPT}$

- Using a divider (M>1) the noise directly introduced by the feedback can be minimized.
- From (3.22) is possible to get a value of $\alpha=\alpha_{OPT}$ (proportional to β, A_V and M) to optimize the noise of the LNA with feedback. The NF obtained can be lower than the LNA without feedback.
- Designing the CG-CS stage, and in particular their bias points, the IM2 cancellation can be realized for the feedback factor that allows the minimum NF ($\alpha_{CANC}=\alpha_{OPT}$).

In this way, it's possible to design a wideband balun LNA with simultaneous IM2 and noise cancellation and with an improvement in terms of IM3. Hence, even if using a feedback, it is possible to obtain a NF lower than the simple noise cancelling.
In the next paragraphs a test chip implementing this kind of feedback and the measurements of NF, IIP2 and IIP3 are presented.

3.3.1 Test chip

A feedback transconductor with low output noise is implemented in the design (Figure 3.15). The common-mode voltage is sensed with two pair of small MiM (metal-insulator-metal) capacitors, instead of two resistors as in [3.3]. This allows to filter the signal and to reduce the noise. The two pairs of capacitors are different because the capacitance of the MOS P and MOS N driven are different. Using the definitions introduced in Figure 3.11, the $G_{m,FB}$ is realized with a PN stage cascoded and is:

Noise analysis of real implementation

$$G_{m,FB} = g_{mFB,P} + g_{mFB,N} \tag{3.24}$$

The divider is realized with a simple current mirror in which the current mirrored is M times less than the current of the feedback. In this design the M factor is equal to 4. The contribution of noise directly added by the feedback is $2\gamma\alpha/MA_{V,diff}$ (3.21). Considering $\alpha=g_{m,FB}R_{CG}$ and $A_{V,diff}=g_{m,FB}R_{CG}$ the contribution of noise added by this kind of feedback (F_{FB}) becomes :

$$F_{FB} = \frac{\gamma G_{m,FB}}{M g_{m,CG}} = \frac{\gamma}{g_{m,CG}}\left(\frac{g_{mFB,P} + g_{mFB,N}}{M} + g_{m,1}\left(1 + \frac{1}{M}\right)\right) \tag{3.25}$$

Looking the (3.25), a consideration can be done: not all the contributions of the feedback are divided by M. The contribution of the transistor directly connected to the input appears at the output without attenuation. Consequently, this contribution has to be negligible than the other terms, otherwise the current divider is useless. The total current of the feedback is 430µA on a 1.2V supply voltage.

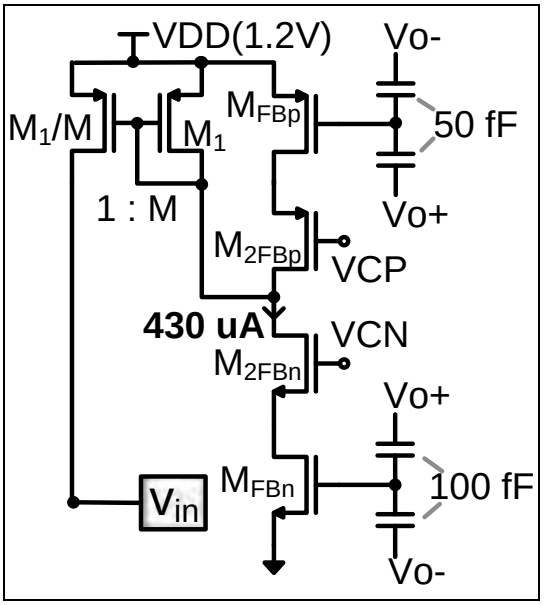

Figure 3.15: Circuital implementation of the low noise IM2 cancellation feedback.

The wideband balun LNA is realized with a CG-CS stage (Figure 3.16). The transconductance of the common source is realized with a PN stage to optimize the power consumption and to don't have a to equalize the DC level at the two outputs. Two bypass capacitors are used at the input of the CS to decouple the DC and a big off-chip inductor is used to have a high impedance towards ground at RF.

CG-CS implemetation

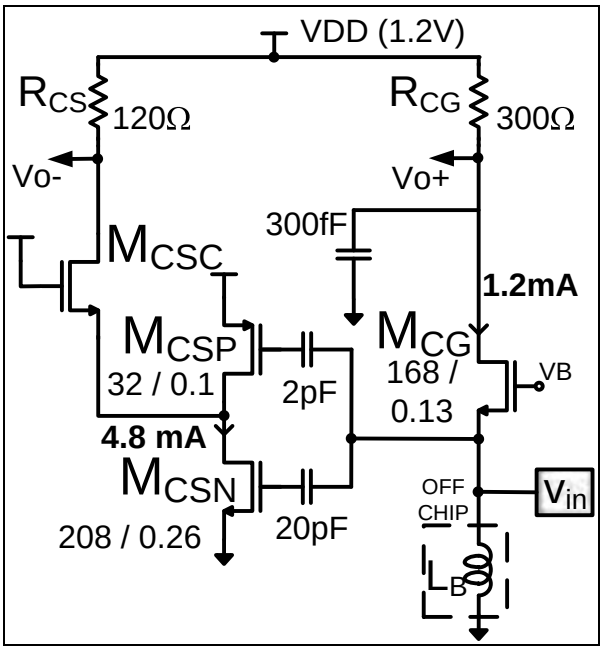

Figure 3.16: Circuital implementation of the wideband balun LNA.

The CS is cascoded, while the CG is not, because this stage is like a cascode for the input source. The two resistors and the two transconductances are different and in particular the β factor is 2.5.
For a variation of the gain of less than 2dB there's a high variation of the IM2 cancellation (Figure 3.17). Due to phase shifts of the cancellation terms, the IIP2 cancellation decreases. The poles in the feedback path, indeed, limit the cancellation because the distortion components re-injected by the feedback are not in anti-phase with the IM2 components without feedback. In any case, in the band of interest (VHF III-UHF IV-V bands) the improvement of the IIP2 is always higher than 10 dB.

Simulation results : IIP2 cancellation vs frequency:

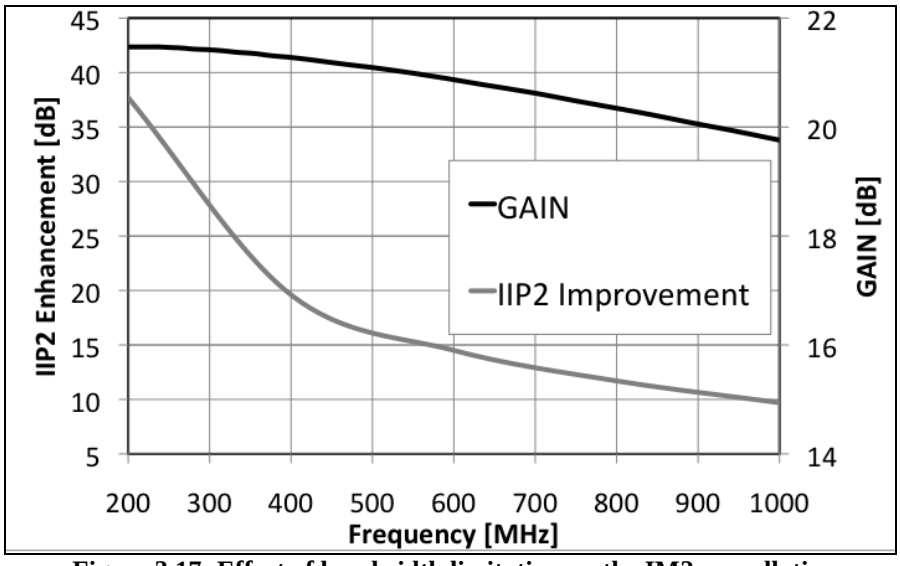

Figure 3.17: Effect of bandwidth limitation on the IM2 cancellation.

In Figure 3.18 the gain and the noise simulated of the wideband balun LNA with IM2 cancellation feedback are plotted. The gain is lower than 21 dB and the noise figure is higher than 2dB and less than 3dB in the whole band of interest.

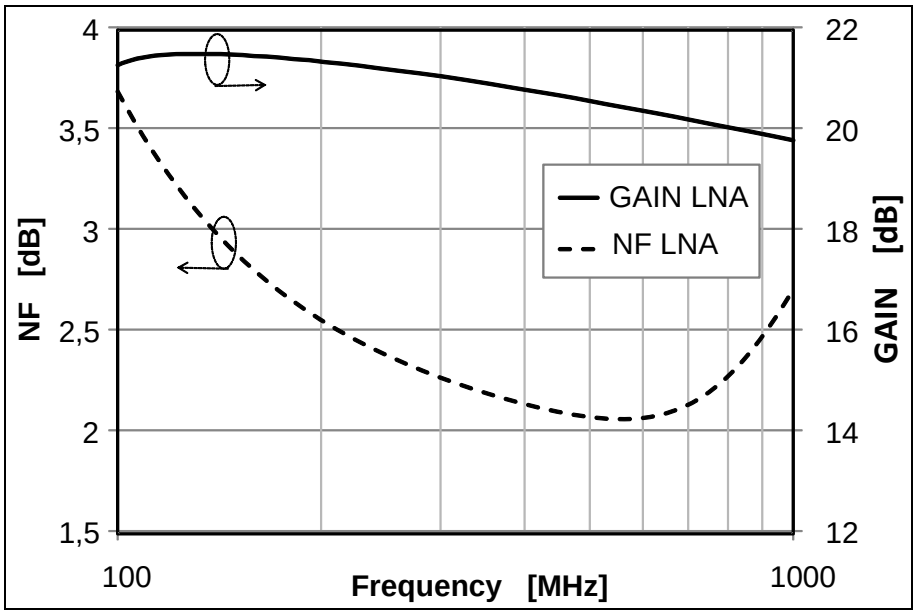

Figure 3.18: Gain and noise simulated for the wideband LNA with feedback.

The test chip for the measurements is divided in two chain: one for the linearity measurement and another for the noise measurement (Figure 3.19). In both of this chain the same instance of the LNA is used, but different stages follow it. The area of the only LNA is 0,056 mm^2.The technology used for the IC is the 90nm TSMC 1P6M with 3µm-thick TOP metal.

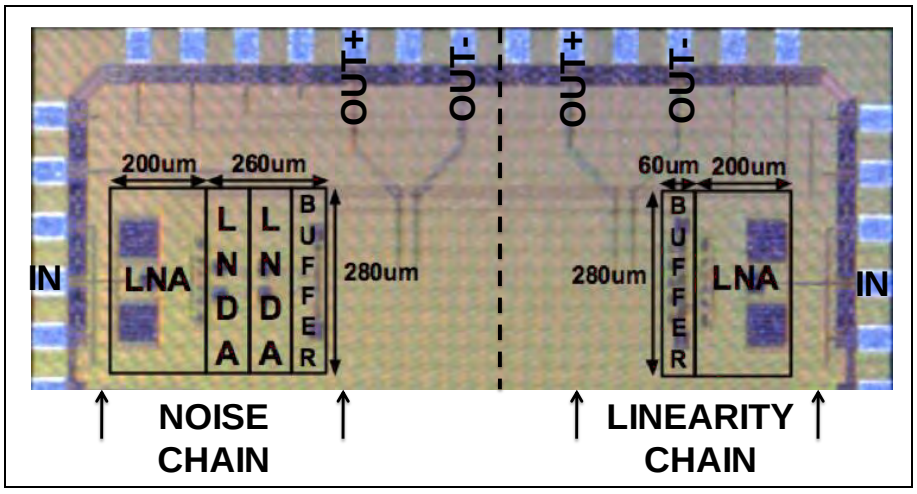

Figure 3.19: Chip photograph.

More in detail to measure the noise of the LNA three buffers to enhance the gain are used. The first two (Figure 3.20) are pseudo-differential stage, the last one is a differential stage. The same

differential stage is used for the linearity chain after a capacitive attenuator. In this way for the noise chain a gain enough high for the noise measurement (>40dB) is realized. Moreover, introducing 20dB of attenuation, the distortion generated by the buffer that allows the difference of the outputs in the linearity chain is negligible. The supply voltage of the buffers is 1.5V.

Measurement strategy: linearity and noise chain

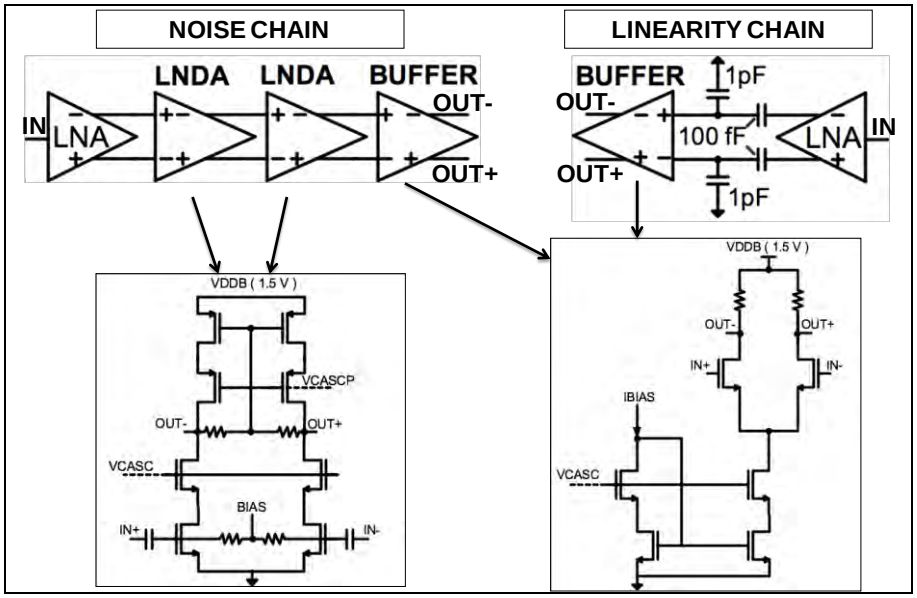

Figure 3.20: Noise and linearity chain.

In the following paragraphs the measurements of NF and IIP2 and IIP3 of the test chip proposed are described.

3.3.2 Experimental results

Two different instances has to be measured: one for the linearity performance and the other for the noise performance.

Noise chain gain and S11

In Figure 3.22 the gain of the noise chain and the input matching are reported. In the whole band of interest the matching condition is satisfied (s_{11}<-15dB). The gain measured fits with the simulation of the noise chain and it's higher than 40dB. Always using the noise chain described in Figure 3.20 the measurement of the noise figure is done. In Figure 3.22 three graphs are plotted. The dashed one that is the NF simulated of the single LNA without buffers, as reported in Figure 3.18. The gray line is the simulation of the NF considering also the three buffers of the noise chain, and the black line is the measurement realized with the spectrum analyzer [3.5]. The difference between the dotted line and gray line is due to the noise introduced by the three buffers. The NF is lower than 3dB for few decades in the centre of our band of interest.

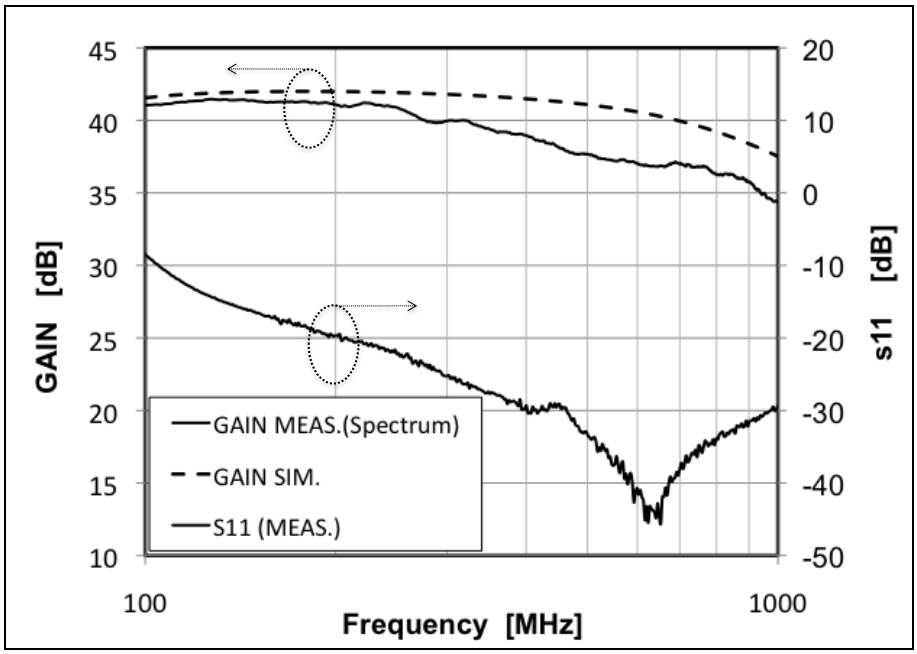

Figure 3.21: Gain of the noise chain and input matching.

Moreover, the flicker noise is lower in measurement than in simulation and instead the noise is higher at high frequency, for the lower bandwidth of the test chip LNA compared with the simulated one. This effect is due to the parasitic capacitance at the output of the LNA.

Noise chain NF vs simulated NF

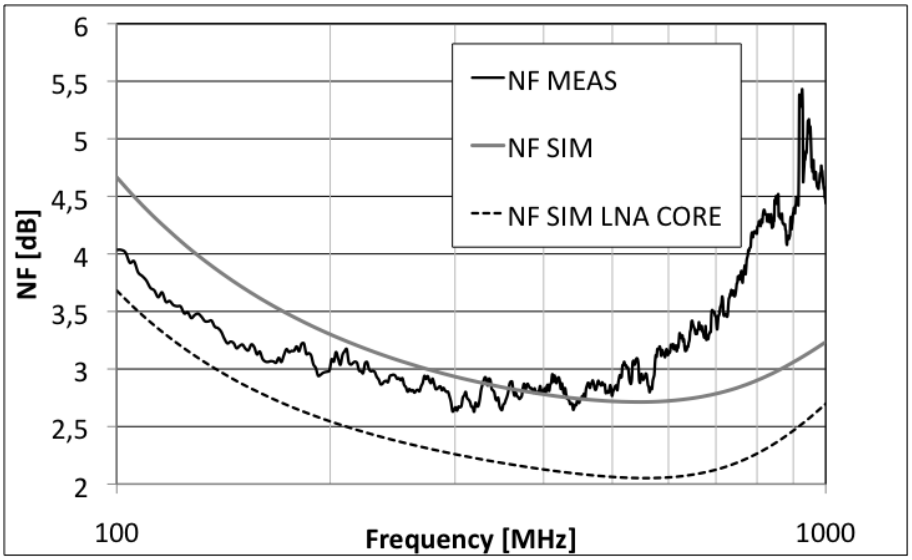

Figure 3.22: Simulation and measurement of the noise chain NF

IIP2 and IIP3 single tone measurements

For the linearity measurements, as described before, the linearity chain shown in Figure 3.20 is tested. The linearity is tested with a one tone test, either for IIP2 than IIP3 performance (Figure 3.23). For this, the results has to be compared with the specification derived in chapter 1 (Selectivity pattern Table 1.6). In Figure 3.23 are reported

the measurements of the test chip with the feedback enabled and disabled for the IIP2 and with feedback enabled for the IIP3.
It's possible to notice that with feedback there's a constant improvement of IIP2 than in the case of the simple noise cancelling topology. This improvement is round 10dB. The absolute value of IIP2 is never lower than 28dBm and for half of the band satisfies the most stringent specification of 33dBm.

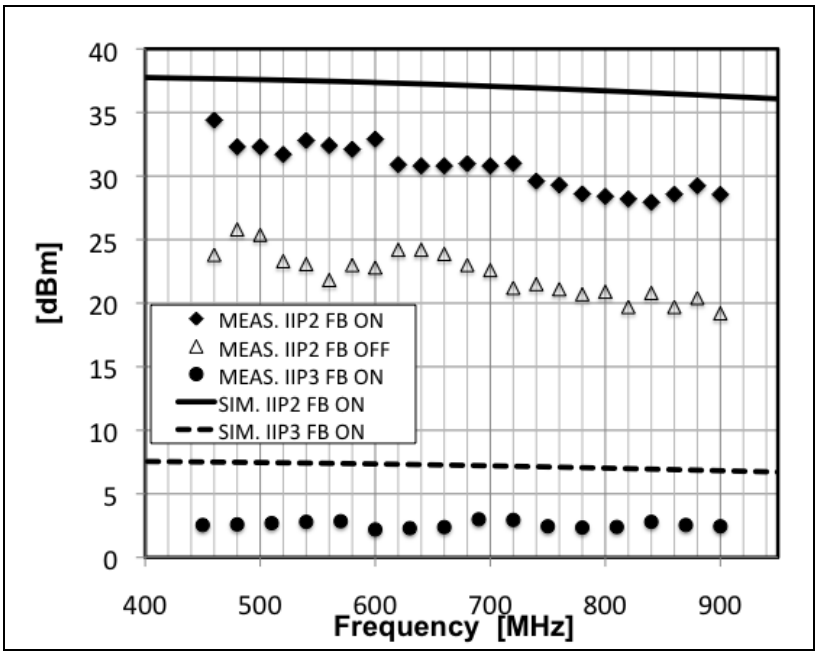

Figure 3.23: IIP2 and IIP3 measurements for a single tone test.

At higher frequency probably the lower values are due to the bandwidth limitation, as explained in Figure 3.17. The IIP3 is always higher than 2.5dBm and so the specification for a single tone test is always satisfied.

IIP3 two tones measurements

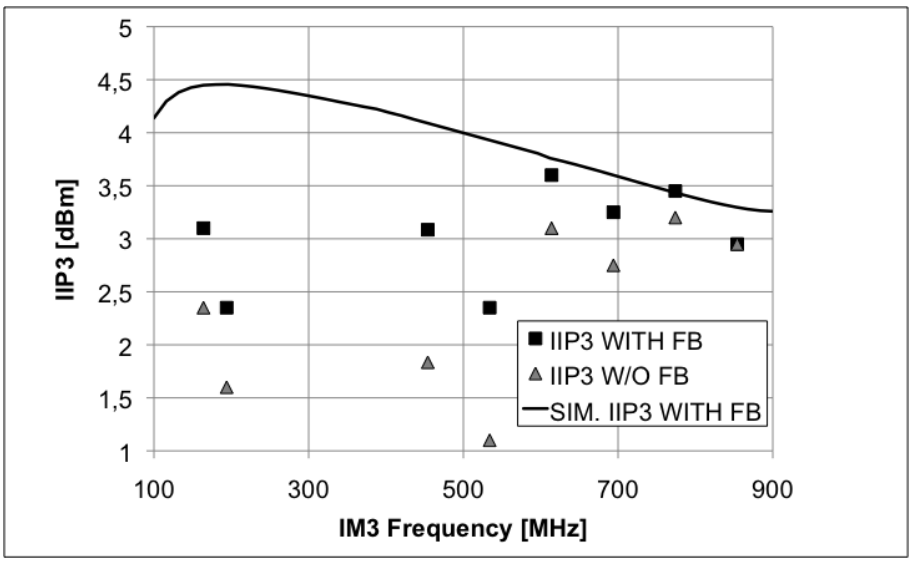

Figure 3.24:IIP3 measurements for two tones test.

The measurements of the IIP3 two tones test are plotted in Figure 3.24. In this case measurements with two tones located at N+2 and N+4 the signal are done. The frequency on the horizontal axis is the frequency of the third order intermodulation. This measurement is described in chapter 1 and the specification of the IIP3 is reported in Table 1.6. For the reasons described in the theory exposed before, an improvement of IIP3 is obtained with the feedback. The improvement is no more than 1dB and it decreases with frequency. In any case the specification in the worst case of -3dBm is always satisfied. In Table 3.1 the comparison with the state of the art is shown.

	TOPOLOGY	IIP2 [dBm]	IIP3 [dBm]	NF[dB]	Power [mW]
Abidi et al. CICC '05 [3.2]	S.E.	4	1	3	11.8
Nauta et al. JSSC '04 [3.1]	S.E.	12	0	2-2.4	35
Nauta et al. JSSC '08 [3.7]	S.E.	>20	0	<3.5	14
Vavelidis et al. ESCIRC '07 [3.8]	DIFF. OUTPUT	>36	-3	3	93(*)
THIS WORK [3.6]	S.E.	28-35	2.5-3	2.8-4.5	7.8
THIS WORK (LNA CORE) [3.6]	S.E.	28-35	2.5-3	2-3.5	7.8

Table 3.1

The performance in term of noise, linearity of second and third order are better than the state of the art with a lower power consumption. The values of second order non linearity are close to the performance obtained with a fully differential solution [3.8].

3.4 Conclusions

The possibility to implement a balun LNA is challenging and interesting in terms of costs and chip area. Nevertheless, as reported in literature [3.1-3.2], the problem of the too low IIP2 is the main disadvantage. In this chapter some possible solutions to the increasing of the IIP2 performance in a single-to-differential amplifier are described. Specifically the IM2 common mode feedback cancellation is considered. An analysis of this solution with Taylor series expansions is reported and general expressions for IM2 and IM3 are deduced and commented. A particular analysis is than realized using the CG-CS topology instead of two ideal amplifiers to appreciate the influence of the feedback on a commonly used solution. At this level the calculations are executed with an ideal implementation of the

feedback. More specific expressions of IM2, IM3 and the noise factor are derived. Considerations on the noise factor terms of the noise cancelling proposed in chapter 2 and of the noise cancelling with feedback presented here are exposed. As a result, a balun LNA with IM2 cancellation can be realized, but the effect on noise of the feedback has to be well evaluated. In a circuital solution published in literature [3.3] indeed, the IIP2 improvement is obtained but with a worsening of the noise performance. Consequently it seems that to have an IM2 cancellation a worse noise performance than the simple noise cancelling is needed. However a new kind of IM2 cancellation feedback is proposed in this chapter. This solution has the same behaviour and the same formulas for IM2 and IM3 derived before, but a different noise factor. Again at the start, for the formulas an ideal feedback is considered. The new improvement than in the previous case is the introduction of a divider in the feedback path that can reduce of a factor M the noise contribution directly introduced by the feedback. Moreover, a design flow to realize the minimum noise IM2 cancellation is introduced. Therefore, for the first time a theory to design a wideband balun LNA with IM2 cancellation, IM3 improvement and simultaneous minimum noise is done. A test chip to validate this theory has been realized. A specific analysis of the impact of a real feedback on a noise cancelling LNA design is proposed and supported by simulations. Finally a description of the measurements with this test chip is illustrated. The performances obtained are close to the specification for VHF III and UHF IV-V derived in chapter 1 and close to the fully differential solution published in literature.

References

[3.1] F. Bruccoleri, E. M. Klumperink, and B. Nauta, "*Wide-band CMOS low-noise amplifier exploiting thermal noise canceling*" IEEE J. Solid-State Circuits, vol. 39, no. 2, pp. 275–282, Feb. 2004.

[3.2] S. Chehrazi, A. Mirzaei, R. Bagheri and A. A. Abidi, "*A 6.5 GHz Wideband CMOS Low Noise Amplifier for Multi-Band Use*" Proc. CICC 2005, pp 801-804, Sept. 2005

[3.3] D. Manstretta, "*A broadband Low-Noise Single-Ended Input Differential Output Amplifier with IM2 Cancelling*", Proceedings of IEEE Radio-Frequency Integrated Circuits Conference, June 15-17, 2008, pp 79-82.

[3.4] R. Bagheri et al., "An 800-MHz–6-GHz Software-Defined Wireless Receiver in 90-nm CMOS," IEEE JSSC, vol. 41, No.12, pp 2860-2876, Dec. 2006

[3.5] "*Noise Figure Measurement Accuracy-The Y Factor Method*" Application Note 57-2.

[3.6] D. Mastantuono and D. Manstretta "*A low noise active balun with IM2 cancellation for multi-band portable DVB-H receivers*" Proceedings of IEEE International Solid State Circuits Conference, 2008.

[3.7] Stephan C. Blaakmeer, Eric A.M. Klumperink , Domine M. W. Leenaerts and Bram Nauta "*Wideband Balun-LNA With Simultaneous Output Balancing, Noise-Cancelling and Distortion-Cancelling*", Proc. IEEE vol. 43, no. 6, pp. 183-193, June. 2008.

[3.8] K. Vavelidis, I. Vassiliou, N. Haralabidis, A. Kyranas, Y. Kokolokis, S. Bouras, G. Kamoulakos, C. Kapnistis, S. Kavadias, N. Kanakaris, E. Metaxakis, C. Kakozidis, H. Peyravi, *A 65nm CMOS Multi-Standard, Multi-Band TV Tuner*, Proc. IEEE, 2007.

4

Single Ended Input Direct Conversion DVB-H Tuner

Building high performance RF receivers is a critical step towards the implementation of single chip radio. The target of low cost and high performances requires more challenging design solutions. In the market of mobile TV, in particular, a high degree of programmability in multistandard operation is required. A commonly used solution to the problem of multiband multimode operations is the implementation of several individually tuned and optimized RF front end, when possible sharing the IF circuit blocks [4.1]. A single path wideband solution, instead, requires a low noise and linear wideband LNA. In this chapter the new balun LNA with IM2 feedback cancellation of chapter 3 is used. The choice of the down-conversion stage and of the base band circuit to guarantee low noise and high interference immunity is described. A test chip of the entire front end has been realized and the measurements are reported.

4.1 Multimode Multiband tuner design.

First of all for the design of a broadband front end, receiver architecture has to be chosen. Typical techniques include using external band pass filters that track the signal carrier, or the up-down conversion super-heterodyne architecture. Another approach can be the direct downconversion. As proposed in literature [4.1-4.2] a direct conversion TV tuner for DVB-H is a viable, low cost low power alternative. The advantages of this architecture are: the reduction of complexity, the requirement of fewer external components and the elimination of need for image suppression filtering. The main problems instead are: DC offset, flicker noise and I/Q channel amplitude and phase imbalance.

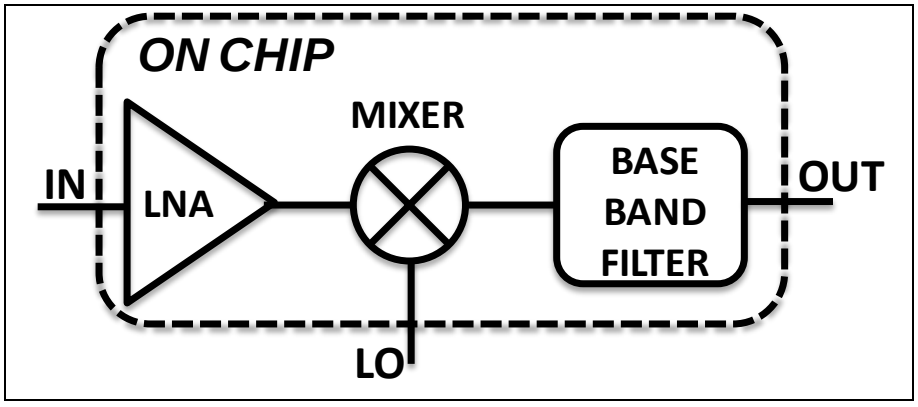

Figure 4.1:Block diagram of the RF front end.

Three main blocks compose the front end: the LNA the downconverter stage and the base band filter (Figure 4.1). To cover the whole band of interest two approaches can be followed. The first adopts a multipath front end and the second one is to use a single path one. The first solution can be realized with different narrow band LNAs, as described in chapter 2, and sharing the base band blocks. The second solution can be achieved with a narrow band reconfigurable LNA [4.3] or with a wideband LNA. In this chapter the solution of a wideband amplifier is chosen. In particular the implementation of the wideband balun LNA with low noise IM2 cancellation is preferred. The mixer and the base band circuits are described in detail in the next paragraphs.

Low NF and High linearity scenarios

The main performances required by a TV standard are low NF, high linearity and high SNR to allow robust operation in the mobile environment is necessary. Nevertheless, to reduce the power consumption, it's necessary to realize the performance only in the scenario in which they need. For example, a high linearity is needed

when there are strong interferers that can generate distortion that falls in the channel of interest. On the other hand, the minimum noise figure is necessary only when the signal received level is minimum. So, in order to minimize power consumption different configurations can be used depending on the actual scenario. To get this goal, the receiver has to be designed to be reconfigured in terms of performance. So not only a multiband, but also a multimode solution has been implemented and it is described in this chapter.

Performance reconfigurability

4.1.1 Single ended and fully differential non-linearity

Before describing the peculiarity of a wideband receiver, a brief introduction to distortion in a single ended, in a single to differential and in fully differential stages (e.g. an LNA) is done.
As well known, at the output of a single ended amplifier with two input interferers all even and odd intermodulation products and harmonics are generated (Figure 4.2).

Distortion in single ended stage

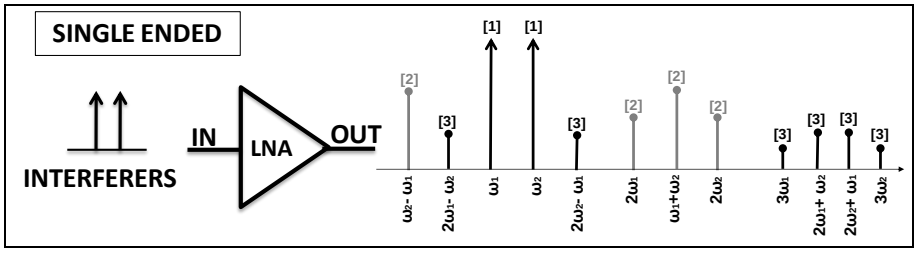

Figure 4.2: Generation of distortion in a single ended topology.

In the single to differential stage the distortion is comparable to the single ended case (Figure 4.3).

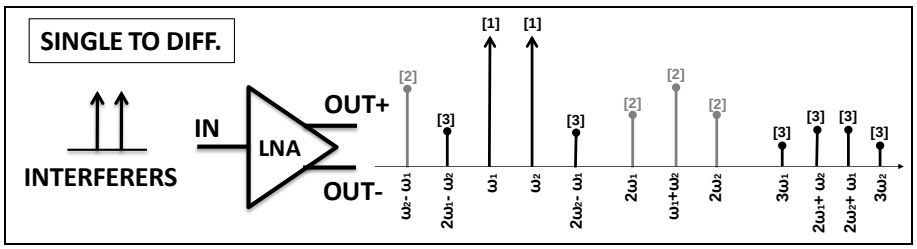

Figure 4.3: Generation of distortion in a single to differential topology.

Indeed, as described in the previous chapter in Figure 3.1, the single to differential stage is like two single ended stages with the same input. Moreover, the two paths are not equal (one is inverting and one is non-inverting) to have a differential output. So at the output there's a difference of two systematically different outputs and so the level of distortion is comparable to the single ended stage. In particular, the

Distortion in single to differential stage

amplitude of the IM2 is reduced with the cancellation feedback described in chapter 3. In other words, with the single to differential conversion realized with the LNA is the second order distortion shown in Figure 4.3 that has to be reduced with a common mode feedback.
In a fully differential stage instead, the two paths are equal and the inversion is due to the inverted input signals (Figure 4.4).

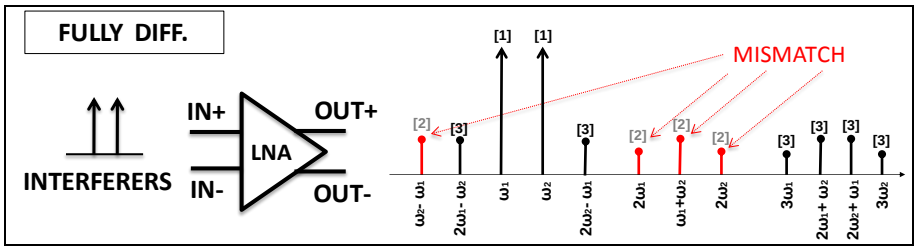

Figure 4.4: Generation of distortion in a fully differential topology.

Even and odd distortion in fully differential stage

So, the even order distortion of a fully differential amplifier is null without mismatches, looking just the differential output. The common mode even order distortion, instead, is not zero and it's the mismatch that transforms the common mode distortion to a fully differential distortion. The even order distortion is in phase and with the same amplitude at the two outputs of a differential stage and so, without statistic differences due to the process, it's cancelled sensing the differential output. This is not the case for odd distortions, which are in anti-phase. In this case the common mode distortions at the two outputs are not cancelled at the differential output, even if there aren't mismatches. In the odd distortion case to reduce the differential distortion, it is necessary to reduce the common mode distortion. In other words, if the common mode even order distortion is not null, without statistic differences, the differential even order distortion is null. On the other hand, to cancel the odd differential output distortion has to be null also the common mode one.

4.1.2 Non-linearity in a wideband receiver

Distortion in a narrowband stage

In a narrow band LNA the intermodulation distortion is due to two interferers close to each other (for example interferers in adjacent channels). In a wideband LNA the distortion can be generated for two tones intermodulation (not necessary close to each others) or for the harmonic distortion of a single tone. Indeed, the band covers several decades of frequency and so also the harmonic distortion is significant for the LNA. The specifications for these two different distortions are

considered respectively in the linearity pattern and in the selectivity pattern in chapter 1.

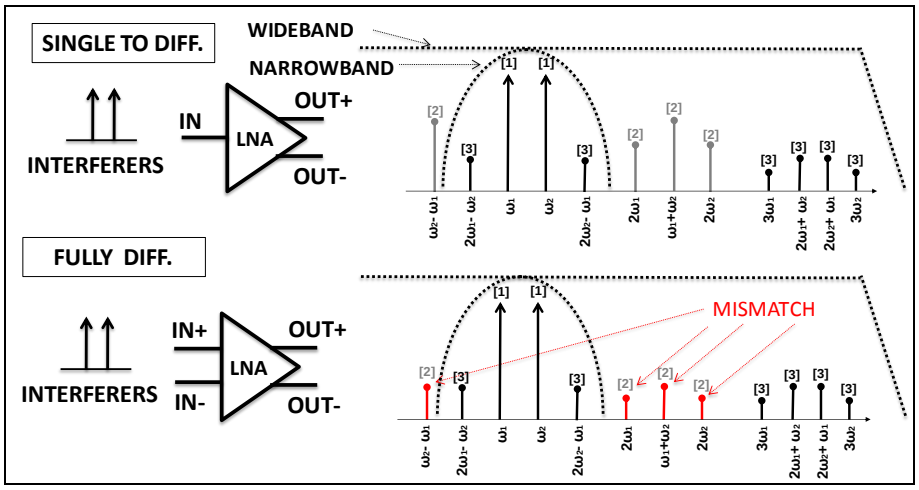

Figure 4.5: Comparison of generation of distortion between wideband and narrow band LNA in single to differential and fully differential topology.

Specifically, the distortion considered in a narrowband LNA is the third order non-linearity of two tones close to each other (Figure 4.3). On the other hand, the IM2 generated is out of band for the LNA and it is filtered. For a wideband LNA instead all the harmonics (gray ones) and intermodulation products (black ones with circular top) can fall in band. In conclusion, these concepts can be summarized:

Distortion in a wideband stage

- If the LNA is narrowband the IM2 generated by two far away tones is filtered. Also the harmonic intermodulation products of second and third order are filtered.
- If the LNA is wideband the IM2 can fall in band without filtering. Also the harmonic intermodulation products of second and third order are critical for a wideband LNA.
- The IM3 due to two interferers close to each other is a problem for both wideband and narrowband LNAs.

So the generation of distortion is caused by the choice of the circuital solution (fully differential or single to differential) that are sensitive to different channel conditions (third order distortion due to close tones, second order distortion caused by far away tones and harmonic distortion). Moreover, the generation of second order distortion is in every case a difference between the single ended distortions: in one case caused by the mismatch and in the other by the different single ended paths. As a result, the problem isn't the generation of distortion

Distortion due to channel condition and circuital solutions

Distortion in a wideband front end

by itself, but transformation of the common mode distortion to a differential component.

This is the same for the mixer stage. The generation of even order distortion of the downconverter stage is due to the mismatch, because the mixer is fully differential. Anyway, the even order distortion of the wideband LNA can appear at the differential output even if the mixer is ideal.

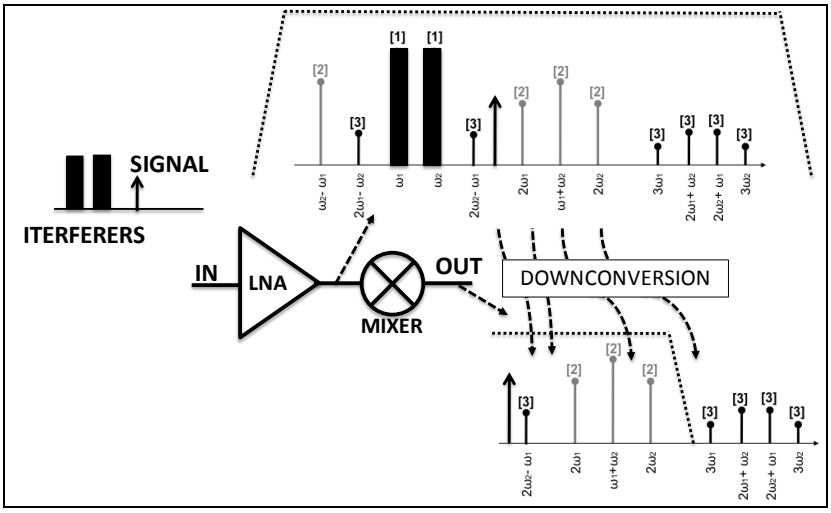

Figure 4.6:Simple description of the generation of distortion in a chain wideband LNA+mixer.

That's because the distortion generated by the LNA at the differential input appears downcoverted by the local oscillator (LO). So, if the even order distortion falls in band of the signal at the output of the LNA, it will be at the output close to the signal also after an ideal downconversion.

In the case of a narrowband front end, instead, the even order distortion generated by harmonics or by two far away tones are filtered and so the main contribution is the one introduced by the mixer itself. About odd order intermodulation, the concept is the same described for the even case, but there isn't a dependence on the process variations like in the even case and it isn't filtered. Indeed, if the IM3 of the LNA is in the desired channel, it can appear at the output just translated at a lower frequency, even if the mixer is without mismatches.

4.2 Wideband LNA

Active balun LNA with low noise IM2 cancellation

The LNA used for the design of the down conversion architecture, as said, is the wideband balun LNA with low noise IM2 cancellation shown in chapter 3. The schematic of this LNA and of the feedback are reported in (Figure 4.7).

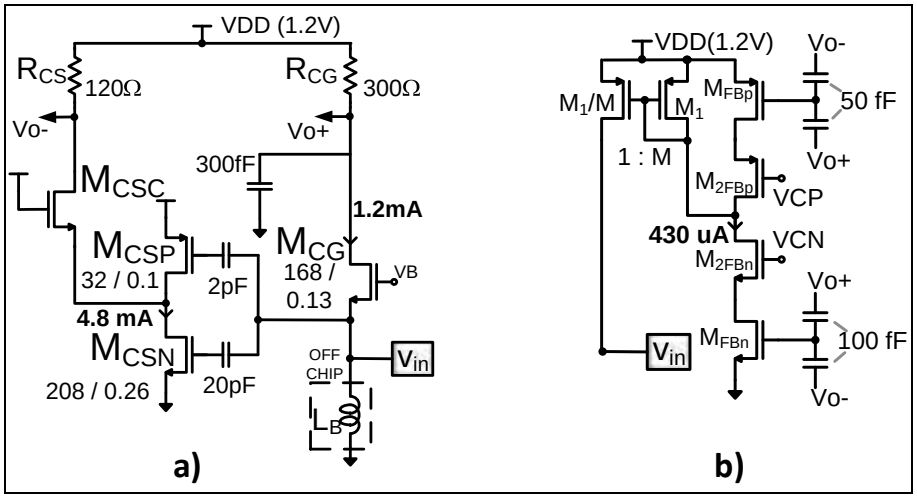

Figure 4.7:Wideband balun LNA (a) with low noise IM2 cancellation feedback (b).

The performance and the considerations are the same exposed in chapter 3.

4.3 Downconverter stage

The downconverter stage is realized with a passive mixer. In this way low flicker noise and high linearity can be obtained [4.4-4.5]. The passive mixer is driven in current by a transconductance stage. The base band filter provides the low output impedance that loads the mixer. So in this paragraph the mixer is considered with this low impedance at the output, but the description of the base band filter is done in the next paragraph. Fundamental parameters for the design of a mixer are the conversion gain, the linearity (second and third order linearity) and the noise.

Downconverter specifications

The specifications of the front-end in terms of noise and IIP3 for the downconverter are calculated. The NF considered in the standard in chapter 1 for the entire front end (NF_{TOT}) is less than 5 dB. Considering an LNA noise figure of 2dB (NF_{LNA}), it's possible to evaluate the NF required of the downconverter stage (NF_{DW}) [4.4]:

Noise figure

$$NF_{DW} = 10\log_{10}[1 + (F_{TOT} - F_{LNA})A_{v,LNA}^2] = 22\,dB \qquad (4.1)$$

with $A_{v,LNA}$=10. The input referred noise in 5.65 nV/sqrt(Hz). The IIP3 specification of the front end is derived from the selectivity and

the linearity pattern of chapter 1. The one tone test IIP3 is 2.5 dBm, while the two tones test is -3 dBm. The IIP3 specification for the LNA ($IIP3_{LNA}$) and for the downconverter stage ($IIP3_{DW}$) can be extrapolated from the specifications of the front-end ($IIP3_{TOT}$) with the following expressions [4.4]:

IIP3

$$\frac{1}{IIV3^2_{TOT}} = \frac{1}{IIV3^2_{LNA}} + \frac{A^2_{v,LNA}}{IIV3^2_{DW}} \tag{4.2}$$

$$IIP3_{TOT} = 10\log_{10}(IIV3^2_{TOT}) + 10\log_{10}(\frac{1}{2Rs*10^{-3}}) \tag{4.3}$$

with $A_{v,LNA}$ the voltage gain of the LNA stage and R_S the source impedance (50Ω in this case). Two specifications of IIP3 are given by the standard, so two values are derived. Considering the simulated performances of the LNA (one tone test IIP3=10dBm, two tones test IIP3=5dBm) the downconverter stage one tone test IIP3=23dBm ad the two tones test IIP3=18dBm. In Table 4.1 the specifications of noise and IIP3 for the downconverter are summarized.

	NF[dB]	IIP3[dBm]
Linearity Pattern L2	22	18
Selectivity Pattern S1	22	23

Table 4.1:Specifications for the downconverter stage.

4.3.1 Transconductance stage.

The first block of the downconverter stage is a transconductor. In this paragraph is described the design of this stage. The topology used, shown in Figure 4.8, is a PN pseudo differential stage. As well known in literature [4.4-4.5], this stage has good performance in terms of noise and third order linearity. The stacking of the PMOS and NMOS allows to reduce the current consumption for a given noise and linearity. In particular it is:

Gain

$$G_m = g_{mP} + g_{mN} \tag{4.4}$$

From the Equation 4.4 the noise factor of the transconductor (F_{TR}) is:

Noise factor

$$F_{TR} = 1 + \frac{\gamma}{(g_{mN} + g_{mP})R_S} \tag{4.5}$$

At the same time also the performance of IIP3 is high because the topology is pseudo differential [4.4-4.5].

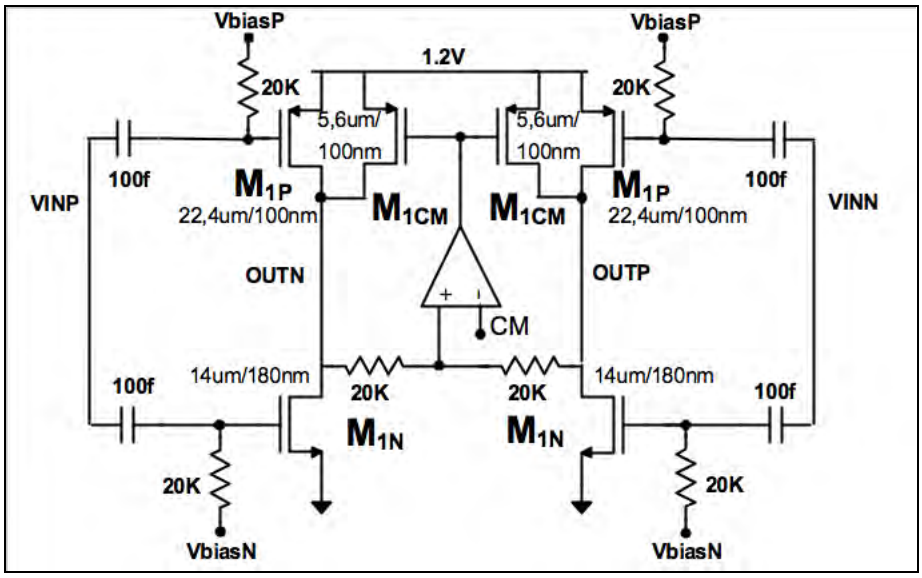

Figure 4.8:Transconductance stage.

In a simple way, the differential stage has a low overdrive voltage than a pseudo differential one and so the IIP3, that is proportional to the overdrive, is higher.

Transconductance design flow

Therefore, a design flow can be followed for the design of a PN transconductor:

- Fixed the ratio between g_{mP} and g_{mN}, the overdrive voltage is fixed and so the third order linearity [4.6]. An optimum in IIP3 can be found for a certain ratio.
- Fixed the dimensions of the MOS and the I_{bias}, the G_m is fixed and so the noise. Increasing the I_{bias} , the noise is reduced but the linearity is the same, for a given ratio between MOS P and MOS N.

In Figure 4.9 the noise in the band 100MHz-1GHz is shown for two values of transconductance 10mS (High G_m) and 5mS (Low G_m). The IIP3 in both these cases is constant in band and equal to 20 dBm. In the schematic of the transconductance stage the common mode feedback is shown: it senses the common mode at the outputs and with an opamp it drives two P MOS. The P MOS are driven to have the same DC voltage at the outputs imposed by an external common mode reference. The supply voltage is 1.2V and the dc current of the entire stage is 7mA in the case of low G_m and 11mA in the case of high G_m.

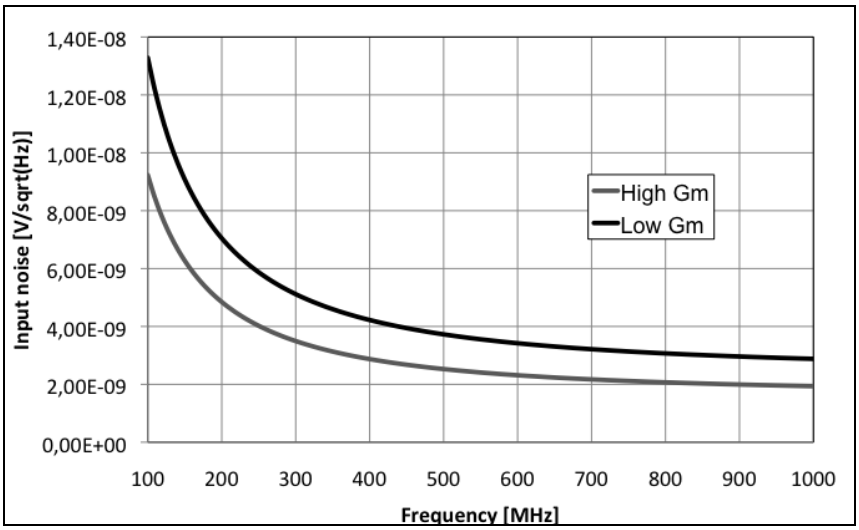

Figure 4.9:Simulated noise of transconductance stage.

Simulated performances

The dimensions of the MOS used in the design are shown in Figure 4.8. The main performances of the transconductance stage in Figure 4.8 are summarized in Table 4.2.

	Noise[nV/√Hz]	IIP3[dBm]	Power [mW]
Gm Stage	2	20	13,2

Table 4.2

4.3.2 Switching stage

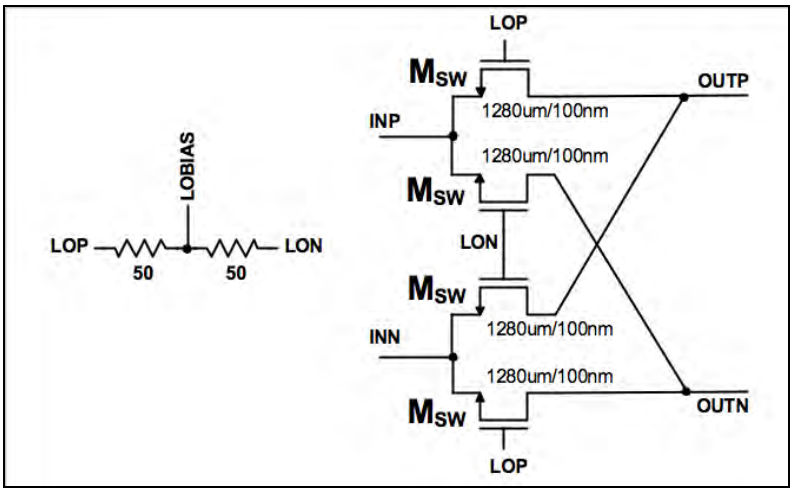

Figure 4.10:Switching stage.

The switching stage schematic is shown in Figure 4.10. It's the double balance version and the inputs are the outputs of the transconductance stage. The outputs are loaded by the base band stage described in the next paragraph. The conversion gain (G_C) of the donwconverter stage (transconductance and switching pair) is [4.4-4.5]:

Conversion gain

$$G_C = G_m e_C R_{LOAD} \tag{4.6}$$

where R_{LOAD} is the load resistance of the next stage and e_C is the efficiency of conversion [4.4-4.5]:

$$e_C = \frac{2}{\pi} \frac{R_{OUT}}{(R_{LOAD} + R_{SW}) + R_{OUT}} \cos \pi \frac{\Delta t}{T} \tag{4.7}$$

R_{OUT} is the output impedance of the downconverter stage, R_{SW} is the on impedance of the switch; Δt is the time of overlap of the waves that drive the switches (LOP and LON in Figure 4.10) and T is the period of the local oscillator. For a square wave (or for a large sinewave) and for an $R_{OUT}>>(R_{LOAD}+R_{SW})$ the conversion gain is $2/\pi$. The dependence on the R_{LOAD} and R_{SW} of the conversion gain is shown in Figure 4.11.
The expression of the R_{SW} is:

$$\frac{V_{DS}}{I_{DS}} = R_{SW} = \frac{1}{\beta(V_{GS} - V_{th} - \frac{V_{DS}}{2})} \tag{4.8}$$

with V_{DS} and I_{DS} the voltage and current from the drain and source of two of a single switch, V_{GS} the gate source voltage, V_{th} the threshold voltage, and $\beta=(W/L)\mu_n C_{OX}$. μ_n and C_{OX} are fixed parameters for the technology.

IIP3 and e_C vs R_{SW}

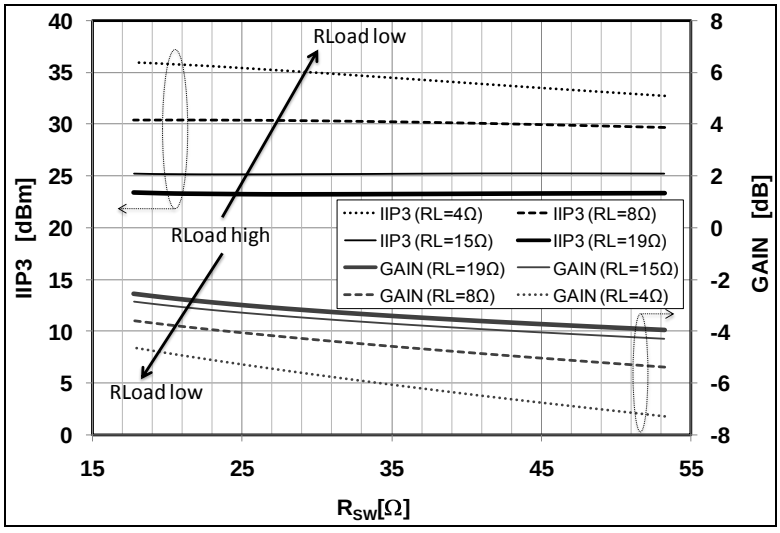

Figure 4.11:IIP3 vs R_{SW} and Gain vs R_{SW} for different values of R_{LOAD}.

If the previous and the next stage of the switching pairs are considered perfectly linear, the distortion is generated by the non linearity of the switch, proportional to V_{ds} channel modulation. Concerning the linearity, three parameters have to be considered: R_{LOAD}, R_{SW} and the bias voltage of the switch [4.4-4.5]. To have a high IIP3 (Figure 4.11) R_{SW} has to be low to reduce the V_{ds} channel modulation so, from the expression 4.8, the switches has to be large and the bias voltage has to

be high. At the same time also R_{LOAD} has to be as low as possible to improve IIP3 (Figure 4.11).
The disadvantage of using large devices is the high power to drive the switch, and the increasing of the noise of the switch (Figure 4.12)

Noise vs R_{SW}

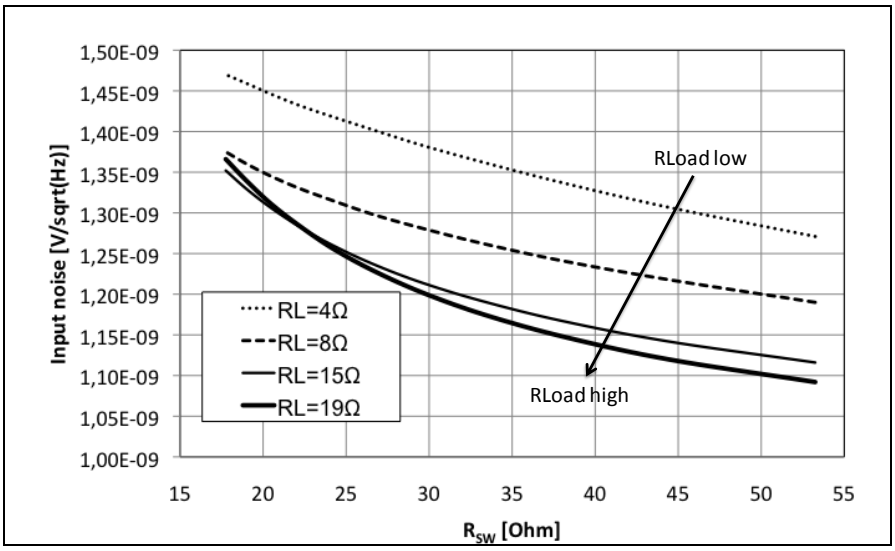

Figure 4.12:Noise vs R_{SW} for different values of R_{LOAD}.

The equivalent current noise generator of a switch on is in fact:

$$\frac{di_n^2}{df} = \frac{4kT\gamma}{R_{SW}} \tag{4.9}$$

In other terms, increasing R_{LOAD} and R_{SW} the noise is lowered (Figure 4.12) because the G_C is higher and the equivalent noise of the switch is lower. This is true as far as the reduction of the e_C is lower than the enhancement of the G_C or again as far as $R_{OUT}>>R_{LOAD}+R_{SW}$. The IIP3 and noise plotted in Figure 4.11 and Figure 4.12 are referred at the input of the downconverter stage.
To enhance the gain and improve the linearity the LO chosen is a square wave and the DC value of the switches (LO_{bias} in Figure 4.10) is 1.1V. The LO amplitude is 2V pk-pk. In this way the mixer works in on-overlap region [4.4-4.5]. At the gate of the switches two resistances of 50Ω are used, to improve impedance matching between the signal generator and the IC. In this way the amplitude of the square wave at the input of the switching pairs is well defined independent of interconnect length. The dimensions of the switches are shown in Figure 4.10. The main performances of the switching stage in Figure 4.10 are summarized in Table 4.3.

Simulated performances

	Noise[nV/√Hz]	IIP3[dBm]	Lo Power [mW]
Switching pairs	1.175	30	10dBm

Table 4.3

4.3.3 Base band stage

Opamp virtual ground

The classical way implementation of a low impedance as load of a passive current driven mixer is an opamp with negative feedback (or virtual ground, Figure 4.13). The low impedance is strongly dependent on the characteristics of the opamp in this solution.

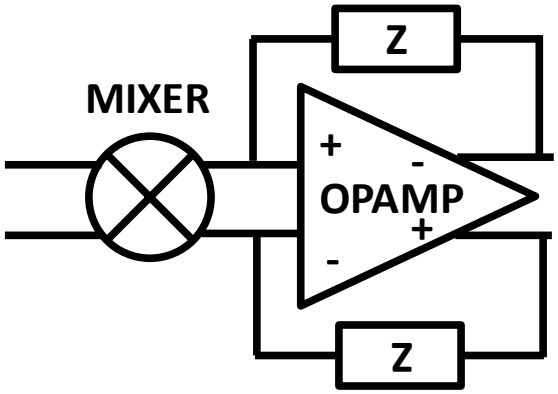

Figure 4.13:Virtual ground with opamp.

Supercascode virtual ground

So, it is possible to realize very low values of impedance, but only in the range of frequency of the opamp. At high enough frequencies the amplifier gain drops and the impedance starts to increase with frequency degrading mixer performance. A possible alternative implementation is a super cascode (Figure 4.14).

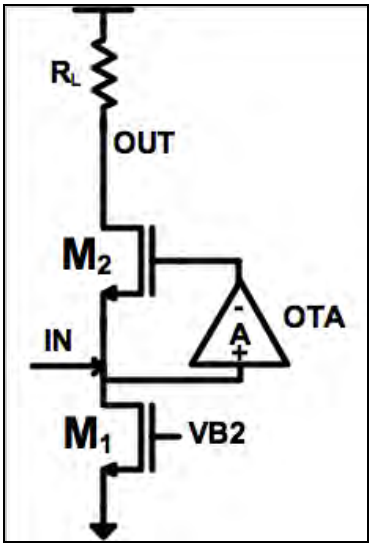

Figure 4.14:Super-cascode.

The key point is to use an opamp in a cascode structure. In this way the higher impedance out of the band of the opamp is lower ($1/g_{m2}$) than the open loop input impedance of the amplifier. Also, the operational amplifier can be a simpler OTA. The output impedance is the gate impedance of the MOS, hence the output stage is not necessary. The OTA bandwidth is still a major limitation.

CG stage vs FB stage

To overcome these limitations and realize an active base band without using an opamp, two solutions are considered. In Figure 4.15 these two solutions are shown: one is a cascode with negative feedback (Figure 4.15a) and the second is a simple common gate stage (Figure 4.15b). The input impedances of the two topologies are:

CG and FB Z_{IN}

$$Z_{IN,CG} = \frac{1}{g_{m2}} \tag{4.10}$$

$$Z_{IN,NEG} = \frac{1}{g_{m2}(g_{m1}R_L + 1)} \tag{4.11}$$

The effect is the same described using the operational amplifier, but with this topology the stage for the amplification is the MOS M_1.

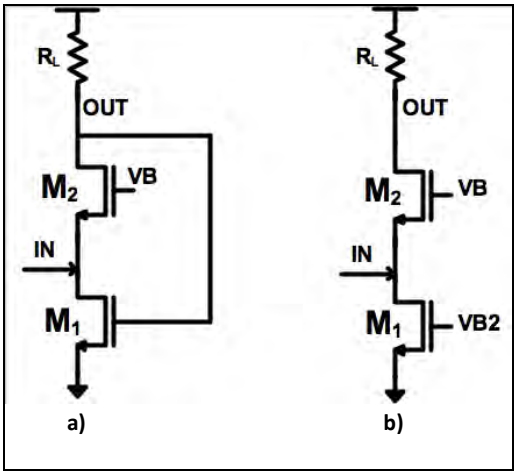

Figure 4.15:Virtual ground with (a) negative Feedback (FB) and (b) simple CG stage (CG).

In both cases the highest impedance is $1/g_{m2}$, so there is the same advantage of the super cascode topology. The simple expression of the voltage gain of the two stages is:

Gain

$$G_{FB} = G_{CG} = g_{m2}R_L \tag{4.12}$$

$Z_{IN,FB}=Z_{IN,CG}$ ($I_{BIAS,FB}\neq I_{BIAS,CG}$)

The two stages are analyzed in two conditions: for the same bias current (so for different input impedances) and after that for the same input impedance (so for different bias current). The linearity and the noise of these two topologies in these two conditions are compared.
Starting from the condition of equal impedance, different R_L are utilized to exploit the same gain. Linearity simulations results are presented in Figure 4.16. The IIP3 referred to the input of the downconverter stage versus the IM3 frequency is plotted. The linearity of the CG is higher than the case with feedback. Anyhow, to obtain the same input impedance more current (round two times) is necessary in the common gate stage than in the feedback case.

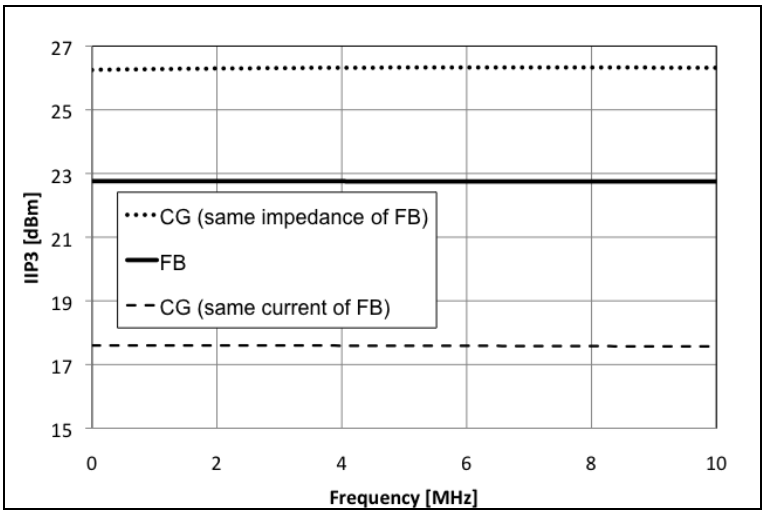

Figure 4.16:Comparison of IIP3 for (a) negative feedback(FB) and (b) simple CG stage.

Concerning the noise, the noise factors of the two solutions (F_{CG} and F_{FB}) have the same expression:

$$F_{CG} = F_{FB} = \mathbf{1} + \frac{\gamma}{g_{m2}R_S} + \gamma g_{m1}R_S + \frac{R_S}{R_L}\left(\frac{\mathbf{1} + g_{m2}R_S}{g_{m2}R_S}\right)^2 \qquad (4.13)$$

Noise factor

The second term is the contribution of the common gate stage, the third of the current generator (M_1) and the forth of the load. Even if the expression is the same for the noise of both stages, the values of the parameters of the circuit are not necessary equal. In particular, for the same input impedance, the dominant contribution in the CG stage is the noise of the current generator, instead in the case with feedback is the M_2 one. That's because in the case without feedback to obtain the same input impedance a higher g_{m2} is necessary, but with a higher current and so with a higher g_{m1}. So a reduction of the second term and an increase of the third are done and in general a higher noise in the CG stage is shown in simulations. The disadvantage of the CG in this condition isn't just the higher power consumption, but also the higher noise.

$Z_{IN,FB} \neq Z_{IN,CG}$
($I_{BIAS,FB} = I_{BIAS,CG}$)

Using instead the same current in the CG and FB, with the same dimensions of the MOS, the same gain is maintained for these two topologies. However the linearity of the FB is higher than the CG (Figure 4.16), and the two topologies have the same power consumption. In this case the noise of the two topologies is the same. That's because the same current and the same dimensions of the MOS are used. Hence in this case the noise factor value and not just the expression is the same.

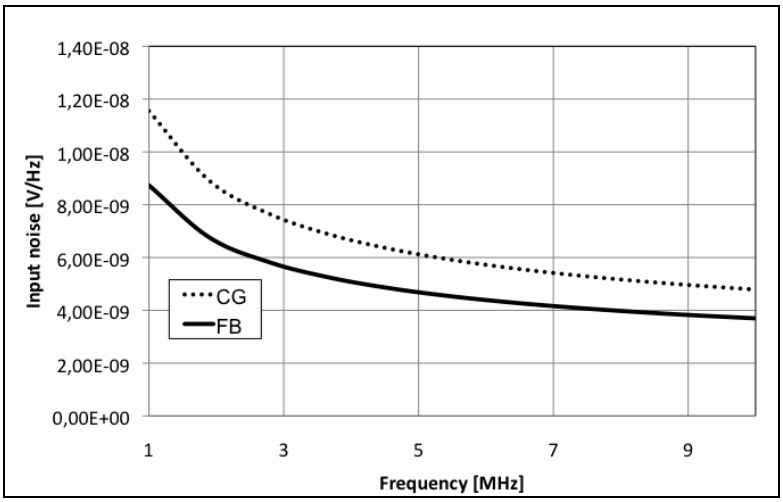

Figure 4.17:Comparison of simulated noise for negative feedback(FB) and simple CG stage referred to the input of the downconverter stage.

It's possible to optimize the noise of M_1 to further lower the noise. Consequently, in the case of different input impedances (so for the same bias current) a lower IIP3, $F_{CG} \leq F_{FB}$ and the same power consumption is achieved.
Hence, from the Figure 4.16 and Figure 4.17 the topology with feedback is noisier, more linear and with a lower Z_{IN} compared with a CG stage for a given power consumption. The CG stage can be more linear with the same power consumption, but noisier for a higher bias current of the feedback case.

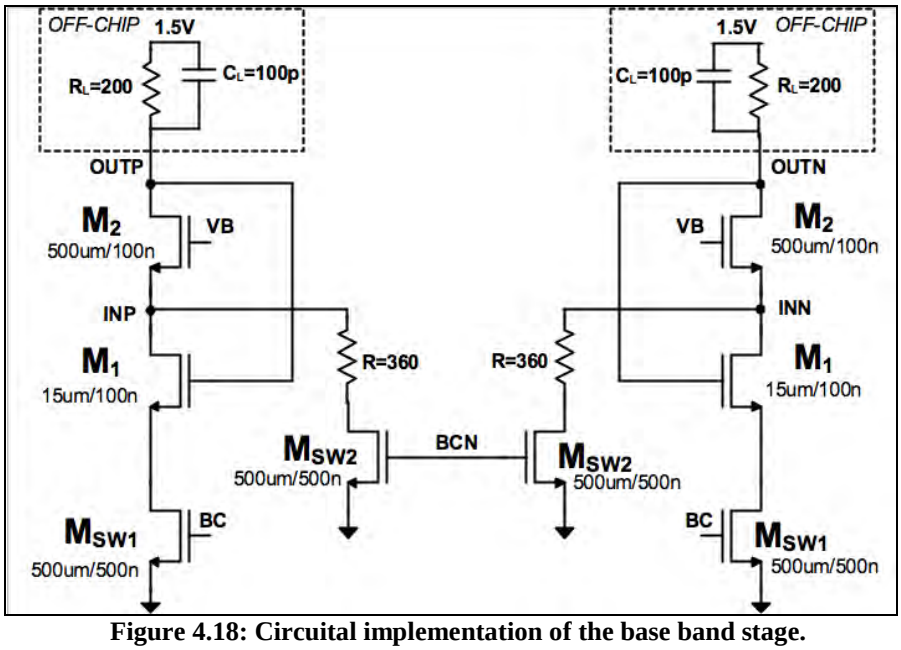

Figure 4.18: Circuital implementation of the base band stage.

Given these considerations, an adaptive approach to exploit the better performances of both configurations is adopted. The base band stage schematic is shown in Figure 4.18. Two configurations are available: a low noise one and a high linearity one.

To reduce the noise of the CG the current generator M_1 with a high overdrive voltage is substituted with a resistor. This second solution is chosen to reduce the flicker noise too.

Low noise configuration: CG

The low noise configuration is active when M_{SW2} is on and M_{SW1} is off. With this solution the virtual ground is a simple common gate degenerated with a resistance R=360Ω. R is chosen to have the same bias current of the high linearity case. The high linearity is achieved when M_{SW1} is on and M_{SW2} is off. In this case, the feedback is closed and the resistive path is open. The two solutions are biased with the same current and so for the analysis done in this paragraph, with different input impedance levels.

High linearity configuration: FB

For the same bias current and with a resistive degeneration the noise of the common gate stage and the linearity are lower (Figure 4.19-Figure 4.20) while the impedance is higher. In the case with feedback, instead the linearity and the noise are higher and the impedance is lower. Also the gain is different in the two configurations, because the load resistance R_L is the same. To improve the linearity and perform a channel selection two capacitances of 100pF are used. The IIP3 referred to the input of the downconverter stage with feedback on, feedback off, with and without C_L and in the optimum case of linearity are plotted in Figure 4.19. The optimum condition is obtained with half of the G_m of the previous transcoductance stage.

Adaptive approach: CG or FB

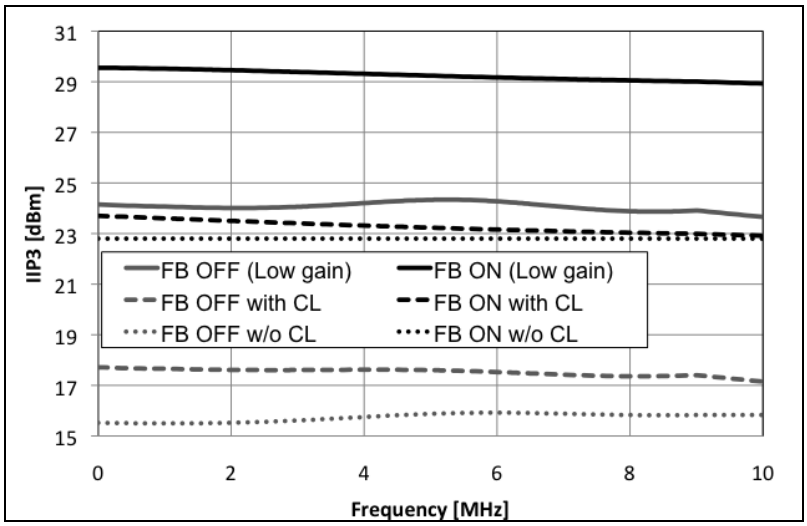

Figure 4.19: IIP3 simulated for feedback on (FB ON) and resistive degeneration (FB OFF), with the effect of C_L and for a lower gain of the previous stage(Low gain).

In Figure 4.20 the noise of the CG and of the feedback stage with the same current are plotted with the noise of the resistive degenerated stage. All the noises are referred at the input of the downconverter stage.

In conclusion, the low noise configuration has a lower noise of the feedback case. No flicker noise due to the current generator is added and at 10Mhz the voltage noise is 1.175 nV/√Hz. In the high linearity condition, considering the low gain for the transconductance case, the

IIP3 is round 29dbm. The bias current of the differential case is 3,2mA on a 1.5V supply voltage.

Noise simulations

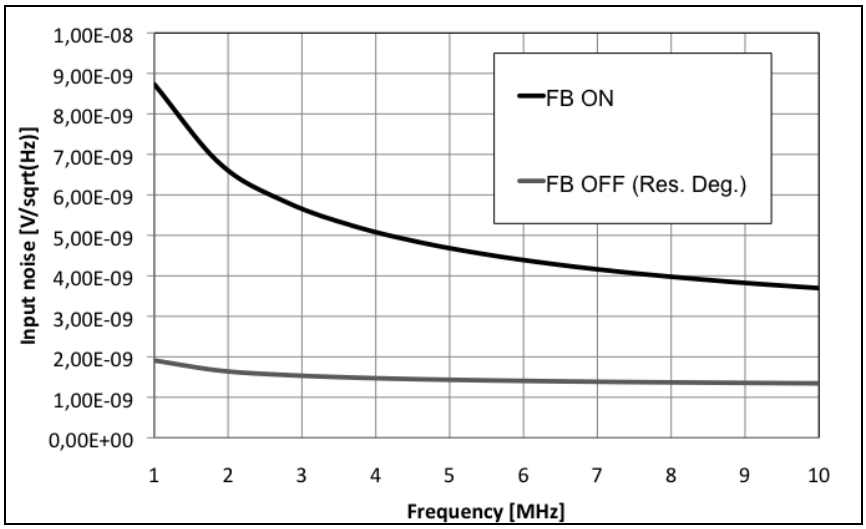

Figure 4.20:Input noise for CG, feedback with the same input impedance(FB ON) and of the resistive degenerated CG with a higher impedance(FB OFF).

Simulated performances

The main performances of the base band stage in Figure 4.18 are summarized in Table 4.4.

	Noise[nV/√Hz]	IIP3[dBm]	Power [mW]
Base Band Stage	1.34	29	4,8

Table 4.4

4.4 Test chip

In this paragraph the entire schematic of the front end and the various configurations adopted are shown. A block diagram of the I/Q version is reported in Figure 4.21.
The mixer can be configured to satisfy the different scenarios in the following way:

High linearity or low noise configuration

- High linearity configuration: only one transconductance stage is active (the G_m is a half) and the feedback stage is active as base band stage.
- Low noise configuration: both the transconductance stages are active (the G_m is the highest) and the CG with resistive degeneration is active as base band stage.

In Table 4.5 the simulated performances of the mixer in the two different cases are summarized and compared with the specification of the standard.

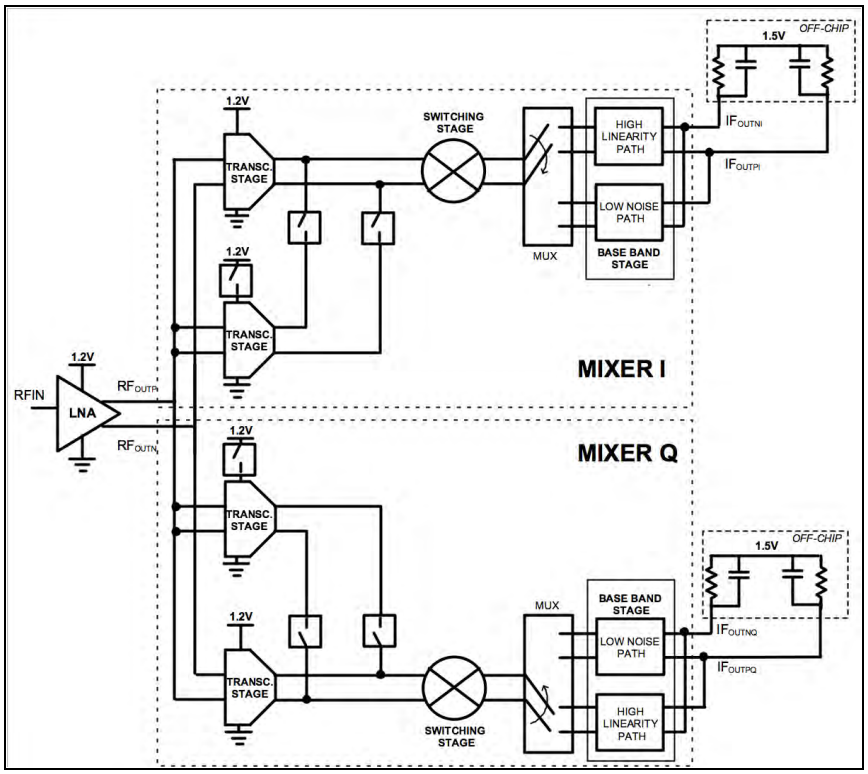

Figure 4.21:Entire schematic of the front end integrated.

SIMULATED MIXER PERFORMANCE	NF[dB] @10MHz	IIP3[dBm] (Linearity test)	IIP3[dBm] (Selectivity test)	GAIN[dB]
Low noise configuration	16	10	19	6
High linearity configuration	22	19	23	-6

Table 4.5

Simulated performances

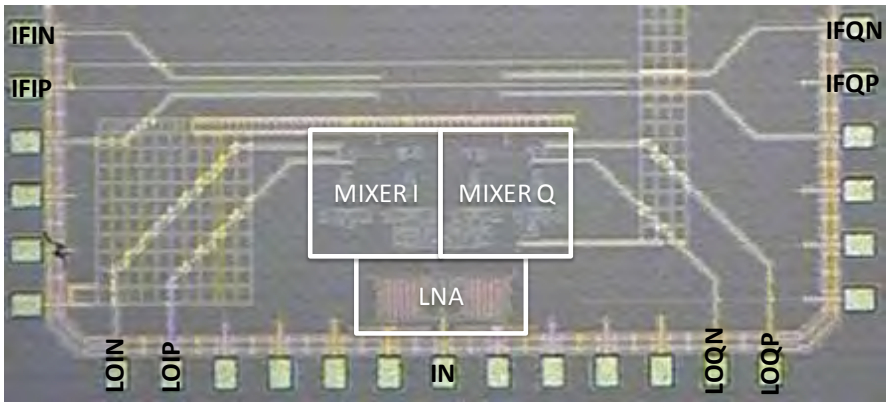

Figure 4.22:Test chip photo.

The area of the only LNA is 0,056 mm^2 and the area of a single mixer is 0,0561 mm^2.The technology used for the IC is the 90nm TSMC 1P6M with 3µm-thick TOP metal. In the next paragraphs the measurements of the entire front end are shown.

4.4.1 Experimental results

Layout parasitic capacitances: 3dB attenuation

Due to a parasitic capacitance at the input of the transconductance stage a lower gain is obtained. So a higher noise of the entire front end is measured. In Figure 4.23 the parasitic capacitance is shown in the transconductance schematic.

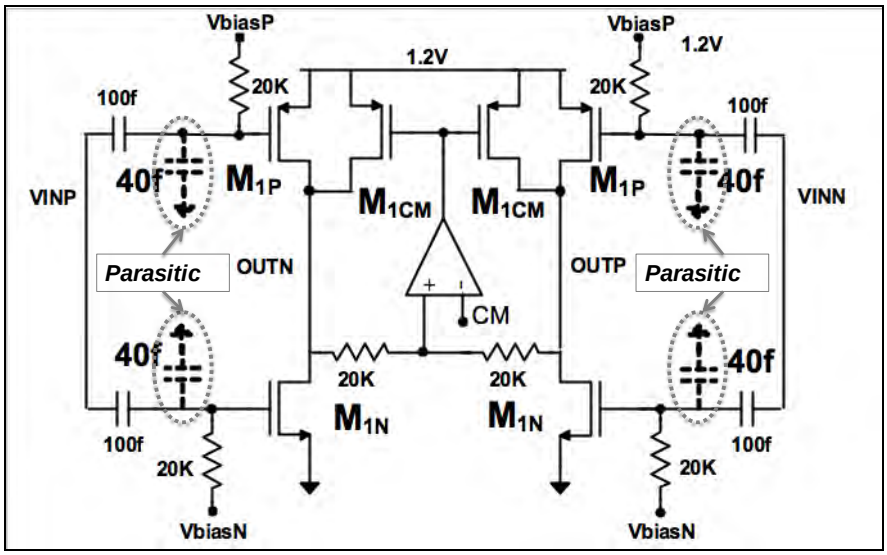

Figure 4.23:Parasitic capacitance at the input of the transconductor.

With a parasitic capacitance of 40fF after the bypass capacitance used between the LNA and the mixer transconductor there is an attenuation of 3dB.

Gain simulations and measurements

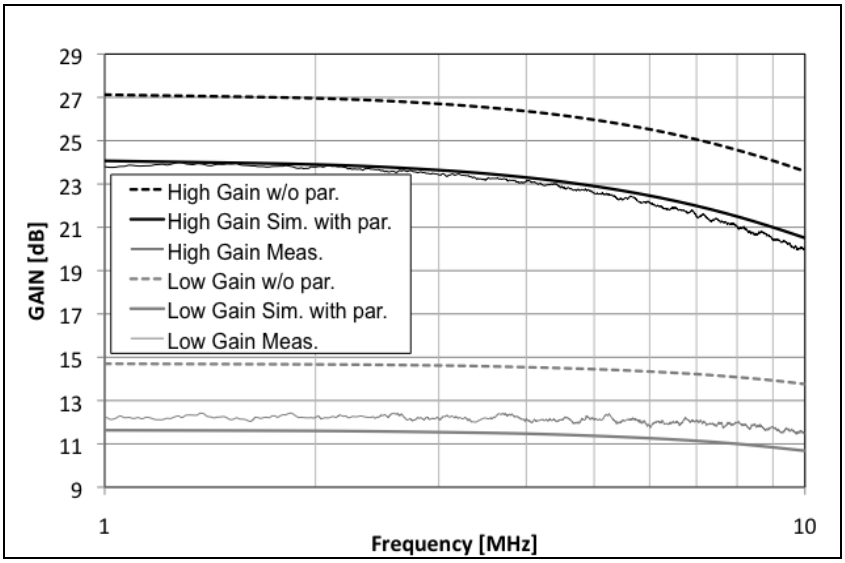

Figure 4.24:Gain of the front end in the low noise and high linearity configurations with and w/o parasitic.

That means a reduction of gain, a worse noise performance and a better linearity. In Figure 4.24 the gain achieved by the whole front end is plotted. The high linearity (black line) and low noise (gray line)

configurations are compared. The dotted lines are the ones without the parasitic capacitance of Figure 4.. A gain lower than 27 dB in the low noise case and of 12 dB in the high linearity case are simulated.

Noise simulations and measurements

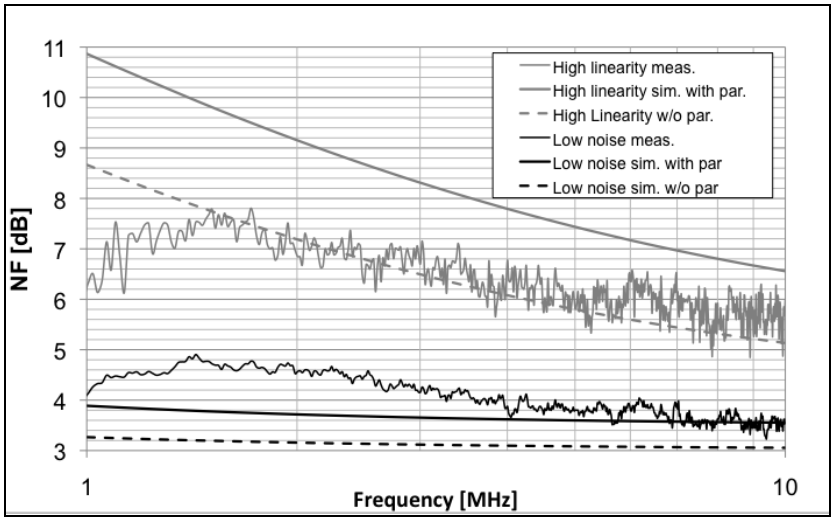

Figure 4.25:Noise Figure of the front end in the low noise and high linearity configurations compared with simulations with and w/o parasitics.

Considering the attenuation due to the capacitances, a 3 dB lower gain is simulated. The gain simulated in the two configurations introducing the attenuation fits with the measurements.

IIP3 simulations and measurements

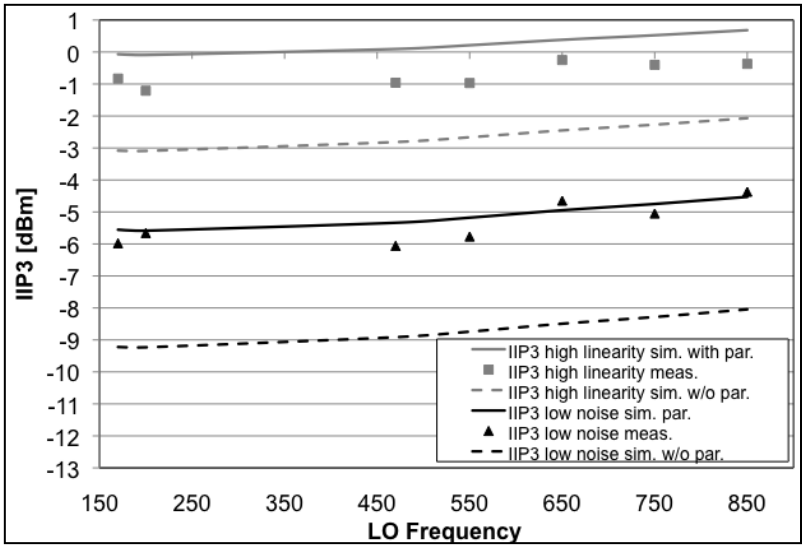

Figure 4.26:Two tones IIP3 measurements in the low noise and high linearity configurations compared with simulations with and w/o parasitics.

The same approach is used for the noise measurements. Again the gray lines are related with the high linearity configuration and the black lines with the low noise one. The dotted lines are simulations results due to the parasitic capacitances as in the case of gain.
The noise from the simulations in the continuous lines is 3 dB @10MHz in the low noise configuration and it is 5dB @10MHz in the

high linearity configuration. Introducing the attenuation the lowest noise figure of the front end becomes 3.5 dB @10MHz. In the high linearity configuration the NF is 5.5 dB @10MHz. The noise is higher at low frequency due to the flicker noise. The decreasing of noise round 1 MHz is caused by the bandwidth of the probe used for the measurements. The performances of DVB-H tuner linearity are shown in Figure 4.26. As the noise figure is higher for the attenuation at the input of the downconverter stage, the linearity is higher for the reduction of the gain of the LNA stage.

State of the art comparison

	TOPOLOGY	IIP2 [dBm]	IIP3 [dBm] (MAX GAIN/MIN GAIN)	NF[dB]	Power [mW]	Supply voltage [V]
Antoine et al. JSSC'05 [4.1]	Fully DIFF.	45	--/12	8.5	193	2.775
Womac et al. ISSCC'06 [4.9]	Single to DIFF.	>27	--/4	3.6	340(*)	2.7
Gupta et al. ISSCC'07 [4.10]	Fully DIFF.	36.5	-14/17.5	4 to 7	540(**)	1.8
Vavelidis et al. ESCIRC'07 [4.2]	Fully DIFF.	>36	-6/-3	3	93(*)	1.2-2.5
THIS WORK	Single to DIFF.	28-35 (LNA STAGE)	-6/-1	3.5(5.5)	54(44)	1.2-1.5

Table 4.6: (*)Considering PLL ,(**)Considering PLL and ADC.

The IIP3 in the low noise configuration (black lines) is higher than -6 dBm and higher than -1 dBm in the high linearity case (gray lines). The IIP3 is plotted in function of the frequency of the LO used for the direct downconversion, so of the wanted signal. The linearity is higher at higher frequency because the gain of the LNA is lower, due to the bandwidth limitation.

In Table 4.6 are summarized the performance of the Tuner compared with the results in literature. The performance of second order non linearity is not measured because to the off chip load resistances mismatches. The mismatch of the load resistance affects the IIP2 measurements and the results are lower than the measurement of IIP2 done for the only LNA. That is not reasonable if a fully differential passive mixer is used, but due to the effect of the off-chip mismatches the measurements are not significant. The simulated IIP2 for the downconverter stage stand alone implying 1% mismatch of the switch dimensions is 65dbm in the high linearity configuration. So as a reasonable value of IIP2 for a solution with the on chip integrated resistances is the performance measured in the previous paragraph for the LNA stand alone. In Table 4.6 this value is reported for the IIP2. IIP2 and noise are comparable with the results obtained for the single

ended solution in [4.8], but the performances in this case are obtained in two configurations. The NF measured is in the case of max gain, the IIP3 in the case of 20dB of attenuation. Moreover considering the case without parasitic capacitance (or with a higher value of the AC coupling capacitance) NF=3dB with a IIP3 higher than the two tones specification of -3 dBm are obtained. These performance are in this last case comparable with the fully differential topology using a multi-LNAs approach shown in [4.2]. Again the power dissipation is lower for the test chip shown in this chapter.

4.5 Conclusions

To cover the VHF and UHF bands different approaches can be chosen. Several narrowband LNAs or a single wideband one can be two different solutions. In this chapter the active balun broadband LNA presented in the previous chapter is considered. Moreover an adaptive approach is followed for the design of the downconverter stage. So a reconfigurability in function of the standard is followed. Two main working conditions are implemented: a high linearity and a low noise one. To obtain this degree of adaptively a proper design of the downconverter stage is done. In particular a variation of the gain caused by the different values of the transconductance stage and the modification of the input impedance and noise of the base band stage are combined to cover the specifications of the standard. Performances close to the fully differential architectures presented in the state of the art are achieved with the test chip integrated. The specifications request to the standard are satisfied.

References

[4.1] P. Antoine, P. Bauser, H. Beaulaton, M. Buchholz, D. Carey, T. Cassagnes, T. K. Chan, S. Colomines, F. Hurley, D. T. Jobling, N. Kearney, A. C. Murphy, J. Rock, D. Salle, and T. Cao-Thong, *A direct-conversion receiver for DVB-H*, IEEE J. Solid-State Circuits, vol. 40, pp. 2536-2546, Dec. 2005.

[4.2], K. Vavelidis, I. Vassiliou, N. Haralabidis, A. Kyranas, Y. Kokolokis, S. Bouras, G. Kamoulakos, C. Kapnistis, S. Kavadias, N. Kanakaris, E. Metaxakis, C. Kakozidis, H. Peyravi, *A 65nm CMOS Multi-Standard, Multi-Band TV Tuner*, Proc. IEEE, 2007.

[4.3] A. Liscidini, G. Martini, D. Mastantuono, and R. Castello " *Analysis and Design of Configurable LNAs in Feedback Common Gate Topologies*" TCAS2

[4.4] S. Borsotti " *Studio di mixer passivi 'current mode' per tecnologie CMOS superscalate*" Tesi di Laurea.

[4.5] D. Sanzogni " *Progetto di un mixer CMOS a bassa distorsione di secondo ordine per applicazioni UMTS*" Tesi di Laurea.

[4.6] W. Sansen " *Distortion in Elementary transistor circuits*" IEEE Transaction on Circuits and Systems II, Vol.46 No. 3, 1999.

[4.7] S. Chehrazi, A. Mirzaei, R. Bagheri and A. A. Abidi, "*A 6.5 GHz Wideband CMOS Low Noise Amplifier for Multi-Band Use*" Proc. CICC 2005, pp 801-804, Sept. 2005

[4.8] Shuzuo Lou and Howard C. Luong, "*A Linearitazation Technique for RF receiver Front-End Using Second-Order-Intermodulation Injection*" IEEE Journal of solid state circuit, vol. 43 no.11 november 2008.

[4.9] M. Womac, A. Deiss, T. Davis, R. Spencer, B. Abesingha, P. Hisayasu "*Dual-Band Single-Ended-Iinput Direct Conversion DVB-H Receiver*" ISSCC, Feb. 2007.

[4.10] M. Gupta, S. Lertaveesin, D. Kang, B-S. Song "*A 48MHz-860MHz CMOS Direct-Conversion TV Tuner*" ISSCC, Feb. 2007.

APPENDIX A

COMMON GATE MULTIPLE FEEDBACK NETWORKS

Series and shunt feedback networks closed around the common gate topology are analyzed, providing a unified expression for input impedance, and LNA matching condition. Successively, analytical expression for gain, noise, linearity, stability conditions and sensitivity to process variation are derived.

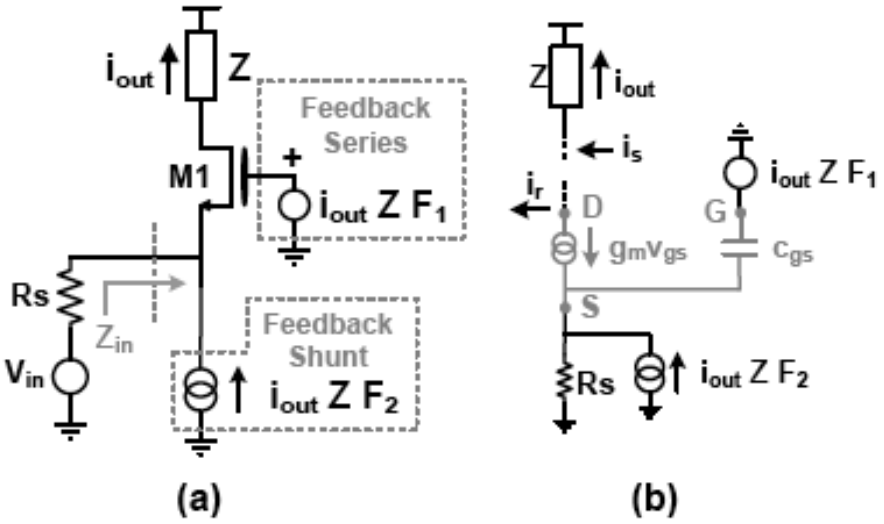

Figure A.1: (a)Shunt-series feedback around common gate stage (b) Return Ratio diagram.

The type of feedback configurations considered in the following analysis are reported Figure A.1(a). In particular F_1 is a voltage (series) feedback returned to the gate (negative for $F_1>0$), while F_2 represents a current (shunt) feedback returned to the source (positive for $F_2>0$). The output of the system is taken as the current flowing through the load Z, making the amplifier transfer function a transconductance. Contrary to the classical feedback description,

Return Ratio teory

based on the loop gain, the analysis will describe all circuit properties in terms of return ratio (RR) [A.1]. This approach has been preferred because it provides a single expression for the input impedance, for both shunt and series feedback. In addition, the return ratio allows to study the amplifier stability in the presence of multiple feedback loops and to model bidirectional paths between input and output. As explained in [A.1] the circuit is divided into two main parts (Figure A.1(b)): the controlled device (in grey), and the feedback portion (in black). Neglecting the gate-source capacitance (assuming a transistor f_T much higher than the working frequency), RR has the following expression:

$$RR = -\frac{i_r}{i_s} = \frac{g_m Z}{1 + g_m R_S}(F_1 - F_2 R_S) \qquad \text{(I)}$$

where g_m is the transistor's transconductance and Rs the driving resistance. The first term in (I) represents the series feedback and the second the shunt one. In addition, the source resistance Rs acts intrinsically as a series feedback for a common gate topology, being a degeneration for the input transistor [A.2].

A.1 Input impedance and matching condition.

The input impedance of the multiple loop LNA can be evaluated (independently of the feedback used), by the return ratio and the Blackman's formula [A.1] as:

Input impedance

$$Z_{in} = Z_{in,OPEN}\frac{1 + RR|_{R_S=0}}{1 + RR|_{R_S=\infty}} = \frac{1}{g_m}\frac{1 + F_1 Z g_m)}{1 - F_2 Z} \qquad \text{(II)}$$

where $Z_{in,OPEN}$ is the input impedance of the circuit with all the loops broken and it is equal to 1/gm. When $F_1>0$ the input impedance increases compared to the common gate topology and the same is obtained for $F_2>0$. On the contrary, reversing the sign of the two feedbacks the input impedance decreases. Equation (II) hints to the possibility of reconfiguring the input impedance acting on F_1, F_2. The LNA's matching condition is derived from (II) when $Z_{in}=R_S$. This forces the transistor's transconductance to be:

Matching condition

$$g_m = \frac{1}{R_S - (F_1 + F_2 R_S)Z} \qquad \text{(III)}$$

Notice that, since for a given R the couple (F_1, F_2) sets the value of the transconductance, the power consumption of the LNA is also uniquely defined. The matching condition expressed by (III) imposes two bounds on the value of F_1 and F_2 as shown below:

$$\begin{cases} \frac{Z}{R_S} F_1 + RF_2 < 1 \\ RF_2 < 1 \end{cases} \quad \text{(IV)}$$

The first one is due to the finite value of the transistor's transconductance, while the second comes from the stability condition as discussed in the next section. Since in-band input matching is required for proper operation, in the following we will assume that (III) is always verified.

A.2 Transconductance gain

The common gate amplifier usually suffers from a poor transconductance gain, here defined as Gm. This happens because the transistor is used as a simple input termination, so that its gm is forced to be equal to $1/R_S$. When using feedback the LNA gain is modified as follows:

Gain

$$G_m = \frac{i_{out}}{v_{in}} = \frac{1}{2R_S(1 - F_2 Z)} \quad \text{(V)}$$

If no feedback is used, (V) gives the gain of a common gate stage i.e. Gm equal to $1/2R_S$. The same result is obtained if only F1 is used (F_2=0) since the current provided by the source goes directly to the output without any amplification. On the contrary, using F_2 the Gm can be modified as a consequence of adding a new current path at the input. Thus, when a high G_m is wanted, a shunt positive feedback should be used.

A.3 Noise Factor

Noise analysis is performed assuming noiseless feedback networks, considering only the noise sources arising from the gain device, plus thermal noise of the load (Z=R). Under these assumptions, the noise figure is given, by the following equation:

$$F = 1 + \frac{\gamma}{g_m R_S} + \frac{R_S}{R}\left(1 + \frac{1}{g_m R_S}\right)^2 \quad \text{(VI)}$$

The second term on the right hand side of (VI) accounts for the MOSFET channel noise, and the third term accounts for the load thermal noise.
The noise figure given by (VI) does not depend, explicitly, on the amount of feedback applied; however the presence of feedback changes the NF through a change in gm according to (III) as shown in the following equation:

Noise factor

$$F_{match} = 1 + \gamma\left(1 - \frac{RF_1}{Rs} - F_2 Z\right) + \frac{Rs}{R}\left(2 - \frac{RF_1}{Rs} - F_2 R\right)^2 \qquad \text{(VII)}$$

where the dependence on feedback is explicit. The second and third term in (VII) have the same origin of the corresponding term in (VI) while the noise figure of the simple common gate LNA is given when F_1 and F_2 are set to zero. The noise figure can be higher or lower compared to the common gate amplifier, depending on the sign of the feedbacks. In particular for positive F_1 and F_2, F_{match} is lower than the common gate one.

A.4 Stability

Even for a multi-loop topology the amplifier stability can be evaluated from the gain/phase margin of the return ratio since there exists a single point that breaks all the loops at the same time [A.1]. For $F_1>F_2R_S$ we have that RR>0 and the two feedbacks act like a single negative one. Two cases are possible:

- Negative feedback with 0<RR<1. If $F_1R<R_S$ we have RR<1 in band. If the maximum gain is obtained in the LNA working band (typical case), the amplifier is then unconditionally stable.
- Negative feedback with RR>1. For these cases, the stability can be evaluated looking at the phase margin and can be guaranteed with a proper choice of Z

For $F_1<F_2R_S$ we have RR<0 and a positive feedback occurs, again two cases are possible:

- Positive feedback with -1<RR<0. In the presence of a positive feedback the amplifier is stable if RR>-1. This can be guaranteed setting $F_2R<1$ in (1), with a safe margin to take into account process variation.
- Positive feedback with RR<-1. In this case the system is unstable.

A.5 Linearity

Assuming the feedback networks are linear, the distortion depends on the transistor operating point and on the effects of the feedbacks on the gate-source voltage swing (V_{GS})[A.3].
The two feedback acts differently on V_{GS} to satisfy the matching condition. In particular, F_1 forces $V_{GS}=V_{in}/(2g_mR_S)$ while F_2 forces V_{GS} to be equal to $V_{in}/2$. Therefore, for a given overdrive, only F_1 influences the amplifier linearity since F_2 does not affects the gate-source voltage swing. On the other hand, for a given bias current the transistor overdrive is defined by (III) and the relationship $I/g_m=V_{ov}/2$ making the linearity dependent also on F_2.
The IIP3 for the three cases considered - simple common gate ($IIP3_{CG}$) series feedback ($IIP3_{F1}$) and shunt feedback ($IIP3_{F2}$) - have been computed using Sansen's theory [A.4] and the coefficients of the V to I transistor characteristic (in strong inversion) defined in [A.5], obtaining:

$$\begin{cases} IIP3_{CG} = \left| \dfrac{16V_{OV}^2(2+\theta V_{OV})^2}{3R_S} \right| \\ IIP3_{F1} = IIP3_{CG} \left| \dfrac{(1+G_{LOOP})^4(1+\theta V_{OV})^2}{1-(1+G_{LOOP})(1+(1+\theta V_{OV})^2)} \right| \\ IIP3_{F1} = IIP3_{CG} \end{cases} \quad \text{(VIII)} \qquad \textbf{IIP3}$$

where θ is a fitting parameter. For a given overdrive voltage V_{ov}, the $IIP3_{F1}$ is approximately equal to the $IIP3_{CG}$ time $|1+Gloop|^3$ since the modulation of the gate-source voltage is inversely proportional to the loop gain [A.2]. On the contrary when F_2 is applied $IIP3_{F2}$ has the same expression as $IIP3_{CG}$, as predicted by the qualitative analysis. On the other hand, for a constant bias current the proper overdrive (different in the three cases) should be used in each expression.

A.6 Sensitivity

The RR sensitivity to the a generic circuits parameter x can been defined as follows:

$$S_X^{RR} = \frac{x}{RR}\frac{\partial_{RR}}{\partial_X} \quad \text{(IX)}$$

The RR sensitivities to gm, F_1, F_2 were evaluated for |RR| close to unity, where a possible spread of the process could increase the gain

causing instability. In particular the following results has been obtained:

$$S_{g_m}^{RR} = \frac{x}{RR}\frac{\partial_{RR}}{\partial_x} \tag{X}$$

$$S_{F_1}^{RR} = \frac{F_1}{F_1 - F_2 R_S} \overset{RR\to 1}{\Rightarrow} \cong F_1 \frac{g_m R}{1 + g_m R_S} \quad . \tag{XI}$$

$$S_{F_2}^{RR} = \frac{F_2 R_S}{F_1 - F_2 R_S} \overset{RR\to 1}{\Rightarrow} \cong F_2 R_S \frac{g_m R}{1 + g_m R_S} \tag{XII}$$

The sensitivity of RR to the input transconductance gm is always lower than 1 and decrease as gm increases. On the other hand (XI) and (XII) show that the sensitivity to F_1 and F_2 is lower than one choosing $|F_1 R|<Rs$ and $|F_2 R|<1$ respectively. The latter condition is always verified in the first quadrant where all the performance (IIP3 and Gain, NF) are improved compare to the common gate. For all cases the sensitivity to the load R is equal to 1.

A.7 Adaptive Optimization

The previous sections have shown that, assuming constant overdrive, the two feedback networks control respectively one design parameter, without affecting the other one (i.e. F_1 acts on the linearity while F_2 on the gain).

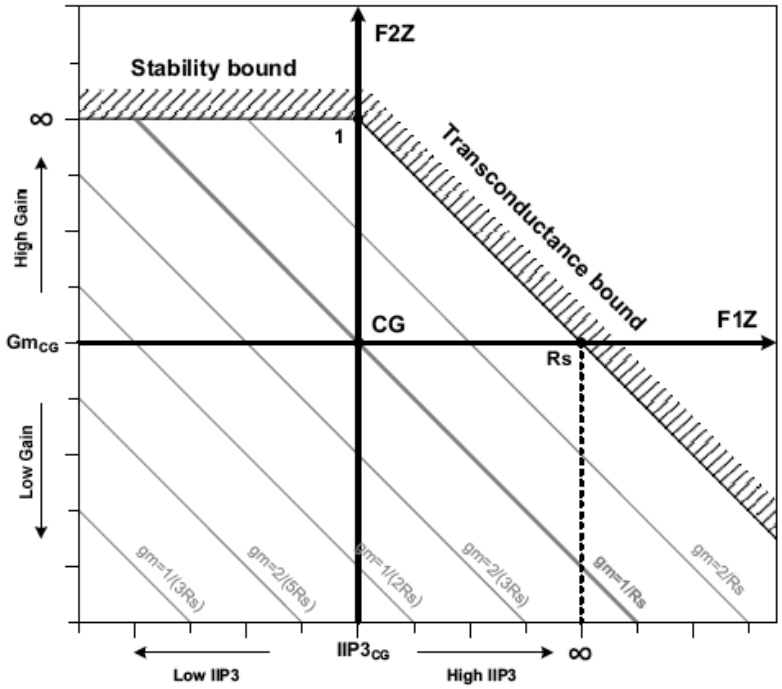

Figure A.2: Feedbacks plane.

It follows that, acting on F_1 and F_2, the amplifier can be simply optimized to reach the desired performance. This flexibility leads to the development of a new design strategy which aims at satisfying different scenarios reconfiguring the receiver in real time.
For a given overdrive voltage, the equations derived in the previous sections allow to draw the diagram of. Figure A.2. In this plot, the effects of $F_1 \bullet R$ and $F_2 \bullet R$ on G_m (V) and IIP3 (VIII) are shown explicitly, while the effect on NF follows indirectly through the value of gm drawn on the figure in parametric form (VI). In the figure gain and IIP3 are normalized to those of the common gate amplifier CG. The diagram is completed with the forbidden region derived from (IV), i.e. the transconductance bound corresponding to a transistor gm equal to infinity and the stability bound that imposes $F_2 \bullet R<1$. In gray it is shown the portion of plane where $F_2 R_S > F_1$, corresponding to an overall positive stable feedback as discussed previously. Exploring all the configurations in the plane ($F_1 \bullet R$, $F_2 \bullet R$) it is possible to exchange performance, with power consumption. In particular, when F_1 and F_2 are both positive, the amplifier properties are all improved compared to the common gate amplifier, at the cost of a larger power consumption. On the contrary when F_1 and F_2 are both negative a lower g_m is required, reducing power consumption but also gain and linearity. The diagram and the previous equations provide a methodology for the design of feedback common gate LNA summarized in the following steps:

- Starting from a target noise figure NF and transconductance gain Gm, gm and F_2 are set from (VI) and (V) respectively.

- Then the value of F_1 is univocally derived from the matching condition (III) or from the diagram in Figure A.1Figure A.2.

- Finally, the desired IIP3 can be obtained acting on Vov by changing the transistor aspect-ratio and bias current while keeping g_m constant.

In conclusion, to enhance system linearity a series feedback has to be used, while, for a gain greater than the common gate one, a shunt positive feedback is needed.

References

[A.1] Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer *Analysis and design of analog integrated circuits*, Proc. IEEE vol. 39, no. 2, Feb. 2004.

[A.2] P. Rossi, A. Liscidini, M. Brandolini, F. Svelto, "*A Variable Gain RF Front-End, Based on a Voltage-Voltage Feedback LNA, for Multistandard Applications*", Solid-State Circuits, IEEE Journal of , Vol. 40 , Num. 3 , Mar. 2005. pp. 690 – 697..

[A.3] A. Liscidini, M,. Brandolini, D. Sanzogni, R. Castello, "*A 0.13 m CMOS front-end for DCS1800/UMTS/802.11b-g with multi-band positive feedback low noise amplifier*" Solid-State Circuits, IEEE Journal of , Vol. 41 , Num. 4 , April 2006. pp. 981 – 989.

[A.4] W. Sansen, "*Distortion in elementary transistor circuits*," IEEE Trans. Circuits Syst. II: Analog Digit. Signal Process., vol. 46, no. 3, pp. 315– 325, Mar. 1999.

[A.5] A. Liscidini, M,. Brandolini, D. Sanzogni, R. Castello, "*A 0.13 m CMOS front-end for DCS1800/UMTS/802.11b-g with multi-band positive feedback low noise amplifier*" Solid-State Circuits, IEEE Journal of , Vol. 41 , Num. 4 , April 2006. pp. 981 – 989.

[A.6] A. Liscidini, G. Martini D. Mastantuono, and R. Castello " *Analysis and Design of Configurable LNAs in Feedback Common Gate Topologies*" on Volume 55, Issue 8, Aug. 2008 Page(s):733-737, IEEE Transaction on Circuits and Systems Part II: Express Briefs (TCAS2).