MULTI-BIT A/D CONVERTERS WITH HIGH RESOLUTION AND LOW-POWER

A Ph.D. Thesis

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To Jiannan, Sen and my parents

CONTENTS

LIST OF FIGURES

LIST OF TABLES

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ACRONYMS

ADC	Analog-to-digtal converter
AFF	Analog feed-forward
CQFP	Ceramic quad flat pack
CT	Continuous time
CMOS	Complementary metal-oxide-semiconductor
CMFB	Common mode feedback
dBc	dB to carrier
dB_{FS}	dB to full scale voltage
DAC	Digital-to-analog converter
DEM	Dynamic element matching
DFF	Digital feed-forward or D flip-flop
DFM	Digital frequency modulation
DSP	Digital signal processing
DNL	Differential non-linearity
DT	Discrete time
DWA	Data weighted averaging
ENOB	Effective number of bits

FCA	Folded cascode amplifier
FFT	Fast Fourier transform
FOM	Figure of merit
$\mathrm{FOM_S}$	FOM based on Schreier's definition
$\mathrm{FOM_W}$	Walden's FOM
FSM	Finite state machine
GBW	Gain bandwidth product
GCS	Gated current source
I&M	Instrumentation and measurement
INL	Integral non-linearity
MIM	Metal insulator metal
NTF	Noise transfer function
OSR	Oversampling ratio
OTA	Operational transconductance amplifier
PCB	Printed circuit board
PCM	Pulse code modulation
PSD	Power spectrum density
QPSK	Quadrature phase shift keying
RFCA	Recycling folded cascode amplifier
SAR	Successive approximation
SDEM	Smart dynamic element matching
SFDR	Spurious free dynamic range
SNR	Signal to noise ratio
SNDR	Signal-to-noise-and-distortion ratio
STF	Signal transfer function
THD+N	Total harmonic distortion plus noise
TI	Time interleaved
VCCS	Voltage control current source
VLSI	Very large scale integration
ZCD	Zero crossing detector
$\Sigma\Delta$M	Sigma-Delta modulator

CHAPTER 1

INTRODUCTION

Analog-to-digital (A/D) and digital-to-analog (D/A) conversions are indispensable and ubiquitous in the digitized world nowadays. The devices which convert a continuous-time continuous-amplitude signal to the counterpart with discrete-time and discrete-amplitude is called A/D converters (ADCs). On the contrary, the transformation from a discrete-time discrete-amplitude signal to a continuous-time continuous-amplitude format is performed by D/A converters (DACs). Both ADC and DAC consist the term data converter. The scope of this thesis, is to deal with high performance ADCs which are realized by modern very-large-scale-integration (VLSI) technlogy.

Since the invention of pulse code modulation (PCM) [1], people from both academy and industry dedicate themselves to the research and development of data converters for over 80 years. The driven force underlying is the requirement of utilizing an ever-increasing computation capability from digital computers to process signals in digital domain. However, due to the analog nature of the real world, the original analog signals should be digitized before being processed in a digital fashion.

Generally, ADCs can be divided in 2 categories: Nyquist-rate type and oversampling modulator. The Nyquist-rate ADCs is probably named after the famous Nyquist sampling theorem [2][3], which states that the sampling frequency F_S should be at least 2 times of the signal bandwidth B_W in order to keep the original information. For example, architectures such as pipeline and flash can be classified into Nyquist-rate type ADCs, and the common features are large bandwidth and low-medium ($<$ 12-bit) resolution [4][5]. On the other hand, ADCs with $F_S > 2B_W$ belong to oversampling type, which generally have a better tolerance of circuit imperfections and are able to achieve high resolution ($>$ 12-bit). However, the signal bandwidth of oversampling ADCs is smaller than that of Nyquist-rate modulators, such as $\Sigma\Delta$ and incremental ADCs reported in [6]-[8].

1.1 Motivation and Objectives

In this thesis, we are focusing on the design of ADCs which are able to achieve high resolution. In terms of the architectures, two types of ADCs have been selected for our study: the $\Sigma\Delta$ type and incremental architecture. Since its original patent in [9] and circuit realization [10], $\Sigma\Delta$Ms have been fully investigated by numerous researchers because they can achieve a high degree of insensitivity to analog circuit imperfections. For discrete time (DT) $\Sigma\Delta$Ms, the resolution normally ranges from 14-bit to 21-bit with B_W from 400 Hz to 2 MHz. While for continuous time (CT) $\Sigma\Delta$Ms, the obtained resolution spanning from 10-bit to 14-bit, however, with B_W from 10 MHz to 150 MHz [11]. Regarding incremental modulators, they share the same schemes with $\Sigma\Delta$Ms, providing a sample-to-sample conversion. Incremental ADCs are suitable for applications such as instrumentation and measurement (I&M), which usually require are high resolution, good linearity, low offset and lower power dissipation [8]. The achieved resolutions for incremental ADCs ranges from 16-bit to 22-bit, and the B_W spans from DC up several kHz at most.

One of the most significant parameters of ADCs is the power efficiency, which is measured by the figure of merit (FOM) discussed in Chapter 2. The low-power design for ADCs are self evident, especially for modulators used in portable applications. For example, with modern CMOS technologies, high speed ADCs can obtain data rates more than 20G SPS with power consumption from 1.2 W to 10 W [12]. It is impractical to operate such blocks in the battery driven devices, such as mobile phones and tablets.

For $\Sigma\Delta$Ms and incremental ADCs, one way to reduce to power dissipation is to utilize multi-bit quantization. In general, modulators use comparator as quantizer and 2-level DAC do not suffer from non-linearity problem, however, the swing of the op-amps is large and may result in op-amps operating in slewing mode, leading to high power consumption of these blocks. On the contrary, the adoption of multi-bit quantization can reduce the output swing of op-amps are thus, giving rise to significant reduction of power consumption of op-amps. Nevertheless, the non-linearity of multi-bit DAC would degrade the overall performance of the modulator, if the mismatch between unity element in multi-bit DAC were not compensated for. The problem can be solved by dynamic or static digital correction methods, such as the dynamic element matching (DEM) algorithms [13].

Table 1.1 Research Target of $\Sigma\Delta$ and Incremental ADCs.

ADC Type	Resolution	Bandwidth	Power Consumption	Technology
DT $\Sigma\Delta$M	$\geq$ 12-bit	2 MHz	$<$ 2.0 mW	0.18 μm CMOS
Incremental ADC	$\geq$ 18-bit	5 kHz	$<$ 0.5 mW	0.18-0.5 μm CMOS

The motivation of this work is to search for new architectures and circuit techniques to achieve high resolution ADCs based on multi-bit quantization, which can be divided into 2 parts: 1) For $\Sigma\Delta$Ms, since the current DEM algorithm is able to compensate for the mismatch, we focus on the architectures and related circuit techniques for minimizing power consumption (e.g. op-amp reduction [6]). 2) For incremental ADCs, because the existing DEM algorithms cannot properly compensate for the mismatch of multi-bit DAC, the motivation is to search for a digital assistance method which is able to suppress the non-linearity issue.

The aforementioned motivations lead us to the specifications of two ADCs, as shown in Tab. 1.1. With regard to the DT $\Sigma\Delta$M, we targets at 12-bit resolution over 2 MHz bandwidth using 0.18 μm CMOS technology. The power consumption should be within 2.0 mW. The incremental modulator,

however, is expected to achieve 18-bit resolution over 5 kHz bandwidth adopting a mixed 0.18-0.5 μm CMOS technology. The power dissipation should be less than 0.5 mW.

1.2 Structure of the Thesis

The thesis is organized in the following way: Chapter 2 introduces the background of high resolution ADCs. The $\Sigma\Delta$ and incremental types are chosen and are investigated in detail. In Chapter 3, the effects of mismatch between unity element in multi-bit DAC are studied for both $\Sigma\Delta$ and incremental architectures. Because existing DEM algorithms are not able to fully compensate for the non-linearity of multi-bit DAC in incremental ADCs, a Smart-DEM algorithm is proposed with simulation results demonstrating its near-ideal error correction capability. Chapter 4 and 5 explain the design and implementation of a 17-bit second-order incremental ADC. In order to achieve the target resolution, Chapter 4 first analyses the key design parameters of incremental ADCs, namely the order of the architecture, the resolution of quantizer and the number of clock periods per sample. The selection of optimal incremental architectures with multi-bit quantization is then discussed. Based on Chapter 4, Chapter 5 describes the circuit implementation and measurement results of a 17-bit second-order incremental ADC, which features with 3-bit DACs assisted by second-order Smart-DEM algorithm. In Chapter 6, a single op-amp 0+2 second-order 12-bit $\Sigma\Delta$M is discussed. With the help of the first stage, input swing of the second stage is significantly reduced, which relaxes the requirement of the op-amp and allows low-power design. With 3-phase non-overlap clocks, the quantization error of the second stage is shaped by a second-order high pass noise transfer funtion (NTF) while using only one op-amp. The summary and conclusion of the thesis are given in Chapter 7. Limitations from kT/C noise for different order incremental ADCs are derived in Appendix A. Finally, Appendix B lists the author's publications during his 3-year Ph.D. study.

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CHAPTER 2

A/D CONVERTERS FOR HIGH RESOLUTION

This chapter deals with the background of ADCs aiming for high resolution ($\geq$12-bit). To start with, a general introduction about ADCs' history and current status is given. Since $\Sigma\Delta$ and incremental ADCs are particularly suitable for achieving high resolution, they are selected and are detailed investigated, spanning from basic ideas to state-of-the-art information. For $\Sigma\Delta$Ms, we focus on the architectures and design techniques which can achieve more than 12-bit resolution and low-power dissipation, such as op-amps reduction technique proposed in [1][2]. Due to the nature of high resolution of incremental ADCs, we concentrate on structures and methods for attaining more than 18-bit and low-power consumption. In particular, multi-bit quantization such as the one reported in [3] is a promising method and is detailed analysed in this chapter.

2.1 Background on A/D Converters

2.1.1 A Brief History

Probably nowadays it is difficult to determine exactly when the first data converter was invented. According to a survey on data converter history written by W. Kester, the earliest recorded data converter can date back to the 18^{th} century, and is not an electronic system at all, but hydraulic [4]. At that time, this system was built to meter the water and functions as an 8-bit DAC. Later, when the

telegraph and telephone were created, the requirement of increasing communication capability through a single wire led to the invention of pulse code modulation (PCM) and consequently, pushed data converters into the history. In 1937, Reeves designed one of the earliest all electronic data converters which includes a 5-bit ADC and DAC [5]. It is worthy to point out that the 5-bit ADC provides a 6k SPS output data rate by using vacuum tube technology.

In 1946, the first computer ENIAC was born and an increasing requirement of digital signal process (DSP) demands for various ADCs for different applications. In 1954, an 11-bit 50k SPS ADC based on vacuum tube technology was developed by B. M. Gordon, which is believed to be the first commercial product of ADCs. However, the vacuum tube based data converters at that time are very bulky and consume plenty of power. The inventions of transistor and later integrated circuit gradually change this situation. These new technologies give rise to reduction on both the size and power dissipation of data converters between 1950s to 1970s. In 1970s, the first generation of monolithic data converters were born. For instance, the first complete monolithic ADC is AD571 based on successive approximation (SAR) architecture in 1978, which achieved 10-bit resolution with 25 μs conversion time [6].

It is interesting to point out that almost all the basic architectures of data converters were invented by 1960s, to name a few, flash, SAR, pipeline, $\Sigma\Delta$, incremental, etc. Perhaps the most well known architecture is $\Sigma\Delta$ type. However, the basic idea underlying $\Sigma\Delta$ was first patented in 1960, [7], and first implemented in 1962, [8], which are more than 50 years up to now.

The most significant driving force behind data converters since 1970s, however, is the continuous development of transistor technologies. The complementary metal oxide semi-conductor (CMOS) technology, because of its low static power, became dominant in late 1970s. The feature size of CMOS transistors, decreased from around 125 μm in 1950s to less than 22 nm up to date, which means that more transistors or functionality can be integrated on a single chip. This phenomenon is well described in the famous Moore's law which says that the number of transistors integrated on single chip doubles every 18 months [9]. The continuously increased digital computation capability and the analog nature of the world determine the widely usage of data converters. To date, data converters are used almost everywhere, including sensor applications, wireless communication infrastructure, health care and life science and so on. With regard to ADCs, the achieved resolutions range from 3-24 bits, while the bandwidth spans from DC to more than 10 GHz [10]. According to the expectations reported in [11], ADCs would be implemented in 10-11 nm CMOS technology with 40 mV power supply by 2020. The expected FOM_S is approximately 0.2 fJ/conv-step, while the state-of-the-art value was 2.2 fF/conv-step [12].

2.1.2 Applications and Categories

As mentioned above, data converters are necessary components for the modern electric systems. According to a market survey reported by [13], data converters are becoming the second largest analog component after power management circuits, with unit shipments about 2.9 billion units in 2010 to an expected quantity of around 4.7 billion units by 2015 (stand-alone data converters). Regarding ADCs, the starting point of our study is however, to get familiar with the applications in which ADCs are used. Moreover, for each type of application, corresponding ADC architectures and specifications should be investigated. The typical applications for ADCs are listed as follows

► **Instrumentation and Measurement Applications**: includes applications such as digital multimeter and portable weight scale [15]. The bandwidth of ADCs used in these applications is limited from DC to few kHz, while the resolution requirement is generally more than 16-bit to even 24-bit. Moreover, these ADCs needs to achieve good linearity and low offset. Low-power consumption is also an important factor especially for portable applications. ADCs based on incremental and dual-

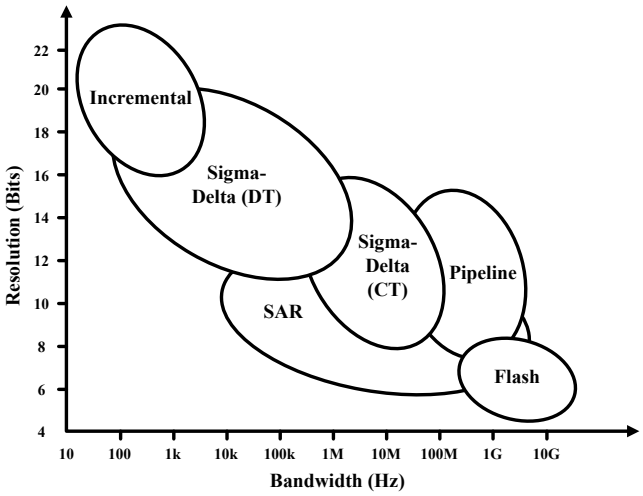

Figure 2.1 ADC architectures for typical resolution and bandwidth requirements.

slope architectures are well suitable to meet these requirements, such as an third-order incremental ADC which attained 22-bit [16].

► **Biomedical and Health Care Applications**: demand for low-power ADCs with low bandwidth and low-moderate resolutions. For example, EEG, ECG and bioimplantable systems require ADCs with data rate less than 200k SPS, and the resolution is between 6-10 bits [17]. In this case, ADCs based on SAR architecture are good choices, such as a 9.1-bit 1k SPS SAR ADC consuming only 53 nW [18].

► **Audio Applications**: generally require ADCs with bandwidth from kHz to few hundreds kHz and THD+N ranging from 60 dB to more than 100 dB. For instance, the voice communication through telephone needs 4 kHz bandwidth and 60-70 dB THD+N. However, high quality DVD audio requires 16-bit to 24-bit resolutions with a sampling rate from 44.1k SPS to 192k SPS. To meet these requirements, $\Sigma\Delta$ ADCs are appropriate candidates. One example is a multi-bit $\Sigma\Delta$ ADC which can obtain 24-bit resolution with 216k SPS output data rate [19].

► **Wireless and Wireline Applications**: demand for modulators with low-medium resolution and large bandwidth. For instance, digital FM (DFM) and LTE-advanced require ADCs with banwidth spanning from 20 MHz to 100 MHz with more than 10-bit resolution. In this case, continuous $\Sigma\Delta$ modulators are appropriate candidates to meet the specification [20]. However, applications such as radar, software-defined radio and multi-channel satellite reception require 2.5-3.0G SPS data rate. One solution is to use the time-interleaved (TI) SAR ADC with 3.6G SPS and 11-bit resolution [21]. Moreover, the 40Gb/s optical QPSK systems require sampling rate more than 24G SPS with 6-bit resolution. In this case, a TI SAR ADC reported in [22] is a good choice which obtained 40G SPS sampling rate and 6-bit resolution with a power consumption less than 1.5 W.

Fig. 2.1 illustrated conventional ADC architectures for typical resolution and bandwidth. It can be seen that DT $\Sigma\Delta$ and incremental types dominate the region when 12-bit or more resolution and less than 2 MHz bandwidth are required.

2.1.3 Specifications

The performance of ADCs is determined by a large set of parameters. Readers may refer to more detailed literature such as [23], to have a better understanding of the full set of specifications. Nonetheless, the items listed below are of the most importance and are used in the overall thesis.

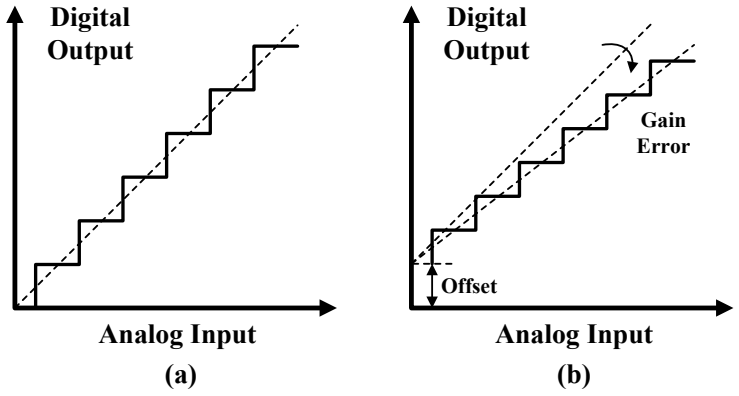

Figure 2.2 Offset and gain error of ADCs.

► **Resolution**: determines the minimum quantity of analog signal which can be detected by ADCs. For example, a 14-bit ADC with a full scale voltage (V_{FS}) of 2V can differentiate the minimum voltage $122.1\mu V$.

► **Bandwidth**: specifies the maximum frequency of input sinusoid signal which leads to a $\sqrt{2}/2$ attenuation of the amplitude after the A/D conversion.

► **Signal-to-noise-ratio (SNR)**: indicates the ratio between signal power (P_S) and noise power (P_N), which is always expressed in dB format as follows

$$SNR = 10 \times log_{10} \frac{P_S}{P_N} \tag{2.1}$$

► **Signal-to-noise-and-distortion ratio (SNDR)**: is similarly to the definition of SNR, except the non-linear distortion term. The SNDR can be estimated as

$$SNDR = 10 \times log_{10} \frac{P_S}{P_N + P_H} \tag{2.2}$$

where P_H refers to the total harmonic distortion generated by circuits or systems.

► **Spurious free dynamic range (SFDR)**: is defined as the ratio of power between fundamental signal to the power of largest harmonic distortion. SFDR is usually measured in dBc (dB to carrier) or in dB_{FS} (dB to full scale range).

► **Offset**: quantifies the amount by which the actual characteristic is linearly shifted from its ideal position. Fig. 2.2 (b) illustrates the real characteristic, which is shifted up with an offset compared with the ideal curve shown in Fig. 2.2 (a).

► **Gain Error**: is defined as the different slopes between the real characteristic curve and the ideal transfer function, which can be seen in Fig. 2.2 (b).

► **Differential non-linearity (DNL)**: is a term describing the deviation between 2 analog quantities corresponding to adjacent input digital codes. Ideally, analog voltages corresponding to 2 adjacent

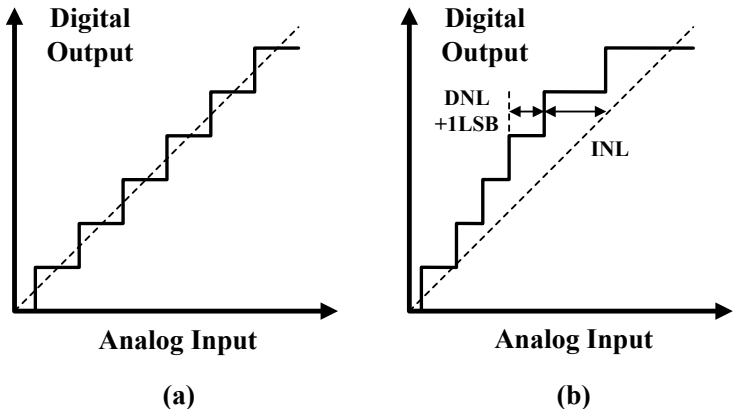

Figure 2.3 DNL and INL of analog-to-digital converters.

digital codes are exactly one least significant bit LSB apart. DNL is measured as the largest deviation in terms of 1 LSB step, which is shown in Fig. 2.3 (b).

► **Integral non-linearity (INL)**: is described as the deviation of an actual transfer function from the ideal characteristic, which is represented in LSB or percent of full-scale range. The INL magnitude depends on the position chosen for ideal characteristic. Here, we use end-point INL as illustrated in 2.3 (b).

► **Effective number of bits (ENOB)**: measures the signal-to-noise and distortion ratio with bits. SNDR in dB and ENOB are linked by

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{2.3}$$

► **Figure of merit (FoM)**: is introduced in order to compare the performances between various ADCs which may differ widely in architectures and specifications. One of the most commonly used figure of merit is known as "Walden's" FOM [24] which is defined as

$$FOM_W = \frac{P}{2B_W \times 2^{ENOB}} \tag{2.4}$$

where P is the power consumption of the ADC. FOM_W is an key parameter to measure ADC's power efficiency and it is expressed in pico-joules per conversion step (pJ/conv-step). Another popular figure of merit is Schreier's definition which can be described as

$$FOM_S = SNDR + 10log_{10}\frac{B_W}{P} \tag{2.5}$$

FOM_S is expressed in dB and its value increases for better performing modulators. According to [10], both FOM_W and FOM_S work well only across a limited range of SNDR. For low-resolution ADCs, evaluation based on FOM_W is more suitable, whereas FOM_S is more appropriate for modulators targeting at high resolutions.

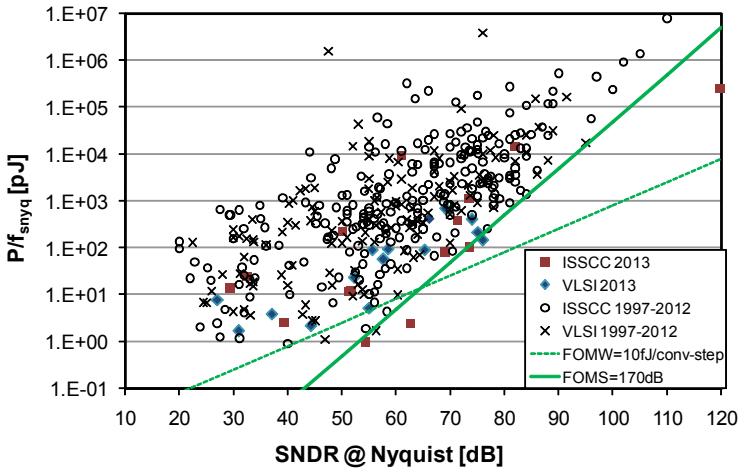

Figure 2.4 Power efficiency of ADCs with respect to SNDR.

2.1.4 State of the Art of ADCs

In this subsection, we use the data reported in [10] to investigate state of the art ADCs. The sources of the data are from the results published at IEEE International Solid-State Circuits Conference (ISSCC) and the VLSI Circuit Symposium since 1997. Fig. 2.4 plots the power per Nyquist sample with respect to the obtained SNDR. As seen in Fig. 2.4, several ADCs with the best power efficiency in terms of FOM_W were published in ISSCC 2013, such as a 10/12-bit 40k SPS SAR ADC with FOM_W 2.2/2.7 fJ/conv-step [12]. Regarding high resolution ADCs, a 6.3 μW 20-bit incremental ADC was proposed in [25] with a FOM_S of 182.7 dB.

Besides the power efficiency, the achievable bandwidth is also a key parameter. This is because that, in general, when a design is pushed toward the speed limits under a certain technology, the power efficiency is always sacrificed [26]. Fig. 2.5 illustrates the obtained ADCs' bandwidth in terms of SNDR. The dash line represents the performance of an ideal sampler with sinusoid input and a sampling clock with 100 $\mathrm{fs_{RMS}}$ jitter. It can be noticed that ADCs with highest bandwidth over all the resolutions should use a sampling clock with jitter less than 1 $\mathrm{ps_{RMS}}$. However, in order to attain an ADC comparable with state of the art, a better sampling clock with jitter lower than 100 $\mathrm{fs_{RMS}}$ should be adopted. For instant, the TI pipeline ADC proposed in [27] uses a sampling clock with measured jitter 70 $\mathrm{fs_{RMS}}$, which achieved 14-bit resolution with a 2.5 GSPS output data rate.

2.2 $\Sigma\Delta$ A/D Converters

As mentioned before, one of the most significant breakthroughs in the field of data conversion is $\Sigma\Delta$ modulation. On the basis of oversampling and quantization noise shaping, $\Sigma\Delta$Ms are able to tolerate circuit imperfections and thus, the strict requirements of the analog components can be relaxed. In this section, we shall starts from the first-order $\Sigma\Delta$M to explain the underlying theory. Moreover, high-order structures are investigated to show the tradeoff between different sets of design parameters. The

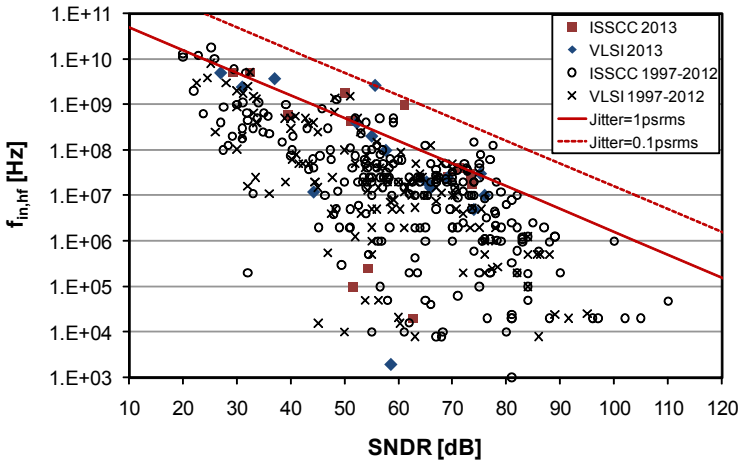

Figure 2.5 Conversion bandwidth of ADCs versus SNDR.

third part will discuss state of the art ΣΔMs architectures and circuit techniques in terms of low-power dissipation.

2.2.1 First-Order ΣΔ A/D Converter

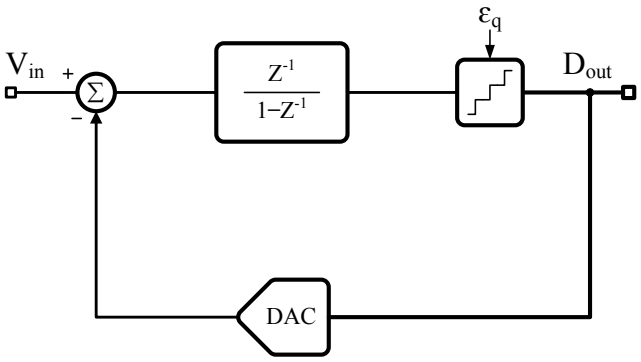

Figure 2.6 First-order ΣΔ ADC block diagram.

A conventional ΣΔ ADC consists of a delayed integrator, a multi-bit quantizer and corresponding DAC, as depicted in Fig. 2.6. The study in z domain gives rise to the transfer function as below

$$D_{out}(z) = V_{in}(z)z^{-1} + (1 - z^{-1})\epsilon_q(z) \tag{2.6}$$

As seen in (2.6), both input signal $V_{in}(z)$ and quantization error $\epsilon_q(z)$ contribute to digital output $D_{out}(z)$, by multiplying different transfer functions. For $V_{in}(z)$, the transfer function is called signal

transfer function (STF). The transfer function of $\epsilon_q(z)$, however, can be known as noise transfer function (NTF). Thus, using these terms, (2.6) can be rewritten as

$$D_{out}(z) = V_{in}STF(z) + \epsilon_q(z)NTF(z) \tag{2.7}$$

where $STF(z) = z^{-1}$ and $NTF(z) = 1 - z^{-1}$. Since $z = e^{j\omega}$ (F_S normalized to 1 Hz) and by mathematical calculations, the NTF of first-order $\Sigma\Delta$M can be represented by

$$NTF(jw) = 1 - e^{-j\omega} \tag{2.8}$$

Thus,

$$|NTF(w)|^2 = 4sin^2(\frac{\omega}{2}) \tag{2.9}$$

The result shows that the quantization error ϵ_q is high-pass shaped by $|NTF(w)|^2$. Fig. 2.7 plots the power spectrum density (PSD) of D_{out} of first-order $\Sigma\Delta$ ADC. The input signal is -3 dB_{FS} sinusoid waveform at normalized frequency 0.0016. A 2-bit quantizer is used and the DAC has 5 levels. The 2 reference voltages are V_{ref} and -V_{ref}. The full scale voltage V_{FS} is thus equal to $2V_{ref}$. As noticed in Fig. 2.7, the PSD of original ϵ_q is supposed to be white, is high-pass shaped with 20 dB/dec. The achieved SNR is 42.6 dB, which is equivalent to 6.78-bit.

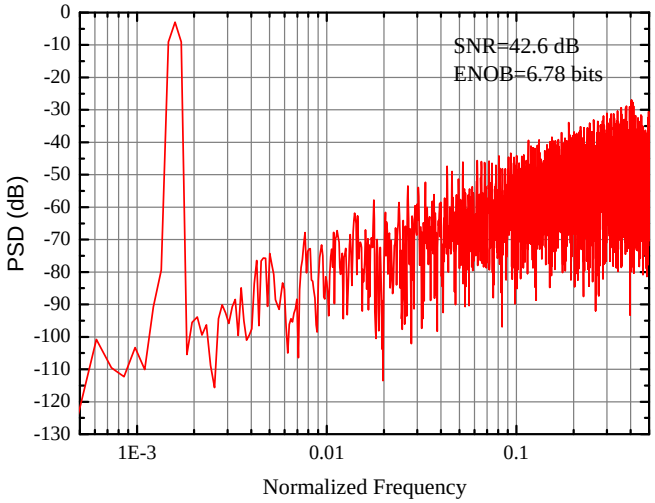

Figure 2.7 PSD (8096-point FFT) of D_{out} of the first-order $\Sigma\Delta$ ADC with -3 dB_{FS} sinusoid waveform input at normalized frequency 0.0016. The OSR is 16.

Besides noise shaping, the second key element of $\Sigma\Delta$ modulation is oversampling. In order to quantitatively describe it, the oversampling ratio (OSR) is defined as $F_S/(2 \times B_W)$. For a fixed B_W, a higher OSR can be obtained by increasing F_S. Consequently, the SNR of $\Sigma\Delta$Ms is improved. The reason is that, considering a unilateral representation of the PSD, the power of quantization error is distributed over the first-Nyquist zone. The SNR is calculated by the ration between the power of signal and the power of the noise within B_W. Thus, larger OSR gives rise to reduction of power of quantization error in the band of interest. In this case, the SNR of the corresponding $\Sigma\Delta$M is improved.

The resolution of quantizer b_q can also affect the performance of $\Sigma\Delta$Ms, where b_q is defined as $log_2(V_{FS}/V_{LSB})$. Generally, the quantization error can be regarded as white noise, whose power can

be estimated by

$$P_{NQ} = \frac{V_{LSB}^2}{12} \tag{2.10}$$

As seen in (2.10), by increasing b_q, the quantization interval V_{LSB} can be smaller, leading to a reduction of the power of quantization error P_{NQ}.

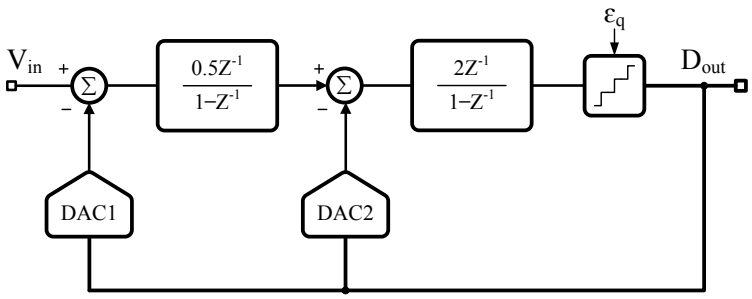

Figure 2.8 Second-order ΣΔ ADC block diagram.

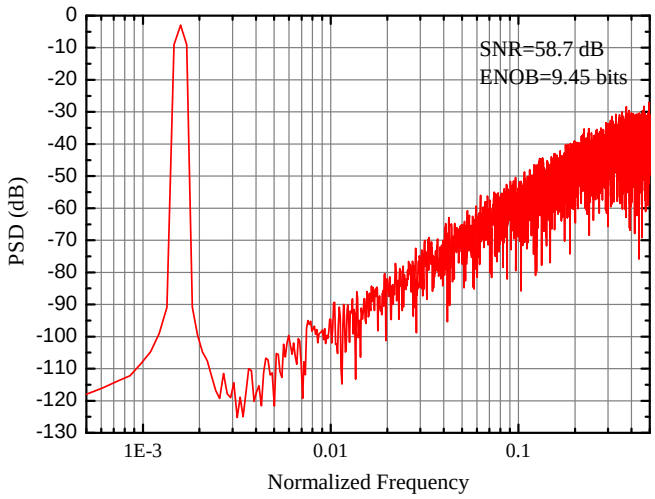

Figure 2.9 PSD (8096-point FFT) of D_{out} of the second-order ΣΔ ADC with -3 dB_{FS} sinusoid waveform input at normalized frequency 0.0016. The OSR is 16.

With the previous discussion, the resolution of first-order ΣΔM is determined by OSR and b_q. The relationship between SNR and those design parameters can be expressed as

$$SNR_{1ord,\Sigma\Delta} = 6.02b_q + 1.76 - 5.17 + 9.03 \times log_2(OSR) \tag{2.11}$$

2.2.2 High-Order ΣΔ A/D Converter

The performance of first-order ΣΔ ADC is limited. One method of boost the performance is increase the order of the structure. Fig. 2.8 shows a second-order ΣΔM which consists of 2 delayed integrators

with different coefficients, a multi-bit quantizer and DAC. The study in z domain leads to the transfer function as below

$$D_{out}(z) = V_{in}(z)z^{-2} + \epsilon_q(z)(1 - z^{-1})^2 \tag{2.12}$$

where ϵ_q is high-pass shaped by a second-order NTF. The benefit of second-order structure against first-order scheme is obvious: the power of quantization error within the band of interest experiences a larger suppression because of a second-order NTF. To compare the performance with the first-order architecture, same design parameter are chosen $b_q = 2$ and $OSR = 16$. As noticed in Fig. 2.9, the PSD of ϵ_q is shaped with 40 dB/dec due to the second-order high-pass NTF. The achieved SDR is 58.7 dB, which is equivalent to 9.45-bit.

For a Nth-order $\Sigma\Delta$ ADC whose NTF and STF has a denominator equal to 1, the SNR can be estimated as follows

$$SNR_{Lord,\Sigma\Delta} = 1.78 + 6.02q_b - 10log_2\frac{\pi^2 L}{2L+1} + 3.01(2L+1)log_2(OSR) \tag{2.13}$$

where L, q_b and OSR are the 3 key parameters when designing $\Sigma\Delta$Ms. The optimum designs of $\Sigma\Delta$ ADCs are attained by a good tradeoff between these parameters. In general, high-order modulators guarantee high resolution, but a large number of op-amps are needed, which means the power dissipation will be increased. Moreover, high OSR grants good resolution at the cost of increased F_S, which leads to high power consumption in the overall circuit. The use of multi-bit architectures benefits the modulator with extra resolution, however, it increases the design complexity with more comparators required in the quantizer. Another issue comes from the non-linearity of the multi-bit DAC, which should be carefully compensated for in order to prevent performance degradation.

2.2.3 State of the Art of $\Sigma\Delta$Ms

According to previous subsections, we know that the selection of 3 parameters: the order of the modulator L, the resolution of the quantizer b_q and the oversampling ratio OSR affects the modulator's performance. Here, we analyse the architectures and design techniques of state of the art $\Sigma\Delta$Ms based on these 3 parameters, in order to achieve highest power efficiency (FOM).

For a fixed sampling frequency F_S, double sampling is a very attractive technique to obtain an equivalent sampling frequency $2F_S$. This solution boosts the operation speed of SC based integrators because op-amps are integrating charge on both phases [28]. Fig. 2.10 illustrates a double sampling integrator with 2 non-overlap clocks ϕ_1 and ϕ_2. It can be noticed that 2 groups of input sampling capacitors allows charge injection in both phases and keep op-amp busy all the time. Further, ADC architectures on the basis of doubling sampling methods increase the resolution, without consuming extra power. Unfortunately, several drawbacks limit the use of double sampling techniques. The first is that, considering the simplest implementation of double sampling integrator shown in Fig. 2.10, any mismatch between the 2 sampling capacitors gives rise to the folding of the power around $F_S/2$ on spectrum to the band of interest. This problem can be solved by adding an SC integrator with a fully floating input branch [29] or with a modified version reported in [30]. The other limitation is due to the timing constraint. Since the integrator uses both clock phases for charge injection, the quantization operation and the DEM technique should be performed between the gap of the non-overlap clocks. A good solution to solve this issue is to add 2 branches with one-unit-time delay in the modulator's architecture, as reported in [31].

The aforementioned double sampling techniques increase the OSR with a fixed L and q_b. The other way of enhancing ADCs performance is enlarge L with minimum number of op-amps, such as

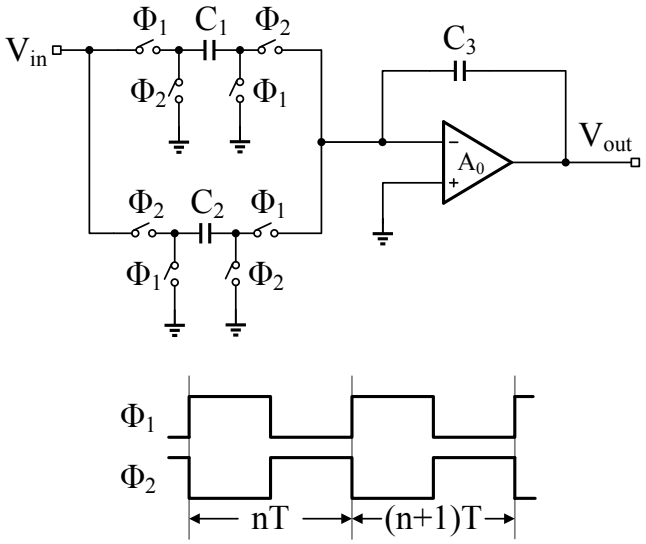

Figure 2.10 Schematic of a double sampling integrator implemented with SC circuits.

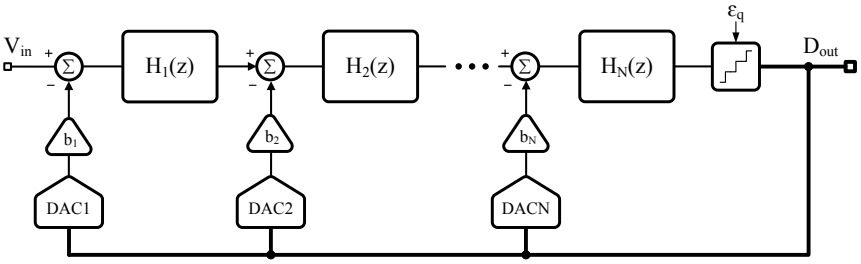

Figure 2.11 Nth-order ΣΔM with multiple feedback paths block diagram.

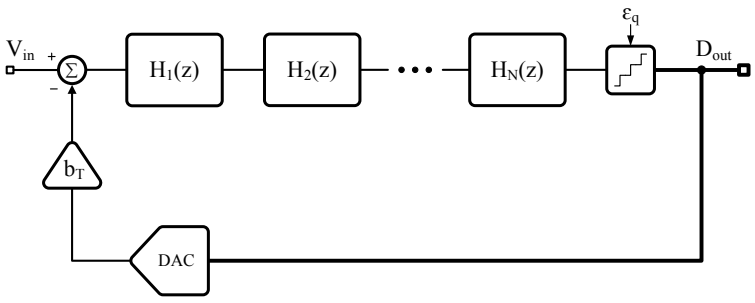

Figure 2.12 Nth-order ΣΔM without intermediate feedback paths block diagram.

the solution reported in [2]. Fig. 2.11 illustrated the block diagram of a general Nth-order ΣΔM with multiple feedback paths. Using the method proposed in [2], it is possible to remove all the intermediate feedback paths, giving rise to the scheme plotted in Fig. 2.12, where

$$b_T = b_1 + \frac{b_2}{H_1(z)} + ... + \frac{b_N}{H_1(z)H_2(z)...H_{N-1}(z)} \tag{2.14}$$

After removing the intermediate feedback paths, it is possible to combine N integrators to a single block, which can be expressed as

$$H_T = \frac{z^{-p}}{(1-z^{-1})^N} \tag{2.15}$$

where N is the number of integrators and p is the number of delays along the signal path. With this technique, a second-order ΣΔM using single op-amp was proposed in [32], which achieved a peak SNDR 63 dB over 1.94 MHz bandwidth. Recently, another op-amp reduction technique was presented in [1], in which a low-power SC third-order ΣΔ modulator using only one op-amp was proposed. The scheme employs swing reduction techniques so as to relax the requirements on the swing and slew-rate of all the internal nodes. Measurement results show that the modulator achieved 84 dB peak SNDR and 88 dB dynamic range over 100 kHz signal bandwidth. The total power consumption is 140 μW and corresponding FOM_W is 54 fJ/conv-step. In [33], a third-order DT ΣΔ modulator was proposed which uses two op-amps. The quantizer is realized on the basis of the traditional dual slope ADC, however, with a small modification in the discharging phase, a first-order quantization noise shaping is attained. In this case, a second-order loop filter using two op-amps together with a first-order quantizer forms the third-order ΣΔ architecture.

The resolution of quantizer b_q can also be boosted to increase the modulator's performance. In [34], a ΣΔ ADC using a noise-shaped two-step integrating quantizer was presented. The quantizer used in the scheme can attain 8-bit resolution and thus, the OSR is drastically reduced. The measurement results shows that the prototype achieved 70.7 dB peak SNDR at 80MHz F_S (OSR=8) and FOM_W is 280 fF/conv-step.

Innovation is in progress not only in architecture level, but also in the field of circuit design. For instance, the ΣΔM proposed in [35] utilizes class-C inverter instead of op-amp, hence, the required power consumption is significantly reduced. It was demonstrated that the prototype attained 81 dB peak SNDR over 20 kHz bandwidth. The power consumption is 36 μW from a 0.7 V supply and the FOM_W is 98 fJ/conv-step. Moreover, when ΣΔ architectures adopt op-amp based integrators, the output swing of op-amps should be minimized in order to relax the requirements on slew rate and bandwidth. In this case, the analog feed-foward (AFF) and digital feed-forward (DFF) techniques can be utilized, such as the ΣΔM reported in [36].

2.3 Incremental A/D Converters

Incremental ADCs are always used in instrumentation and sensing applications, such as readout of bridge transducers and biomedical acquisition systems [37][38]. The advantages of incremental ADCs are good linearity, high resolution, low offset and low power dissipation. Although sharing the same structures of ΣΔ modulators ($\Sigma\Delta Ms$), incremental ADCs reset the output of op-amps every N clock periods and provide a sample-to-sample conversion, thus they can be classified as Nyquist-rate data converters. This section begins with the basic operation of first-order and high-order incremental modulators, and then follows the discussion of incremental architectures using comparator

as quantizer and multi-bit quantization. Finally, state-of-the-art incremental ADCs' architectures and circuit techniques are introduced.

2.3.1 First-Order Incremental Converters

Incremental ADC comes from the combination of ΣΔM and dual-slope ADC, which was first presented by Van De Plassche in 1978 [39]. Fig. 2.13 shows the block diagram of a first-order incremental ADC. It is constituted of a delayed-integrator, a comparator and a 2-level DAC. The working principle is as follows: at the beginning of a conversion cycle, the output of the integrator is reset. For incremental ADCs, the frequency of input signal ranges from DC to few kHz at most, thus V_{in} can be regarded as constant $\overline{V_{in}}$. In each clock cycle, V_{in} subtracts V_{out} and the difference is accumulated at the output of integrator, where V_{out} is the analog version of the digital output D_{out}. Since a comparator is used in the modulator, D_{out} has two possible values. Whenever the input of the comparator goes above zero, D_{out} becomes 1, and the corresponding V_{out} is V_{ref}. Otherwise, D_{out} equals to -1 and $V_{out} = -V_{ref}$. At the end of the Nth clock period, the residue voltage at the output of integrator is

$$V_{res}(N) = \sum_{i=1}^{N-1} \overline{V_{in}} - \sum_{i=1}^{N-1} D_{out}(i)V_{ref} \tag{2.16}$$

where $-V_{ref} < V_{res}(N) < V_{ref}$ holds. This is ensured by the stability of the feedback loop. Thus, the input signal can be estimated as

$$\overline{V_{in}} = \frac{\sum_{i=1}^{N-1} D_{out}(i)V_{ref}}{N-1} + \frac{V_{res}(N)}{N-1} \tag{2.17}$$

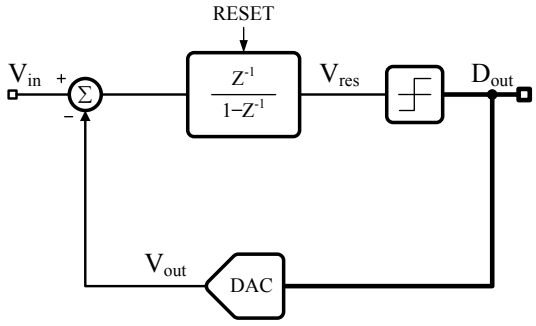

Figure 2.13 First-order incremental ADC block diagram.

As seen in (2.17), the first term of right-hand side is the digital estimation of $\overline{V_{in}}$. The quantization error is the second term, which is determined by the residue voltage of integrator $V_{res}(N)$ and the number of clock cycles per sample N. Here, ϵ_q is used to represent the quantization error as below

$$\epsilon_q = \frac{V_{res}(N)}{N-1} \tag{2.18}$$

The quantization error ϵ_q should be within half quantization interval V_{LSB}, thus

$$|\epsilon_q| < \frac{V_{LSB}}{2};\ V_{LSB} = \frac{V_{FS}}{2^{R_{1ord}}} \tag{2.19}$$

where $V_{FS} = 2V_{ref}$ is the full scale voltage and R_{1ord} is the maximum resolution that the first-order incremental scheme plotted in Fig. 2.13 can achieve. By using (2.16)-(2.20), the resolution of first-order incremental scheme can be derived as

$$R_{1ord} = \frac{V_{res}}{\max\{|\epsilon_q|\}} = log_2(N-1) \tag{2.20}$$

2.3.2 High-Order Incremental Modulators

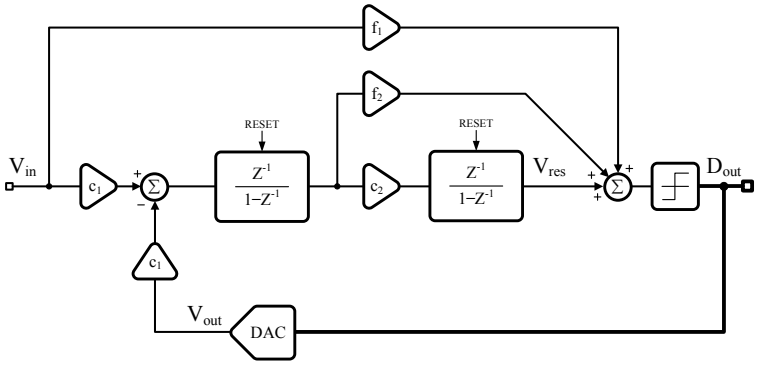

Figure 2.14 Second-order feed-forward incremental modulator block diagram.

Unfortunately, the conversion efficiency of a first-order incremental ADC is low. Methods for increasing the resolution are augmenting the number of clock periods N and using more effective schemes with cascaded accumulators. High-order incremental ADCs, therefore, contain multiple integrators with reset. The key point is to increase the accumulation efficiency, maintain the stability of structure and keep $V_{res}(N)$ minimized [16], [40]-[44].

In order to maintain stability of the loop filter, distributed feedback or feed-forward paths are usually used in incremental ADCs. Although the inaccurate feed-forward coefficients cause error along the accumulation path, it is just a gain factor since the input signal is almost constant. However, it is quite difficult to analyse the error due to the inaccurate feedback coefficients. This is because the feedback signal varies in time and injects signal in different locations. Based on the above analysis, for high-order incremental ADCs, the recommended way to maintain stability is to use multiple feed-forward paths and the adoption of more than 1 DAC should be prevented.

A conventional second-order incremental modulator is discussed here to show how the conversion efficiency changes compared with the first-order structure. As seen in Fig. 2.14, this structure contains 2 delayed-integrators. Along the accumulation path there are 2 coefficients c_1 and c_2. In order to keep the loop stable, two feed-forward paths are included with coefficients f_1 and f_2. This scheme also employs a comparator and 2-level DAC. Using the same method, $V_{res}(N)$ for this second-order architecture can be written as

$$V_{res}(N) = c_1c_2 \sum_{i=1}^{N-1} \sum_{j=1}^{i-1} \overline{V_{in}} - c_1c_2 \sum_{i=1}^{N-1} \sum_{j=1}^{i-1} D_{out}(i)V_{ref} \tag{2.21}$$

Similarly, the input signal can be represented as a digital estimation part and a quantization error as follows

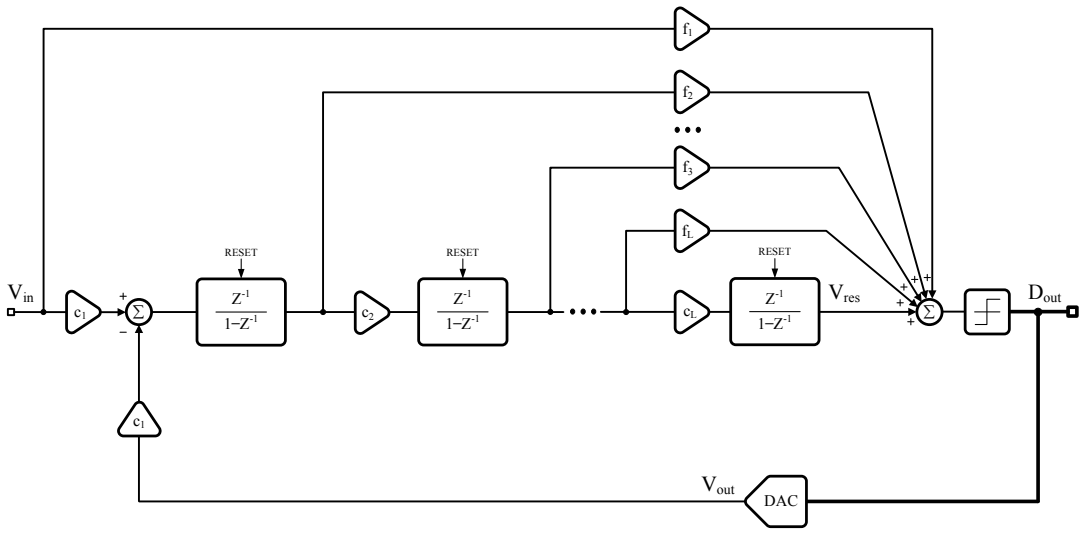

Figure 2.15 Lth-order incremental ADC architecture.

$$\overline{V_{in}} = \frac{c_1 c_2 \sum_{i=1}^{N-1} \sum_{i=j}^{i-1} D_{out}(i) V_{ref}}{M} + \frac{V_{res}(N)}{M} \tag{2.22}$$

where M is a constant which can be expressed as

$$M = \frac{c_1 c_2 (N-1)(N-2)}{2!} \tag{2.23}$$

Notice that M is a quadratic function of N. It means that the quantization error of second-order architecture can be much smaller than the counterpart of first-order scheme, provided a relative large N is used. The resolution of the second-order structure is derived as

$$R_{2ord} = log_2(M) = log_2 \frac{c_1 c_2 (N-1)(N-2)}{2!} \tag{2.24}$$

To compare the conversion efficiency of first-order and second-order incremental ADCs, (2.20) and (2.24) are used with $N = 1024$ and $c_{1,2} = 1$. The reason that c_1 and c_2 are chosen to be 1 is to simplify the situation. The stability is ensured with proper selection of f_1 and f_2. Both calculations and simulation results show that the first-order structure achieves a maximum resolution 10-bit, while the second-order architecture can obtain 19-bit.

An Lth-order incremental modulator with multiple feed-forward paths, feedback paths and coefficients is illustrated in Fig. 2.15. It consists of L delayed integrators, a comparator and a 2-level DAC. Along the accumulation path, there are L different coefficients $c_{1,2,...,L}$. Moreover, to maintain the stability of the loop filter, L feed-forward paths are introduced with coefficients $f_{1,2,...,L}$. In order to estimate the resolution of Lth-order incremental ADC, an equivalent model is plotted in Fig. 2.16. In this model, the feed-forward paths are removed since the purpose of them is to maintain stability and they do not affect the conversion efficiency. Using this model, it can be seen that during N clock periods, the difference between $c_1 V_{in}$ and $c_1 V_{out}$ is continuously injected at the input of the first integrator and

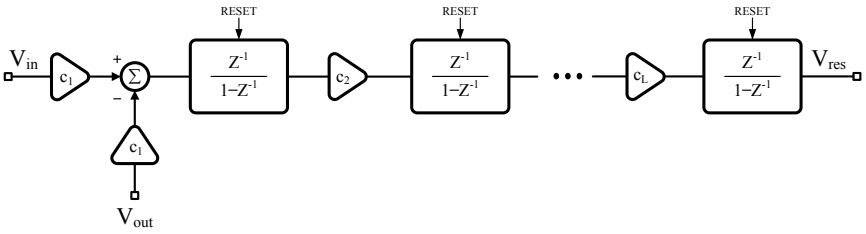

Figure 2.16 The equivalent model of Lth-order incremental ADC.

then accumulates though L integrators. Hence, at the end of N clock period, the final accumulation result can be expressed as

$$V_{res}(N) = c_1 c_2 ... c_L \sum_{i_1=1}^{N-1} \sum_{i_2=1}^{i_1-1} ... \sum_{i_L=1}^{i_{L-1}-1} \{\overline{V_{in}} - D_{out}(i_L) V_{ref}\} \tag{2.25}$$

Thus

$$\overline{V_{in}} = \frac{1}{M} c_1 c_2 ... c_L \sum_{i_1=1}^{N-1} \sum_{i_2=1}^{i_1-1} ... \sum_{i_L=1}^{i_{L-1}-1} D_{out}(i_L) V_{ref} + \frac{V_{res}(N)}{M} \tag{2.26}$$

where

$$M = c_1 c_2 ... c_L \frac{(N-1)(N-2)...(N-L)}{L!} \tag{2.27}$$

By combining (2.25)-(2.27), the resolution of Lth-order incremental converter can be written as

$$R_{Lord} = log_2 \frac{c_1 c_2 ... c_L (N-1)(N-2)...(N-L)}{L!} \tag{2.28}$$

2.3.3 Multi-Bit Incremental Converters

In general, the quantizer adopted in incremental ADCs is 2-level comparator, so as to avoid the non-linearity of multi-bit DAC due to the mismatch of unity elements. However, the drawback is that the output swing of integrators is large and may result in op-amps working in slewing mode. When the order of the scheme L is larger than 2, stability of the loop demands for the use of fractional coefficients along the accumulation path, which degrades the conversion efficiency. For example, in the third-order modulator described in [16], $c_1 = 0.5674$, $c_2 = 0.5126$, and $c_3 = 0.3171$. Using (2.28) with $N = 128$, the resolution is 14.9-bit, which is 3.4-bit less than the maximum achievable (with $c_{1,2,3} = 1$). Another case is the fourth-order modulator reported in [42]. Coefficients c_1, c_2, c_3 and c_4 are 0.25, 0.4, 0.22, and 0.11, respectively. With N=128, the achievable resolution is 14.6-bit while the maximum theoretical resolution is 23.3-bit. The resolution loss in this case is, hence, more than 8.7-bit.

On the contrary, incremental ADCs based on multi-bit quantization and DAC do not suffer from aforementioned problems. Nonetheless, the non-linearity of multi-bit DAC of incremental ADCs needs to be properly compensated for. For $\Sigma\Delta$Ms, static or dynamic calibration such as dynamic-element-matching (DEM) are effective ways to compensated for non-linearity of DAC. However, those methods are not suitable for incremental ADCs. To our best knowledge, very few papers studied this problem. As an alternative solution reported in [3], a second-order incremental structure uses a 3-bit intrinsic linear DAC and achieved 18-bit resolution.

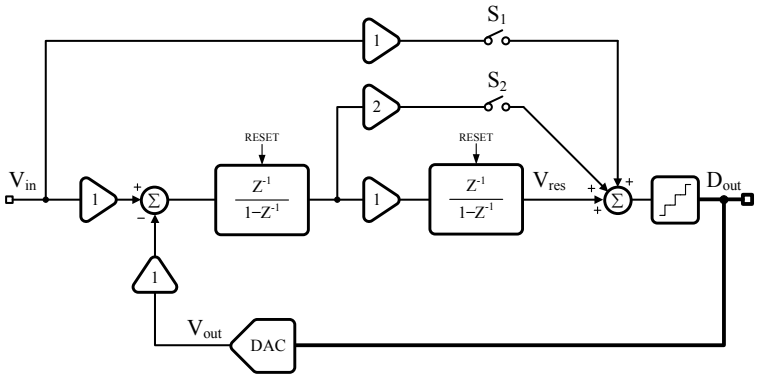

Figure 2.17 Second-order feed-forward multi-bit incremental ADC block diagram.

To begin with the discussion of multi-bit incremental ADCs, let us consider a second-order structure shown in Fig. 2.17. Compared with the scheme in Fig. 2.14, it can be noticed that the comparator and 2-level DAC are now replaced with multi-bit counterparts. Moreover, the coefficients are selected with values $c_{1,2} = f_1 = 1$ and $f_2 = 2$. To understand how the multi-bit DAC enhances the overall performance of the modulator, rewrite (2.21) to a multi-bit version

$$V_{res}(N) = \sum_{i=1}^{N-1}\sum_{j=1}^{i-1}\overline{V_{in}} - \sum_{i=1}^{N-1}\sum_{j=1}^{i-1} D_{out}(i)V_{refm} \tag{2.29}$$

$$V_{refm} = \frac{V_{FS}}{2^{b_q}} \tag{2.30}$$

where $D_{out} \in [-2^{b_q-1}, 2^{b_q-1}]$ and b_q is the resolution of the quantizer. Thus, $\overline{V_{in}}$ can be described as

$$\overline{V_{in}} = \frac{\sum_{i=1}^{N-1}\sum_{j=1}^{i-1} D_{out}(i)V_{refm}}{M} + \frac{V_{res}(N)}{M} \tag{2.31}$$

where

$$M = \frac{(N-1)(N-2)}{2!} \tag{2.32}$$

When comparing (2.23) ($c_{1,2} = 1$) and (2.32), it can be found that M for second-order structures with 2-level quantization and multi-bit quantizer are the same. It means that multi-bit quantization does not contribute extra bits performance, unless the residue voltage $V_{res}(N)$ can be further reduced. This can be solved by introducing 2 switches S_1 and S_2 in the scheme as plotted in Fig. 2.17. The operation principle is as follows: during the reset clock period, S_1 and S_2 are closed while the output of integrators are reset. From first to $(N-1)th$ clock period, the modulator works normally with S_1 and S_2 closed. At Nth clock period, S_1 and S_2 are opened. $V_{res}(N)$ is digitized by the multib-bit quantizer and the generated digital code is $D_{out}(N)$. Thus, a reduced version of residue voltage can be expressed as

$$\widehat{V_{res}} = V_{res}(N) - D_{out}(N)V_{refm} \tag{2.33}$$

Using (2.33), (2.31) can be reorganized as

$$\overline{V_{in}} = \frac{\sum_{i=1}^{N-1}\sum_{j=1}^{i-1} D_{out}(i)V_{refm}}{M} + (\frac{D_{out}(N)V_{refm}}{M} + \frac{\widehat{V_{res}}}{M}) \tag{2.34}$$

Since $-(1/2)V_{refm} < \widehat{V_{res}} < (1/2)V_{refm}$, by using (2.34), the resolution of the multi-bit second-order incremental modulator can be estimated as

$$R_{2ord} = log_2 \frac{(N-1)(N-2)}{2!} + b_q \tag{2.35}$$

According to (2.24) and (2.34), the resolution of second-order multi-bit incremental modulator increases b_q-bit with respect to the counterpart using a 2-level quantization and DAC.

In general, for an Lth-order incremental ADC with b_q-bit quantization and ideal DAC, the expected resolution is

$$R_{Lord} = log_2 \frac{c_1 c_2 ... c_L (N-1)(N-2)...(N-L)}{L!} + b_q \tag{2.36}$$

The above analysis shows that multi-bit incremental ADCs can boost the resolution with b_q-bit. Other advantages are 1) reduced swing of integrators leading to low-power design; 2) better stability giving rise to larger coefficients $c_{1,2,...,L}$ along accumulation path, which prevent degradation of conversion efficiency. Nonetheless, incremental ADCs using multi-bit quantization suffers from the non-linearity of multi-bit DAC and kT/C noise limitation, which will be discussed later in Chapter 3.

2.3.4 State of the Art of Incremental Converters

In order to obtain high resolution incremental ADCs, the order of the scheme L can be increased and the residue voltage V_{res} should be minimized. In 2006, a 22-bit third-order incremental modulator using 2-level quantization was reported in [16], whose scheme is the same as one plotted in Fig 2.15 with $L = 3$. To the best of author's knowledge, it is the incremental modulator which achieved highest resolution in the open literature up to date. Meanwhile, a fourth-order design was proposed in [42] and the obtained resolution is 16-bit.

To minimize V_{res}, a second-order incremental scheme with extended-range was report in [44]. The second-order architecture is the same as the one plotted in Fig. 2.14, while the second-stage is a 9-bit SAR modulator. The key point is that after the first-stage generates a coarse residue voltage V_{res}, the 9-bit SAR stage uses V_{res} to produce a refined residue voltage $\widehat{V_{res}}$ and a digital code. In this case, V_{res} is reduced and the performance of the modulator is improved. With the extended-range technique, the maximum achieved SNDR of the second-order modulator proposed in [44] is 86.3 dB and the FOM_W is 1.46 pJ/conv-step. Another technique which is able to reduce V_{res} and avoid using extra stage was reported in [46][47]. For example, the modulator proposed in [46] uses a 2-step conversion: the first-step is to use a conventional second-order feed-forward structure as illustrated in Fig. 2.14; the second-step is, however, to reconfigure the hardware to a first-order incremental scheme. Specifically, the second op-amp is configured as a voltage buffer to maintain V_{res} and the first op-amp is adopted to perform a first-order incremental operation. Compared with the aforementioned extended-range technique, the hardward reconfiguration technique is more efficient in terms of power consumption, however, at the expense of a lower output data rate.

In recent years, novel incremental architectures base on multi-bit quantization and DAC appear. As discussed previously, multi-bit incremental architectures benefit from better conversion efficiency and stability than schemes with 2-level DAC. Nonetheless, the non-linearity of multi-bit DAC needs to be properly compensated for. In [3], an intrinct 3-bit DAC is adopted to avoid non-linearity problem. The 3-bit DAC, however, uses a single capacitor and jnjects the charge at a speed of 8 times of sampling

frequency according to the digital output. Although the linearity of 3-bit DAC is guaranteed, the power dissipation of the second-order modulator is 6 mW. Another example can be seen in [45], where a third-order incremental architecture with a 5-level DAC was proposed. The modulator uses a foreground calibration mode to measure the mismatch of 4 unity capacitors. During normal conversion mode, the digital output is calibrated with the mismatch values in the digital domain. The obtained SNDR is 81.5 dB and the total power consumption is 6.7 mW.

Besides DT incremental ADCs, designs of CT counterparts are also in progress. A first-order CT incremental modulator is adopted to build a 16-channel neural interface, due to its implicit anti-aliasing filtering property [37]. Garcia extended the CT incremental converter to a third-order structure, which greatly enhances the conversion efficiency with respect to the first-order counterpart, giving rise to a design with peak SNDR 64 dB and 96 μW power consumption over 2 kHz bandwidth [38]. The low-power consumption is due to the requirement of bandwidth and slew-rate is more relaxed in CT ADCs than that of DT modulators.

Novelties of the designs mentioned above are mostly from architecture level. Aiming for low-power dissipation with good FOM, several novel circuit techniques are used in incremental ADCs published recently [25] [48]. For instance, an incremental modulator based on zoom ADC scheme was reported in [25], which achieved 20-bit resolution. To reduce the power consumption, traditional op-amp based integrators are replaced with inverter based counterparts, which gives rise to a total power consumption of $6.3\mu W$ and the best $FOM_S = 182.7dB$ up to now. In [48], a conventional second-order incremental structure is implemented with a self-timed technique instead of traditional synchronized clock scheme. The charge transfer circuits based on gated current source (GCS) and zero-crossing detector (ZCD) are utilized to replace the op-amp based integrators. This design obtained 14-bit resolution, which is relatively low compared with the already achieved performance using conventional schemes and circuit techniques. However, it is still a good trial in order to implement all digital incremental ADCs, especially with the continuously scaled CMOS technology.

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CHAPTER 3

DYNAMIC CONVERSION OF MISMATCH

The non-linearity of DAC is caused by the mismatch between unity elements, which affects the overall performance of the modulator. In this chapter, we first discuss the performance degradation of both incremental and $\Sigma\Delta$ ADCs due to the non-linearity of DAC and then the error correction methods. Regarding $\Sigma\Delta$ ADCs targeting to more than 12-bit resolution, the existing DEM methods can properly compensate for the non-linearity, such as data weighted averaging (DWA) [1] and segmented DEM [2]. In terms of incremental modulators, however, the already published error correction methods are not suitable when more resolution 18-bit resolution is required. In this chapter, a Smart-DEM algorithm appropriate for high resolution incremental modulators is presented. Theoretical analysis and simulation results of design examples demonstrate the effectiveness of the proposed method.

3.1 Effect of Mismatch and DEM Methods

In this section, we start with the study of kT/C noise limitation for both $\Sigma\Delta$ and incremental modulators, which determines the minimum capacitance of input sampling capacitor of ADCs. With this value, the matching accuracy of unity elements is estimated and consequently, the effect on the performance of modulators due to the mismatch in multi-bit DAC is investigated. Existing DEM methods are introduced in the last part of this section.

3.1.1 kT/C Noise Limitation

It is known that for DT modulators, the kT/C noise is uniformly distributed in the first Nyquist zone on the spectrum. With regard to ΣΔMs, the total power contributed by kT/C noise is significantly reduced due to a relatively large OSR, since the out-of-band noise does not need to be included. With mathematical calculation, the minimum input sampling capacitor of ΣΔMs can be estimated as

$$C_S = \frac{8kT}{V_{FS}^2 \times OSR} 10^{\frac{ENOB \times 6.02 + 1.76}{10}} \tag{3.1}$$

where ENOB is the expected resolution of the modulator and V_{FS} is the full scale voltage. The premise of (3.1) is that the quantization error of the modulator is not included in the total power of noise. For 12-bit ΣΔMs with V_{FS}=1.8 V and OSR=16, the estimated C_S is 16 fF. In such a case, the constraint of input sampling capacitor mainly comes from the matching accuracy of unity elements in multi-bit DAC.

Incremental modulators are always used to achieve more than 16-bit resolution. This results in the thermal noise, or kT/C noise in a discrete-time (DT) system, becomes dominant contributor among quantization noise and other noise sources in circuits or systems. In this case, C_S should be large enough to suppress kT/C noise. For instance, considering a single-ended implementation of the second-order incremental modulator as depicted in Fig. 2.17. In each clock cycle, the noise injected on the input sampling capacitor is $2kT/C_S$. After N clock periods, the total noise power accumulated at V_{res} node can be described as follows

$$V_{n,tot}^2 = \frac{2kT}{C_S} \sum_{i=1}^{N-2} i^2 \tag{3.2}$$

Therefore, the input referred noise of the second-order modulator can be derived as

$$V_{n,in}^2 = \frac{V_{n,tot}^2}{G_{2ord}^2} \tag{3.3}$$

where G_{2ord} is the gain for the input signal and can be represented by $(N-1)(N-2)/2$. In order to achieve R_{2ord} resolution, $V_{n,in}$ should be less than half V_{LSB}, which gives rise to

$$C_S > \frac{8kT \sum_{i=1}^{N-2} i^2}{G_{2ord}^2 V_{LSB}^2}; V_{LSB} = \frac{V_{FS}}{2^{R_{2ord}}} \tag{3.4}$$

Following (3.4), $R_{2ord} = 18, N = 256, V_{FS} = 3.3V, q_b = 3$ and corresponding $V_{LSB} = 12.6\ \mu V$ are chosen as an example. The calculated minimum C_S is 1.1 pF. Using this value, we can estimate the matching accuracy between unity elements in the 3-bit DAC. For the modern 0.18 μm CMOS technology, the typical 3σ matching accuracy of MIM capacitors is below 1.5% and the capacitance density is $2fF/um^2$. However, to keep some margin when considering the parasitic capacitance in real circuit implementation, a relatively larger 3σ matching accuracy is chosen which is 2.0%. The size of unity capacitor in 3-bit DAC is $8.3\mu m \times 8.3\mu m$ and thus, the corresponding 3σ matching accuracy is 0.25%.

3.1.2 Mismatch Effect for ΣΔ ADCs

To study the effect of mismatch for ΣΔMs, the second-order feed-forward architecture is utilized as illustrated in Fig. 3.1. This scheme is similar to the one plotted in Fig. 2.17, however, without the reset

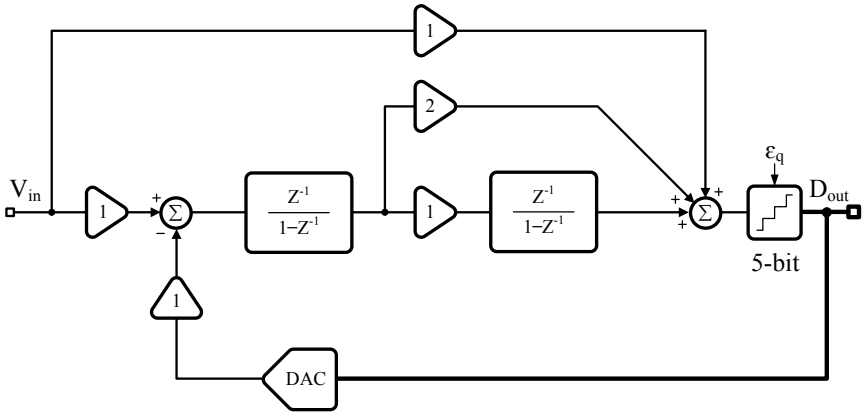

Figure 3.1 Second-order 5-bit feed-forward $\Sigma\Delta$ ADC block diagram.

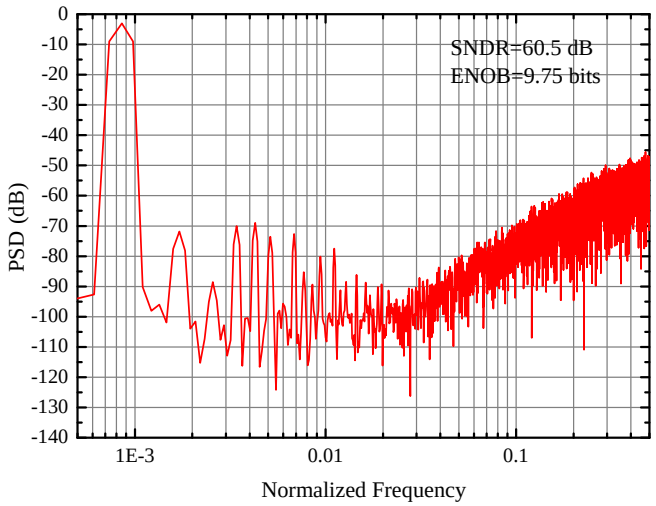

Figure 3.2 PSD (8096-point FFT) with σ=1.0% mismatch for 32 unity elements of DAC. The input signal is a sinusoid waveform at normalized frequency $8.54 \cdot 10^{-4}$ whose amplitude is -3 dB_{FS}. The OSR is 16.

signal of integrators. The quantizer is 5-bit and thus 32 unity elements are contained in the DAC. The mismatch between unity elements are modelled as a random variable which obeys normal distribution with zero mean and variance equal to σ.

Ideally when there is no mismatch between the unity elements, the achieved SNDR with behavioural simulation is 76.4 dB (ENOB = 12.39-bit). Fig. 3.2 shows the PSD of D_{out} using 8096 points FFT with $\sigma = 1.0\%$ mismatch. The achieved SNDR is 60.5 dB which is equal to 9.75-bit resolution. The resolution loss compared with the ideal case is 2.64-bit. In order to reduce the performance degradation, the mismatch between unity elements is reduced to $\sigma = 0.1\%$. The same behavioural simulation is performed and the the result is illustrated in Fig. 3.3. The attained SNDR is 74.9 dB (12.15-bit) and the resolution loss compared with that in ideal case is 1.5 dB (0.24-bit).

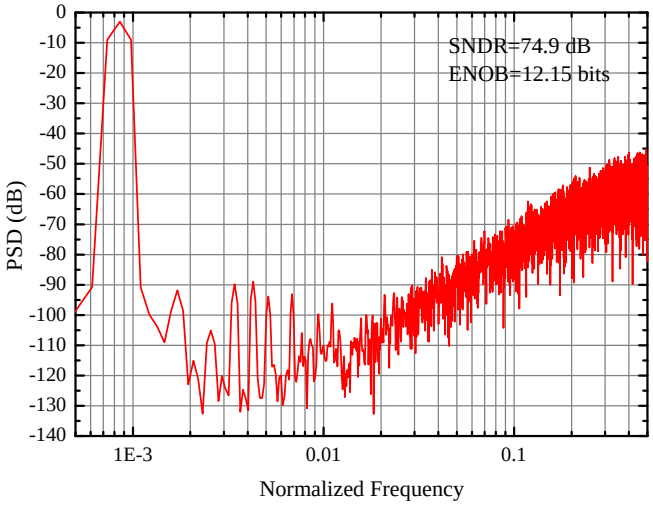

Figure 3.3 PSD (8096-point FFT) with σ=0.1% mismatch for 32 unity elements of DAC. The input signal is a sinusoid waveform at normalized frequency $8.54 \cdot 10^{-4}$ whose amplitude is -3 dB_{FS}. The OSR is 16.

3.1.3 Mismatch Effect for Incremental Modulators

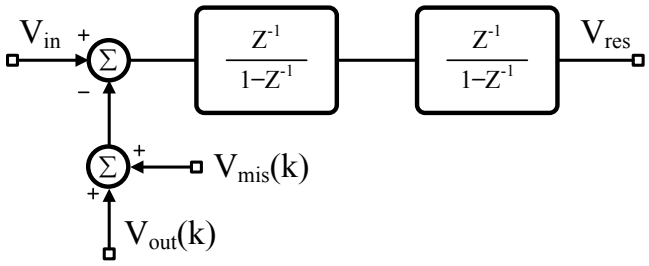

Figure 3.4 Equivalent model of second-order incremental ADC with non-ideal multi-bit DAC.

To investigate the mismatch effect of incremental modulators, the second-order architec-ture is adopted as illustrated in Fig. 2.17. Previously, we demonstrated that quantization error can be estimated with (2.34). However, it is the ideal case. In reality, the mismatch between unity elements in multi-bit DAC results in a larger INL and DNL than those obtained under the ideal situation. Here, we utilize an equivalent model of the second-order structure with non-ideal multi-bit DAC, which is shown in Fig. 3.4. Suppose the resolution of DAC is b_q-bit, the number of unity elements is therefore $N_u = 2^{q_b}$. As illustrated in Fig. 3.4, the DAC provides 2 feedback signals in the kth clock period: one is $V_{out}(k)$, the ideal analog version of $D_{out}(k)$; the other one is $V_{mis}(k)$, which is the total error injected due to mismatch and can be described as

$$V_{mis}(k) = 2V_{refm} \sum_{i=1}^{N_u} \epsilon_i D_{out}(i,k) \tag{3.5}$$

where $\epsilon_i (i = 1, 2, ..., N_u)$ are the values of mismatch (in percentage) and $D_{out}(i, k)(i = 1, 2, ..., N_u)$ is the digital code of ith-bit of $D_{out}(k)$. Since incremental ADCs use several integrators along the signal path, an error injected at the beginning of a conversion generally has a larger accumulation than the error injected near the end of the conversion. Thus, the weights $W(k)(k = 1, 2, ..., N)$ are introduced to indicate the amplification of an error injected at kth clock period. Consequently, the total error appears at V_{res} at the end of Nth clock period is

$$V_{mis} = \sum_{k=1}^{N} V_{mis}(k) \times W(k) \tag{3.6}$$

Combining (3.5) and (3.6), we have

$$V_{mis} = V_{refm} \sum_{i=1}^{N_u} \epsilon_i W_i \tag{3.7}$$

where $W_i (i = 1, 2, ..., N_u)$ are the total accumulated weight corresponding to $\epsilon_i (i = 1, 2, ..., N_u)$ after a full conversion cycle (N clock periods). Using (3.7), rewrite (2.34) and $\overline{V_{in}}$ can be expressed as

$$\begin{aligned} \overline{V_{in}} =& \frac{\sum_{i=1}^{N-1} \sum_{j=1}^{i-1} D_{out}(i) V_{refm}}{M} + \frac{D_{out}(N) V_{refm}}{M} \\ &+ \frac{\widehat{V_{res}} + V_{mis}}{M} \end{aligned} \tag{3.8}$$

Consequently, the resolution of second-order incremental converter can be estimated

$$R_{2ord} = log_2 \frac{MV_{ref}}{max\{\widehat{V_{res}} + V_{refm}\epsilon_{tot}\}};\ \epsilon_{tot} = \sum_{i=1}^{N_u} \epsilon_i W_i \tag{3.9}$$

As seen in (3.9), the achievable resolution of the second-order incremental ADC illustrated in Fig. 2.17 depends on the ϵ_{tot} term. In Section 3.3, behavioural simulations will show how this term affects the modulator's performance, when different digital error correction methods are utilized.

3.1.4 Dynamic-Element-Matching Techniques

The dynamic-element-matching technique is well known with the function to convert mismatch associated with multi-bit DAC into shaped noise. As a result, the power of the noise that remains in the signal band is low. The first DEM technique was reported in [3]. By selecting the DAC elements randomly, the SFDR is improved. However, the noise introduced by the mismatch of elements is white and spreads over the entire spectrum. The data weighted averaging (DWA) algorithm was later presented in [1]. The main operation principle of DWA is to use the elements of DAC with a cyclical order. In this case, the noise associated with the mismatch is high-pass shaped by a first-order NTF. Unfortunately, the DWA suffers from in-band tones. Some modified DWA techniques and other DEM technique such as tree structured DEMs are proposed afterwards [2], [4]-[7]. In summary, most existing DEM techniques reduce the spurious tones by spreading the power over the spectrum, however, at the cost of increased noise floor.

For $\Sigma\Delta$Ms aiming for 12-bit or more resolution, the aforementioned methods such as DWA [1] and segmented DEM [2] are good solutions. However, since incremental modulators belong to Nyquist-rate data converter, the requirement of achieving good resolution is to provide accurate sample-to-sample

conversion, rather than to obtain good noise shaping. For incremental modulators, the weight of signal injected at the beginning of the conversion is larger than the weight of that injected close to the end of the conversion. Thus, conventional DWA algorithm can not properly compensate for the error caused by mismatch. In the next section, a Smart-DEM algorithm for high-order multi-bit incremental ADCs is proposed, which is able to achieve a near-ideal compensation even for a large mismatch. Behavioural simulation results and comparison between conventional DEMs and Smart-DEM are given in Section 3.3.

3.2 Smart-DEM Algorithm

In this section, the working principles of Smart-DEM algorithm are described. Generally, for a q_b-bit DAC without extra levels, the summation of mismatch of all the unity elements is zero (otherwise it can be regarded as a gain factor), which means

$$\sum_{i=1}^{N_u} \epsilon_i = 0;\ N_u = 2^{q_b} \tag{3.10}$$

According to (3.7) and (3.10), it can be noticed that if the weights of the mismatch were well balanced, the total error ϵ_{tot} could be reduced. The ideal case is that, if all the weights W_i are equal, ϵ_{tot} becomes 0. However, as discussed before, this is not an easy task with conventional DEM techniques. The weight of error depends on the time when the signal is injected. For second-order structure, the weight of error is a linear function with respect to the time of signal injection. If the modulator is third-order scheme, the weight becomes quadratic function versus time so forth.

In order to balance the weights of error, a Smart-DEM algorithm is proposed. The key point of this algorithm is that, during N clock periods, Smart-DEM algorithm balances the W_i $(i = 1, 2, ..., N_u)$, thus minimizing ϵ_{tot} $(i = 1, 2, ..., N_u)$. Before describing the operation principles of Smart-DEM algorithm, we first introduce the estimation of 2 important parameters — $V_{mis}(k)$ and $W(k)$.

3.2.1 Multi-Bit DAC and Mismatch

For the sake of simplicity, we begin the discussion with second-order incremental scheme illustrated in Fig. 2.17. Behavioural simulation results show that with ideal 3-bit quantization, the swing of DAC is $1.25V_{ref}$. It means that 2-extra levels needs to be added, thus, the number of unity elements in DAC is $N_u = 10$. According to (2.24), the number of clock periods N is chosen to be 256, so as to obtain 18-bit resolution.

Fig. 3.5 plots the conventional single-ended implementation of the first integrator and 3-bit DAC with switched-capacitor circuits. Notice the DAC contains 10 capacitors with equal nominal value C_u and $D_{out}[10 : 1]$ is the digital output of the modulator in a thermometrical fashion. The mismatch of unity capacitors in DAC can be represented with $\epsilon_i (i = 1, 2, ..., 10)$. Tab. 3.1 shows the relationship between $D_{out}[10 : 1]$ and the corresponding error cause by the mismatch of 10 unity capacitors. As seen in Tab. 3.1, the first column shows the 11 possible thermometrical codes of $D_{out}[10 : 1]$. The second column illustrates the related error caused by mismatch corresponding to a certain input code. It can be noticed that ϵ_i has both positive and negative signs, and it is not good from circuit implementation point of view. By using (3.10), the negative signs can be transformed to the complementary counterparts and this is shown in the last column.

For example, when the second-order modulator generates a digital output $D_{out}[10 : 1] = 0000000011$, it means that the control signals for 8 capacitors are negative and for the other 2 capacitors

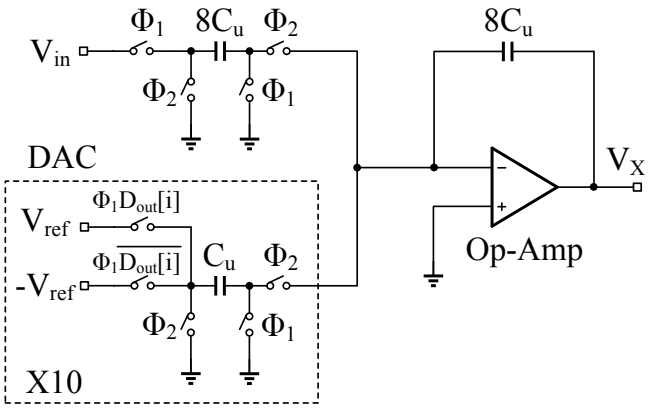

Figure 3.5 Conventional implementation of the first integrator and 3-bit DAC (11 levels).

Table 3.1 The relationship between $D_{out}[10:1]$ and $V_{mis}(k)$ for conventional DAC.

$D_{out}[10:1]$	$V_{mis}(k)$	$V_{mis}(k)$ with (3.10)
1111111111	$V_{refm}\sum_{i=1}^{10}\epsilon_i$	0
0111111111	$V_{refm}(\sum_{i=1}^{9}\epsilon_i-\epsilon_{10})$	$2V_{refm}\sum_{i=1}^{9}\epsilon_i$
0011111111	$V_{refm}(\sum_{i=1}^{8}\epsilon_i-\sum_{i=9}^{10}\epsilon_i)$	$2V_{refm}\sum_{i=1}^{8}\epsilon_i$
0001111111	$V_{refm}(\sum_{i=1}^{7}\epsilon_i-\sum_{i=8}^{10}\epsilon_i)$	$2V_{refm}\sum_{i=1}^{7}\epsilon_i$
0000111111	$V_{refm}(\sum_{i=1}^{6}\epsilon_i-\sum_{i=7}^{10}\epsilon_i)$	$2V_{refm}\sum_{i=1}^{6}\epsilon_i$
0000011111	$V_{refm}(\sum_{i=1}^{5}\epsilon_i-\sum_{i=6}^{10}\epsilon_i)$	$2V_{refm}\sum_{i=1}^{5}\epsilon_i$
0000001111	$V_{refm}(\sum_{i=1}^{4}\epsilon_i-\sum_{i=5}^{10}\epsilon_i)$	$2V_{refm}\sum_{i=1}^{4}\epsilon_i$
0000000111	$V_{refm}(\sum_{i=1}^{3}\epsilon_i-\sum_{i=4}^{10}\epsilon_i)$	$2V_{refm}\sum_{i=1}^{3}\epsilon_i$
0000000011	$V_{refm}(\sum_{i=1}^{2}\epsilon_i-\sum_{i=3}^{10}\epsilon_i)$	$2V_{refm}\sum_{i=1}^{2}\epsilon_i$
0000000001	$V_{refm}(\epsilon_1-\sum_{i=2}^{10}\epsilon_i)$	$2V_{refm}\epsilon_1$
0000000000	-$V_{refm}\sum_{i=1}^{10}\epsilon_i$	0

are positive. For a conventional DAC plotted in Fig. 3.5, the total positive voltage injected is $v_{refm}\sum_{i=1}^{2}(1+\epsilon_i)$ and the negative voltage is $-v_{refm}\sum_{i=3}^{10}(1+\epsilon_i)$. With (3.10), the negative voltage can be converted to positive equivalent, which is shown in the third column in Tab. 3.1. Thus, the total positive voltage injected with $D_{out}[10:1]=0000000011$ is $-(3/4)V_{ref}+2V_{refm}\sum_{i=1}^{2}\epsilon_i$.

Fig. 3.6 illustrates the schematic of an integrator with a bipolar DAC. The benefit of a bipolar DAC is that it can achieve the same function as a conventional DAC does, with only half number of unity elements. The working principle of the bipolar DAC is as follows: the digital input $D_{out}[10:1]$ is encoded to generate control signals $A[5:1]$ and $B[5:1]$, as illustrated in Tab. 3.2. Since the left side of the capacitor C_u is connected to positive or negative references either during ϕ_1 or ϕ_2, the digital controls $A[5:1]$ and $B[5:1]$ can give rise to positive, negative or null injection. By employing (3.10), the negative signs can be removed with complementary code and it is shown in the last column in Tab. 3.2.

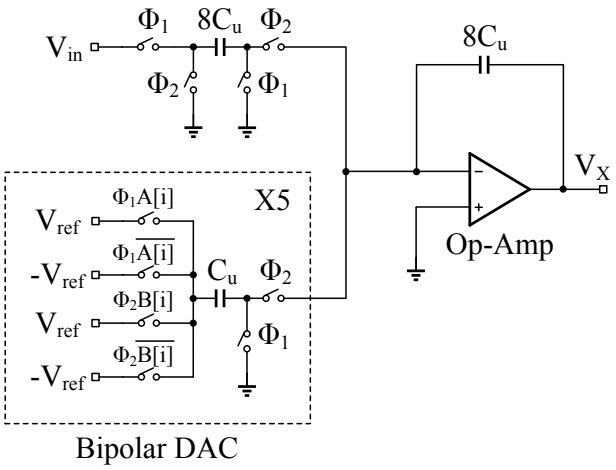

Figure 3.6 First integrator and 11-level bipolar DAC implementation.

Table 3.2 The relationship between $D_{out}[10:1]$ and $V_{mis}(k)$ for bipolar DAC.

$D_{out}[10:1]$	$A[5:1]$	$B[5:1]$	$V_{mis}(k)$	$V_{mis}(k)$ with (3.10)
1111111111	11111	00000	$2V_{refm}\sum_{i=1}^{5}\epsilon_i$	0
0111111111	11111	10000	$2V_{refm}\sum_{i=1}^{4}\epsilon_i$	$2V_{refm}\sum_{i=1}^{4}\epsilon_i$
0011111111	11111	11000	$2V_{refm}\sum_{i=1}^{3}\epsilon_i$	$2V_{refm}\sum_{i=1}^{3}\epsilon_i$
0001111111	11111	11100	$2V_{refm}\sum_{i=1}^{2}\epsilon_i$	$2V_{refm}\sum_{i=1}^{2}\epsilon_i$
0000111111	11111	11110	$2V_{refm}\epsilon_1$	$2V_{refm}\epsilon_1$
0000011111	11111	11111	0	0
0000001111	00000	00001	$-2V_{refm}\epsilon_1$	$2V_{refm}\sum_{i=2}^{5}\epsilon_i$
0000000111	00000	00011	$-2V_{refm}\sum_{i=1}^{2}\epsilon_i$	$2V_{refm}\sum_{i=3}^{5}\epsilon_i$
0000000011	00000	00111	$-2V_{refm}\sum_{i=1}^{3}\epsilon_i$	$2V_{refm}\sum_{i=4}^{5}\epsilon_i$
0000000001	00000	01111	$-2V_{refm}\sum_{i=1}^{4}\epsilon_i$	$2V_{refm}\epsilon_5$
0000000000	00000	11111	$-2V_{refm}\sum_{i=1}^{5}\epsilon_i$	0

3.2.2 The Weight of Error for Multi-Bit DAC

In order to compensate for the error generated from multi-bit DAC, the number of its accumulation for a certain incremental modulator during N clock cycles should be calculated. For second-order incremental converter, if the error from DAC enters at kth $(1 \leq k \leq N)$ period after the reset, the error is stored though the first integrator with one clock period delay, then it is accumulated as a linear function on the second integrator. Thus, the weight of the error caused by mismatch in kth clock period is

$$W_{2ord}(k) = N - k - 1 \tag{3.11}$$

Regarding third-order incremental modulators (3 integrators with unit time delay), if an error from DAC enters at $kth(1 \leq k \leq N)$ clock period after the reset, the error is stored at the output of the first integrator. The second integrator accumulates the error linearly. After that, a quadratic accumulation of this error is achieved with the third integrator. In this case, the weights can be estimated as

$$W_{3ord}(k) = \frac{(N-k-1)(N-k-2)}{2!} \tag{3.12}$$

In general, for Lth-order incremental converter described in Fig. 2.15, the weights can be expresse as

$$W_{Lord}(k) = \frac{(N-k-1)(N-k-2)...(N-L)}{L!} \tag{3.13}$$

3.2.3 The Principle of Smart-DEM Algorithm

The idea of Smart-DEM algorithm is to dynamically balance the weights of error along the data conversion of N clock periods for one sample. The detailed operation is described below:

► **Step 1**: before starting a new conversion cycle, reset the total weights of all the elements W_i $(i = 1, 2, ..., N_u)$ to zero.

► **Step 2**: in each clock cycle, select the unity elements with the minimum weight. If it is the last clock period, jump to Step 4.

► **Step 3**: calculate the weight of current clock period $W(k)$ $(k = 1, 2, ..., N)$ and update the weights of the selected elements, then go back to Step 2.

► **Step 4**: finish the conversion cycle.

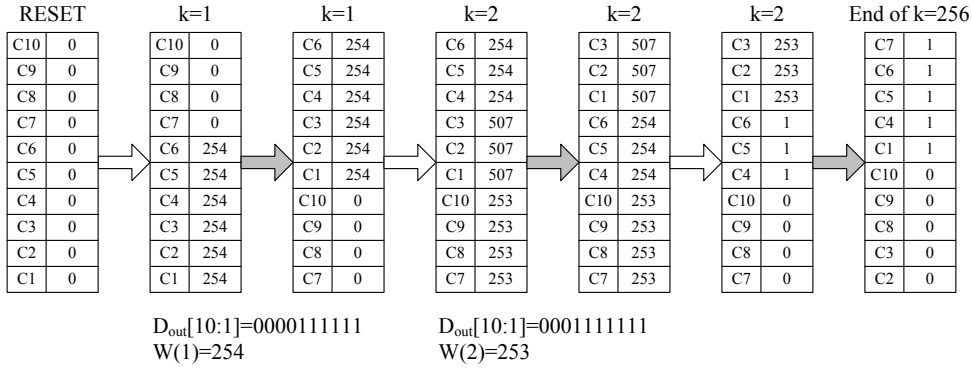

Figure 3.7 The status of the weights in Smart-DEM with $V_{in} = 0.305V_{ref}$.

The following is an example to explain how the Smart-DEM algorithm works. Fig. 3.7 shows accumulated weights of unity elements with respect to clock period. Before the data conversion starts, the weight of each element is reset to 0. In first clock period, $D_{out}[10:1] = 0000111111$ and the decimal value is 6 (the decimal value of $D_{out}[10:1]$ is from 0 to 10, with a common mode value 5). By using Tab. 3.1, we know that the total error caused by mismatch is $2V_{refm}\sum_{i=1}^{6}\epsilon_i$. According to the Smart-DEM algorithm, 6 unity elements with the minimum weights should be chosen and the corresponding weight needs to be updated. Therefore, unity elements C1-C6 are selected. Regarding to (3.11), the associated weight is calculated as 254. This value is added to the existing weight of C1-C6. After that, the weight array is sorted and the larger values are moved at the top of the stack.

In second clock period, $V_{in}[10:1] = 0001111111$ and decimal number is 7. Similarly, 7 elements with the minimum weight are selected which are C4-C6 and C7-C10. However, the corresponding weight of this clock period changes to 253. This value is again added to the current weights of these elements. After sorting algorithm, the minimum weight in the array is subtracted from all weights in case of hardware overflow. This is because the word length of weights is limited in real circuit. Finally, after 256 clock periods, the $W_i(i = 1, 2, ..., 10)$ is no more than 1 and the total effect of the mismatch is negligible.

3.3 Design Examples and Simulation Results

In this section, high-order incremental architectures utilizing Smart-DEM algorithm are discussed. Design guidelines from circuit implementation point of view are given in order to achieve low power design and maintain stability of the structure. Two design examples for second-order and third-order incremental converters are detailed explained and behavioural simulation results demonstrate the effectiveness of Smart-DEM algorithm.

3.3.1 Design Consideration of Employing Smart-DEM Algorithm

In order to design high-resolution low power incremental converter using Smart-DEM algorithm, design guidelines are given as below

1. The output swing of integrators should be minimized to improve the linearity of the op-amps, as well as to reduce the number of comparators in the quantizer.
2. The coefficients along the accumulation path should not degrade the overall performance of the modulator.
3. The input referred kT/C noise should be suppressed to be comparable with quantization counterpart. The input sampling capacitance should be affordable, otherwise, increase the number of clock periods N to lower kT/C noise.
4. There should be only one feedback path in which a DEM algorithm (e.g. Smart-DEM) can be effectively used.

The guideline 1) considers how to achieve low-power dissipation of the analog circuit. Item 2) results in easier implementation of the analog coefficients and avoids performance degradation. The guideline 3) explains the limitation due to kT/C noise and the corresponding noise reduction methods. The purpose of last item is to reduce the complexity of digital block, which is used to compensated for the mismatch of the multi-bit DAC. By adopting these guidelines, second-order and third-order design examples are discussed in the following subsections.

3.3.2 Second-Order Incremental Modulator Example

As previously mentioned, the second-order architecture illustrated in Fig. 2.17 is the first design example, which is plotted again in Fig. 3.8. It can be noticed that D_{out} is encoded in a Smart-DEM block and the generated control signals are then used to select proper unity elements in 3-bit DAC. This structure was previously used in both $\Sigma\Delta$ converter and incremental modulators [8][9]. The advantage of this structure is that due to the feed-forward paths, the swing of both op-amps are reduced. However, the incremental converter presented in [9] employs 2-level DAC and an extended stage to reduce the

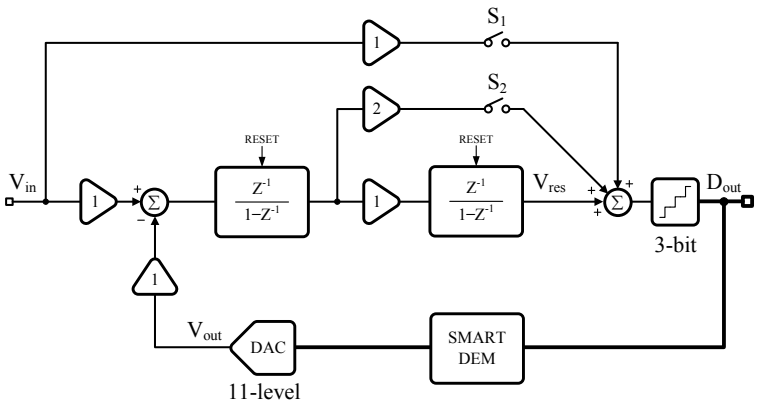

Figure 3.8 Second-order 3-bit feed-forward incremental architecture with Smart-DEM block.

residue voltage V_{res}. Here, this second-order architecture is used to explain the design of multi-bit incremental converter assisted by Smart-DEM algorithm.

In Section 3.2, we mentioned that for 3-bit quantization, the swing of DAC is $1.25V_{ref}$ and thus 10 unity capacitors are used. Moreover, the 3-bit quantizer demands for 10 comparators instead of 8. With $N = 256$, the number of levels of digital output is 259080, corresponding to 17.98-bit resolution. By extensive behavioural level simulations, the swing of the first op-amp is below $0.25V_{ref}$. For the second op-amp, the swing is within $0.125V_{ref}$. In this case, the power consumption of op-amps can be significantly reduced. Regarding to the Smart-DEM realization, the number of standard cells after synthesis is below $1.5k$ with $C_u = 10$ and $N = 256$. This number can be further reduced when a bipolar DAC is utilized. With modern CMOS technologies, the power consumption of Smart-DEM block is insignificant, especially when the power supply of digital block is low.

To demonstrate the effectiveness of Smart-DEM algorithm, 2 groups of simulations are performed. Design parameters $N = 256, b_q = 3$ and $V_{FS} = 3.3$ are selected. In the first group, the mismatch obeys a normal distribution with $\mu = 0$ and $\sigma = 0.08\%$. Fig. 3.9 illustrates the performance comparison of the same second-order scheme in three different cases: mismatch of unity elements not compensated for, assisted with conventional DWA method, and compensated for with the Smart-DEM algorithm. The input is a constant voltage ranging from -V_{ref} to V_{ref}. As seen in Fig. 3.9, the maximum INL with no compensation is about 101 LSB. When using DWA, the maximum INL is reduced to 0.9 LSB. The Smart-DEM is able to keep the error within 0.5 LSB for entire range. In this case, although DWA can guarantee a good performance if half-bit resolution loss is allowed, Smart-DEM is able to fully compensate for the mismatch and achieved near-ideal performance.

Moreover, it is useful to compare the performance of different DEMs when a larger mismatch is given. Fig. 3.10 illustrate the performance comparison when the mismatch obeys $\mu = 0$ and $\sigma = 0.8\%$. The maximum INL without DEM algorithm is 1019.6 LSB and for DWA is 4.3 LSB. However, with the compensation of Smart-DEM algorithm, the maximum INL is still limited within 0.5 LSB over the entire input range.

Fig. 3.11 shows the weight accumulation of 10 unity elements of 3-bit DAC of the second-order architecture illustrated in Fig. 3.8. Since 10 curves overlap with each other and the difference is difficult to observe, only the last 50 clock periods are plotted here. The input signal is $0.123V_{ref}$. At the end of the conversion, the maximum weight is 17786 while the minimum one is 17784. The

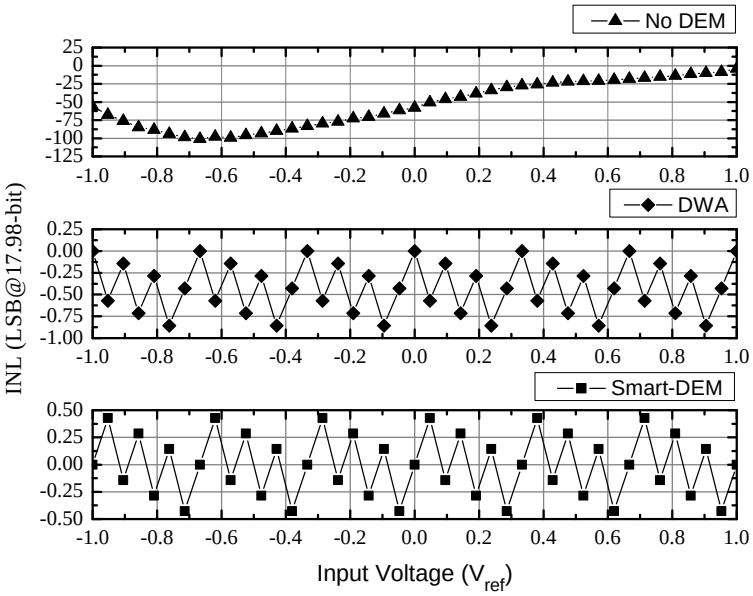

Figure 3.9 Resolution comparison for second-order incremental converter without DEM (top), with DWA (middle) and with Smart-DEM (bottom). The mismatch of unity elements obeys normal distribution with $\mu = 0$ and $\sigma = 0.08\%$.

weights for all the elements converge to the same level with a maximum difference of 2, which results in a negligible residual error.

3.3.3 Third-Order Incremental Modulator Example

The second design example is a third-order incremental converter illustrated in Fig. 3.12. In order to compare the conversion efficiency between the third-order structure and second-order scheme, the target resolution is also selected to be 18-bit. This structure is similarly to the architectures published in [10][11]. None the less, several features are included to convert it into a high-resolution multi-bit incremental modulator.

Firstly, the use of multi-bit quantizer and DAC benefits the modulator extra bits resolution and reduces the swing of op-amps. The second point is that several feed-forward paths are added to maintain the stability of structure while the coefficients along the integration path do not degrade the overall performance. In order to lower the swing of the first op-amp, coefficient 0.5 and 2 are introduced at the input of first and second integrators. Finally, a quantized version of V_{in} is added to D_{out}, which means that the amplitude of the real input signal is reduced to less than half quantization interval of the quantizer. However, this is at the cost of increased swing of multi-bit DAC. According to (2.28), in order to achieve 18-bit resolution, design parameters $N = 61$ and $q_b = 3$ and $V_{FS} = 3.3V$ are selected. The input sampling capacitance is calculated to be 6.37 pF (Appendix A) and the corresponding matching accuracy is around $3\sigma = 0.1\%$. The scheme is simulated on behavioural level with a full scale 273760, which is equivalent to 18.06-bit resolution. By sweeping the amplitude of input signal, the swing of all three op-amps is below $0.25V_{ref}$. Nevertheless, the output of the DAC is 75% more than the full scale, thus the DAC needs 6 extra levels and the total levels of DAC is 15.

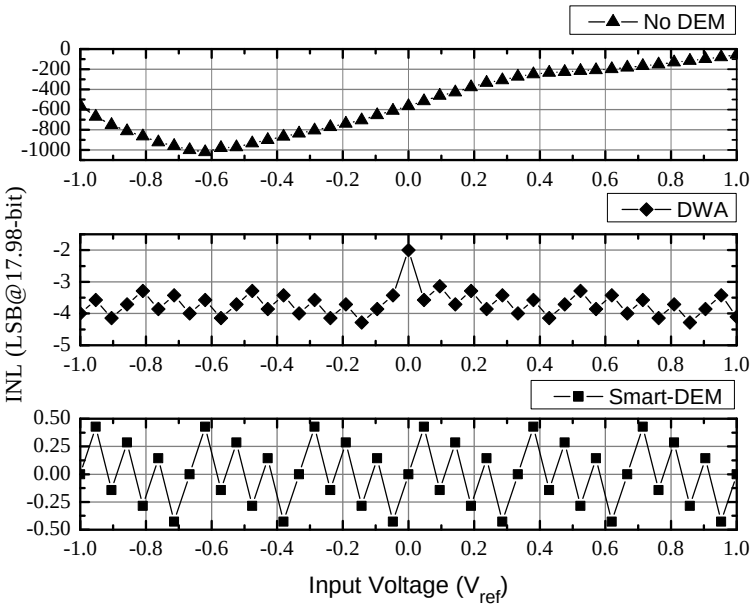

Figure 3.10 Resolution comparison for second-order incremental converter without DEM (top), with DWA (middle) and with Smart-DEM (bottom). The mismatch of unity elements obeys normal distribution with $\mu = 0$ and $\sigma = 0.8\%$.

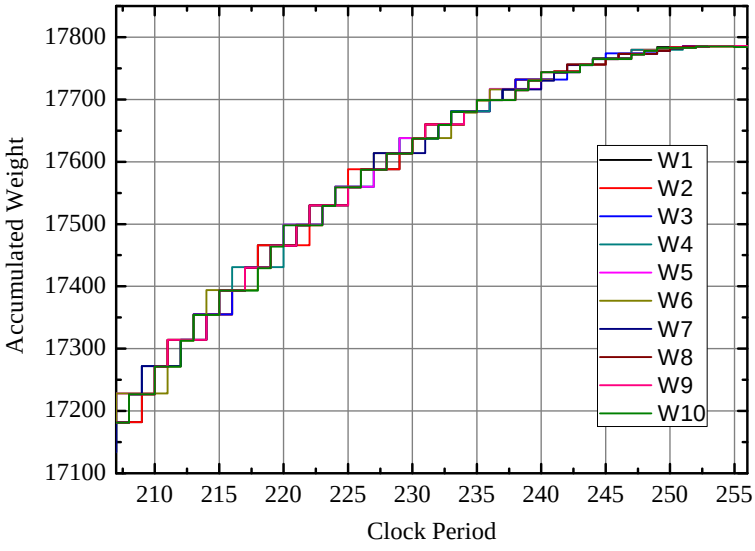

Figure 3.11 Accumulated weights of mismatch of 10 unity elements for second-order 3-bit feed-forward architecture with constant $V_{in} = 0.123V_{ref}$.

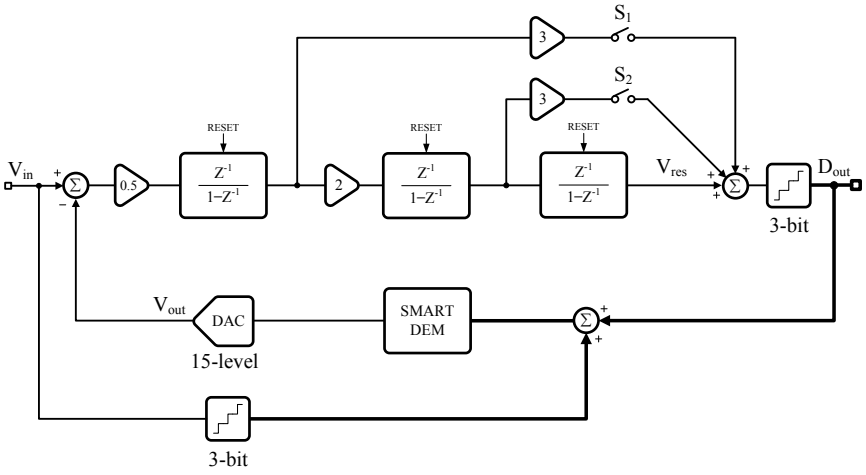

Figure 3.12 Third-order 3-bit feed-forward incremental architecture with Smart-DEM block.

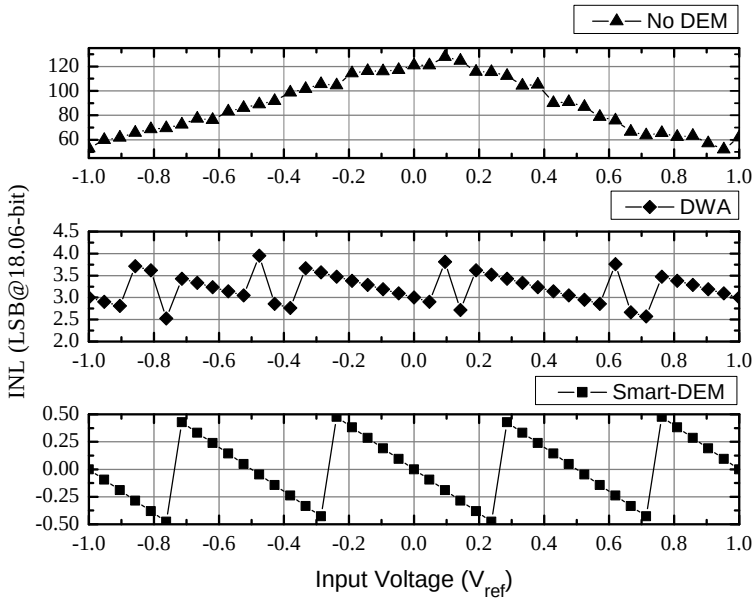

Figure 3.13 Resolution comparison for third-order incremental converter without DEM (top), with DWA (middle) and with Smart-DEM (bottom). The mismatch of unity elements obeys normal distribution with $\mu = 0$ and $\sigma = 0.035\%$.

The number of unity elements is 14. If the positive-negative DAC is used, the number of unity elements is can be reduced to 7, resulting in a compact Smart-DEM algorithm implementation.

To demonstrate the Smart-DEM algorithm for third-order incremental architecture, 2 groups of simulations are also performed. Fig. 3.13 shows the performance comparison of the third-order scheme

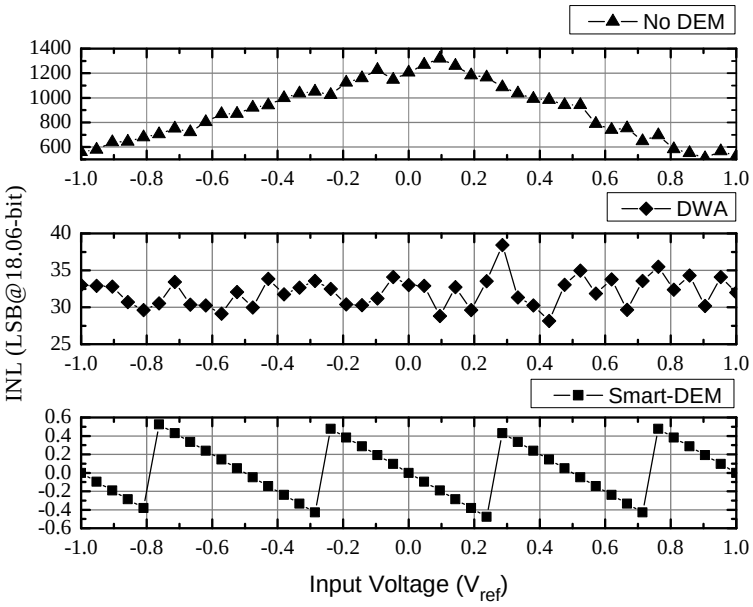

Figure 3.14 Resolution comparison for third-order incremental converter without DEM (top), with DWA (middle) and with Smart-DEM (bottom). The mismatch of unity elements obeys normal distribution with $\mu = 0$ and $\sigma = 0.35\%$.

in three different cases. The mismatch for the 14 unity elements obeys normal distribution with zero mean value and $\sigma = 0.035\%$. The input is a constant voltage ranging from -V_{ref} to V_{ref}. The maximum INL without compensation is about 127.8 LSB. When using DWA method, the error is not linear with a maximum of 3.9 LSB. The Smart-DEM is able to keep the error within 0.5 LSB for entire range.

For the second group simulation, the mismatch for the 14 unity elements obeys normal distribution with zero mean value and $\sigma = 0.35\%$. The input is a constant voltage ranging from -V_{ref} to V_{ref}. The maximum INL without compensation, however, is 1319.8 LSB. With DWA method, the maximum error is 38.4 LSB. The Smart-DEM is able to keep the error within 0.53 LSB for entire range. This value is slightly larger than the expected 0.5 LSB because of the imbalance of the weights at the end of Nth clock period.

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CHAPTER 4

A 17-BIT INCREMENTAL A/D CONVERTER: DESIGN CONSIDERATIONS

This chapter and Chapter 5 describe the design and implementation of a 17-bit incremental A/D converter. The focus of this chapter is the design considerations to achieve high resolution incremental ADCs. Aiming at target specifications, the fundamental design parameters, namely, the order of the incremental structure, the resolution of quantizer and the number of clock periods per sample are discussed. The purpose of the second part is to search for optimal architectures based on multi-bit quantization. Special architecture's requirements need to be take into consideration in order to utilize the Smart-DEM algorithm as well as to keep the modulator compact. The third part shows that by introducing feedback paths in a first-order incremental scheme, the conversion efficiency can increase exponentially. This structure turns out to be the well-known algorithmic architecture. Study manifests that with proper calibration techniques, the algorithmic architecture has the potential to achieve more than 14-bit resolution.

4.1 General Considerations for Incremental Schemes

As already mentioned in Chapter 2, incremental ADCs are always used in instrumentation, measurement and sensor applications, which requires high resolution, good linearity, low offset and low-power. The starting point of this research of incremental ADCs is to have an overview of the specifications, which are listed as follows:

- **Resolution**: 18-bit

► **Bandwidth**: 5kHz
► **Clock Periods**: $\leq$300
► **Power Consumption**: $\leq$0.5mW

To accomplish the goal, design strategies on both architecture level and circuit level should be investigated. Considerations on architecture level are with higher priority with respect to circuit level. Meanwhile, design strategies on architecture level should be further studied to understand if they are feasible from circuit implementation point of view.

With regard to incremental converters, the fundamental design parameters are the order of the structure L, resolution of the quantizer q_b, number of clock periods N, as illustrated in (2.36). When L and q_b are chosen, the corresponding N can be estimated. For example, to obtain 16-bit resolution with $L = 2$ and $q_b = 0$ (2-level comparator), the required clock period is 364. However, the premise of this calculation is that the power of kT/C noise introduced by the input stage of the modulator is less than the power of quantization noise. When the kT/C noise dominants, the maximum achievable resolution does not obey (2.36). Thus, for the design of incremental converters, L, q_b and kT/C noise should be of the most importance. Detailed discussion about these parameters is in the following subsections.

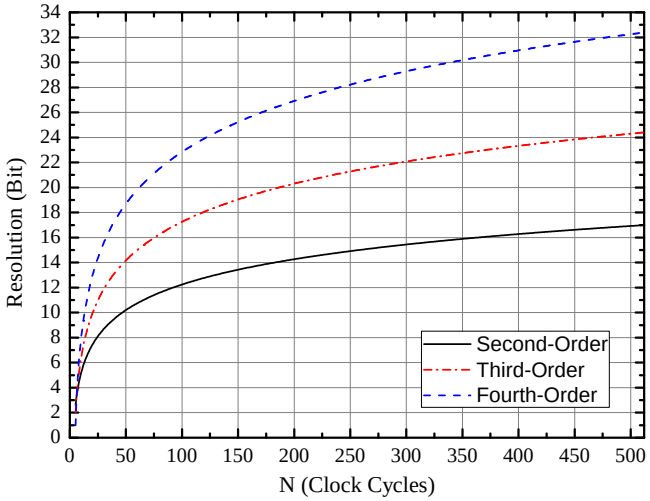

Figure 4.1 Resolution versus clock periods for different order incremental structures.

4.1.1 Second-Order or Higher-Order

To the best of the author's knowledge, the already published incremental ADCs ranges from first-order to fourth-order, among which the second-order structure is of the most usage. The benefit of utilizing high-order structure is the better conversion efficiency. Let us compare the conversion efficiency between second-order, third-order and fourth-order structures by using the general form of incremental ADC illustrated in Fig. 2.15. To simplify the situation, the stability of the loop filter is not taken into consideration and design parameters $c_1, c_2, c_3, c_4 = 1$ and $b_q = 0$ are chosen. Fig. 4.1 shows the maximum achievable resolution with respect to clock period for three different cases. As can be noticed, in order to achieve 16-bit resolution, 365, 75 and 33 clock periods are required for second-order, third-order and fourth-order structures, respectively.

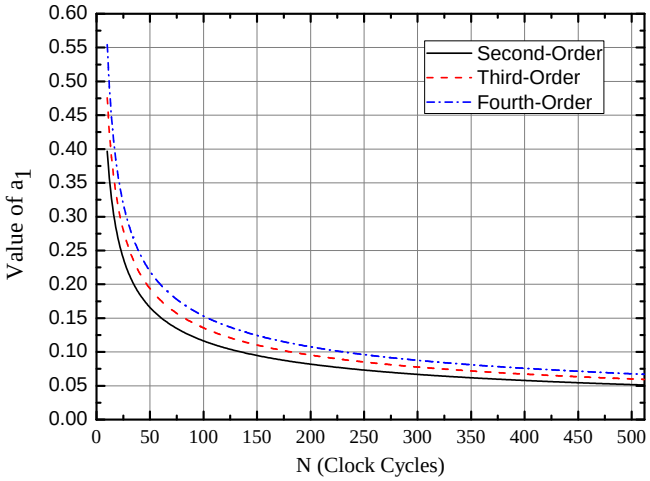

Figure 4.2 The coefficient α_1 with respect to clock periods.

Higher-order incremental architectures, however, have several drawbacks which affect the overall performance. First of all, for incremental schemes more than second-order with comparator as quantizer, the stability issue of the loop filter requires to use coefficients c_1, c_2, ..., c_L less than 1. For example, in the third-order modulator described in [1], $c_1 = 0.5674$, $c_2 = 0.5126$, and $c_3 = 0.3171$. The corresponding full scale value and the resolution can be estimated by

$$M = c_1 c_2 c_3 \frac{(N-1)(N-2)(N-3)}{3!} \tag{4.1}$$

and

$$R_{3ord} = log_2 \frac{c_1 c_2 c_3 (N-1)(N-2)(N-3)}{3!} \tag{4.2}$$

with N = 128, the resolution is 14.9-bit, which is 3.4-bit less than the maximum achievable value (with c_1, c_2, c_3 = 1). Another case is the fourth-order modulator reported in [2]. Coefficients c_1, c_2, c_3 and c_4 are 0.25, 0.4, 0.22, and 0.11, respectively. With N=128, the achievable resolution is 14.6-bit while the maximum theoretical resolution is 23.3-bit. The loss of resolution in this case is, hence, around 8.7-bit.

The second limitation comes from the input referred kT/C noise. Generally, for an incremental ADC, the input referred noise $V_{n,in}$ should be within half V_{LSB} range, which can be described by

$$V_{n,in} = \alpha_1 \sqrt{\frac{2kT}{C}}; \quad V_{n,in} \leq \frac{1}{2} V_{LSB} \tag{4.3}$$

where α_1 is a constant coefficient determined by the incremental scheme and the number of clock periods. Fig. 4.2 plots the value of α_1 versus N for different incremental schemes with $c_1, c_2, c_3, c_4 = 1$. As can be noticed, the attenuation of $V_{n,in}$ is more effective when a larger N is used. Nevertheless, augment of N means the conversion efficiency decreases. In other words, for a certain incremental architecture, there is a tradeoff between the input referred kT/C noise and number of clock cycles. The second observation is that for a fixed N, although high-order schemes benefit from high conversion efficiency, the input referred kT/C noise is worse. As can be seen from Fig. 4.2, higher-order structure

leads to larger α_1 and hence, larger $V_{n,in}$. Fortunately, with a fixed N, the values of α_1 are comparable for different order incremental architectures.

In fact, the limitation due to kT/C noise can be concluded as follows: increasing L can significantly improve the conversion efficiency and reduce the quantization noise, but $V_{n,in}$ remains the same or even worse. When kT/C noise dominates rather than the quantization error, higher-order structures can not improve the performance and suppression of kT/C noise should be taken into consideration. For instance, to obtain 16-bit resolution, 365 and 75 clock periods are required for second-order and third-order architectures. The corresponding α_1 are 0.061 and 0.157. Thus, the minimum input capacitance for third-order structure should be 6.7 times of the counterpart of second-order structure.

Thirdly, the error caused by circuit imperfections has different impact on the performance of incremental modulators. In general, structures with larger L suffer more than modulators with lower order. Here we use an example to show how circuit imperfections affect the performance of different order incremental architectures. For incremental modulators, the basic building block used in the integrator is op-amp. The circuit imperfections of an op-amp mainly come from limited DC gain, slew rate and bandwidth. Considering an op-amp with limited DC gain, infinite slew rate and bandwidth, behavioural-level simulations using the method proposed in [3] are performed for second-order and third-order structures to achieve 16-bit resolution. Fig. 4.1 plots the INL with respect to the gain of the op-amp in the first integrator (the rest op-amps are ideal). We notice that with the same DC gain of op-amp, third-order structure entails larger INL compared with the second-order structure. When a maximum allowable INL is 0.7 LSB, the DC gain of the first op-amp should be 30 dB and 50 dB for second-order and third-order schemes, respectively.

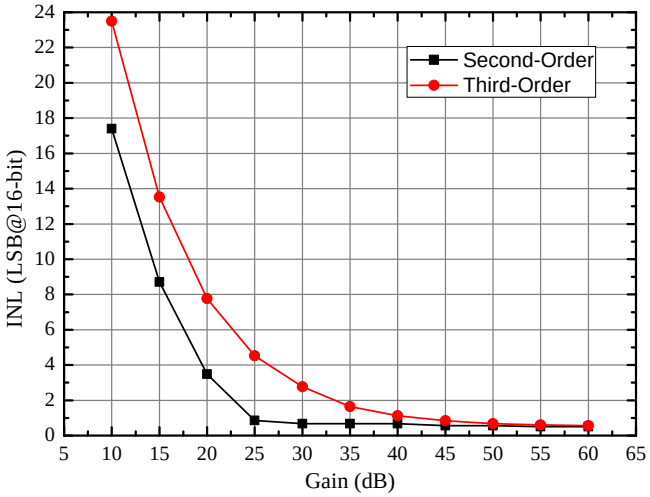

Figure 4.3 INL versus the gain of the first op-amp.

4.1.2 Comparator or Multi-Bit Quantization

In Chapter 2, we briefly introduced the existing incremental modulators and most of them employ comparator as quantizer. Incremental architecture based on multi-bit technique is seldom explored, as already mentioned before. Here, we shall discuss the pros and cons of both techniques in order to obtain optimal design strategies for the targeting specifications.

Utilizing multi-bit quantization can reduce the output swing of integrators, leading to low-power design. While a 2-level quantizer may result in the op-amps working in the slewing mode and thus, the power dissipation is higher compared with the former case. For example, the second-order scheme illustrated in Fig. 2.17 is configured with 2-level or 3-bit quantization. When a constant input signal $V_{in} = 0.707$ V is applied, the output swing of the first op-amp is 4 times of the swing when using 3-bit quantizer, as plotted in Fig. 4.4. The situation of the swing of the second op-amp is similar and is not shown here.

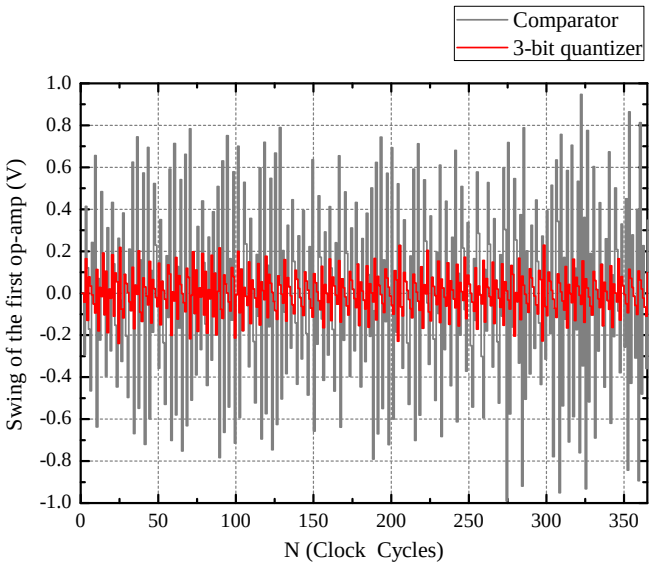

Figure 4.4 Output swing of the first op-amp utilizing 2-level or 3-bit quantization with $V_{in} = 0.707$ V.

The second advantage of using multi-bit quantizer is that the coefficients along the accumulation path $c_1, c_2, \ldots, c_L$ are larger than the counterparts of 2-level quantization scheme. The third-order example presented in [1] with coefficients $c_1 = 0.5674$, $c_2 = 0.5126$, and $c_3 = 0.3171$ demonstrates this observation. When combining multi-bit quantization with digital assisted techniques, good stability of the loop filter and reduced amplitude of the input signal allow using coefficients $c_1, c_2, c_3 = 1$, giving rise to good conversion efficiency.

Thirdly, with q_b-bit quantizer, the maximum achievable resolution exceeds q_b-bit than the counterpart using 2-level quantizer. This is evident according to (2.36). For example, a conventional second-order scheme requires 375 clock periods to achieve 16-bit resolution. Whereas for a 3-bit second-order structure, the required clock cycles is reduced to only 130.

The drawback of multi-bit quantization is the non-linearity of the multi-bit DAC. The non-linearity is due to the mismatch between the unity elements of the DAC. In Chapter 3, effects of mismatch and related DEM techniques are detailed studied for both incremental and $\Sigma\Delta$ ADCs. Regarding to the design of incremental ADCs, the proposed Smart-DEM algorithm is able to compensate for the mismatch, achieving a near-ideal multi-bit DAC. To summarize, incremental architectures based on multi-bit quantization is superior to comparator based structures from both power dissipation and conversion efficiency point of view. The non-linearity of multi-bit DAC can be properly solved by digital assisted technique, giving rise to an optimal choice for designing incremental ADCs.

4.1.3 Design Strategies for Target Specifications

On the basis of previous considerations, optimal design parameters $L = 2 \sim 3, q_b = 3 \sim 5$ are chosen to achieve 18-bit resolution. Using a 0.18 μm CMOS technology with analog power supply 3.3 V, combinations of different L and q_b and other design parameters are listed in Tab. 4.1.

Table 4.1 Design parameters of incremental ADCs to achieve 18-bit.

N_{ord}	q_b	N	α_1	C
Second-order	3-bit	256	0.0724	1.096 pF
Second-order	4-bit	183	0.0857	1.535 pF
Second-order	5-bit	93	0.1207	3.045 pF
Third-order	3-bit	61	0.1747	6.379 pF
Third-order	4-bit	49	0.1957	8.004 pF
Third-order	5-bit	39	0.2206	10.171 pF

where N is the number of clock cycles, α_1 is the coefficient of kT/C noise according to (4.3) and C is the value of input sampling capacitance. As can be seen in Tab. 4.1, larger L and q_b lead to better conversion efficiency. For example, when $L = 3$ and $q_b = 5$, the number of required clock periods is 39, which is only 15% of the needed clock periods with $L = 2$ and $q_b = 3$. However, the reduction of N worsens the noise performance, resulting in 10 times larger capacitance. Regarding to the design of 18-bit incremental ADC, the preferable choice is to use the second-order structure with $q_b = 3 \sim 4$, because of the relative low C and acceptable N. Third-order structures can also be utilized, however, the kT/C noise needs to be suppressed with a larger N so as to keep the noise level comparable with the counterpart in the second-order structure. In this case, the good conversion efficiency of third-order scheme is somehow sacrificed, nonetheless, the resulting architectures can still have better performance than the second-order structures.

According to these design parameters, now let us consider the specific architecture design. For a conventional scheme illustrated in Fig. 2.17, a foreseeable problem is the analog summation block, which gives rise to considerable power consumption to achieve an accurate summation function. One way to avoid such a block is to implement the summation in digital domain and it will be detailed discuss in the next section.

Based on above analysis and design strategies in Section 3.2, guidelines for high-order, multi-bit and low-power incremental ADCs with digital assistance can be concluded as follows

1. The structure does not use analog feedforward paths which lead to extra analog blocks.
2. The output swing of integrators should be minimized to improve the linearity of the op-amps, as well as to reduce the number of comparators in the quantizer.
3. The coefficients along the accumulation path should not degrade the overall performance of the modulator.
4. The input referred kT/C noise should be suppressed to be comparable with quantization error. The value of input sampling capacitance should be affordable, otherwise, increase the number of clock periods N to lower kT/C noise.
5. There should be only one feedback path in which a DEM algorithm (e. g. Smart-DEM) can be effectively used.

The guidelines 1) and 2) consider how to achieve low-power dissipation of the analog circuit. Item 3) results in easier implementation of analog coefficients and avoids performance degradation. The guideline 4) explains the limitation due to kT/C noise and corresponding noise reduction methods. The purpose of last item is to reduce the complexity of digital block, which is used to compensate for the non-linearity of multi-bit DAC. By adopting these guidelines, different second-order and third-order schemes are discussed in the next section.

4.2 Non Conventional Incremental Structures

Following the design strategies in the last section, we shall find out the proper architectures so as to employ the multi-bit quantization and DEM techniques. This section starts from second-order structure and then extends to third-order scheme. With digital assisted actions in the last part, the swing of equivalent input signal is considerably reduced, thus, leading to low-power design of the analog circuit.

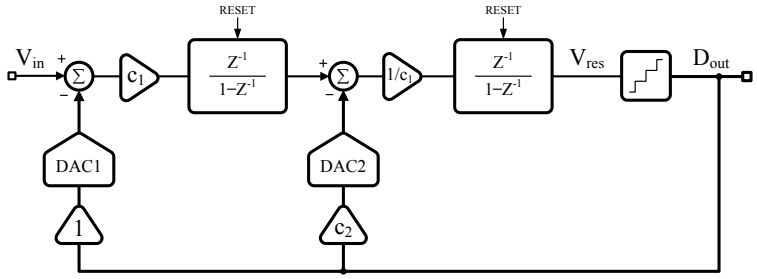

Figure 4.5 Second-order incremental scheme with two feedback paths.

4.2.1 Second-Order Architectures

A second-order incremental converter is the cascade of two integrators. As it happens for time-invariant schemes, it is necessary to control the cascade of more than one integrator for keeping constrained the output of intermediate nodes. The request is not ensuring stability as needed in filters or $\Sigma\Delta$ architectures; however, since a similar action is required, the designer can take advantage of the method used in time-invariant schemes.

Second-order $\Sigma\Delta$ architectures use an auxiliary injection at input of the second integrator or employ feed-forward branches toward the quantizer. The latter solution is not optimal, because for multi-bit schemes, it is necessary to use extra analog power for adding the feed-forward branches. The use of an auxiliary injection, as shown in Fig. 4.5, can be used at two purposes: optimize the swing at the op-amp outputs or improve the feedback factor of integrators. There is an additional degree of freedom on the choice of the coefficients c_1 and c_2. The real benefits are, indeed, limited. The use of $c_1 = 0.5$ and $c_2 = 0.75$ reduces the maximum swing of the op-amps by 15% and, obviously, improves the feedback factor of the second integrator, provided that the subtraction is performed with different SC circuits.

Fig. 4.6 shows an alternatively solution that avoids intermediate injection without feed-forward paths. The use of a transversal filter and the proper choice of coefficients c_1 and c_2 control the signal swing of the two integrators. The choice of the coefficients can be done with the help of the z transfer

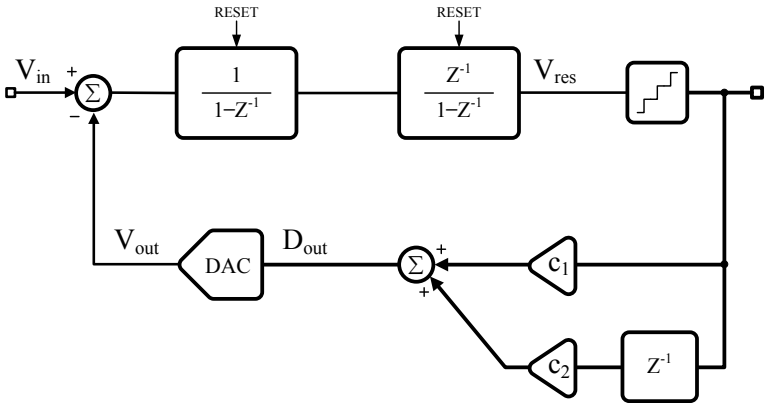

Figure 4.6 Second-order incremental scheme with one feedback path.

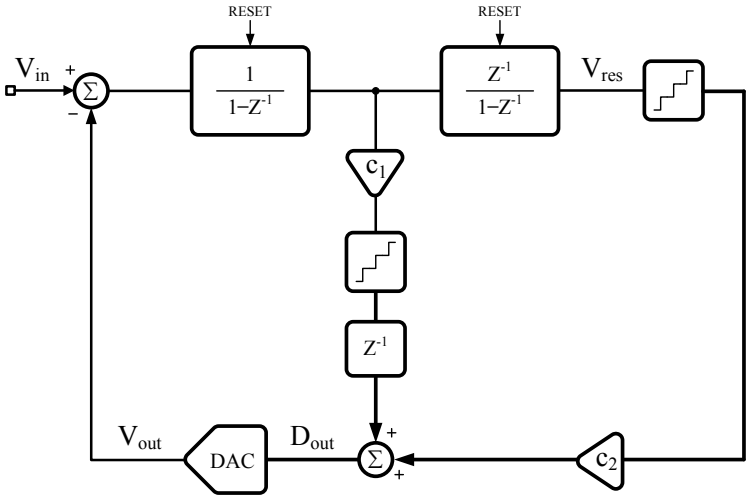

Figure 4.7 Second-order incremental scheme with two quantizers.

function of the time-invariant equivalent. The study in the z-domain gives rise to a denominator in the noise transfer function (NTF) and signal transfer function (STF), which can be expressed as

$$D_{2ord}(z) = 1 + (c_1 - 2)z^{-1} + (c_2 + 1)z^{-2}. \tag{4.4}$$

The position of poles of the time-invariant counterpart inside the unity circle verifies stability. Moreover, their placement can bring about possible reduction of the op-amp swings. For example, with $c_1 = 2, c_2 = -1$ and $q_b = 3$, $D_{2ord}(z)$ is equal to 1. Simulations show that swings are $0.8V_{ref}$, $1.3V_{ref}$ and $2V_{ref}$ for the outputs of first integrator, second integrator and the DAC, respectively. However, when design parameters $c_1 = 1, c_2 = 0.5$ and $q_b = 3$ are chosen, there are two poles ($p_1 = 0.5 + 0.5j$ and $p_2 = 0.5 - 0.5j$) inside the unity cycle. Thus, the stability of loop filter is ensured. The corresponding swings for the first integrator, second integrator and the DAC are $0.2V_{ref}$, $2.1V_{ref}$ and $1.2V_{ref}$.

Fig. 4.7 shows a third possible architecture. It uses two quantizers at the output of integrators. The signal fed back at the input is the addition of the two digital outputs. The use of an extra quantizer is a limited cost because the power consumed by a comparator is much less than the one of an op-amp with the same speed. Removing the intermediate injection improves the feedback factor of the second integrator, thus allowing to spare power. The study of the time-invariant equivalent of this second-order structure shows a denominator in the STF and NTF as follows

$$D_{2ord}(z) = 1 + (c_1 + c_2 - 1)z^{-1} + (c_1 - 1)z^{-2} \tag{4.5}$$

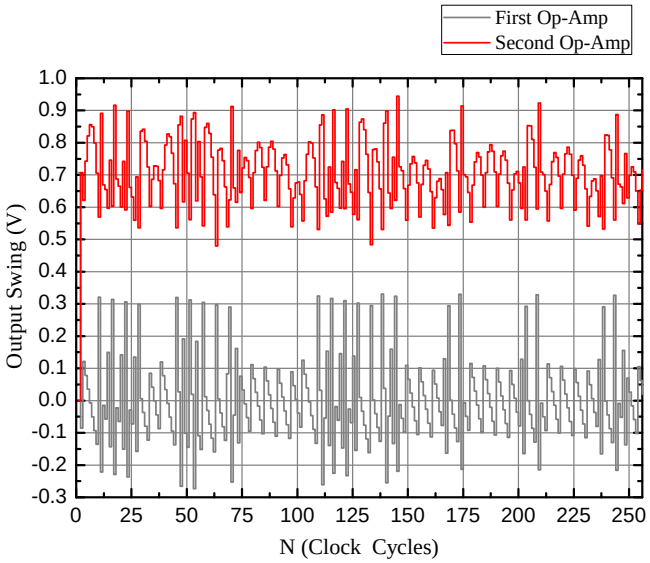

Figure 4.8 Output swing of op-amps for second-order scheme with two quantizers with $0.707V_{ref}$ input.

Simulations show that different set of design parameters c_1, c_2 and b_q optimize the variation of output swing at the input of the quantizer. For instance, with $c_1, c_2 = 1$ and $b_q = 3$, the output swing of two integrators is less than $0.4V_{ref}$. Fig. 4.8 shows the waveform of the outputs of op-amps under these parameters when given $0.707V$ constant input ($V_{ref} = 1$). Notice that the waveform of the output of second op-amp is around the input amplitude, however, simple circuitry enables an amplitude shift around zero. Therefore, a small swing corresponds to relaxed slewing request, low dynamic range and reduced number of comparators in the flash.

4.2.2 Third-Order Architectures

Methods similar to the one discussed for the second-order incremental converter can be extended to higher order. Fig. 4.9 shows a third-order incremental ADC scheme with single digital DAC and FIR filter along quantizer loop. The digital filter uses three taps with two delays. Parameters c_1, c_2 and c_3 of the filter can be critical for stability. The z transfer functions of the time-invariant counterpart has a denominator given by

$$D_{3ord}(z) = 1 + (c_1 - 3) + (c_2 + 3)z^{-2} + (c_3 - 1)z^{-3} \tag{4.6}$$

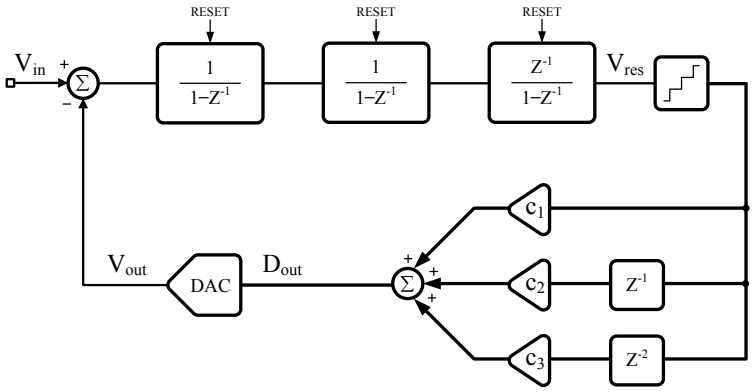

Figure 4.9 Third-order incremental ADC with one feedback path.

whose zeros must be in the unity circle. With $c_1 = 3$, $c_2 = -3$ and $c_3 = 1$, the swings of the outputs of three integrators and DAC are $V_{ref}, 1.2V_{ref}, 0.5V_{ref}$ and $4V_{ref}$, respectively. The benefit of this structure is that the stability is ensured with compact digital filter. Nonetheless, the DAC dynamic range must be larger than the input to accommodate the larger error due to the difficulty in controlling a cascade of three integrators.

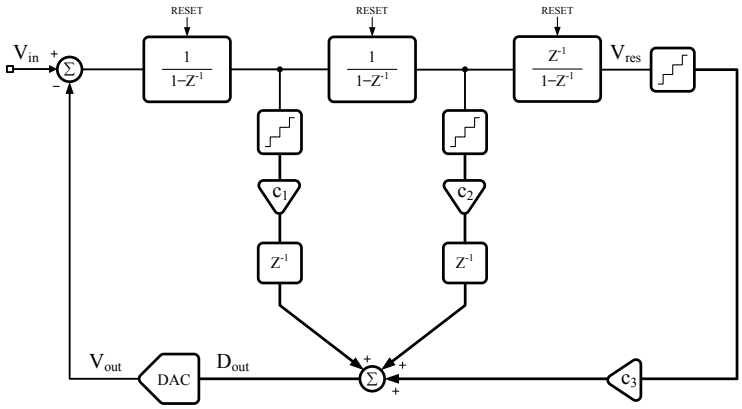

Figure 4.10 Third-order incremental ADC with three quantizers.

Fig. 4.10 shows the block diagram of a third-order incremental ADC with multiple quantizers. The strategy is more effective in controlling the integrator output voltages because there is a monitor of each of them. The resolution of the three ADCs is supposed to be the same. The choice of the parameters c_1, c_2 and c_3 can give rise to unstable situations or reduce the swing at output of accumulators. The study of the time-invariant scheme outlines a denominator of the transfer functions, which can be represented as follows

$$D_{3ord}(z) = 1 + (c_1 + c_2 + c_3 - 3)z^{-1} - (2c_1 + c_2 - 3)z^{-2} + (c_1 - 1)z^{-3} \tag{4.7}$$

whose zeros must be inside the unity circle. Simulations that change the parameters within the stability range identify the optimum set. Notice that different values of the $c_{1,2,3}$ parameters weight in a different manner the control of the accumulator outputs. Since a large swing in one of them affects the following, it is logical to assume $c_1 = c_2 = c_3$. Simulations with 3-bit quantizers give rise to minimum swings with $c_{1,2,3} = 1$. In this case, the swings of the outputs of three integrators and DAC are V_{ref}, $0.5V_{ref}$, $0.5V_{ref}$ and $2V_{ref}$. Compared with the conventional third-order incremental structure, the swing of the first op-amp is at almost the same level. Meanwhile, the waveform of the third op-amp's output remains around the value of the input signal. These drawbacks can be solved with the digital assisted actions in the following subsections, thus, leading to an optimal architecture for third-order multi-bit incremental ADCs.

4.2.3 Digital Assisted Actions

The operation of the proposed high-order incremental converters, in addition to the foreseen processing, can be suitably assisted with a number of actions. They concern the digital measure of mismatches, digital calibration and the shift of signals to keep them in the most effective region.

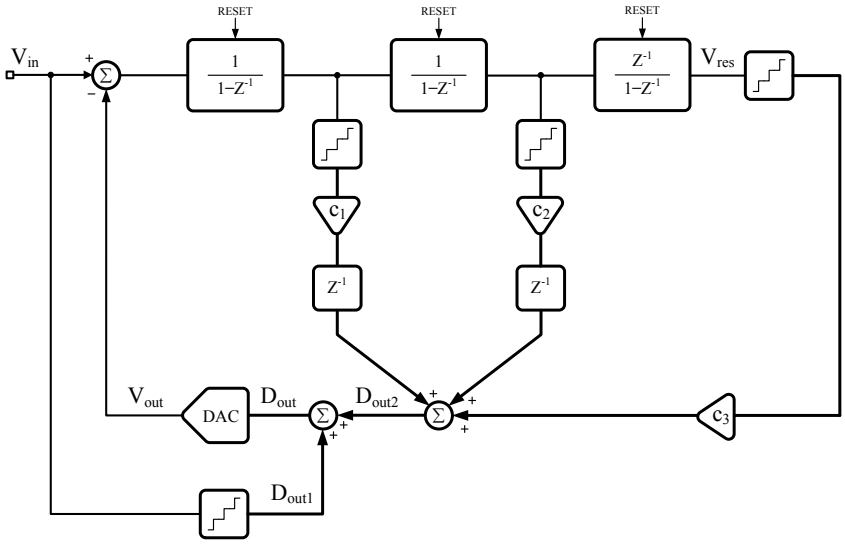

Figure 4.11 Third-order incremental ADC with three quantizers and input level shift.

An architecture with limited output swing in integrators improves the overall performance. That result is naturally achieved by multi-bit quantizers that limit the error in the signal estimation. However, there are two key problems: the linearity of the DAC that must be better than the overall resolution; the need of shifting signals around the quiescent amplitude. The first issue involves the measure of the mismatch, possibly done in a foreground fashion using the converter itself. The digital measures of the mismatch, stored in a memory, are the input of a digital calibration. The method is a good alternative to the dynamic matching used in multi-bit $\Sigma\Delta$ modulators because the DEM technique is not for Nyquist-rate converters.

A level shift at the input of the flash results if the input of the DAC is

$$D_{out} = D_{out1} + D_{out2} \tag{4.8}$$

where D_{out1} is a quantized version of input. This is done with the added summation node in Fig. 4.11. Since the input is constant for the entire conversion cycle, its quantization can be performed before starting the conversion cycle. The conversion is done at zero cost by one of the two ADCs used by the architecture and stored in a temporary memory. Simulations show that the output swings for three integrators and DAC are $0.5V_{ref}$, $0.4V_{ref}$, $0.3V_{ref}$ and $2V_{ref}$, which is a significant improvement compared with the former case when the digital assisted action is not used.

4.3 Algorithmic A/D Conversion

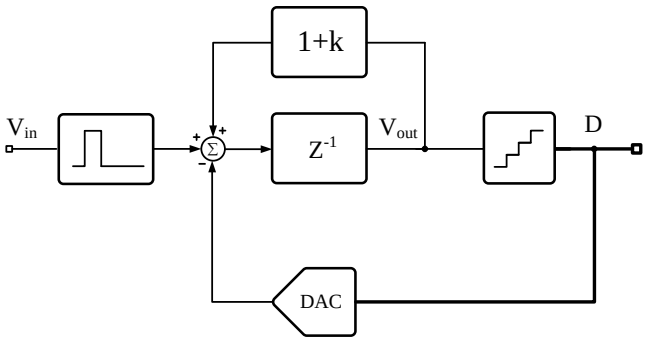

Figure 4.12 Conceptual block diagram of algorithmic converter. The quantizer can be a simple comparator or a multi-bit scheme.

Previous study shows that with second-order structure, the accumulation efficiency of the input signal is proportional to N^2, while for third-order scheme is proportional to N^3. From mathematical point of view, a good way to further enhance the accumulation efficiency is to accumulate the input exponentially, namely α^N ($\alpha > 1$). This can be implemented by simply introducing a feedback path with coefficient k to a conventional first-order incremental structure. The conceptual scheme of such a modulator is illustrated in Fig. 4.12. The input signal enters a loop at the beginning of the conversion cycle. The use of active devices multiplies the signal by a factor $m = (1 + k)$ every clock period while $\pm V_{ref}$ enters the loop under the control of a comparator. The control loop keeps limited the amplitude of the output voltage V_{out}. Therefore, the following equation can be derived

$$V_{out}(n) = V_{in}m^n - \sum_{i=0}^{n-1} D(n-1-i)V_{ref}m^{n-1-i} \tag{4.9}$$

where, for single bit, $D(i)$ is ± 1 depending on the output of the comparator at the corresponding clock period. $D(n-1)$ is the quantization of V_{in} in the reset clock period.

Interestingly, the structure illustrated in Fig. 4.12 turns out to be the so-called algorithmic ADC. Algorithmic converters [4] are attractive solutions because they achieve high resolution with a number of clock periods comparable with the number of bits. They are similar to the SAR converters but an active multiplication of the signal every clock period keeps the input of the quantizer (typically a simple comparator or a flash) at a suitable large level. Normal architectures use a multiplication by 2 of the signal around the feedback loop. The input injected at the beginning of the conversion cycle is enhanced together with the signal of a DAC injected under the control of a DAC and a logic block.

Possible variants to the basic algorithm are the use of a multi-level quantizer and the pre-conversion of the input with another conversion method which generates a residual (the incremental, for instance) and the refinement of the resolution by using the algorithmic method. The latter case is used in [5]: the algorithmic architecture is configured as a first order incremental and after a number of accumulation of the input, the scheme becomes algorithmic. The result is that the number of bit determined in the preliminary phase increases the final resolution. There are many possible schemes which realize the multiplication by m. One [4] uses a loop with two amplifiers; another follows the scheme of Fig.4.12 with a positive feedback injecting k times the output at the input every conversion period. Obviously the second solution is more power and area effective as it uses only one active element.

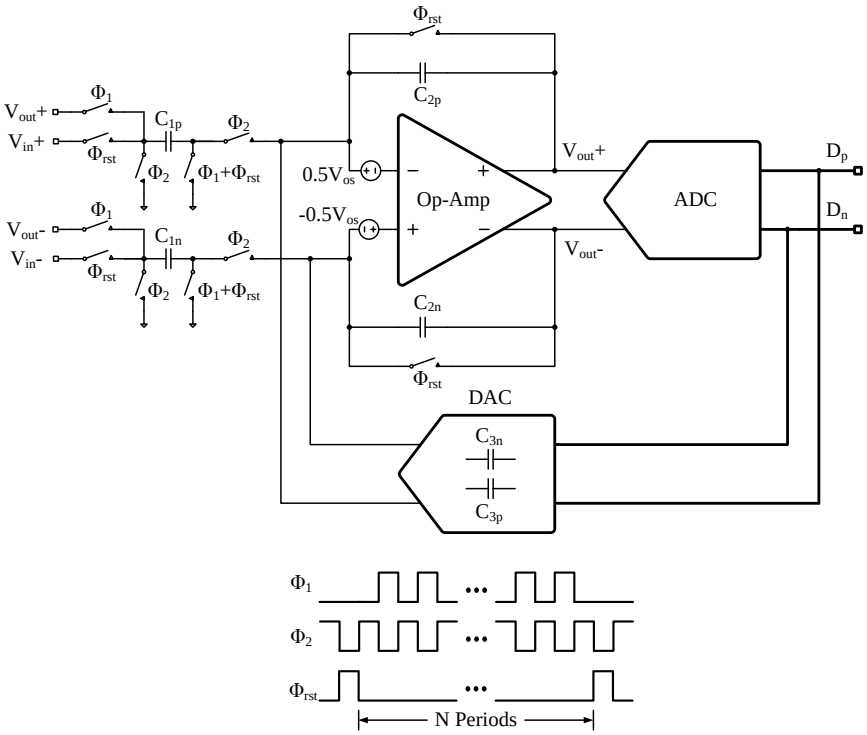

Figure 4.13 Possible circuit implementation of a fully-differential algorithmic converter. The DAC establishes a C_3 load from virtual grounds to ground.

The limits to the practical implementation come from the error caused by the accuracy of the multiplying factor and, in case of multi-level DAC the mismatch between the unity elements. The use of operational amplifiers implies reduction of performance caused by finite gain, offset and limited speed. Passive components are normally supposed with equal value. The matching accuracy, which must be better than the inverse of the digital dynamic range of the data converter, depends on the area of the element. Typical processes and reasonable sizes ensure accuracy between 2^{-10} to 2^{-12} range.

Achieving resolutions of more than 12-bit imposes efforts in the active devices design and corrections of technological inaccuracy. Indeed, experimental results of a previous published solution [5] showed that it is possible to achieve 12-bit resolution relying on the accuracy normally granted by available technology. Aiming at more aggressive performance, the following content analyses the

limits caused by the use of real elements, then methods for compensating for those limits for getting more than 14-bit are described.

4.3.1 Limitations of Algorithmic Architectures

The implementation limits make the algorithmic method not very attractive. The SAR scheme achieves 10 or more bit without requiring signal amplification. This makes the method superior as far as the power consumption is concerned. For resolution of 14-bit or more, the SAR technique becomes problematic and the use of schemes with active functions becomes almost indispensable.

In order to analyse the limits we refer to the possible circuit implementation shown in Fig. 4.13. It is a fully differential scheme with a single op-amp and a multi-bit quantizer with a charge-generator DAC. Capacitor C_1 (and its complementary counterpart) samples the input during the reset phase. Then it injects its charge into C_2 before starting the conversion algorithm. The same switched capacitor structure C_1 amplifies the output by $m = (C_1 + C_2)/C_2$ and the DAC closes the feedback loop with an equivalent capacitance C_3 which loads the differential virtual grounds. Two differential voltage generators model the op-amp offset. The finite gain of the op-amp is A_0.

Let us consider the limits of finite gain before. The charge conservation during each conversion period is

$$\begin{aligned} V_{out}(n)(1+\frac{1}{A_0}) =& V_{out}(n-1)(1+\frac{1}{A_0})C_2 \\ &+V_{out}(n-1)C_1 - \frac{V_{out}(n)}{A_0}C_1 \\ &+D(n-1)V_{ref}C_3 - \frac{V_{out}(n)}{A_0}C_3 \end{aligned} \tag{4.10}$$

leading to

$$V_{out}(n) = \frac{a_2 V_{out}(n-1) + D(n-1)V_{ref}}{a_1} \tag{4.11}$$

where

$$\begin{aligned} a_1 =& \frac{C_1}{A_0} + (1+\frac{1}{A_0})C_2 + \frac{C_3}{A_0} \\ a_2 =& C_1 + (1+\frac{1}{A_0})C_2 \end{aligned} \tag{4.12}$$

It is evident that for different input amplitudes the digital data and the feedback give rise to a sequence of output amplitudes unrelated to the input. The result is a non linear overall error whose extent is large with low finite gains. Since estimating the effect is difficult, we used the above equation in a behavioural model to determine errors as shown in Fig. 4.14. The result is that a given target resolution determines a minimum finite gain. With our best knowledge, it is almost impossible to correct with digital methods the limit caused by the finite gain of the op-amp. If the loss of 0.5-bit is admitted, a 16-bit converter requires $100\,dB$ finite gain.

The number of bits of the quantizer augments the resolution of a converter without increasing the number of clock periods. However, the mismatch between unity elements used in the DAC limits the linearity and adds an error whose effect is equivalent to noise. A viable solution is to employ a three-level DAC. That is because with fully differential implementations, it is possible to ensure intrinsic symmetrical responses. The three-level DAC grants an extra bit of resolution at the expense of two comparators in the flash. However, a three-level DAC leads to imperceptible non-linearity because of possible different widths of the quantization intervals representing the three logic levels. Simulation results show minor harmonic terms as outlined in the output spectrum of Fig. 4.15 (thresholds at

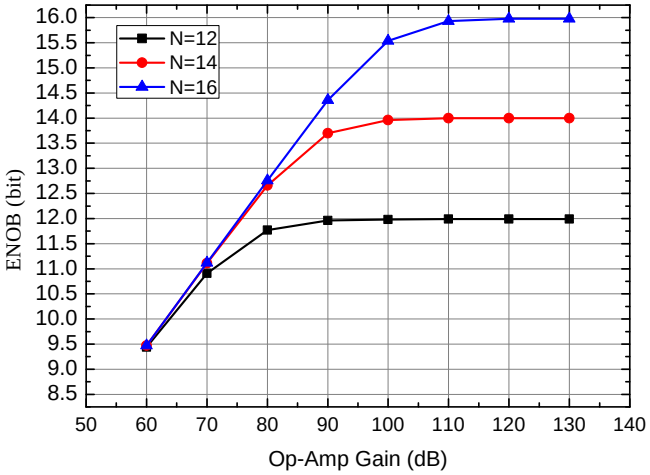

Figure 4.14 Equivalent number of bit versus the finite gain of the op-amp used in an algorithmic converter.

$\pm 0.5V_{ref}$). The tones are at around $-100\,dB_{FS}$, denoting a limited distortion contribution normally below common specifications.

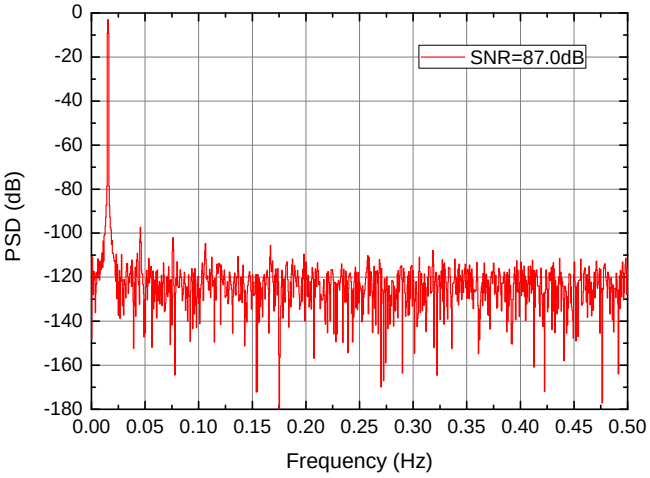

Figure 4.15 Spectrum of an algorithmic converter with a 3-level quantizer.

The offset of the operational amplifier causes a shift in the injection of the signals returning back from the op-amp output and the one determined by the DAC. Accounting for the offset limit (and supposing the gain of op-amp is very large) the charge conservation equation leads to

$$\begin{aligned}[V_{out}(n) - V_{os}]\,C_2 = &[V_{out}(n-1) - V_{os}]\,C_2 + \\ &[V_{out}(n-1) + V_{os}]\,C_1 + \\ &[-D(n-1)V_{ref} + V_{os}]\,C_3\end{aligned} \tag{4.13}$$

supposing $C_1 = C_2 = C_3$ it results

$$V_{out}(n) = 2V_{out}(n-1) - D(n-1)V_{ref} + 2V_{os} \tag{4.14}$$

Notice that there are two consequences related to the limit caused by offset. Looking from the DAC output point of view, offset corresponds to a shift of the input by $V_{os}(1 + \frac{C_1+C_3}{C_2})$, which is equivalent to a corresponding input referred offset. The situation is different when looking at the output multiplication effect. Indeed, since the circuit achieves the multiplication by adding a replica of the output voltage V_{out}, the consequence of offset is to alter the multiplication factor. In the special case that the output equals to the minus offset, the multiplication reduces to 1, and in general is,

$$m = 1 + \frac{V_{out} + V_{os}}{V_{out}} \tag{4.15}$$

which changes in an unpredictable, pseudo-random manner, depending on the sequence the output voltage.

The use of the above equations to build a behavioural model verifies expected result. The output shows an offset and worsening of the equivalent number of bit because of a pseudo-white noise. Fig. 4.16 compares spectra with a $-3\,dB_{FS}$ input sine wave and zero or $4\,mV$ offset. The expected full scale SNR of the converter is $98\,dB$. The circuit uses two level quantizer with $V_{ref} = \pm 1V$. Result show that just $4\,mV$ degrade the performance by $33.1\,dB$ corresponding to a loss of 5.5-bit.

Fig. 4.17 plots resolution versus offset with expected 16 and 18-bit and $V_{ref} = \pm 1V$. The loss strongly depends on sine wave amplitude and frequency. However, $0.85\,mV$ and $0.37\,mV$ offset causes a loss of 1 bit for the two foreseen resolutions. The result shows that in order to ensure high resolution, the essential range of offset should be sub $1\,mV$.

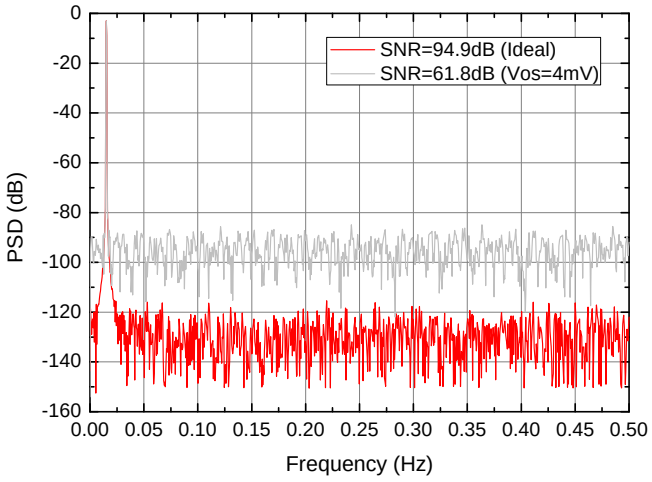

Figure 4.16 Output spectrum with zero offset and 4 mV offset, showing an increase of the noise floor.

Another important limit is given by the error caused by capacitor mismatch. Even if it is possible to limit the error, the technique such as the one proposed in [6] works well until 12-bit. Mismatch determines the accuracy of used base of numbering system, typically 2 when C_1 is chosen nominally equal to C_2. Moreover, the mismatch between capacitors C_1 and C_2 gives rise to gain error. The difference between the effective and the expected multiplication factor causes an error which increases

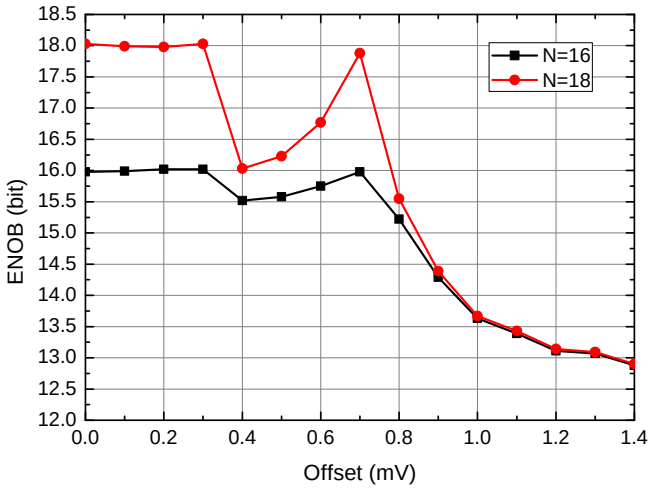

Figure 4.17 Equivalent number of bit at output of a 16-bit an 18-bit algorithmic cover for different offset values.

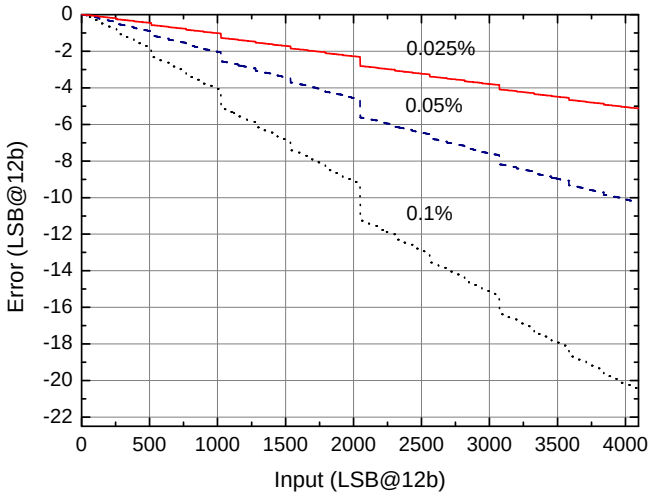

Figure 4.18 Error caused by capacitor mismatch for a 12-bit ADC.

with the code. Fig. 4.18 shows the error for a 12-bit algorithmic converter with mismatches by 0.1%, 0.05% and 0.025%. Result shows a gain error and a non linear error whose maximum occurs at the mid-scale. In order to constrain the DNL below 1 LSB, a matching accuracy about $1/2^N$ is necessary, where N is the number of bit of the converter. Since with modern technologies it is possible to get 1-σ matching accuracy in the order of 0.05%, designing converters more than 10-12 bit requires actions capable to correct the mismatch limit.

4.3.2 Error Correction Methods

The correction of static errors in data converters can be done in the background or the foreground [7]. Here we suppose to measure errors using a foreground approach. It is possible to extend the method to background by interleaving the foreground method with normal operation.

The previous sections outlined two key limits: offset of the op-amp and mismatch between C_1 and C_2. In order to achieve good resolution, the measurement of these non-ideal factors is necessary. Notice that the scheme of Fig. 4.13 can be reconfigured as a first order incremental converter. After the reset of the capacitor in feedback across the op-amp, it accumulates the input signal for a given number of clock periods, say $N = 2^r$. The incremental algorithm uses only the DAC feedback. Neglecting mismatches, the final output of op-amp is

$$V_{out}(N) = NV_{in} - \sum_{i=1}^{N} V_{ref} D(i) \tag{4.16}$$

where $D(i)$ is ± 1, denotes the sign of $V_{out}(i)$ at the i-th clock period. The use of a large number of clock periods N measures the quantity under calibration with an r-bit resolution.

The use of the scheme of Fig. 4.13 in the incremental converter mode enables us to measure offset and mismatch by the following configurations:

► **Measure of offset**: disable SC structure with C_1. According to (8) the digital accumulation at output determines the offset. The accuracy of the measure is within the matching between the capacitors C_2 and C_3.

► **Measure of mismatch between C_1 and C_2**: inject a fraction α of reference voltage with SC structure C_1 and then disable it (case a). Repeat the measure with the role of C_1 and C_2 reversed and same fraction α of reference at input (case b).

After N clock periods the digital outputs in the two cases provide the following measures

$$Y_a = (\alpha V_{ref} + V_{os}) C_1 / C_3; \tag{4.17}$$

and

$$Y_b = (\alpha V_{ref} + V_{os}) C_2 / C_3; \tag{4.18}$$

with r bit of accuracy. The ratio between Y_a and Y_b determines the mismatch.

The measure of offset and mismatch can be done by a specific calibration cycle at the power-on or during inactivity periods (foreground calibration). Alternatively, it is possible to use an extra clock period per conversion and use that clock period with the incremental configuration (background calibration). In the latter case a calibration supplementary capacitor, which is inserted during the extra phase, should be employed.

The measure of offset enables its correction in the analog domain with different methods. For instance, it is possible to properly shift reference voltages or to suitably correct offset by an extra op-amp input pair. The correction of mismatch can be done by digital processing that transforms the measured result into binary.

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CHAPTER 5

A 17-BIT INCREMENTAL A/D CONVERTER: DESIGN AND IMPLEMENTATION

This chapter describes a second-order 3-bit incremental converter, which employs a novel Smart-DEM algorithm to compensate for the mismatch of unity elements of multi-level DAC. The design, which is fabricated in a mixed 0.18-0.5-μm CMOS technology, obtains more than 17-bit resolution over a 5 kHz bandwidth by using 256 clock periods per sample. A single-step chopping technique is adopted which leads to a residual offset of 9.7 μV. The measured power consumption is 280 μW and the achieved Figure of Merit (FOM_S) is 177.5 dB.

5.1 Proposed Architecture

Based on architecture illustrated in Fig. 4.7 with $c_{1,2} = 1$ and $b_q = 3$, the proposed second-order scheme is derived and shown in Fig. 5.1. It is the cascade of two sampled-data integrators (one without delay, the other with delay) with three ADCs, which digitize the input signal and the outputs of the two integrators. The digital output is the addition of the three analog-to-digital conversions. The quantization step of each ADC is $V_{FS}/8$. For such a second-order modulator, the maximum achievable resolution is

$$R_{2ord} = log_2 \frac{N(N-1)}{2!} + b_q \tag{5.1}$$

With $N = 256$ and $b_q = 3$, R_{2ord} is equal to 17.99-bit and the full scale value is 261,120.

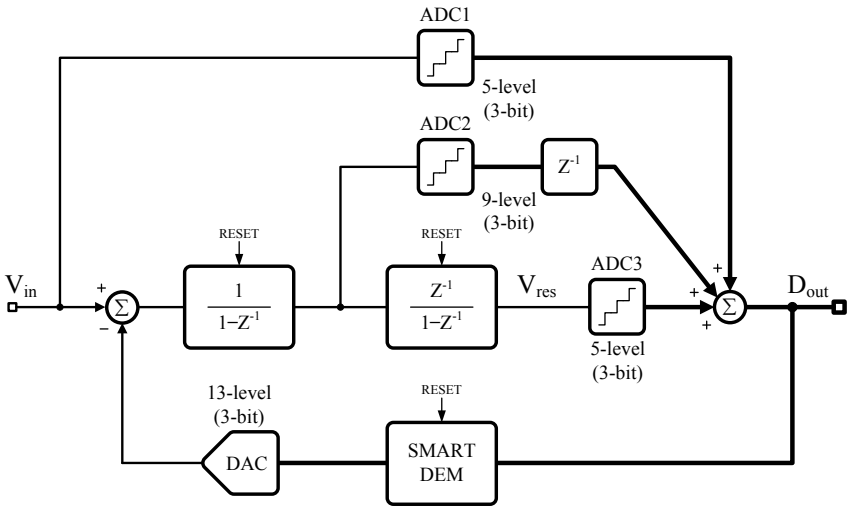


Figure 5.1 Proposed second-order incremental ADC block diagram.

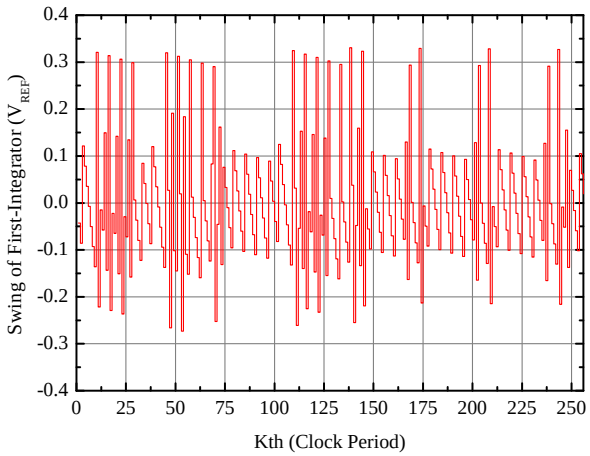


Figure 5.2 Swing of the first-integrator under constant input $0.707V_{ref}$.

The digital feedforward paths limit the swing at the output of the op-amps. Notice that Fig. 5.1 mimics with digital paths the second-order scheme proposed in [1]. The scheme ensures stability and limits the op-amp swings. Fig. 5.2 show the swings of the first integrator when a constant signal $V_{in} = 0.707V_{ref}$ is applied. With extensive behavioural level and transistor level simulations, the output swing of both the first and second integrators is within $0.4V_{ref}$. This allows the use of only 4 comparators instead of 8 for ADC2 and ADC3. The output swing of DAC is $1.5V_{ref}$. This means that for a 3-bit DAC, 4 extra unity elements should be added to extend the total level of DAC from 9 to 13. However, with a bipolar DAC structure, the number of unity elements is reduced to 6, which is affordable in terms of both implementation complexity and power dissipation.

Finally, in order to compensate for the mismatch of 6 unity elements, a Smart-DEM block is added to properly select the unity elements in the multi-level DAC in each clock period. The details of Smart-DEM principle and implementation will be discussed in the following sections.

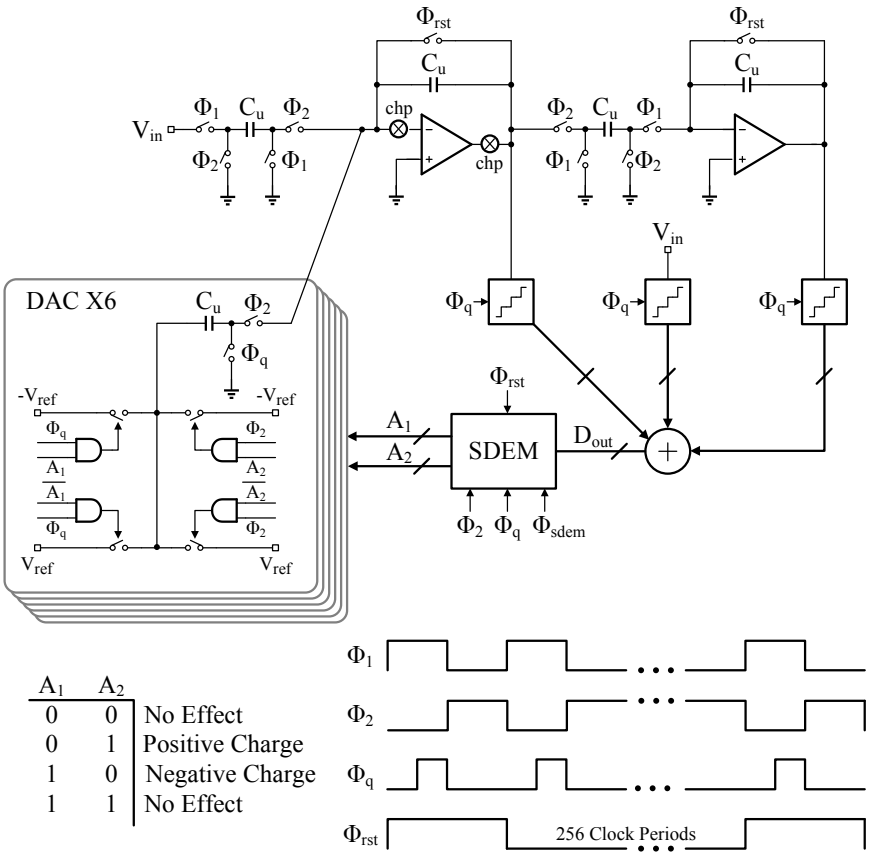


Figure 5.3 Proposed second-order incremental ADC schematic diagram.

5.2 Analog Building Blocks

Fig. 5.3 shows the schematic of the proposed second-order incremental ADC. The 2 integrators are implemented with switched capacitor (SC) circuits. By using different clock phases ϕ_1, ϕ_2, and ϕ_{rst}, the integrators can performance charge, injection or reset functions. The different delays of integrators are realized by proper control of the switches with various clock phases. Notice that the first op-amp contains a chopper, which is used for the cancellation of offset of the modulator. As mentioned previously, ADC1 contains 8 comparators, while ADC2 and ADC3 use 4 comparators due to the reduced output swing of integrators. The 3 quantizers digitize the input signal and the outputs of 2 integrators. A digital summation block uses these 3 digital quantization results to generate the output of the modulator D_{out}.

The most critical parts of this design are the Smart-DEM (SDEM) block and the bipolar DAC. As seen in Fig. 5.3, the Smart-DEM block is under the control of ϕ_q (charge the DAC), ϕ_2 (discharge the DAC), ϕ_{rst} (reset the Smart-DEM) and ϕ_{sdem} (Smart-DEM internal operations). The output signals of Smart-DEM block are $A_1[6:1]$ and $A_2[6:1]$, which are used to properly select unity elements in the DAC. In the following subsections, the design and implementation of the analog building blocks and related techniques are detailed explained, which include op-amp and single-chopping method, bipolar DAC with controls and low-power comparator.

5.2.1 Operational Amplifiers

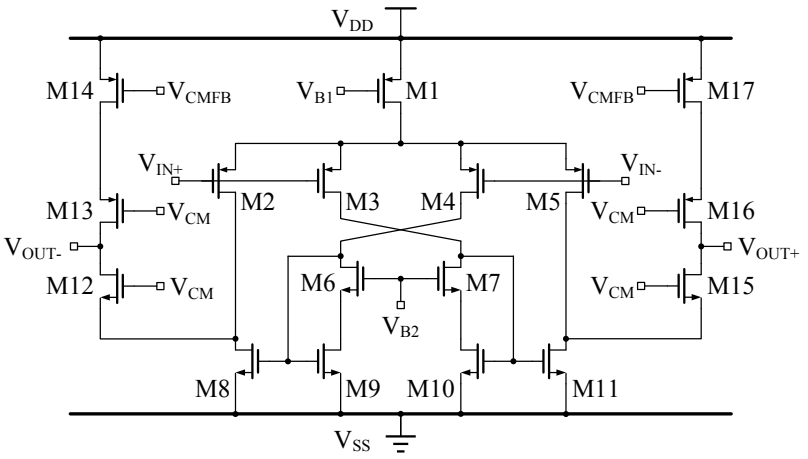


Figure 5.4 Recycling operational amplifier schematic diagram.

The performance of an op-amp is limited by various factors, mainly the DC gain, bandwidth and slew rate. Ideally, the values of these 3 parameters should be infinite and the op-amp behaves as a voltage control current source (VCCS). In reality, limited values of these 3 parameters give rise to circuit imperfections. For the second-order incremental ADC depicted in Fig. 5.3, error caused by circuit imperfections of the first op-amp is accumulated linearly by the second integrator. Hence, specifications of the first op-amp are more strict than those of the second op-amp. Besides, in order to achieve 18-bit resolution, a large C_S is required to suppress kT/C noise from the input of the modulator. In this design, V_{FS} is 3 V under a 3.3 V analog power supply. The C_u is 450 fF and the total input capacitance for 8 unity elements is 3.6 pF. In such a case, it is very difficult to achieve sufficient bandwidth and slew rate under a very low power dissipation budget with conventional op-amps. Special architectures and design techniques on op-amps should be adopted so as to meet the strict specifications.

The first op-amp scheme, shown in Fig. 5.4, is a fully differential recycling folded cascode amplifier (RFCA), with discrete-time common mode control (not shown in the figure). V_{B1} and V_{B2} are biasing voltages generated by a bias circuit(not shown in the figure) while V_{CM} is the common mode voltage. The reason of a utilizing such an op-amp is that, as explained in [2], this structure can boost the gain, bandwidth and slew-rate without affecting noise performance or introducing additional offset.

Firstly, let us compare the equivalent transconductance Gm of RFCA and traditional folded cascode amplifier (FCA). As seen in Fig. 5.4, two input PMOS transistors in FCA structure are split to 4 equal

transistors in RFCA schematic. When applying a small differential voltage signal $\triangle V_{in}$ between V_{in+} and V_{in-}, the generated small current signal $2gm_2 \triangle V_{in}$ is amplified $(1+k)/2$ times at the outputs of RFCA because of the current mirrors (M6-M11), where gm_2 is the transconductance of M2 (or M3) and k is the ratio of M9 to M8. With this observation, the equivalent transconductance of RFCA can be estimated as

$$Gm_{RFCA} = (1+k) \times gm_2 \tag{5.2}$$

while for FCA structure, we have

$$Gm_{FCA} = 2 \times gm_2 \tag{5.3}$$

According to [2], the reasonble value of k is between 2 to 4. In this design, $k = 3$ is chosen and by using (5.2) and (5.3), $Gm_{RFCA} = 2 \times Gm_{FCA}$ can be achieved. In this case, the RFCA is able to double the equivalent transconductance with the same power consumption and slightly area cost for 4 additional NMOS transistors (M6, M7, M9 and M10).

The second parameter to be studied here is the output resistance RO. With regard to RFCA, the output resistance can be derived as

$$RO_{RFCA} \approx gm_{12} r_{ds12} (r_{ds8} \parallel r_{ds2}) \parallel gm_{13} r_{ds13} r_{ds14} \tag{5.4}$$

where gm_{12} and gm_{13} indicates transconductance of M12 and M13. Moreover, r_{ds2}, r_{ds8}, r_{ds12}, r_{ds13} and r_{ds14} mean small drain source resistance of M2, M8, M12, M13 and M14. Using the same method, RO_{FCA} is also estimated, which has the same representation as (5.5) and it is not shown here. However, the use of less current in M2, M5, M8 and M11 gives rise to an augment of the corresponding r_{ds}. Since Gm_{RFCA} is twice of Gm_{FCA}, the gain of RFCA is 6 dB higher than the gain of FCA considering the same RO. Therefore, an overall DC gain enhancement of $8 \sim 10$ dB can be observed in the RFCA compared to the FCA [2].

The RFCA illustrated in Fig. 5.4 is implemented with $0.18\mu m$ CMOS technology. The simulated DC gain and gain bandwidth product (GBW) under typical conditions is 95 dB and 19 MHz. The second op-amp is a conventional fully differential folded cascode amplifier, which obtained 83 dB gain and 21 MHz GBW.

5.2.2 Single Step Chopping Technique

The accurate sample-to-sample conversion of incremental ADCs demands for low offset. However, if offset cancellation methods were not properly adopted, the offset of op-amps would result in large offset at the digital output of the modulator. The reason is that, for a second-order incremental ADC, the offset of the first op-amp is accumulated parabolically on V_{res} node, while the offset of the second op-amp is linearly integrated at V_{res}. Hence, offset nulling techniques are necessary for incremental modulators. Several offset cancellation methods were proposed in open literature, such as a fractal sequence technique reported in [3] for a third-order modulator. However, the drawback of this technique is its limitation on the number of clock periods per conversion cycle. Another effective method is the single step chopping technique presented in [4], which is adopted in a second-order incremental ADC and the measured residual offset is 1.5 μV.

With regard to the second-order modulator illustrated in 5.1, the offset of the first integrator is the main source of the output offset, but even other contributions affect the overall offset. This circuit compensates for all the sources by a single chopping of the input stage [4]. If a single chopping occurs at the Kth clock cycle out of N, the offset of the first op-amp, V_{os1}, reverses while the remaining source, V_{os2}, referred to the input of the second op-amp is unchanged. In this case, the input referred offset becomes

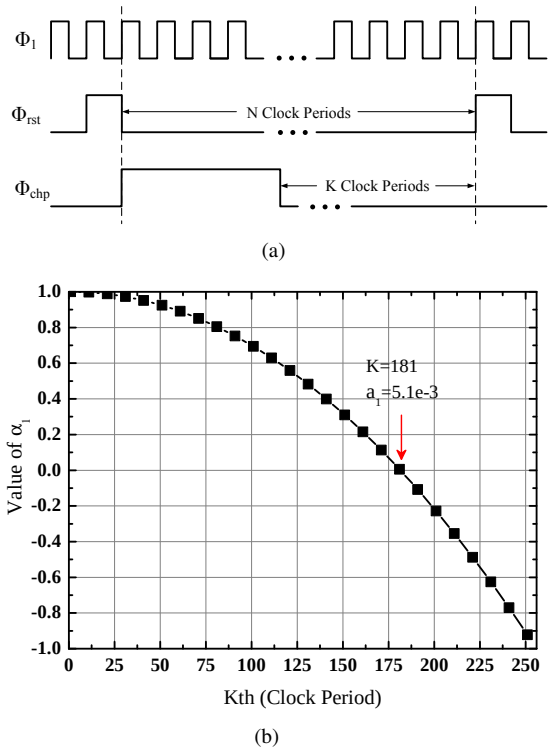


Figure 5.5 (a) Single step chopping clock; (b) The value of α_1 with respect to kth clock period for chopping.

$$\begin{aligned} V_{os,in} &= \left[1 - \frac{2(K-1)(K-2)}{(N-1)(N-2)} V_{os1}\right] + \frac{2}{N-2} V_{os2} \\ &= \alpha_1 V_{os1} + \alpha_2 V_{os2} \end{aligned} \tag{5.5}$$

Fig. 5.5(a) illustrates the chopping clock phase ϕ_{chp} with respect to ϕ_1 and ϕ_{rst}, which is not shown in Fig. 5.3. By trimming the value of K, it is possible to obtain a value of α_1 which compensates for both offset sources. Fig. 5.5(b) plots the value of α_1 versus K. If $N = 256$ and $K = 181$, the offset of the first op-amp is multiplied by $\alpha_1 = 5.1 \times 10^{-3}$ while $\alpha_2 = 7.9 \times 10^{-3}$. V_{os1} diminishes by a factor 196 and V_{os2} is naturally reduced by 127.

5.2.3 Bipolar DAC and Controls

As seen in Fig. 5.3, the bipolar DAC contains 6 unity capacitor with nominal value $C_u = 0.45$ pF. Rewrite (3.10), we have

$$\epsilon_1 + \epsilon_2 + ... + \epsilon_6 = 0 \tag{5.6}$$

As discussed in Section 3.2, the left terminal of each capacitors in bipolar DAC can be connected to V_{ref} or $-V_{ref}$ either during ϕ_q or ϕ_2. With proper control signals $A_1[6:1]$ and $A_2[6:1]$, the bipolar DAC can realize positive, negative or null injection. Tab. 5.1 illustrates the relationship between $D_{out}[12:1]$, $A_1[6:1]$, $A_2[6:1]$ and $V_{mis}(k)$. The $D_{out}[12:1]$ has 13 digital codes, with a decimal

value from 0 to 12. The digital code corresponding to the common mode level is 6. The output swing of the 3-bit DAC is $1.5V_{ref}$.

The following are several examples to explain the usage of Tab. 5.1. For instance, when a digital code 6 is the output of the summation block, its thermometric representation is $D_{out}[12:1] = 000000111111$. Regarding to Tab 5.1, we can find the related control signals are $A_1[6:1] = 111111$ and $A_2[6:1] = 111111$. Hence, The equivalent mismatch $V_{mis}(k)$ introduced in this clock period is 0. However, if the digital code is 1, the corresponding thermometric representation is $D_{out}[12:1] = 000000000001$. Referring to Tab. 5.1, the control signals are $A_1[6:1] = 000000$ and $A_2[6:1] = 011111$. Thus, the related $V_{mis}(k)$ is represented by $-2V_{refm}\sum_{i=1}^{5}\epsilon_i$. Using (5.6), the negative sign can be removed and finally $V_{mis}(k) = 2V_{refm}\epsilon_6$.

Table 5.1 The relationship between $D_{out}[12:1]$ and $V_{mis}(k)$.

$V_{in}[12:1]$	$A_1[6:1]$	$A_2[6:1]$	$V_{mis}(k)$	$V_{mis}(k)$ with (5.6)
111111111111	111111	000000	$2V_{refm}\sum_{i=1}^{6}\epsilon_i$	0
011111111111	111111	100000	$2V_{refm}\sum_{i=1}^{5}\epsilon_i$	$2V_{refm}\sum_{i=1}^{5}\epsilon_i$
001111111111	111111	110000	$2V_{refm}\sum_{i=1}^{4}\epsilon_i$	$2V_{refm}\sum_{i=1}^{4}\epsilon_i$
000111111111	111111	111000	$2V_{refm}\sum_{i=1}^{3}\epsilon_i$	$2V_{refm}\sum_{i=1}^{3}\epsilon_i$
000011111111	111111	111100	$2V_{refm}\sum_{i=1}^{2}\epsilon_i$	$2V_{refm}\sum_{i=1}^{2}\epsilon_i$
000001111111	111111	111110	$2V_{refm}\epsilon_1$	$2V_{refm}\epsilon_1$
000000111111	111111	111111	0	0
000000011111	000000	000001	$-2V_{refm}\epsilon_1$	$2V_{refm}\sum_{i=2}^{6}\epsilon_i$
000000001111	000000	000011	$-2V_{refm}\sum_{i=1}^{2}\epsilon_i$	$2V_{refm}\sum_{i=3}^{6}\epsilon_i$
000000000111	000000	000111	$-2V_{refm}\sum_{i=1}^{3}\epsilon_i$	$2V_{refm}\sum_{i=4}^{6}\epsilon_i$
000000000011	000000	001111	$-2V_{refm}\sum_{i=1}^{4}\epsilon_i$	$2V_{refm}\sum_{i=5}^{6}\epsilon_i$
000000000001	000000	011111	$-2V_{refm}\sum_{i=1}^{5}\epsilon_i$	$2V_{refm}\epsilon_6$
000000000000	000000	111111	$-2V_{refm}\sum_{i=1}^{6}\epsilon_i$	0

5.2.4 Low-Power Comparator

Fig. 5.6 shows the schematic of the fully differential voltage comparator adopted in this second-order incremental modulator [5][6]. The comparator consists of two stages, namely the pre-amplifier and the regenerate latch. Transistors M1-M9 forms the pre-amplifier with 9 dB DC gain and the total biasing current is 0.5 uA with 3.3 V analog power supply. The regenerate latch consists of transistors M10-M17. When the clock signal V_{CLK} is low, the outputs of the comparator V_{OUT+} and V_{OUT-} are reset to 3.3 V. Meanwhile, the intermediate nodes V_X and V_Y are connected with a PMOS switch in order to erase the history information. The outputs of the comparator is generated when V_{CLK} is high. In this case, the pre-amplifier senses the difference of the 4 input terminals and the outputs of the pre-amplifier are V_X and V_Y, which drive the input transistors M18 and M19 of the regenerate latch. With $V_{CLK} = 3.3$ V, the second stage becomes 2 back-to-back CMOS inverter. The difference of discharge speed on V_{OUT+} and V_{OUT-} determines the final outputs. Simulation results show that the typical delay of this comparator is 2 ns and the sensitivity is less than 1 mV. The offset of the comparators does not affect the performance of the modulator, as demonstrated with simulations on both behavioural level and transistor level.

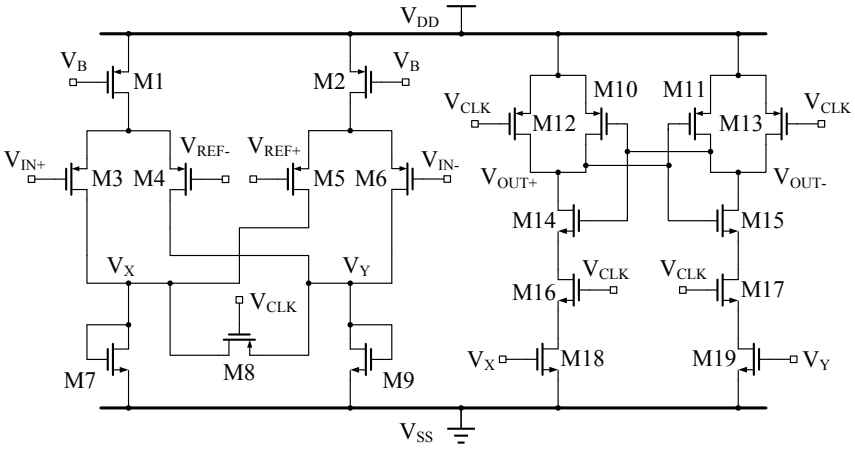


Figure 5.6 Low-power comparator schematic diagram.

5.3 Digital Building Blocks

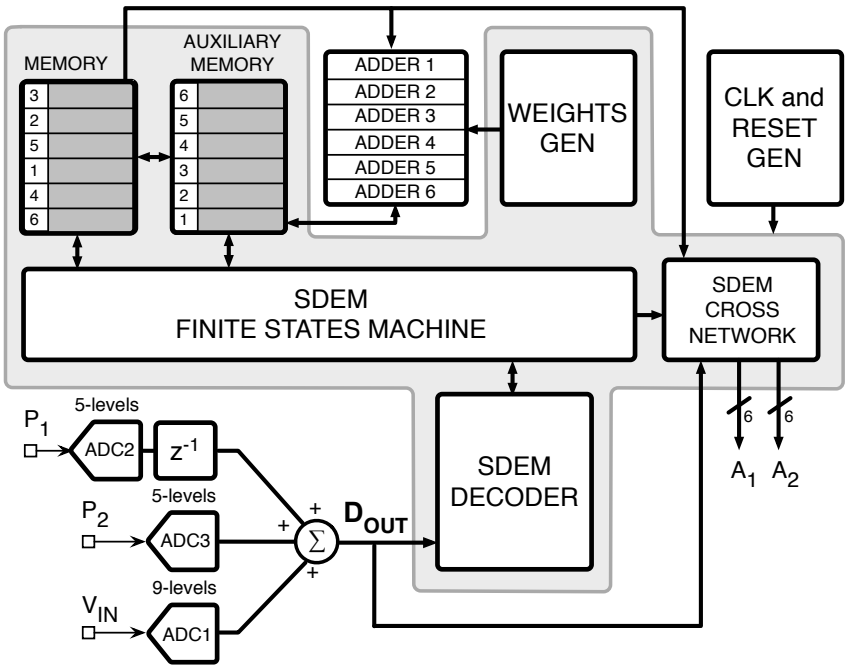


Figure 5.7 The block diagram of Smart-DEM implementation.

This section discusses about the digital circuits employed in the proposed second-order incremental ADC. Since the operation principles of Smart-DEM were comprehensively introduced in Chapter 3, the first part of this section focuses on the implementation of the Smart-DEM algorithm with modern CMOS technology. Following the Smart-DEM block, we shall briefly introduce the second digital block — the multi-phase clock generator.

5.3.1 Smart-DEM Block

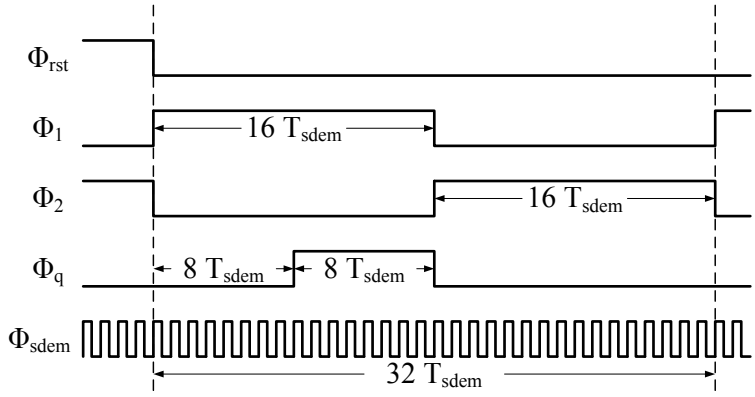


Figure 5.8 Clock phases used in Smart-DEM block.

Fig. 5.7 shows the block diagram of Smart-DEM algorihm implementation in this design. The working flow is as follows: the summation of the outputs of 3 quantizers D_{out} is an integer number ranging from 0 to 12 for 13 levels. The SDEM encoder transform D_{out} to 2 temporary control signals $A_{1t}[6:1]$ and $A_{2t}[6:1]$. Under the control of SDEM finite state machine (FSM), the weight corresponding to the current clock period is calculated. Whereafter, it is added to the weights of the selected unity elements. The insert-sorting algorithm orders the results, temporarily stored in the auxiliary memory. The minimum of values is subtracted to reduce the required length of registers and returned back to the primary memory. The cross network uses the new order of elements in the next clock period to give rise to the $A_1[6:1]$ and $A_2[6:1]$ output control signals.

As depicted in Fig 5.3, the SDEM FSM block is under the control of clock phases ϕ_2, ϕ_q, ϕ_{sdem} and ϕ_{rst}. Fig 5.8 illustrates more detailed relationship of these clock phases. The master clock ϕ_{sdem} runs 32X of the analog sampling clock ϕ_1. When ϕ_q is high, the SDEM FSM uses the current D_{out} and internal information and generates correct control signals $A_1[6:1]$ and $A_2[6:1]$ in $2T_{sdem}$. The rest $6T_{sdem}$ is used for the DAC to charge the unity capacitors. When ϕ_2 becomes high and ϕ_q turns low, $A_1[6:1]$ and $A_2[6:1]$ control the bipolar DAC to properly inject the charge on the first integrator for $16T_{sdem}$. Meanwhile, SDEM FSM updates its internal status and prepares a new sorted table of weights for the operation of the next clock period.

Fig. 5.9 illustrates the transition of state (S_{FSM}) of SDEM FSM. The operation flow is explained as follows: when the modulator is reset by ϕ_{rst}, S_{FSM} is set to RST. As seen in Fig. 5.8, a full analog sampling clock period starts from the positive edge of ϕ_1 to the negative edge of ϕ_2. During the first $8T_{sdem}$, S_{FSM} is set to START and SDEM FSM does not operate. This period is used by the second integrator to inject the charge. When the positive edge of the $9th$ T_{sdem} arrives, the SDEM block receives the input signal from the summation node $D_{out}[12:1]$ and transforms it to $A_{1t}[6:1]$ and

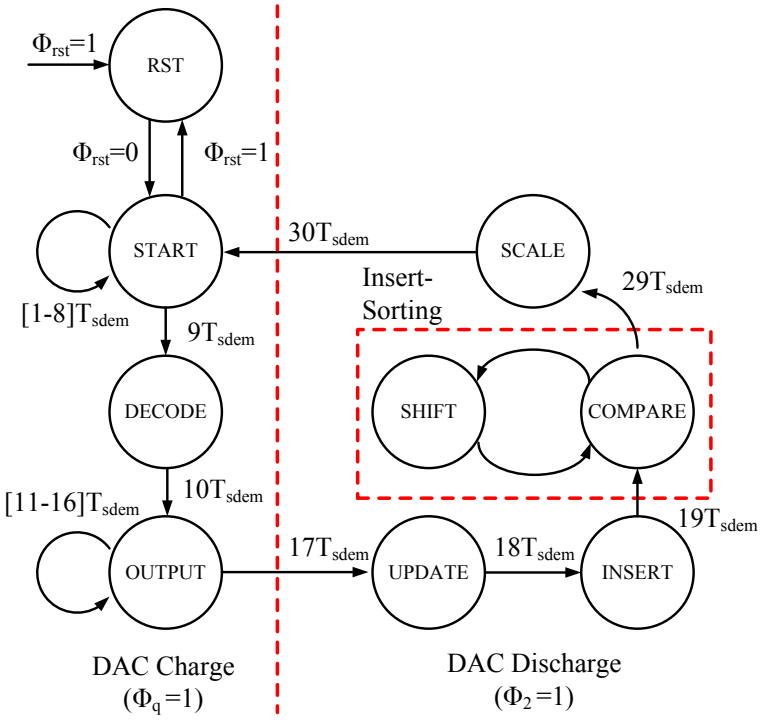


Figure 5.9 State transition diagram of SDEM finite state machine.

$A_{2t}[6:1]$ ($S_{FSM} = DECODE$). In the next T_{sdem}, the cross network uses $A_{1t}[6:1]$, $A_{2t}[6:1]$ and weight table in the primary memory of SDEM to generate the real controls $A_1[6:1]$ and $A_2[6:1]$ ($S_{FSM} = OUTPUT$). From $11th\ T_{sdem}$ to $16th\ T_{sdem}$, the bipolar DAC charges the unity capacitors under the control of $A_1[6:1]$ and $A_2[6:1]$. At the same time, the SDEM FSM simply maintain the status $S_{FSM} = OUTPUT$.

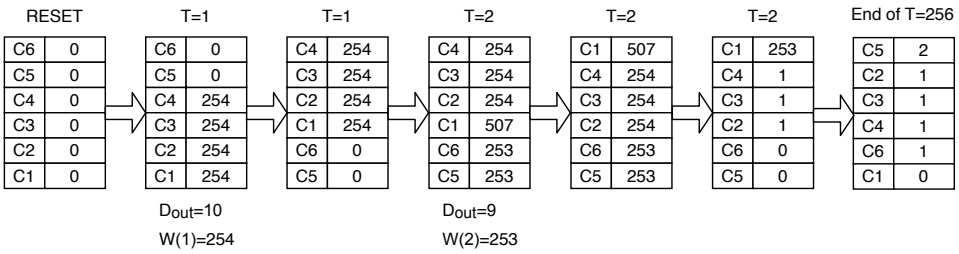


Figure 5.10 The status of the weights in SDEM block with $V_{in} = 0.926V_{ref}$. The range of D_{out} is from 0 to 12 and the common mode level is 6.

When the ϕ_2 is high, the DAC starts to inject its charge on the first integrator. When arriving the positive edge of the first T_{sdem} ($17th\ T_{sdem}$ in the whole analog clock period), SDEM FSM updates the weights of unity elements selected in $10th\ T_{sdem}$ ($S_{FSM} = UPDATE$). Consequently, the weights

of unity elements are no longer in a sorted order. An insert-sorting algorithm is thus performed by SDEM to order the weights. Before the sorting algorithm starts, it is necessary to copy the weights in the primary memory to the backup memory and then reset the main memory to 0. After that, the second step is to insert the weight of the unity elements at the bottom of the backup memory ($S_{FSM} = INSERT$). At this point, the preparation of the insert-sorting algorithm has been finished. The SDEM FSM uses the next $10T_{sdem}$ to sort the weights in the backup memory and than copy these values to the primary memory ($S_{FSM} = SHIFT, COMPARE$). After the sorting algorithm, an operation named scale is performed, which requires all the weights subtract the minimum weight in the primary memory from themselves ($S_{FSM} = SCALE$). The reason of this operation is to prevent hardware overflow, since the word length of the weight is limited. After the scale operation, S_{FSM} is set to START to wait for the operations in the next analog clock period.

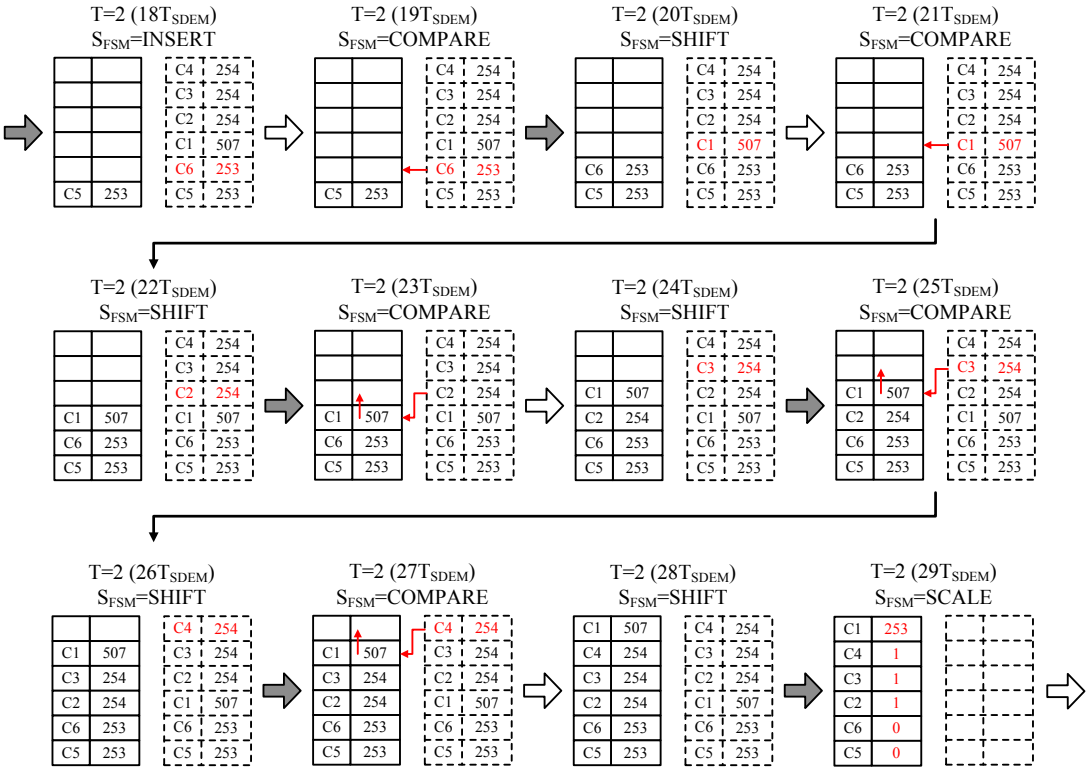


Figure 5.11 Insert-sorting algorithm example for the proposed second-order incremental ADC ($V_{in} = 0.926V_{ref}$ and $T = 2$).

An example of the insert-sorting algorithm in illustrated in Fig. 5.11. This example starts from the $18th$ T_{sdem} in the second analog clock period (T=2) when a constant $V_{in} = 0.926V_{ref}$ is applied to the input of the proposed second-order incremental ADC (Fig. 5.10). As seen in Fig. 5.11, in the $18th$ T_{sdem}, the content of the primary memory (solid-line) is copied to the auxiliary memory (dash-line). Meanwhile, all the weight information in the primary memory is erased except the one at the bottom of the array. An pointer CUR_IDX is set to 253 (C6), which indicates the next weight for insert operation is 253 (C6). In the next T_{sdem}, SDEM FSM compares the weight pointed by the CUR_IDX

with all the weights already inserted in the primary memory. Since 253 (C6) is the same with 253 (C5), SDEM FSM simply insert 253 (C6) at the adjacent position above 253 (C5) in $20th\ T_{sdem}$ and updates the CUR_IDX to point to 507 (C1). Similarly, C1 (507) is inserted into the primary memory at the adjacent position above 253 (C6) and the CUR_IDX points to 254 (C2). However, in the $23rd\ T_{sdem}$, SDEM FSM compares 254 (C2) with 507 (C1), 253 (C6) and 253 (C5) and find out that 507 (C1) is larger than 254 (C2). Under such a situation, in the next T_{sdem}, 507 (C1) is shifted up one position, while 254 (C2) is inserted into the original position occupied by 507 (C1). Following this method, SDEM FSM uses the insert-sorting algorithm to move the larger value to the top of the weight array and smaller value to the bottom. At the end of $28th\ T_{sdem}$, all the weights in the primary memory are in a sorted order. To prevent hardware overflow, the scale operation is performed in the $29th\ T_{sdem}$, which means all the weights need to subtract the minimum weight 253 (C5) from themselves. As seen in Fig. 5.11, the largest weight in the primary memory after the scale operation is 253 (C1) while the minimum one is 0 (C5).

With regard to Smart-DEM implementation, it is firstly described in Verilog-HDL, which is then transformed to a gate-level netlist (about 1.2k gates) by Design Compiler. For the standalone Smart-DEM digital block, NC Verilog is used for both behavioural-level and gate-level verification. Whereafter, a mixed-signal simulator SpectreVeriog is adopted for the full chip verification.

5.3.2 Multi-Phase Clock generator

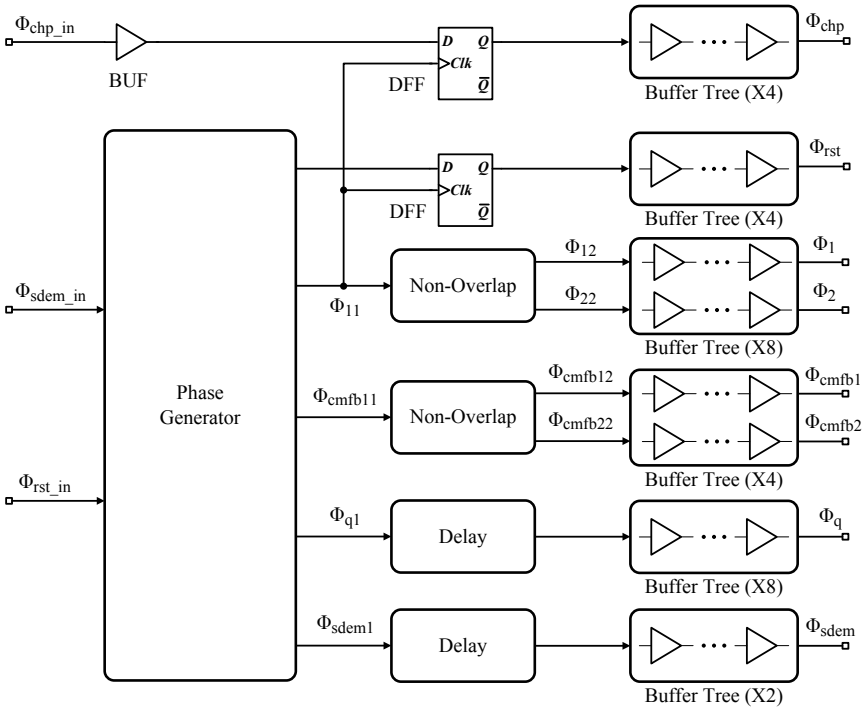


Figure 5.12 Multi-phase clock generator block diagram.

In order to drive the SC circuits and the Smart-DEM block, an on-chip multi-phase clock generator is included in this design. As seen in Fig. 5.12, the inputs of the clock generator are ϕ_{chp_in}, ϕ_{sdem_in} and ϕ_{rst_in}. ϕ_{chp_in} is the chopping signal used for single-step chopping operation. ϕ_{sdem_in} is the master clock of the whole chip, and ϕ_{rst_in} is the reset signal generated manually on the PCB board. The phase generator, as can be seen in Fig. 5.12, is used to generate the analog sampling phase ϕ_{11} and ϕ_{q1} (divide-by-32), clock signal for the common mode feedback (CMFB) of the op-amps ϕ_{cmfb11} (divide-by-256) and reset signal for both analog and digital circuits ϕ_{rst1}. Moreover, the phase generator buffers itself and outputs ϕ_{sdem1}. Meanwhile, 2 D-flip-flops (DFF) are used to align ϕ_{rst1} and ϕ_{chp_in} with ϕ_{11}. It can be noticed that 2 non-overlap blocks are employed. The first one generates 2 non-overlap clocks ϕ_{12} and ϕ_{22}, which are further buffered by X8 buffer trees to become the main analog sampling clock ϕ_1 and ϕ_2. Using ϕ_{cmfb11}, the other non-overlap block generates ϕ_{cmfb12} and ϕ_{cmfb22}. These 2 signals then go though X4 buffer trees and turn into ϕ_{cmfb1} and ϕ_{cmfb2} used for the CMFB circuits of op-amps. In order to compensate for the delay due to the non-overlap blocks, several delays are added to minimize the skew between different clock signal paths. Finally, it can be noticed that a bank of buffer trees are included with different sizes (X2, X4 and X8). These buffer trees are used to boost the driving capability for 8 output clocks, depending on the different loads of various clocks.

5.4 Experimental Results

This section describes the experimental results of the proposed second-order incremental ADC. To start with, the design of testing board and measurement setup are described. Whereafter the measurement results are detailed discussed. A comparison of the proposed modulator with state of the art is given in the last part of this section.

5.4.1 Test Setup

An experimental prototype of the proposed second-order 3-bit incremental ADC is fabricated in a 0.18-0.5-μm CMOS technology with dual poly and 6 metal layers. Fig. 5.13 shows the chip microphotograph with main circuital blocks highlighted. The active area is 1270×900 μm^2 (the chip area is 1600×1300 μm^2). To avoid interferences, a shield of top metal completely covers the capacitive DAC array. The area of the Smart-DEM block is 260×260 μm^2, only 6% of the active area.

The chip was packaged in a 48-pin ceramic quad flat pack (CQFP). Custom 4-layer printed circuit boards (PCBs) were designed to measure the 48-pin CQFP prototype, which includes a mother board and a daughter board. Fig. 5.14 (a) shows the top layer of the mother board designed in Altium software, while Fig. 5.14 (b) illustrates the fabricated board with components soldered. In order to minimize interferences, the mother board contains 3 different power supplies, namely VDDA (3.3 V for analog circuits), VDDD33 (3.3 V for multi-phase clock generator) and VDDD15 (1.5 V for Smart-DEM block). With regard to the usage of 4 layers on the mother board, signals are routed on the top layer and bottom layer. The power plane is on the top layer for VDDA. The remaining 3 layers are used for ground plane. Since there are only serveral connections of the digital power supplies (VDDD33 and VDDD15), they are also routed on the top layer. Meanwhile, the input clocks ϕ_{sdem_in}, ϕ_{rst_in} and ϕ_{chp_in} are routed on the third layer to reduce the interferences, because the 2 adjacent layers are mostly covered by ground signal. The main functions of the mother board are listed below: 1) providing 3 different power supplies and ground; 2) generating adjustable voltage references and current sources; 3) provides interfaces for input signals (V_{in}, ϕ_{sdem}, ϕ_{rst} and ϕ_{chp}) and digital outputs (D_{out}). The

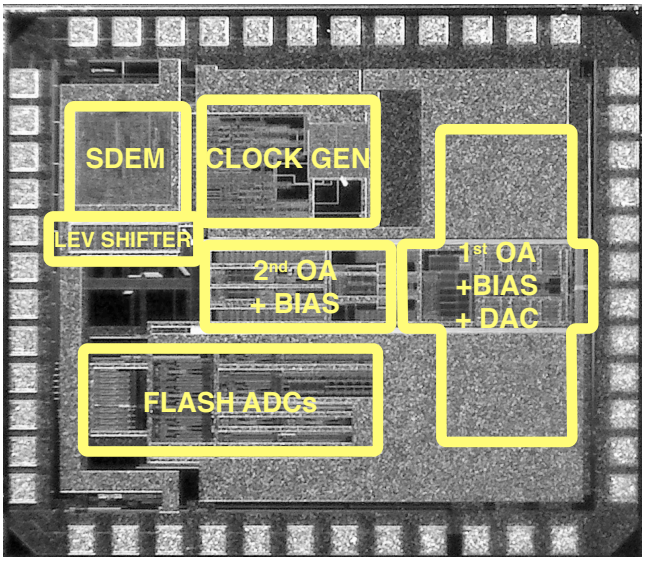
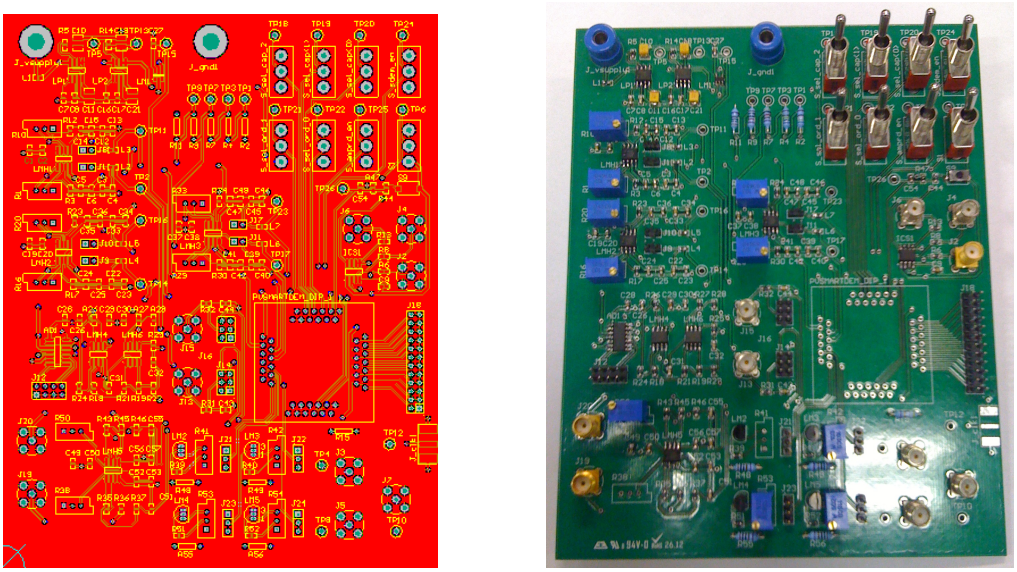


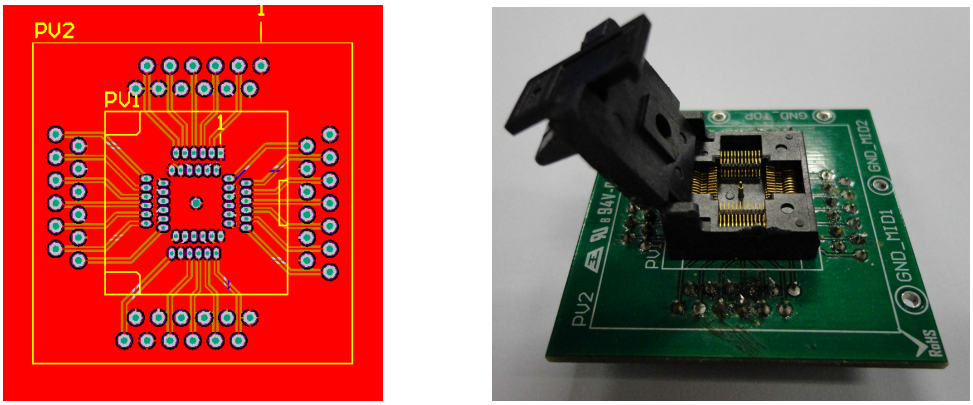
Figure 5.13 PVSMARTDEM chip microphotograph.



(a) (b)

Figure 5.14 (a) Top layer of the mother board in Altium; (b) Fabricated 4-layer test board with components soldered.

daughter board, however, employs a 48-pin socket to hold the chip, allowing fast replacement of chips during measurement. Fig. 5.15 (a) shows the top layer of the daughter board in Altium software. Since the distance between adjacent pins is very small, all the 4 layers are used for routing the signals



(a) (b)

Figure 5.15 (a) Top layer of the daughter board in Altium; (b) Fabricated daughter board with 48-pin socket.

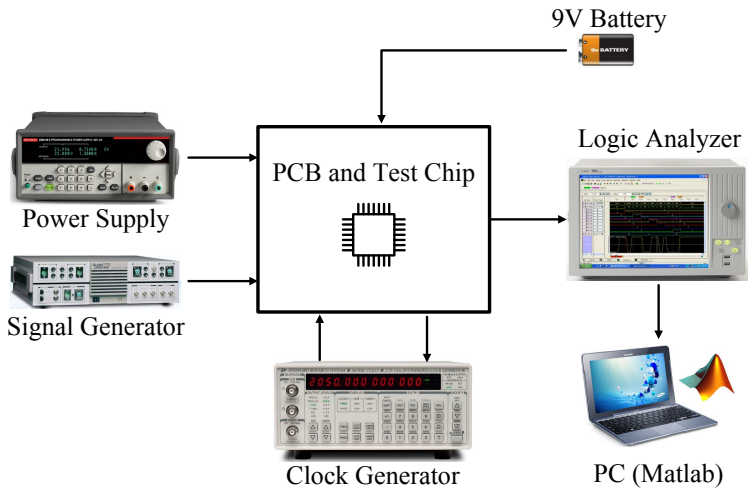


Figure 5.16 Measurement setup block diagram.

(include 3 power supplies and 1 ground). Fig. 5.15 (b) illustrates the fabricated daughter board with the 48-pin socket.

Fig. 5.16 shows the block diagram of the measurement setup. The PCBs together with the chip are powered by a 8 V power supply, which is used by the components on the mother board to generate 3 power supplies mentioned previously. Since the analog sampling frequency of the chip is 10 kHz, a fully differential input signal with a maximum bandwidth 5 kHz is provided by an audio precision signal generator. Meanwhile, the master clock ϕ_{sdem} which runs 32X of the analong sampling frequency (2.56 MHz) and chopping clock phase ϕ_{chp} are produced by a clock generator. A 9 V battery pack is utilized to produce low noise common mode voltage 1.65 V and 2 reference voltages 3.15 V and 0.15 V. The logic analyzer collects the digital output D_{out}, the main analog sampling clock

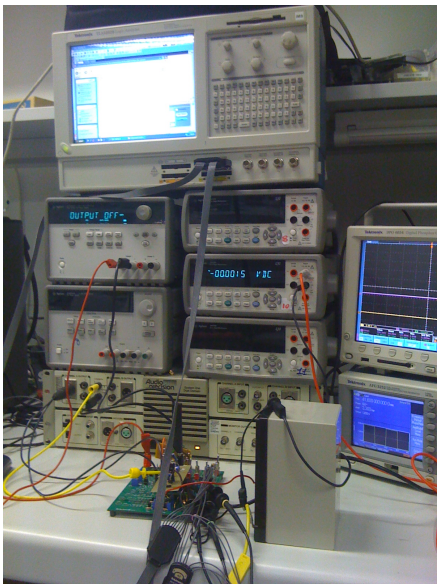


Figure 5.17 Measurement setup in laboratory.

ϕ_1 and the internal reset phase ϕ_{rst} and these signals are then sent to a PC for data processing in Matlab software. Fig. 5.17 shows the measurement setup with various instruments in laboratory.

5.4.2 Measurement Results

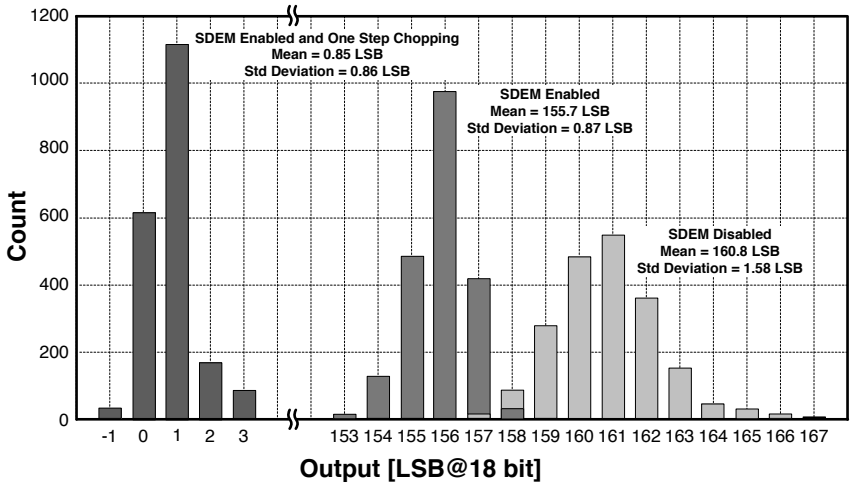


Figure 5.18 Histograms of repeated measures with shorted inputs.

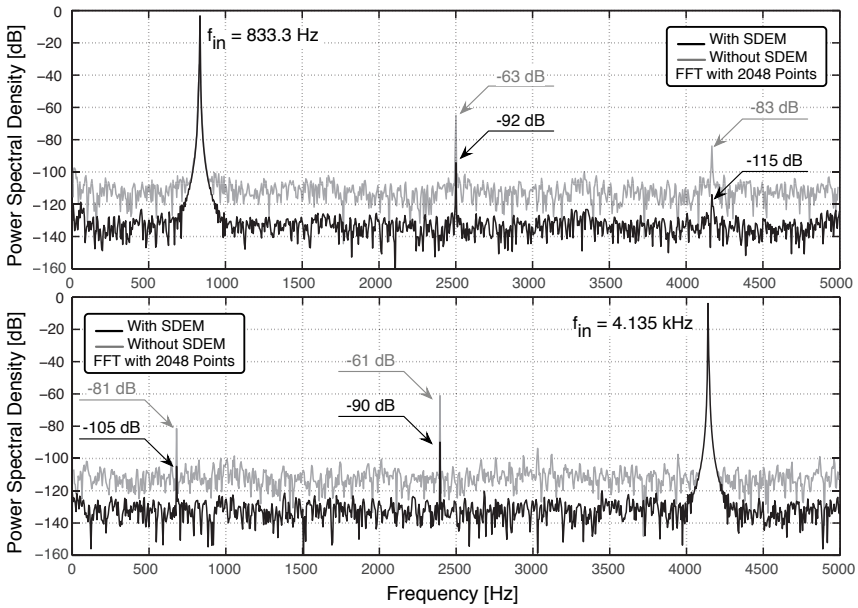


Figure 5.19 Measured output spectra.

Fig. 5.18 gives histograms of 2048 repeated measurements on the same part with zero input. The three histograms are for Smart-DEM block disabled, Smart-DEM enabled, and Smart-DEM enabled plus one step chopping at $K = 180$. The standard deviation of the histograms measures the input referred noise voltage. It is 1.58 LSB (18 μV) and 0.87 LSB (10 μV) without and with Smart-DEM. Indeed, mismatch increases the inaccuracy. The mean of the histogram measures the input offset (160.8 LSB = 1.84 mV and 155.7 LSB = 1.78 mV, respectively). Again, the mismatch causes the difference. The one step chopping at $K = 180$ leads to $\alpha_1 = 16.1 \times 10^3$; the residual offset becomes 0.85 LSB (9.7 μV). The result indirectly estimates a -2.42 mV offset for the second op-amp.

Fig. 5.19 shows the converter output spectra (FFT with 2048 points) with $2dB_{FS}$ sine waves at 833.3 Hz and 4.135 kHz, respectively, with and without SDEM. With SDEM and low frequency, the measured SNDR is 105 dB, equivalent to 17.15 bit. The SNDR at Nyquist drops by 1.3 dB with a loss of 0.22 bit. Third harmonic distortion dominates the SFDR: 92 dB with low frequency signal and 90 dB when the signal is close to the Nyquist frequency. The fifth harmonic is well below the third one in both cases. As Fig. 5.19 shows, the SNDR value drops to 82 dB without Smart-DEM and harmonics are significant.

Fig. 5.20 illustrates the DNL obtained with the sine wave histogram method and an input sine wave of $50 - mV_{pp}$. The limited explored interval results from the memory of the instrument (8 Mb). The measured DNL within the $[-0.8, 1]$ LSB range confirms the value of measured SNDR.

The measured power consumption of the modulator is about 200 μW for the analog part and 80 μW for the digital part. The achieved FOM_S is 177.5 dB following the Schreiers formula, while it is equal to 190 fJ/conv-step when using the Waldens expression (FOM_W).

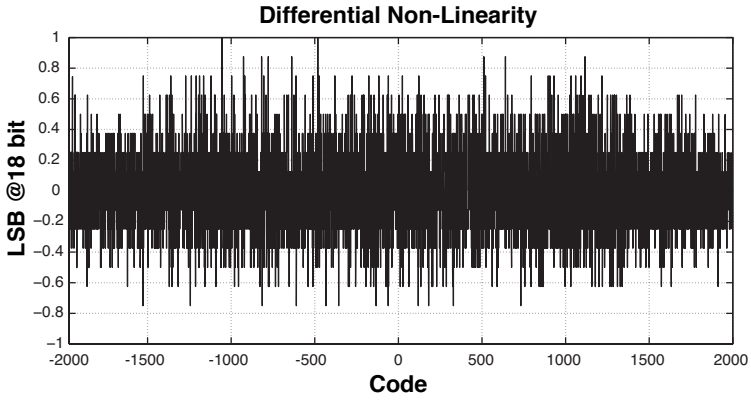


Figure 5.20 Measured DNL.

Table 5.2 Performance Comparison between proposed incremental ADC with state of the art.

	This Work	ISSCC2013 [7]	ISSCC2013 [8]	ANALOG INTEGR CIRC S.[4]	JSSC2010 [9]	JSSC2005 [3]
Year	**2013**	2013	2013	2012	2010	2006
BW (Hz)	$\mathbf{5 \cdot 10^3}$	12.5	667	$1 \cdot 10^3$	$500 \cdot 10^3$	7.5
F_S (Hz)	$\mathbf{10 \cdot 10^3}$	25	$1.333 \cdot 10^3$	$2 \cdot 10^3$	$1 \cdot 10^6$	15
SNDR (dB)	**105**	119.8	81.9	110.7	86.3	123
Power (mW)	**0.28**	$6.3 \cdot 10^{-3}$	$19.9 \cdot 10^{-3}$	6	38.1	0.6
V_{DD} (V)	**3.3**	1.8	1.0	3.3	1.8	2.7-5.0
Technology (μm)	**0.5-0.18**	0.16	0.16	0.6-0.18	0.18	0.6
FOM_W (fJ/conv-step)	**192.6**	314.8	1475.7	5722	1460	9537
FOM_S (dB)	**177.5**	182.7	157.1	162.8	160.3	166.4

5.4.3 Performance Comparison

Tab. 5.2 summarizes performances of the proposed second-order incremental ADC and state of the art counterparts. As seen in Tab. 5.2, the obtained FOM_W and FOM_S can be ranked among the best of the selected incremental ADCs. The reason that the proposed modulator achieved good power efficiency, in the first place, is the significant enhancement of conversion efficiency and the reduction of analog power dissipation due to multi-bit quantization. Although a Smart-DEM block is introduced, its power consumption can be quite limited when a low digital power supply is utilized. Secondly, the 17.15-bit resolution over a 5 kHz bandwidth benefits the power efficiency. When targeting to 20-bit or more resolution, incremental modulators suffer from more stringent requirements on the kT/C noise limitation and other analog specifications, such as incremental ADCs reported in [7], [4] and [3]. The

second-order incremental modulator presented in [9], however, achieved 86.3 dB SNDR over a 0.5 MHz bandwidth. According to the best of author's knowledge, this is the highest bandwidth attained by incremental modulators. Under such a situation, the power efficiency is degraded and the obtained FOM_W is 1.46 pF/conv-step. Since the proposed modulator aims at 18-bit resolution (measured 17.15-bit) with 5 kHz bandwidth, these specifications are relatively low compared with the values aforementioned, hence, they are good for incremental modulators to achieve high power efficiency.

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CHAPTER 6

A 12-BIT SINGLE OP-AMP 0+2 $\Sigma\Delta$ A/D CONVERTER

This chapter describes a 12-bit 2-stage $\Sigma\Delta$ ADC implemented with single op-amp. The first stage consists of a 3-bit ADC and DAC, which transforms the input to a coarse digital code together with a quantization error. This quantization error then enters a second-order $\Sigma\Delta$ stage and the output is a fine digital code. The final digital output is the combination of both the coarse part and the fine digital code. The structure benefits from the single op-amp implementation which leads to a second-order noise shaping. The output swing of the op-amp is significantly reduced due to the first-stage, thus, allowing to spare power. With 0.18 μm CMOS technology, simulation results shows that the proposed structure obtains more than 12-bit resolution over a 2 MHz bandwidth. The power consumption is 1.7 mW and the corresponding Figure of Merit ($\mathrm{FOM_W}$) is 104 fJ/conv-step.

6.1 General Considerations

As already mentioned in Chapter 2, $\Sigma\Delta$Ms are always used to achieve high resolution A/D conversion without the need of precisely matched analog components. According to [1] [2], DT $\Sigma\Delta$Ms are good candidates to attain medium-to-high resolution for a bandwidth less than 2MHz. While the CT counterparts are more appropriate to obtain low-to-medium resolution with more than 10 MHz bandwidth. Thus, the starting point of the research of $\Sigma\Delta$Ms is to familiarize with the target specifications, which are listed again as follows:

► **Resolution**: 12-bit

► **Bandwidth**: 2 MHz
► **Power Consumption**: ≤2 mW

In order to meet the above specifications, ΣΔ architectures with DT fashion are taken into consideration. The basic design parameters of ΣΔMs are the order of the structure L, resolution of the quantizer q_b and oversampling ratio (OSR). For stable ΣΔ schemes with denominator equal to 1 in the STF and NFT, the maximum achievable SNR in terms of those parameters can be estimated by (2.13), which is rewritten here for readers' convenience

$$SNR_{Lord,\Sigma\Delta} = 1.78 + 6.02q_b - 10log\frac{\pi^{2L}}{2L+1} + 3.01(2L+1)log_2(OSR) \tag{6.1}$$

Using (6.1), we can calculate the corresponding design parameters in order to meet the specifications listed above. Tab. 6.1 shows the possible combinations of design parameters where $2 \leq L \leq 3$, $3 \leq b_q \leq 5$ and $8 \leq$ OSR ≤ 32.

Table 6.1 Achievable SNR in terms of L, q_b and OSR.

L	q_b	OSR	F_s	SNR	ENOB
2	3	8	32 MHz	52.09 dB	8.36-bit
2	3	16	64 MHz	67.14 dB	10.86-bit
2	3	32	128 MHz	82.19 dB	13.36-bit
2	4	8	32 MHz	58.11 dB	9.36-bit
2	4	16	64 MHz	73.16 dB	11.86-bit
2	4	32	128 MHz	88.21 dB	14.36-bit
2	5	8	32 MHz	64.13 dB	10.36-bit
2	5	16	64 MHz	79.18 dB	12.86-bit
2	5	32	128 MHz	94.23 dB	15.36-bit
3	3	8	32 MHz	61.67 dB	9.95-bit
3	3	16	64 MHz	82.74 dB	13.45-bit
3	3	32	128 MHz	103.81 dB	16.95-bit
3	4	8	32 MHz	67.69 dB	10.95-bit
3	4	16	64 MHz	88.76 dB	14.45-bit
3	4	32	128 MHz	109.83 dB	17.95-bit
3	5	8	32 MHz	73.71 dB	11.95-bit
3	5	16	64 MHz	94.78 dB	15.45-bit
3	5	32	128 MHz	115.85 dB	18.95-bit

Since the target is to achieve 12-bit resolution with minimum power consumption, the design strategy is to avoid using high-order ΣΔ structures and to adopt relatively low sampling frequency. The multi-bit quantization and DAC can be employed. In this case, the chosen architecture should guarantee a minimum input range of the quantizer in order to reduce the number of comparators. Another problem related to the multi-bit quantization is the non-linearity of the DAC. Generally for 12-bit resolution, the non-linearity of multi-bit DAC does not have a significant impact of the modulator's performance. However, extensive simulations are still needed to ensure the achievable resolution.

On the basis of above analysis, certain architectures and design parameters can be chosen from Tab. 6.1. The preferable choices are: (1) $L = 2, q_b = 5$ and OSR=16; (2) $L = 3, q_b = 5$ and OSR=8. In

the former case, the ΣΔM benefits from a low order loop filter and a moderate OSR. The resolution of quantizer is affordable since the maximum number of comparators used is $2^{q_b} = 32$. In case 2, the third-order loop filter benefits the ΣΔM from a low OSR=8, which corresponds to 32 MHz sampling frequency for $B_W = 2$ MHz. Meanwhile, the resolution of the quantizer is also 5. In both cases, by using effective ΣΔ architectures, the input range of the quantizer can be significantly reduced, giving rise to reduction of comparators.

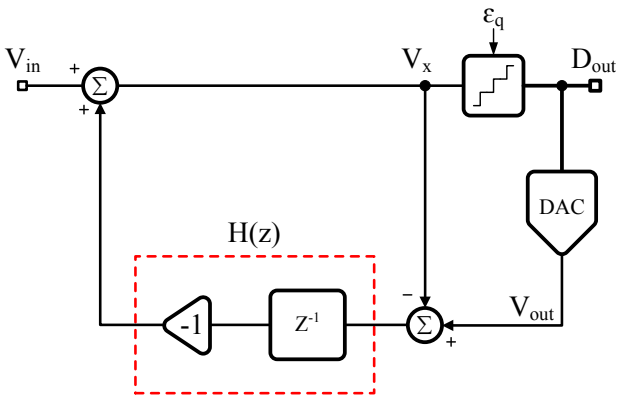

Figure 6.1 First-order ΣΔ ADC block diagram.

With regard to the selection of ΣΔ architectures, the key point is to reduce the power consumption while achieve the target performance. One effective way to minimize the power dissipation, as discussed in Chapter 2, is to reduce the number of op-amps used in the loop-filter. The technique proposed here is different from the integrator multiplexing [3] or double-sampling [4] and it can obtain high-order NTF with single op-amp. We begin the discussion with the first-order ΣΔ structure illustrated in Fig. 6.1, where the quantization error ϵ_q can be estimated by the difference between V_{out} (analog version of D_{out}) and V_X. After one unit time delay, the quantization error is added with V_{in} and the summation result is V_X. To have a better understanding of this structure, the transfer function is expressed in z-domain as follows

$$D_{out}(z) = V_{in}(z) + (1 - z^{-1})\epsilon_q(z) \tag{6.2}$$

where $NTF(z) = 1 - z^{-1}$, which is a conventional first-order high-pass filter.

The scheme plotted in Fig. 6.1 can be easily extended to higher-order ΣΔ architectures, by modifying the transfer function inside the dash box. Using the similar method, a second-order ΣΔ structure is shown in Fig. 6.2. Notice that the difference of this scheme with the one plotted in 6.1 is H(z), which can be represented by

$$H(z) = z^{-2} - 2z^{-1} \tag{6.3}$$

Consequently, the transfer function of the second-order ΣΔM can be described as

$$D_{out}(z) = V_{in}(z) + (1 - z^{-1})^2\epsilon_q(z) \tag{6.4}$$

where the quantization error ϵ_q is shaped by a second-order high-pass NTF. According to the design parameters chosen before ($L = 2, q_b = 5$ and OSR=16), this second-order ΣΔM should obtain 12.86-bit resolution. Behavioural-level simulations demonstrate the expected performance as plotted in Fig.

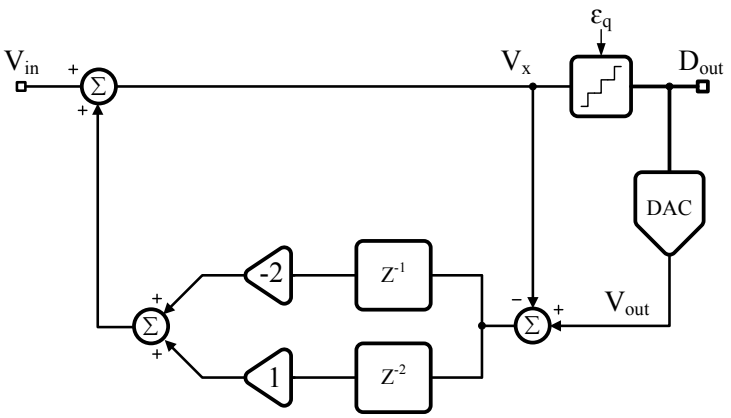

Figure 6.2 Second-order ΣΔ ADC block diagram.

6.3. A -3 dB_{FS} sinusoid waveform at normalized frequency 0.0021 is applied at V_{in} and the PSD of D_{out} shows that the achieved SNDR is 76.7 dB. The result is almost ideal compared with the theoretic value listed in Tab. 6.1.

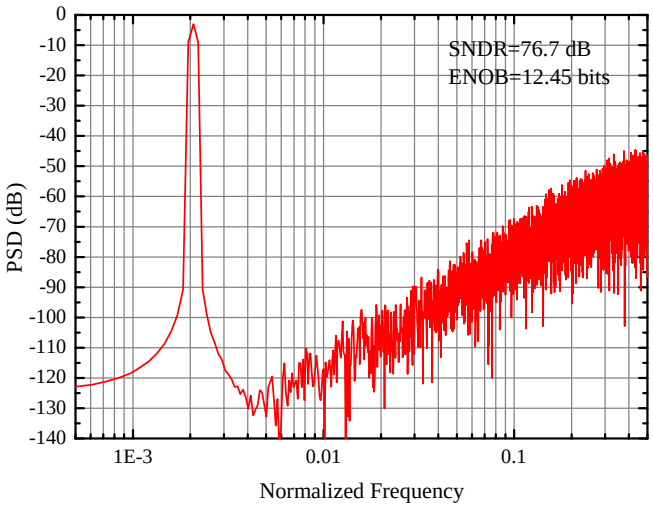

Figure 6.3 PSD (8096-point FFT) of D_{out} of the second-order ΣΔ ADC with ideal 5-bit DAC. The input signal is a sinusoid waveform at normalized frequency 0.0021 whose amplitude is -3 dB_{FS}. The OSR is 16.

Similarly, a third-order ΣΔ architecture can be obtained. Fig. 6.4 illustrates the block diagram of a third-order scheme whose H(z) can be depicted as

$$H(z) = -z^{-3} + 3z^{-2} - 3z^{-1} \tag{6.5}$$

It is evident that the quantization noise is shaped by a third-order high-pass NTF, since (6.6) holds

$$D_{out}(z) = V_{in}(z) + (1 - z^{-1})^3 \epsilon_q(z) \tag{6.6}$$

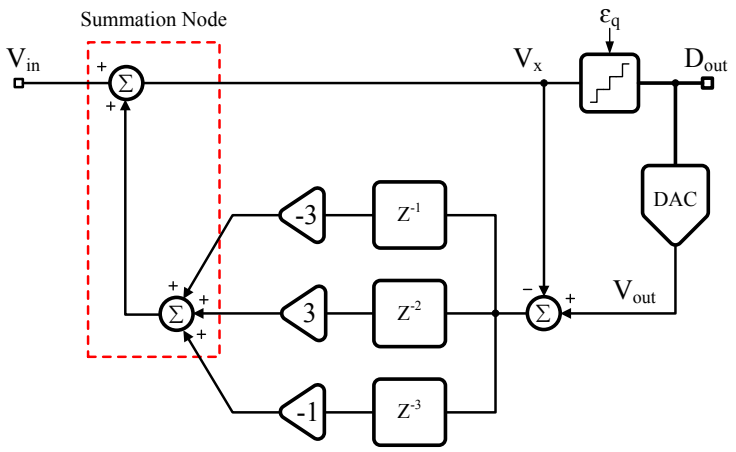

Figure 6.4 Third-order ΣΔ ADC block diagram.

In general, the number of integrators inside ΣΔ loop filter determines the order of the scheme. Nonetheless, architectures shown in Fig. 6.2 and Fig. 6.4 are able to realize second-order and third-order NTF without integrator. Compared with conventional ΣΔMs, the aforementioned ΣΔ architectures are of significant advantages. However, there are a few problems which can not be neglected.

The first issue is the implementation of an accurate summation node. Let us take the third-order structure plotted in Fig. 6.4 as an example. The main operation performed by this structure is the summation of V_{in} with different versions (delay and coefficient) of ϵ_q. Intuitively, this summation function should be with high accuracy. Otherwise, NTF may change due to the inaccuracy of summation and a good third-order noise shaping cannot be guaranteed. One way to realize the add function is to use op-amp together with SC circuits. Fig. 6.5 shows a conventional OTA-based analog adder. In phase ϕ_1, V_1 and V_2 charges C_1 and C_2. Meanwhile, ϕ_{rst} reset the output of op-amp V_X. Then during ϕ_2, the charge on C_1 and C_2 is transferred to C_3. According to this operation flow, an ideal transfer function can be derived

$$V_3(z) = \frac{C_1}{C_3}V_1(z) + \frac{C_2}{C_3}V_2(z) \tag{6.7}$$

Consider the op-amp with finite DC gain A_0 while the bandwidth and slew rate are unlimited. With mathematical calculation, a more precise transfer function is

$$V_3(z) = \frac{C_1}{C_3 + \frac{1}{A_0}(C_1 + C_2 + C_3)}V_1(z) + \frac{C_2}{C_3 + \frac{1}{A_0}(C_1 + C_2 + C_3)}V_2(z) \tag{6.8}$$

Using (6.8), simulations show that for third-order ΣΔ structure, the required A_0 is at least 80 dB. In reality, because of the limitation on bandwidth and slew rate, the desired A_0 may even higher than the value mentioned above.

To achieve an accurate summation node, the bandwidth of op-amp should also be taken into consideration. In Fig. 6.5, supposing the branch of V_2 is disabled and A_0 is infinite, the transfer function from V_1 to V_3 in time domain can be expressed as

$$V_3(nT + T) = V_1(nT + \frac{T}{2})(1 - e^{\frac{-\beta \cdot T}{2 \cdot \tau_0}});\ \tau_0 = \frac{1}{2 \cdot \pi \cdot GBW} \tag{6.9}$$

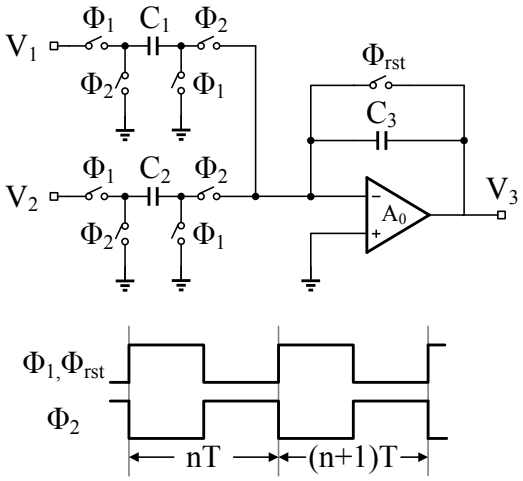

Figure 6.5 Typical OTA-based analog summation block.

where $\beta = C_3/(C_1 + C_3)$ is the feedback factor and GBW is the close loop gain bandwidth product of the op-amp. As seen in (6.9), when a fixed GBW is given, the operation speed of the circuit is determined by the feedback factor β. For the first-order structure illustrated in Fig. 6.1, the calculated β_{1ord} is 1/3. With regard to the second-order and third-order architectures, corresponding feedback factor reduces to 1/5 and 1/9. Hence, in order to obtain the same accuracy of dynamic response as that of the first-order architecture, GBW_{2ord} and GBW_{3ord} should be 1.67 and 3 times of GBW_{1ord}.

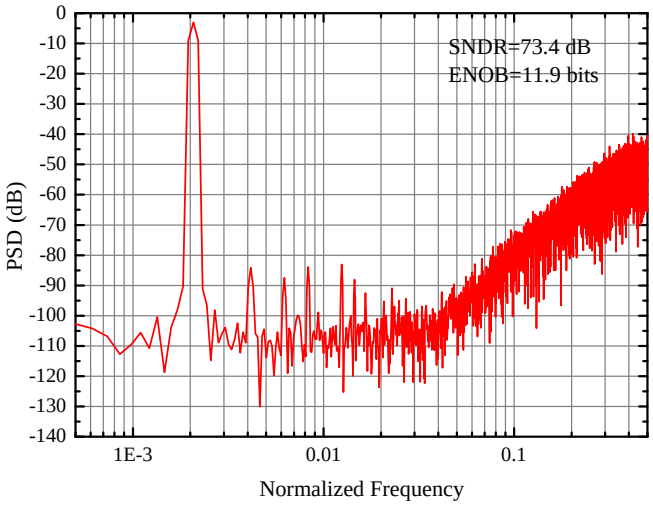

Figure 6.6 PSD (8096-point FFT) with $\sigma = 0.1\%$ mismatch for three 5-bit DACs. The input signal is a sinusoid waveform at normalized frequency 0.0021 whose amplitude is -3 dB_{FS}. The OSR is 16.

Secondly, the voltage swing of V_X is large since it contains a component equal to V_{in}. According to (6.4) and (6.6), the transfer function from $\mathrm{V_{in}}$ to $\mathrm{V_X}$ of the second-order architecture is

$$V_X = V_{in}(z) + (z^{-2} - 2z^{-1})\epsilon_q(z) \tag{6.10}$$

while for the third-order scheme

$$V_X = V_{in}(z) - (z^{-3} - 3z^{-2} + 3z^{-1})\epsilon_q(z) \tag{6.11}$$

If the summation node were implemented with op-amp, the large output swing would result in considerable dynamic error due to the limitations on slew rate and bandwidth. Moreover, since V_X is applied directly to the input of the quantizer, larger V_X means more comparators should be utilized in the scheme and thus more power consumption is required.

The third problem, as mentioned before, comes from the non-linearity of the multi-bit DAC. To demonstrate this point, the third-order $\Sigma\Delta$ scheme illustrated in Fig. 6.4 is selected as our experimental architecture. Design parameters $b_q = 5$ and OSR=16 are chosen. Ideally, the achievable SNDR is 92.3 dB (ENOB=15.04-bit) when a $-3dB_{FS}$ sinusoid waveform with normalized frequency 0.0021 is applied to V_{in}. Fig. 6.6 shows the PSD (8096-point FFT) under $\sigma = 0.1\%$ mismatch of the 5-bit DAC. The achieved SNDR is 73.4 dB (ENOB=11.9-bit) and the degradation of performance is 3.14-bit.

6.2 Proposed Scheme

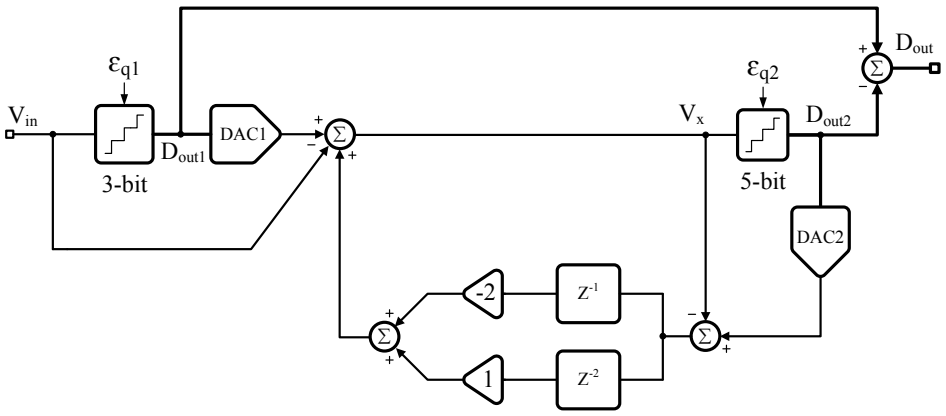

Figure 6.7 Proposed 2-stage $\Sigma\Delta$ ADC block diagram (without integrator).

Fig. 6.7 illustrates the block diagram of the proposed 2-stage $\Sigma\Delta$ ADC. The first stage uses a 3-bit quantizer to digitize V_{in} and generates a coarse digital output D_{out1}. The equivalent input of the second stage, ϵ_{q1}, goes through a second-order $\Sigma\Delta$ structure which is equal to the scheme plotted in Fig. 6.2. The quantization noise of the second stage ϵ_{q2} is shaped by a second-order NTF and the digital output is D_{out2}. The combination of D_{out1} and D_{out2} generates the final digital output of the modulator D_{out}. According to the operation principles, the ideal transfer function can be derived as

$$D_{out}(z) = V_{in}(z) - \epsilon_{q2}(z)(1 - z^{-1})^2 \tag{6.12}$$

To meet target specifications, design parameters $q_b = 5$ and OSR=16 are selected. Based on Tab. 6.1, the proposed 0+2 $\Sigma\Delta$ architecture can obtain an theoretic 12.86-bit resolution. This architecture avoid using the third-order scheme shown in Fig. 6.4 because the requirement on summation node is very difficult to achieve. Moreover, the third-order architecture demands for a strict matching accuracy about $\sigma = 0.05\%$ between unity elements in DAC. With regard to the proposed second-order architecture illustrated in Fig. 6.7, the input swing of $\Sigma\Delta$ stage is significantly reduced with the help of the first stage, giving rise to low-power design. The OSR is 16 for a 2 MHz signal bandwidth. The corresponding sampling frequency F_S is 64 MHz, which is quite affordable considering the budget of the total power consumption of the modulator.

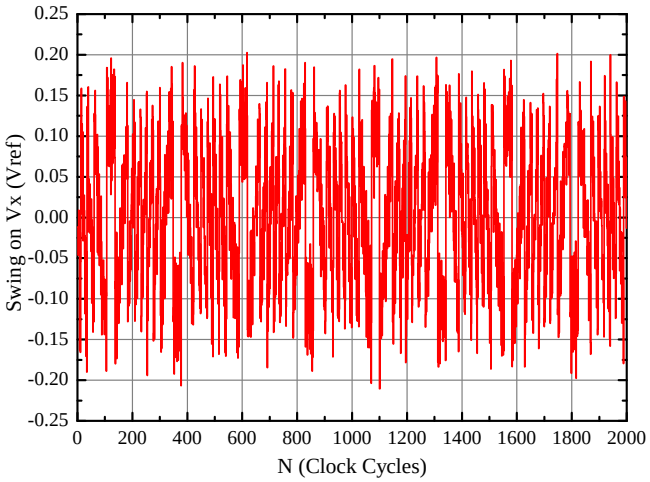

Figure 6.8 Voltage swing on V_X node when $-3dB_{FS}$ sinusoid input at normalized frequency 0.0021 is given.

A few practical design issues related to the proposed second-order architecture are discussed below.

Firstly, let us investigate the voltage swing on V_X, since it affects both the summation accuracy and the power consumption. Fig. 6.8 illustrates the waveform on V_X given $-3dB_{FS}$ sinusoid input at normalized frequency 0.0021. It can be noticed that the voltage swing on V_X is limited within $0.2V_{ref}$. With this value, the number of comparators used in the 5-bit quantizer can be reduced to 8. Thus, the total number of comparators in the modulator is 16. For the op-amp based summation node, low swing loosens the requirements on slew rate and bandwidth and benefits the modulator from low power consumption.

In terms of summation node, we use op-amp based analog adder and related specifica-tions of op-amp are studied. When an op-amp with DC gain A_0 is used, the derived inaccuracy of the summation node is $5/(\mathrm{A}_0 + 5)$. Simulations show that the minimum required DC gain to attain 12-bit resolution is 80 dB. Since a 0.18 μm CMOS technology is utilized in this design, 80 dB DC gain is not difficult to achieve. The feedback factor β_{2ord} of the op-amp is 1/5, which still significantly affects the settling speed of the integrator. As specified later, with certain techniques on circuit implementation, β_{2ord} can be effectively reduced to 1/3 and thus the settling behavioural of the op-amp is improved.

For the non-linearity of DACs, similar simulations are also performed to explore the feasible range of mismatch. Simulation results show that for DAC1, the mismatch is not sensitive. Even $\sigma = 1.0\%$

mismatch can give rise to good conversion result. However, the non-linearity of DAC2 is very critical. Behavioural level simulation results indicate that the mismatch should be limited within $\sigma = 0.2\%$.

The circuit level implementation of the proposed second-order $\Sigma\Delta$M starts from the estimation of the minimum input capacitance. In this design, we use a 0.18μm CMOS technology with 1.8 V analog power supply. According to Section 3.1, the calculated C_S with design parameters $V_{FS} = 1.8V$, OSR=16 and $ENOB = 12$ is 16 fF, which means that the kT/C noise is not a dominant limitation.

Table 6.2 Phases and Operations.

	ϕ_1	ϕ_2	ϕ_q
$\epsilon_{q1}(z)$	Charge	Inject	–
$z^{-2}\epsilon_{q2}(z)$	–	Inject	Charge
$-2z^{-1}\epsilon_{q2}(z)$	Inject	–	Charge

As mentioned before, the feedback factor is 1/5 for the second-order structure proposed in Fig. 6.7. Notice the summation operation can be divided into two parts, the first part is $\epsilon_{q1}(z)$ and the $z^{-2}\epsilon_{q2}(z)$. The other part is $-2z^{-1}\epsilon_{q2}(z)$. To improve the feedback factor, the analong sampling clock period is divided into 3 equal parts, namely ϕ_1, ϕ_2 and ϕ_q. The operations of charge and injection of each branch are shown in Tab. 6.2. In ϕ_1, $\epsilon_{q1}(z)$ charges the input sampling capacitor while $-2z^{-1}\epsilon_{q2}(z)$ injects its charge on the op-amp. Then during ϕ_2, both $\epsilon_{q1}(z)$ and $z^{-2}\epsilon_{q2}(z)$ inject the charge on the op-amp. After ϕ_1 and ϕ_2, the new summation value V_X is ready. In ϕ_q, this value is used to charge the 2 analog delay lines which will be utilized in the next clock period. At the same time, the quantizer compares V_X with references and determines digital output D_{out2}. In this case, β_{2ord} can be improved to 1/3. However, the drawback is the time for each operation is 2/3 of that when only 2 equal clock phases are used.

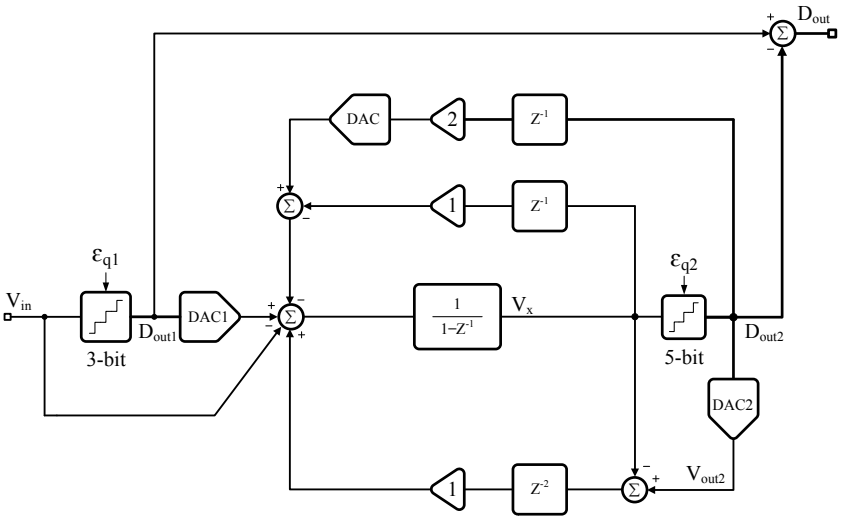

Figure 6.9 Proposed 2-stage $\Sigma\Delta$ ADC block diagram (with integrator).

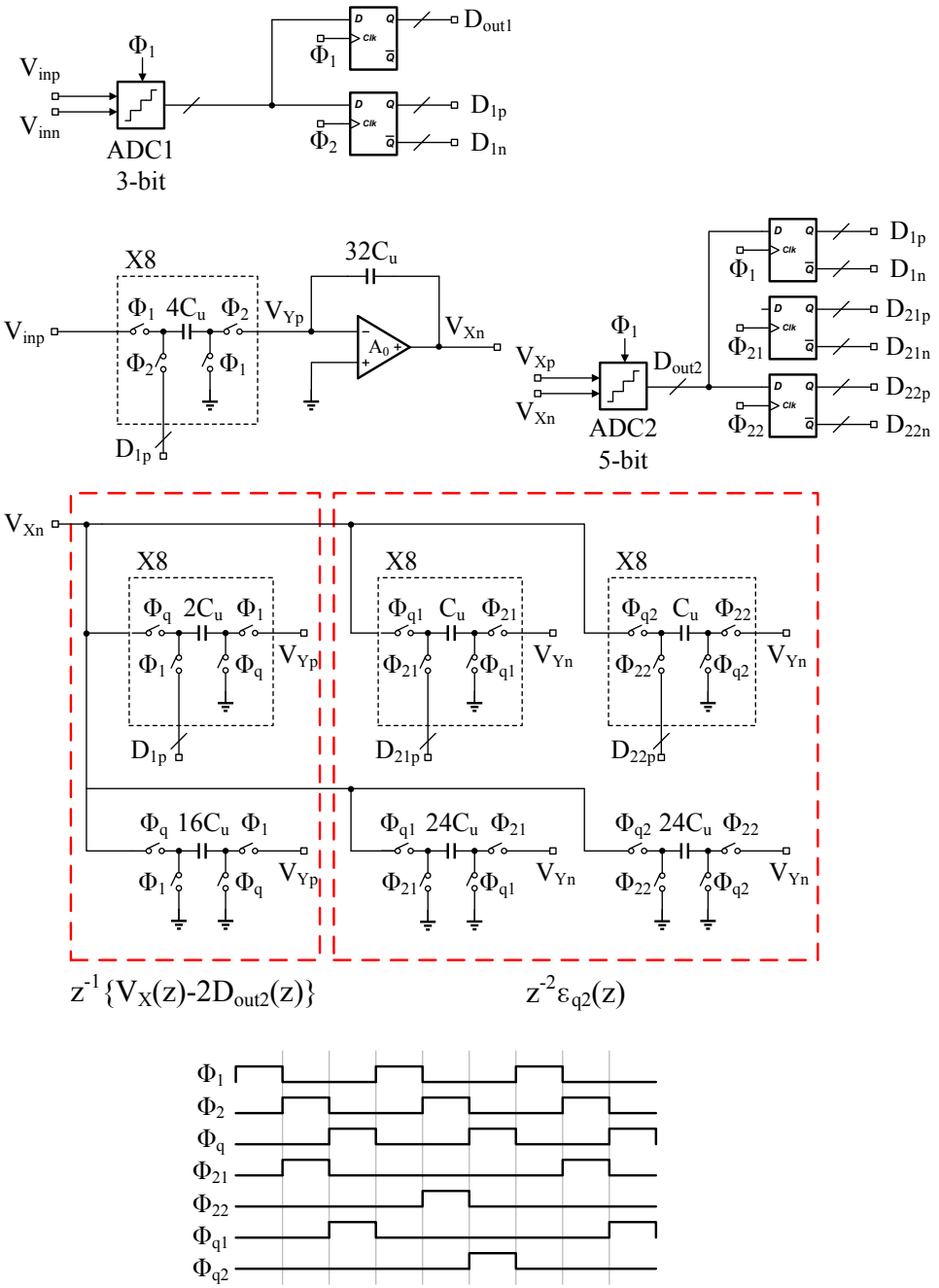

Figure 6.10 Proposed 2-stage ΣΔ ADC schematic diagram.

The other important aspect is that, since an op-amp is used to implement the summation node, there should be an additional clock phase to reset the output of the op-amp. This extra phase needs

considerable time to discharge completely so that it does not disturb the following operation. Since F_S is 64 MHz and the analog clock period is 15.625 ns. It is not wise to spare a portion of the time to discharge the op-amp. In order to solve this problem, the branch of $-2z^{-1}\epsilon_{q2}(z)$ is divided into 2 parts, which can be described as

$$\begin{aligned} -2z^{-1}\epsilon_{q2}(z) =& -2z^{-1}\{V_{out2}(z) - V_X(z)\} \\ =& V_X(z)z^{-1} + \{V_X(z)^{-1} - 2V_{out2}(z)\}z^{-1} \end{aligned} \tag{6.13}$$

From (6.13), we can observe that the summation node can be implemented with an integrator without reset. This is because at the end of nth clock period, $V_X(n)$ is calculated. Meanwhile, the signal $-2\epsilon_{q2}(n)$ contains a component equal to $V_X(n)$, which will be used by the summation operation in the $(n+1)th$ clock period. Thus, $V_X(n)$ can be reused and does not need to be reset. Meanwhile, the feedback signal -2$\epsilon_{q2}(n)$ can be replaced with $V_X(n) - 2V_{out2}(n)$. In this case, the transfer function of the $\Sigma\Delta$M remains the same and the reset issue is solved.

With the above considerations, the modified architecture of the proposed scheme is illustrated in Fig. 6.9. Interestingly, the op-amp is used as an integrator for $-2z^{-1}\epsilon_{q2}(z)$ branch. While for the other 2 branches, the op-amp functions as an analog adder. Under such a configuration, the feedback factor β_{2ord} for the operations in ϕ_1 and ϕ_2 are 1/2 and 1/3, respectively.

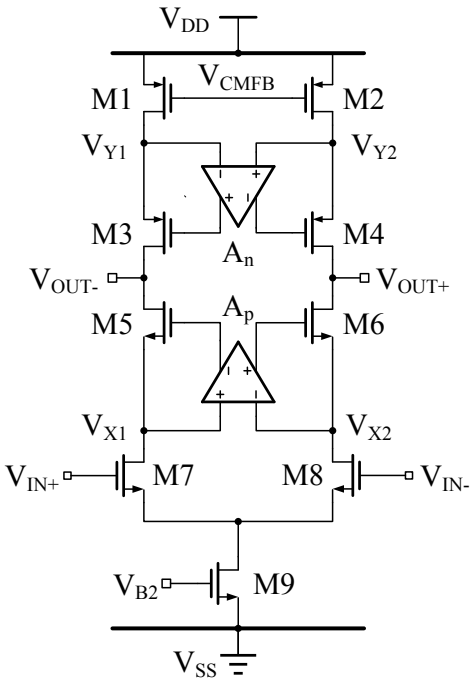

Figure 6.11 Main operational amplifier schematic diagram.

Fig. 6.10 shows the single-ended schematic diagram of the proposed second-order ADC. The circuit consists of one op-amp, 2 quantizers, 2 DACs and related digital controls. The ADC1 is 3-bit and contains 8 comparators. The swing of the op-amp is less than $0.2V_{ref}$, thus, only 8 comparators are required in ADC2. The unity capacitor C_u (MIM type) is 7.5 fF. The input sampling capacitor C_S is

$32C_u$ which is equal to 240 fF. The combination of digital output D_{out1} and D_{out2} generates the final output D_{out}, which is not shown in Fig. 6.10. The SC circuits are used to implement the analog delay lines, which are under the control of various clock phases. As seen in Fig. 6.10, ϕ_1, ϕ_2 and ϕ_q are the 3 clock phases with the equal duty ratio as mentioned before. Meanwhile, ϕ_{21} and ϕ_{22} are the divided by 2 clocks of ϕ_2. Similarly, ϕ_{q1} and ϕ_{q2} and the divided by 2 phases of ϕ_q. These 4 clock signals, however, are used to control 2 sets of capacitors in order to generate the $z^{-2}\epsilon_{q2}(z)$ term.

6.3 Building Blocks

In this section, analog and digital building blocks used in the proposed 0+2 ΣΔM are described. Firstly, a high gain op-amp with large bandwidth is introduced, which is followed by the design of a low-power comparator. The 3-phase non-overlap clock generator is explained in the last part.

6.3.1 Gain-Boost Operational Amplifier

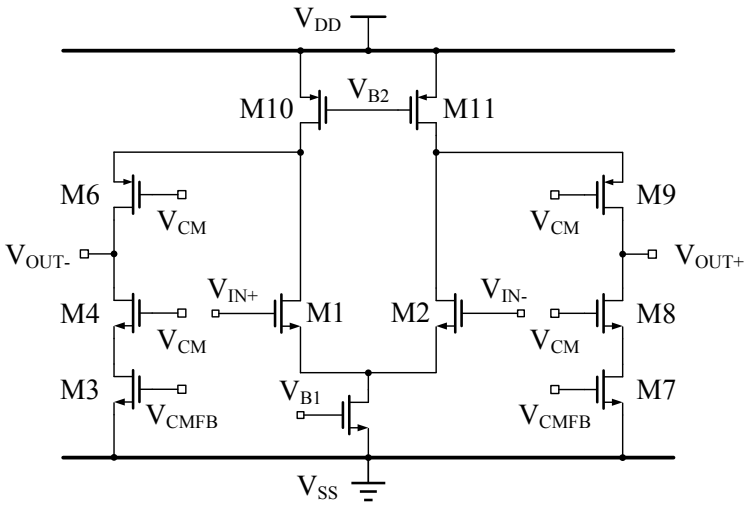

Figure 6.12 Gain booster A_n schematic diagram.

With less than $0.2V_{ref}$ output swing, the conventional telescopic op-amp is employed which is illustrated in Fig. 6.11. As seen in Fig. 6.11, M7-M8 are the NMOS input pair while M1,M2 and M9 form the current sources. Transistors M3-M6 together with A_n and A_p are adopted to boost DC gain of the main op-amp. A_n is a fully differential folded-cascode op-amp with NMOS transistor pair as input, as illustrated in Fig. 6.12. On the other hand, A_p is a fully differential folded cascode op-amp using PMOS transistors as input, which is shown in Fig. 6.13. The reason that 2 types of gain boosters are used is that, the voltages V_{X1} and V_{X2} ($V_{DS9} + V_{DS7}$) are not high enough to drive NMOS transistors while V_{Y1} and V_{Y2} ($V_{DD} - V_{DS1}$) are not low enough to drive PMOS transistors. Hence, gain booster A_p is used for V_{X1} and V_{X2} and regarding V_{Y1} and V_{Y2}, gain booster A_n is adopted.

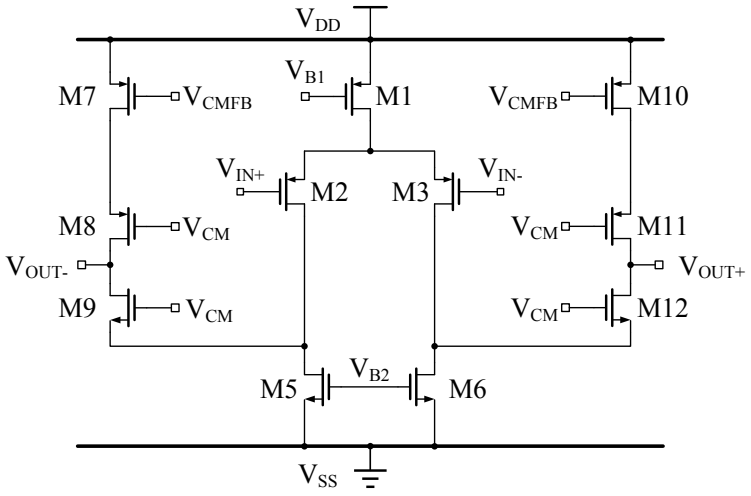

Figure 6.13 Gain booster A_p schematic diagram.

As reported in [5], the restriction on the GBW of gain boosters (GBW_A) in order to ensure fast settling is

$$\beta_{2ord} \cdot GBW_M < GBW_A < \omega_{p2} \tag{6.14}$$

where GBW_M and ω_{p2} are the close loop GBW and the position of the second pole of the main op-amp, respectively.

With above considerations, the telescopic op-amp shown in Fig. 6.11 together with A_p and A_n is implemented with $0.18\mu m$ CMOS technology using 1.8 V analog power supply. The simulated DC gain and GBW under typical condition of A_p are 58.6 dB and 520 MHz. In terms of A_n, the DC gain and GBW are 56.7 dB and 474 MHz. With the help of the gain boosters, simulation results show the DC gain and GBW of the main op-amp is 102 dB and 1.2 GHz (480 fF load). The total power consumption of the op-amp is 1.3 mW (including the gain boosters).

6.3.2 Low-Power Comparator

The structure of the comparator used in this design is the same as that adopted in previous chip, which is replotted in Fig. 6.14. The total bias current of a comparator is 4 μA. The power consumption of 2 quantizers is around 0.12 mW. Simulation results under typical conditions show that the DC gain of the pre amplifier stage is 10.2 dB and the delay of the comparator is 350 ps. The sensitivity is less than 1 mV, which is guaranteed by intensive simulations.

6.3.3 Non-Overlap Clock with Three Phases

As mentioned previously, this design employs 3 non-overlap phases with equal occupation, which are ϕ_1, ϕ_2 and ϕ_q. Fig. 6.15 shows the schematic diagram of the used 3 non-overlap clock phases generator. The working principles are as below: at the beginning of the circuit startup, $D_{1,2,3}$ are reset to 0 (not shown in Fig. 6.15). When the DFFs detect the first positive edge of ϕ_{in}, the outputs of DFFs are updated which means $D_1 = 1$, $D_2 = 0$ and $D_3 = 0$. Notice that during the normal operation of the

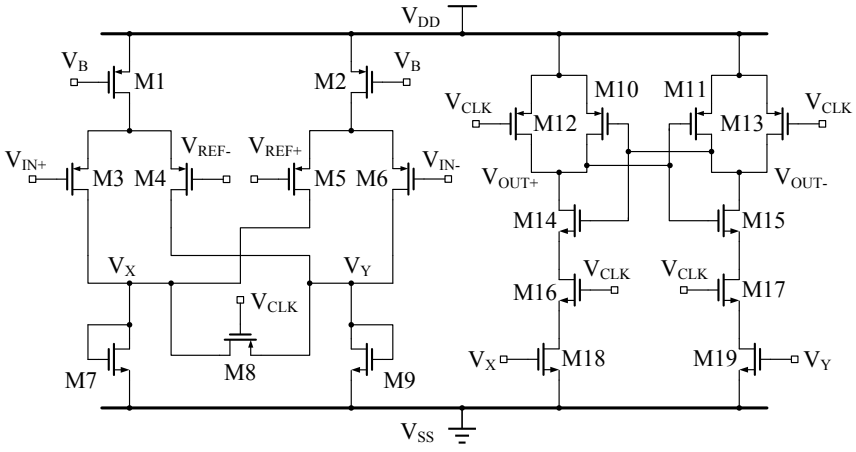

Figure 6.14 Two stage comparator schematic diagram.

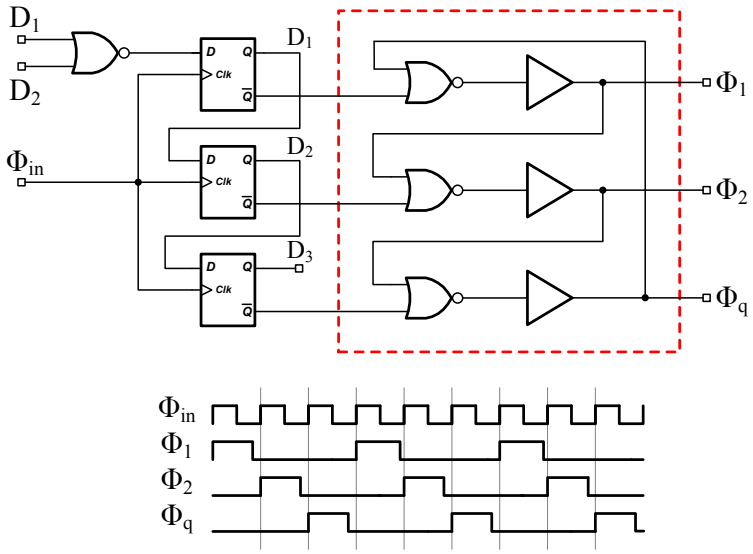

Figure 6.15 Three non-overlap clock phases generator.

phase generator, there is only one high logic in $D_{1,2,3}$ while the other 2 remain low. In the following clock periods, the high logic 1 is passed in a cyclic order from D_1 to D_3 and when D_3 is equal to 1, the high logic will be passed from D_3 to D_1 again. The non-overlap property of 3 clock phases are ensured by the logic in the red dash box. For example, suppose in nth clock period, $D_1 = \phi_1 = 1$ and $D_{2,3} = \phi_{2,3} = 0$. In the $(n+1)th$ clock period, values of DFFs change to $D_{1,3} = 0$ and $D_2 = 1$. However, when ϕ_1 becomes to 0, ϕ_2 cannot change immediately because there is delay from ϕ_1 to ϕ_2. In this case, the non-overlap property of 3 clock phases are guaranteed.

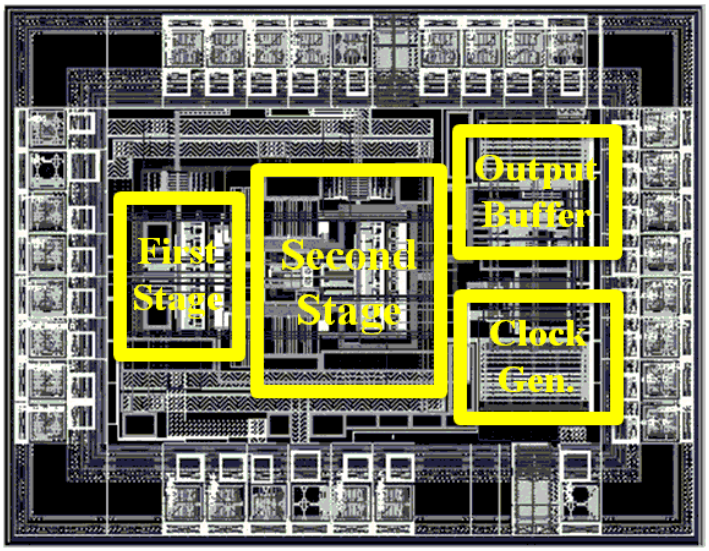

Figure 6.16 PVLPSD2 chip layout.

Using $0.18\mu m$ CMOS technology with 1.8 V power supply, simulation results show the transition time of the clocks is 50 ps and the non-overlap gap between 2 adjacent phases is around 150 ps. This value, however, is sufficient to tolerate the clock skew due to circuit imperfections in the real circumstances.

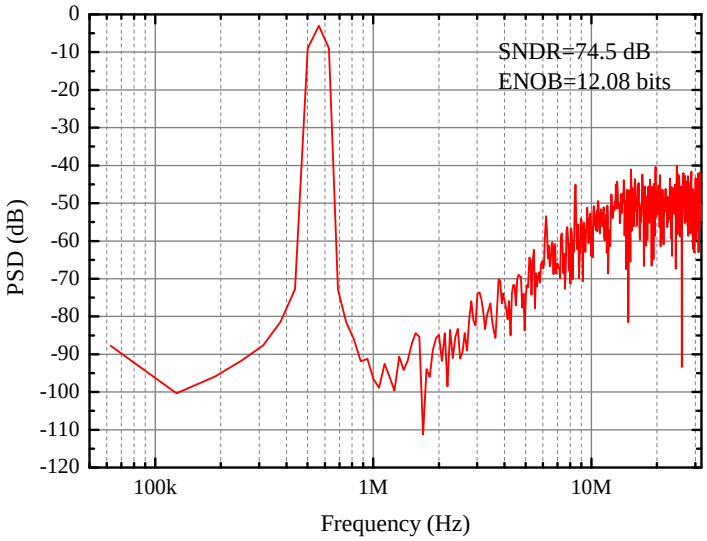

Figure 6.17 PSD (1024-point FFT) with respect to frequency. The input signal is a sinusoid waveform at 562.5 kHz whose amplitude is -3 dB_{FS} ($B_W = 2MHz$). The sampling frequency is 64 MHz and the OSR is 16.

6.4 Simulation Results and Performance Comparison

The proposed single op-amp 0+2 ΣΔ ADC is designed in a 0.18 μm CMOS technology with 6 metal layers. Fig. 6.16 shows the layout of the full chip. The active area is 860×600 μm^2 (the chip area is 1240×970 μm^2). The number of pads used in the chip is 32. To avoid interferences, the power supply and ground signal for analog and digital circuits are separated. Multiple pads for analog power supply and ground are utilized so as to reduce the related IR drop. Other pads are used to provide different input signals (voltage and current references, analog inputs, clock and reset) and digital outputs.

Table 6.3 Performance Comparison between proposed ΣΔ ADC with state of the art.

	This Work	ISSCC2006 [6]	ISSCC2005 [7]	ISSCC2011 [8]	ISSCC2008 [9]
Year	**2013**	2006	2005	2011	2008
Technology (μm)	**0.18**	0.18	0.09	0.18	0.18
V_{DD} (V)	**1.8**	1.8	1.2	1.5	0.7
Bandwidth	**2 MHz**	2.2 MHz	1.94 MHz	1.04 MHz	20 kHz
OSR	**16**	32.7	10	24	100
SNDR (dB)	**74**	78	63	78.2	81
Power	**1.7 mW**	5.1 mW	1.2 mW	2.9 mW	3.6 μW
FOM_W (fJ/conv-step)	**104**	178.5	267.9	210	98.1

The performance of the proposed second-order ΣΔM is verified by transistor level simulations in Cadence software. Fig. 6.17 illustrates the PSD (1024-point FFT) of D_{out} when a -3 dB_{FS} sinusoid waveform at 562.5 kHz is applied. The achieved SNDR is 74.5 dB, which is equal to 12.08-bit resolution. The total power consumption is 1.7 mW and the corresponding FOM_W is 104 fJ/conv-step.

In Tab. 6.3, performance comparison between proposed ΣΔ ADC and state of the art modulators is given. As seen in Tab. 6.3, the Figure of Merit of the proposed modulator (simulation results) is better than those achieved by the counterparts with comparable signal bandwidth. The ADC presented in [9] obtained a slightly smaller FOM_W which is 98.1 fJ/conv-step, however, with a very narrow bandwidth (20 kHz) of the input signal.

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CHAPTER 7

CONCLUSIONS AND FUTURE WORK

This chapter concludes the thesis. Firstly, a summary that briefly introduces the motivation and results of the thesis is presented. Several original contributions are then explained in the next section. Finally the future directions of incremental and $\Sigma\Delta$ ADCs are shortly discussed.

7.1 Summary

Targeting at high resolution and low power, this thesis explored new architectures and circuits techniques for multi-bit incremental ADCs and $\Sigma\Delta$Ms. Conventional second-order and third-order incremental modulators use 2-level quantization, which usually have a long conversion time per sample and high power consumption due to large output swing of op-amps. Compared with 2-level quantization, multi-bit quantization is a more convenient technique for incremental ADCs because it reduces the output swing of op-amps, while keeps the loop stable without fractional coefficients. The non-linearity due to the mismatch between unity elements in multi-bit DAC can be properly compensated for with Smart-DEM algorithm. A prototype chip fabricated in a mixed 0.5-0.18 μm CMOS technology demonstrated the proposed second-order 3-bit architecture, which obtained more than 17-bit resolution over a 5 kHz bandwidth. For $\Sigma\Delta$M, since the target is to achieve 12-bit resolution and the existing DEM techniques are able to compensate for the non-linearity of DAC, we focused on the low-power $\Sigma\Delta$ architectures and design techniques. A 12-bit 0+2 $\Sigma\Delta$ ADC was proposed, which uses a single op-amp to achieve second-order noise-shaping. A prototype chip was designed in a

0.18 μm CMOS technology and simulation results show it can attain 12-bit resolution over 2 MHz bandwidth.

7.2 Contributions

7.2.1 High-Order Smart-DEM Algorithm

In this thesis, a Smart-DEM algorithm for high-order incremental ADCs was proposed, which is able to compensate for the mismatch between unity elements of multi-bit DAC. As discussed in Chapter 3, conventional DEM methods such as DWA can not properly compensate for the mismatch, giving rise to considerable resolution loss especially when higher order structures are used. However, the Smart-DEM algorithm can achieve a near-ideal compensation and thus benefit high order incremental ADCs with better conversion efficiency and reduced swing of op-amps.

7.2.2 Non-conventional Incremental Architectures

In Chapter 4, non-conventional incremental architectures are explored. These incremental ADCs adopt digital feedforward paths to maintain loop stability as well as reduce the swing of op-amps. The use of multi-bit quantization and DAC can help achieve high conversion efficiency for the modulators. The only feedback path allows properly use of Smart-DEM algorithm, giving rise to a near-ideal mismatch compensation. In this case, the obtained multi-bit incremental architectures can provide faster conversion and consume less power than conventional modulators utilizing 2-level quantization.

7.2.3 Single Op-Amp Second-Order $\Sigma\Delta$ Architecture

Chapter 7 proposed a 0+2 $\Sigma\Delta$ architecture. The main feature of this modulator is that, the use of single op-amp achieves second-order noise shaping. A 3-bit flash is introduced to reduce the swing of the input of the $\Sigma\Delta$ stage. To improve the feedback factor of the op-amp, 3 non-overlap clocks can be utilized. Simulation results show that the proposed architecture can meet the specifications and achieve good power efficiency.

7.3 Future Directions

Based on the work of this thesis and recent publications, a few topics are worthy to be investigated in the near future.

7.3.1 Multi-Bit Incremental ADC aiming for 20-Bit

To the best of the author's knowledge, very few incremental ADCs obtained 20-bit or more resolution [1][2]. However, The aforementioned non-conventional architectures and Smart-DEM algorithm can be extended to achieve more than 20-bit resolution. A good design strategy is to combine second-order or third-order incremental architecture with 4-6 bits quantizer. With regard to the Smart-DEM block, an ultra-low power supply can be applied to significantly reduce the power consumption of the digital

circuit. In this case, the multi-bit incremental modulator can achieve 20-bit or more resolution with very low power dissipation.

7.3.2 Multi-Bit CT Incremental Modulator

Incremental ADCs are always implemented in DT fashion. Recently, a few CT incremental modulators were reported in [3][4]. The benefit of CT modulators stems from relaxed requirements on slew rate and bandwidth, giving rise to potentially better power efficiency than their counterparts. To date, only 2-level quantization is utilized in CT incremental modulators. The multi-bit CT incremental ADCs have not been reported in the open literature yet, which is a good direction to further lower the power dissipation of the modulator.

7.3.3 ADCs Utilizing Nanometer CMOS Technologies

As indicated in Chapter 5 and Chapter 6, op-amps employed in the 2 designs require very high DC gain ($>$90 dB). However, in the nanometer CMOS technologies ($\leq$ 65 nm), achieving such a DC gain is very difficult. Consequently, a few techniques attempted to replace op-amps were reported recently [5][6]. A second-order incremental ADC was reported in [5], which replaces op-amps with gated current source (GCS) along with zero-crossing detector (ZCD). The reported resolution is 14-bit, which is relatively low compared with 20-bit or more resolution. However, this is a good way to obtain almost all digital incremental ADC, which has significant advantages when the utilized CMOS technologies are scaled to 32 nm or even less. With regard to $\Sigma\Delta$Ms, a low-power modulator utilizing Class-C inverters was presented in [6], which achieved very low power dissipation because it does not consume static biasing current. Both examples discussed above indicate a good research direction in the near future, because of the continuous scaling of the feature size and power supply of modern CMOS technologies.

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APPENDIX A

KT/C NOISE OF INCREMENTAL ADCS

This appendix derives the input referred thermal noise and limitations on C_S for different order incremental ADCs. In Section 3.1, we briefly introduced the same topic for the second-order incremental architecture plotted in Fig. 2.17. Here, we derive the equations with more details from second-order to Lth-order incremental architectures.

A.1 kT/C Limitation of Second-Order Incremental ADCs

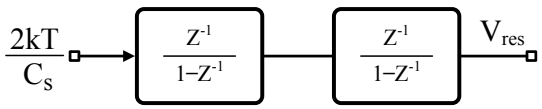

Figure A.1 Second-order incremental ADC equivalent model with kT/C noise as input.

For readers's convenience, the equivalent model of generalized second-order incremental architecture is illustrated in Fig. A.1. Notice that the only effective noise term here is the thermal noise generated by input sampling capacitor C_S. For conventional single-ended SC circuits implementation, in the first clock period, the thermal noise is sampled by the C_S and then injected on the delayed integrator. Consequently, the noise power appeared at the output of the integrator is $2kT/C_S$. From second to

Nth clock period, the second integrator accumulates $\sqrt{2kT/C_S}$ linearly with one-unit-time delay. Hence, at the end of Nth clock period, the total power can be seen at V_{res} node due to the kT/C noise in the first clock cycle is

$$V_n^2(1) = \frac{2kT}{C_S}(N-2)^2 \tag{A.1}$$

Similarly, the noise power at V_{res} node due to kT/C noise injection at ith clock period can be estimated by

$$V_n^2(i) = \frac{2kT}{C_S}(N-i-1)^2 \tag{A.2}$$

Thus, at the end of Nth clock period, the total noise power appeared at V_{res} node is

$$V_{n,tot}^2 = \frac{2kT}{C_S}\sum_{i=1}^{N-2} i^2 \tag{A.3}$$

In order to calculate the input referred kT/C noise, the amplification of the input signal should be derived. For second-order incremental architectures, we have

$$G_{2ord} = \frac{(N-1)(N-2)}{2!} \tag{A.4}$$

Thus, the input referred thermal noise can be derived

$$V_{n,in}^2 = \frac{V_{n,tot}^2}{G_{2ord}^2} \tag{A.5}$$

In order to achieve R_{2ord}-bit resolution, $V_{n,in}$ can not exceed half of V_{LSB}. Consequently, the minimum C_S can be estimated by

$$C_S > \frac{8kT\sum_{i=1}^{N-2} i^2}{G_{2ord}^2 V_{LSB}^2}; V_{LSB} = \frac{V_{FS}}{2^{R_{2ord}}} \tag{A.6}$$

A.2 kT/C Limitation of Third-Order Incremental ADCs

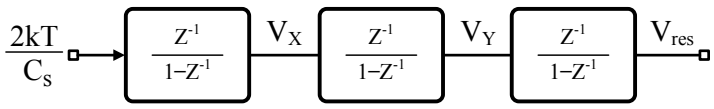

Figure A.2 Third-order incremental ADC equivalent model with kT/C noise as input.

Similarly, the equivalent model of the third-order incremental architecture is shown in Fig. A.2. In the first clock period, the thermal noise is sampled by the C_S and then injected on the delayed integrator. From second to Nth clock period, the noise appeared at V_X is linearly accumulated and the result is V_Y. Moreover, the third integrator accumulated V_Y as a linear function from third to Nth

clock period. Based on the above observation, at the end of Nth clock period, the total noise power seen on V_{res} node due to the kT/C noise injected in the ith clock cycle is

$$V_n^2(i) = \frac{2kT}{C_s}[\frac{(N-2-i)(N-1-i)}{2!}]^2 \tag{A.7}$$

Consequently, the total noise power at V_{res} node at the end of Nth clock period is

$$V_{n,tot}^2(i) = \frac{2kT}{C_S}\sum_{i=1}^{N-3}[\frac{(N-2-i)(N-1-i)}{2!}]^2 \tag{A.8}$$

The amplification from input to V_{res} at the end of Nth clock period is

$$G_{3ord} = \frac{(N-1)(N-2)(N-3)}{3!} \tag{A.9}$$

Thus, the input referred thermal noise of third-order incremental ADCs can be represented by

$$V_{n,in}^2 = \frac{V_{n,tot}^2}{G_{3ord}^2} \tag{A.10}$$

In order to achieve R_{3ord}-bit resolution, $V_{n,in}$ can not exceed half of V_{LSB}. Consequently, the minimum C_S can be estimated by

$$C_S > \frac{8kT\sum_{i=1}^{N-3}[(N-2-i)(N-1-i)]^2}{4G_{3ord}^2 V_{LSB}^2}; V_{LSB} = \frac{V_{FS}}{2^{R_{3ord}}} \tag{A.11}$$

A.3 kT/C Limitation of Lth-Order Incremental ADCs

Following the second-order and third-order architectures, the kT/C noise limitation of Lth-order incremental scheme is also investigated. Using the similar method, when kT/C noise injects at ith clock period, the consequent noise power appears on V_{res} at the end of Nth clock period is

$$V_n^2(i) = \frac{2kT}{C_S}[\frac{(N-1-i)(N-2-i)...(N-L+1-i)}{(L-1)!}]^2 \tag{A.12}$$

Using (A.12), the total noise power seen at V_{res} due to noise injection in all N clock periods can be estimated by

$$V_{n,tot}^2 = \frac{2kT}{C_S}\sum_{i=1}^{N-L}[\frac{(N-1-i)(N-2-i)...(N-L+1-i)}{(L-1)!}]^2 \tag{A.13}$$

However, to calculated the input referred noise, the gain from input to V_{res} should also be derived, which is

$$G_{Lord} = \frac{(N-1)(N-2)...(N-L)}{L!} \tag{A.14}$$

Thus, the input referred noise can be represented by

$$V_{n,in}^2 = \frac{V_{n,tot}^2}{G_{Lord}^2} \tag{A.15}$$

Finally, the minimum input sampling capacitance can be estimated as

$$C_S > \frac{8kT\sum_{i=1}^{N-L}[(N-1-i)(N-2-i)...(N-L+1-i)]^2}{[(L-1)!]^2 G_{Lord}^2 V_{LSB}^2}; V_{LSB} = \frac{V_{FS}}{2^{R_{Lord}}} \tag{A.16}$$

APPENDIX B

LIST OF PUBLICATIONS

1. Y. Liu et al., "A 105-dB SNDR, 10 kSps Multi-Level Second-Order Incremental Converter with Smart-DEM Consuming 280μW and 3.3-V Supply", in *Proc. Eur. Solid-State Circuits Conf. (ESSCIRC)*, pp. 371-374, Sept. 2013.

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