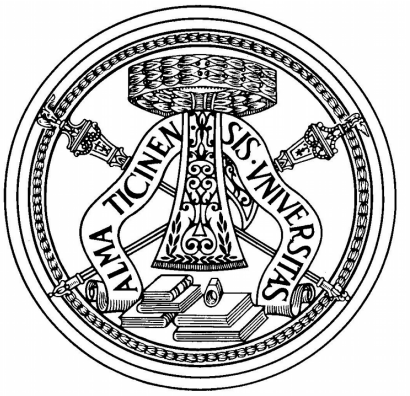

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Dottorato di ricerca in Microelettronica
XXIV ciclo

LC Harmonic CMOS Oscillators for GSM/WCDMA Frequency Synthesizers

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Contents

Introduction

In the last two decades, with the explosive growth of the wireless and wired communication industries, the research related to communication circuits and architectures has received a great deal of attention. Recently, the new services provided by the smartphones have led to a growing demand for fast access to information, which implies a considerable increase of the bit-rate and the down-link/up-link capacity. The new mobile applications have needed the definition of newer and more complex standards, like LTE, able to provide a peak download rate greater than 300Mbit/s due to the use of complex modulation techniques and a high network reconfigurability.

The newest transceivers are becoming more complicated. The major issues are low-cost, low-voltage, and low-power designs, which combine necessary performance with the ability to be manufactured economically in high volumes. Moreover, there is an additional emphasis on integration of heterogeneous parts that constitute a communication transceiver. Modern RF front-end are expected to be reconfigurable and to operate over a wide range of frequencies to satisfy the specs required by several standards, reducing the power consumption.

The new deep sub-micron CMOS technologies, digitally oriented, evolve by themselves in the direction of these goals with the gradual reduction of the transistor size and the increase of the integration density. As a result, the microchips become cheaper, faster, more complex and more power efficient. Despite the low supply voltages and the high threshold reduce both dynamic and static power consumption in the digital section, they limit the design of the analog circuits where the scaling is less attractive. Unlike digital circuits, analog functions are constrained by electronic noise and accuracy requirements, factors that only conditionally benefit from technology scaling and that can even deteriorate for very low supply voltages.

Although digital circuits greatly benefit from the technology evolution, the migration towards all-digital architectures is still a challenging target and the analog circuits are still required in most applications. Applications such as audio, video, and Radio Frequency (RF) communications demand analog circuits as interface with the physical world. However, the research has recently proposed some fully digital architectures. In particular, it has made great progress with regard to the digital frequency synthesis, represented by the All Digital Phase Locked Loop (ADPLL). Compared to the analog frequency synthesizers, the ADPLLs exploit all the advantage of the digital design, especially in term of reconfigurability, speed, re-

liability, reduction in size, cost and power consumption. Furthermore, the digital is used to enhance the performance of the analog circuits thanks to extended calibration and post-processing algorithms. The state of the art presents several works on digital PLLs published in the last decade [1]-[6] where they show different approaches to the system design.

The Digital Controlled Oscillator (DCO) is one of the key building blocks of the digital frequency synthesizers. It replaces the Voltage Controlled Oscillator (VCO) and generates an oscillation whose frequency is proportional to the digital control word. However, the quantization noise introduced by the frequency discretization limits the performance of the DCO and nowadays the target resolution for wireless applications is still quite challenging to make possible a simple transposition of analog solutions into digital ones. The parasitic capacitances prevent the use of standard devices to achieve the fine frequency resolution required to satisfy the phase noise mask of the standards. In the last decade, different works have been published focused on reducing the frequency resolution, proposing different solutions and architecture [9]-[13].

The oscillator is also the most power-hungry element of the frequency synthesizer due to the high spectral purity required by the wireless communication applications. Both academy and industry have investigated and proposed several techniques to reduce the power consumption without any effect on the output phase noise performance. ()

The target of the activity described in this dissertation was the design of Voltage and Digital Controlled Oscillators (VCO/DCO) for multi-standard frequency synthesizers. In particular, the research was focused on studying new DCO architectures that minimized the quantization noise and on reducing the power consumption. Thanks to the collaboration with the Italian design center of Marvell, the research activity was oriented to real application tightly linked to the industrial context. The activity was organized in three main steps.

a) The design of a dither-less DCO based on a capacitive degeneration. The research activity was focused on studying a new simple architecture able to achieve high frequency resolution without using dithering technique and without any effect on the phase noise. The **Chapter 1** describes the problem of the quantization noise, details the proposed solution and compares it to the state of the art.

b) The integration of the DCO into an All Digital PLL (ADPLL). The **Chapter 2** presents the frequency synthesizer, focusing on its two keys building blocks (TDC and DCO). The chapter describes also the calibration and acquisition aiding algorithms, necessary to compensate the non linearity of the TDC and DCO and to minimize the setting time of the system.

c) The design of new oscillator topologies tailored to reduce the current consumption without affecting the phase noise performance. The Power Scalable DCO and the Hybrid Class-C/Class-B VCO, presented in the first part

of the **Chapter 3**, were integrated. They save current reconfiguring the oscillator topology and exploiting the advantages of class-C architecture respectively. The second part of the chapter describes two Dynamic Bias Schemes for Class-C VCOs and shows the simulation results.

All the prototypes are discussed in **Chapter 4** where the results of the measurements are reported.

Chapter 1

The Digitally Controlled Oscillator

The Digitally Controlled Oscillator (DCO) is a particular type of Digital to Analog Converter (DAC) which generates a signal whose frequency is proportional to the input digital control word. Typically it operates in All Digital PLLs (ADPLL) in conjunction with a Time to Digital Converter (TDC) to synthesize a frequency proportional to a reference. The Fig. 1.1 shows the simple block diagram of an ADPLL. The TDC digitalizes the delay between the divider output and the reference signal. The error signal (Δt_e) is filtered by a digital filter loop and used to control the instantaneous frequency of the DCO.

The migration of Phase Locked Loops (PLL) towards all-digital architectures derives form the requirement of high reconfigurability, speed, reliability, reduction in size and cost of digital integrated circuits and the exploitment of the new technologies digitally oriented, with low power supply voltage and high threshold which don't allow sophisticated analog functions. A number of works on digital PLLs has been published since 1960 [7]; the earliest efforts on Digital PLLs fo-

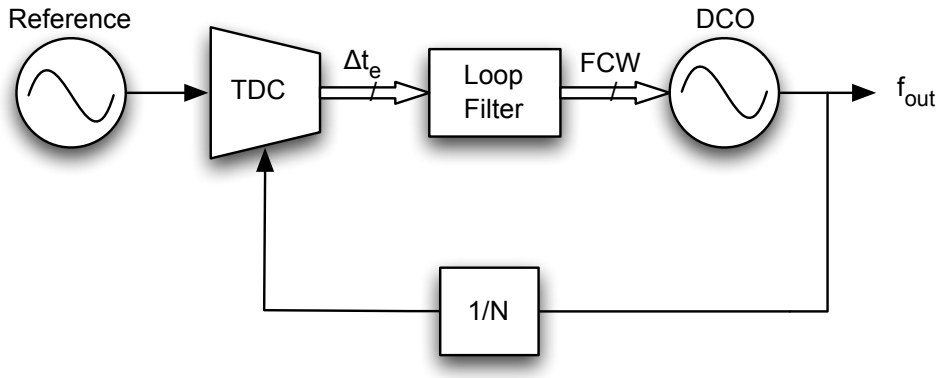

Figure 1.1: *Diagram of an ALl Digital PLL.*

cused on partially replacing the analog PLL components with digital ones. The All Digital PLL (ADPLL) is the result of this evolution process.

However, compared to the analog PLL, the digital solutions introduce the quantization noise and thier performance depend also on the capability of the new technology to obtain the adeguate quantization of time and frequency. In particular, a fine resolution of the time-to digital converter (TDC) is required to minimize the quantization noise introduced in the PLL band, while a tiny frequency discretization of the DCO allows to reduce the noise added far from the carrier. Although the technology evolves by itself in the direction of these goals, with shorter delay stages and smaller parasitic capacitances, the target resolutions for wireless applications are still quite challenging to make possible a simple transposition of analog solutions into digital ones.

The first part of this chapter describes the problem of the quantization noise introduced by the DCO and describe the most significant solutions proposed by the state of the art. In the second part, a digitally controlled oscillator that achieves a minimum frequency quantization step of 150Hz without any dithering is presented. The idea is to exploit an intrinsic effect in the classical LC-tank oscillator [8] and the fine digital tuning is obtained through a capacitive degeneration of a portion of the transistor switching pair used to restore the energies lost by the resonant load. The new tuning circuitry does not appreciably affect the intrinsic oscillator phase noise and allows to trim the frequency with a programmable resolution for calibration and multi-standard operation.

1.1 DCO quantization impact on the phase noise

To analize the effect of the quantization noise on the output phase noise the DCO can be modeled as the cascade of a quantizer (a non linear block) and a VCO as reported if Fig. 1.2.a. The infinite-precision tuning signal d is quantized to a finite-precision tuning word such that it matches the DCO frequency resolution. The actual frequency deviation will be within away from ideal. The frequency deviation is then converted to phase through the $2\pi/s$ integration. In fact, the 2π multiplication denotes the conversion of a linear frequency (in units of hertz) to an angular frequency (in units of rad/s). Since the tuning word normally spans multiple quantization levels, the DCO frequency quantization error is modeled in Fig. 1.2.b as an additive uniformly distributed random variable $\Delta f_{n,0}$ with white noise spectral characteristics. Its variance is:

$$\sigma^2_{\Delta f_0} = \frac{(\Delta f_{ref})^2}{12} \tag{1.1}$$

The total frequency noise power is spread uniformly from zero to the Nyquist frequency. The single-sided spectral density is, therefore, expressed as

$$\frac{1}{2}S_f = \frac{\sigma^2_{\Delta f_0}}{f_R} \tag{1.2}$$

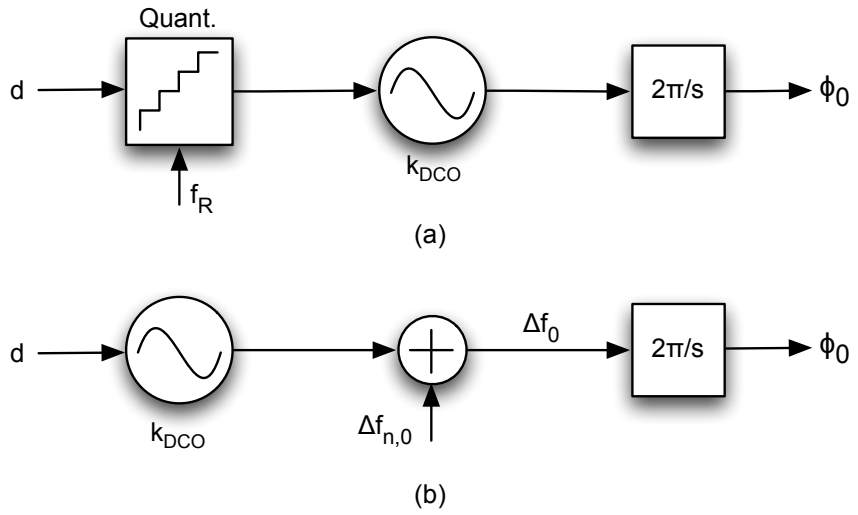

Figure 1.2: *Model of the quantization noise of the DCO.*

The transfer function from the frequency deviation quantization error $\Delta f_{n,0}$ to the phase ϕ_0 of the RF output is $2\pi/s$, so the single-sided power spectral density at the output is

$$L\{\Delta f\omega\} = \frac{1}{12} \cdot \left(\frac{\Delta f_{ref}}{\Delta f}\right)^2 \cdot \frac{1}{f_R} \tag{1.3}$$

This equation is valid from zero to Nyquist frequency. To describe the phase noise at frequencies higher than Nyquist it is necessary to consider the effect of holding the FCW value between two different samples. Equation 1.3 has to be multiplied by the sinc function corresponding to the Fourier transform of the zero-order hold operation:

$$L\{\Delta\omega\} = \frac{1}{12} \cdot \left(\frac{\Delta f_{ref}}{\Delta f}\right)^2 \cdot \frac{1}{f_R} \cdot \ sinc^2\left(\frac{\Delta f}{f_R}\right) \tag{1.4}$$

The equation has the same slope of -20dB/dec of the phase noise associated with the oscillator thermal noise up-converted around the resonant frequency.

Inside the loop of the ADPLL, the transfer function of this additive noise is a high-pass function with the corner frequency equal to PLL bandwidth and unitary magnitude at high frequency. This means the loop doesn't have any effect on the out of band noise and underline the important to keep the quantization noise lower than the analog phase noise because it could affect the spectrum of the synthesizer far away from the carrier. For example, in the design of a DCO for GSM applications, the target frequency resolution is only a kHz with the respect to a tuning range of several hundred MHz around the carrier. In fact, assuming $f_{LO} = 1.8GHz$ and the reference clock $f_R = 26MHz$, a $\Delta f = 700Hz$ produces a phase noise of -174dBc/Hz at the offset of 20MHz far from the carrier, much lower than the ana-

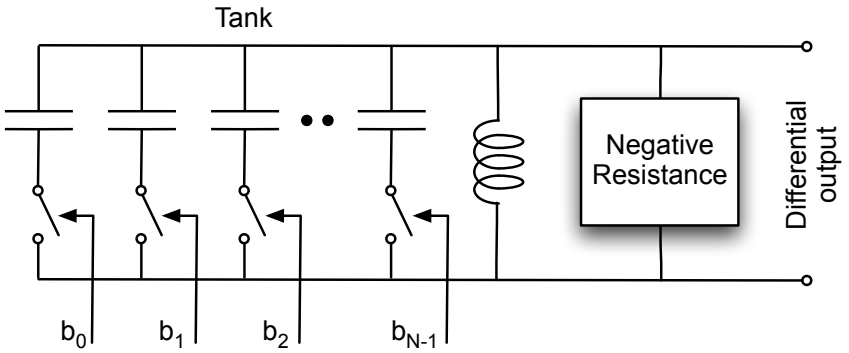

Figure 1.3: *LC tank-based oscillator with switchable capacitors.*

log phase noise introduced by the active devices and the tank of the DCO and tolerated by the GSM standard [10].

1.2 The state of the art

Due to the challenging out-of-band emission mask, an LC tank oscillator is a mandatory choice in terms of phase noise performances. The idea behind a digitally controlled LC tank oscillator is shown from a higher system level in Fig. 1.3. The resonant frequency of the parallel LC tank is established by the well-known formula:

$$f_{LO} = \frac{1}{2\pi\sqrt{LC_{tank}}} \tag{1.5}$$

where L and C_{tank} are the values of the inductance and the capacitance respectively. The oscillation is perpetuated by a negative-resistance device, which is normally built as a positive-feedback active amplifier network which restores the energy losses that occur in the tank and, to a first approximation, does not affect the oscillator frequency. The frequency f_{LO} could be controlled by changing either the inductance L, the capacitance C_{tank}, or some combination thereof. However, in a monolithic implementation it is more practical to keep the inductor fixed while changing the capacitance of a voltage-controlled device such as a varactor or, in the digital domain, using the switched capacitances. A variation δf_{LO} of the DCO is obtained acting on the resonant capacitance so that:

$$\frac{\delta f_{LO}}{f_{LO}} \propto -\frac{\delta C_{tank}}{2C_{tank}} \tag{1.6}$$

where δC_{tank} is the change in the total capacitance of the tank C_{tank}. A frequency resolution $\delta f_{LO}/f_{LO}$ of less than a few ppm (e.g. 1kHz over 3.6GHz) would required almost the same tank capacitance resolution $\delta C_{tank}/C_{tank}$. When the maximum capacitance in the tank is in the order of pico-Farad, this corresponds to an

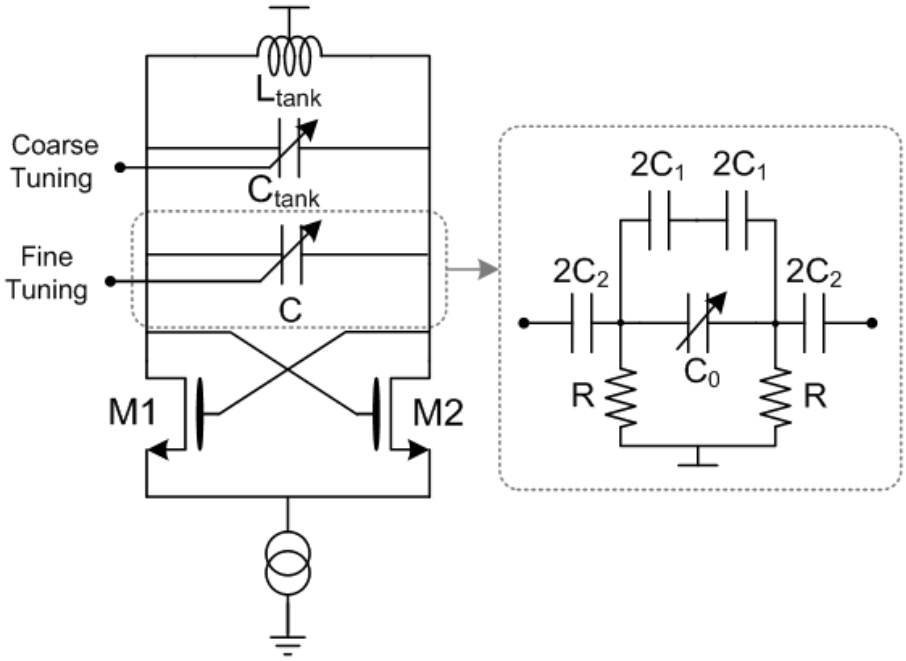

Figure 1.4: *Scheme of thecspscitive divider network.*

unitary capacitive elements of the order of atto-Farad that cannot be easily integrated [11].

The next two sections present the state of the art showing the solution based on a capacitive divider network [12] and the dithering technique [10] respectively.

1.2.1 The Capacitive Divider Network

The use of a capacitive divider network is a solution presented by Y. Chen *et al.* [12]. The oscillator scheme and the structure of the tank capacitance are reported in Fig. 1.4. The idea is to act on the resonant load of the tank using the two capacitances C_1 and C_2 in series and in parallel to the tuning capacitance C_0. For C_1 and C_2 greater than C_0, the capacitive divider network performs a shrinking effect on C_0 so that the variation of the tuning capacitance δC_0 reflected in parallel to the tank is equal to:

$$\delta C_{tank} = \left(\frac{C_2}{C_0 + C_1 + C_2}\right)^2 \delta C_0 \tag{1.7}$$

The resistors R have to be big enough so as not to influence the equivalent capacitance severely.

The shrinking effect has the advantage to discrete the tuning capacitance C_0 in steps of fF that can be easily integrated. Otherwise, the condition C_1 and C_2 greater than C_0 means that the value of the two capacitances C_1 and C_2 depends on the

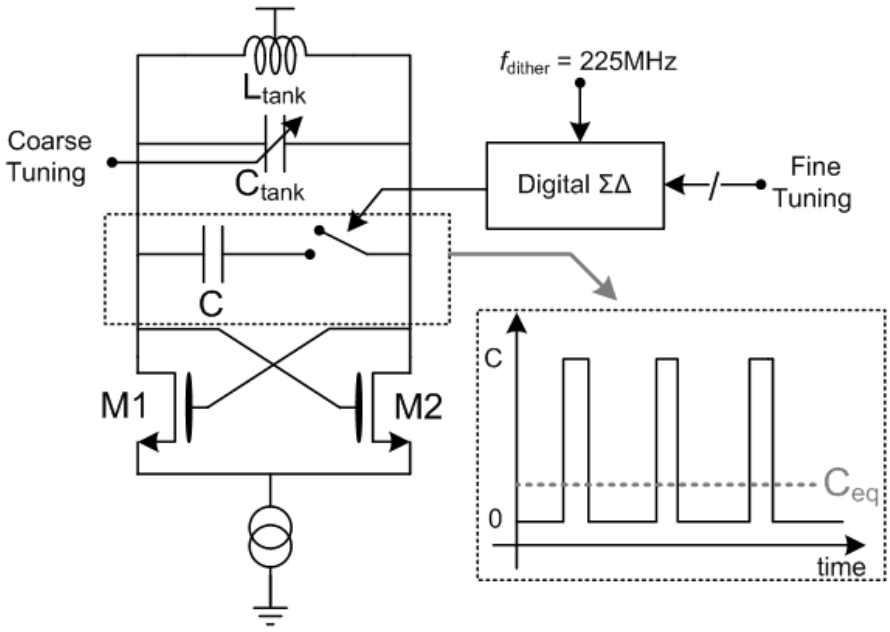

Figure 1.5: *Scheme of the dithering technique.*

tuning range and the length of the fine tuning word and they grow exponentially with the number of bits. Assuming for the GSM standard a tuning range of 10MHz and a frequency resolution of few kHz [10], the two capacitance can be easily of the order of pF. Consequently their parasites have an important role in the determining the oscillation frequency and tuning range. This sensitivity to parasites and also mismatches limit the robustness of the final design [12].

1.2.2 Dithering Technique

A more reliable technique proposed by Staszewski *et al.* consists in the dithering of the less significant bits of the DCO frequency control word like in a sigma delta DAC [7]. The principle of this approach is shown in Fig. 1.5. A ΣΔ modulator toggles the capacitance C in parallel to the tank at high frequency in order to obtain an average equivalent value (C_{eq}) between 0 and C depending on the duty-cycle of the modulator output. This solution reduces considerably the equivalent DCO frequency resolution (from 12kHz to 30Hz in [10]) but, as it occurs in any sigma-delta data converter, the quantization noise is moved to higher frequencies where the phase noise specs may be even more challenging. The Fig. 1.6 reports the different of the output phase noise due to the quantization when the dither is used and not. The dithering technique makes the quantization noise negligible close to the carrier, but at higher offset its contribution could be dominant.
Moreover, the dithering technique introduces spurs which can be reduced only increasing the equivalent frequency resolution.

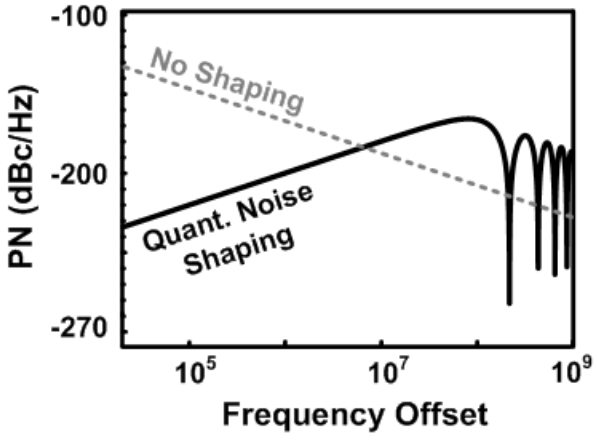

Figure 1.6: *Phase Noise comparison between dither and dither-less solutions.*

Due to this problem, the order of the ΣΔ modulator and the frequency of dithering must be particularly high (3^{rd} order and 225MHz) to satisfy the emission mask requirements far away from the carrier [10]. The high order of the modulator involves also stability problems with increase the complexity and the power consumption of the system.

1.3 Capacitive Degeneration

All the solutions presented in literature try to improve the DCO resolution working at the level of the oscillator tank, either making a custom design of the capacitive element or exploiting some kind of shrinking effect of the elements of the LC resonator [10]-[15]. The idea of the capacitive degeneration [16] is to move part of the tuning bank from the tank to the sources of the switching pair of the LC oscillator exploiting an intrinsic shrinking effect present in the structure (Fig. 1.7). The portion of the capacitive array still in parallel to the tank (named coarse tuning bank) is used to compensate process and temperature variation while the portion at the source of M1 and M2 (named fine tuning bank) is used for the DCO modulation inside the PLL. This approach allows an easier design of both coarse and fine tuning banks. It doesn't introduce any capacitive load at the oscillator output which affects the center frequency and tuning range, avoids the use of dithering and, moreover, doesn't introduces any additional drawbacks on the DCO phase-noise performance.

To better understand the principle of this solution, the oscillator can be analyzed through the equivalent scheme reported in Fig. 1.8 where the switching pair is modeled as a negative resistance in shunt with the resonant load. The structure has been studied using a small signal time variant analysis [17], where the MOS

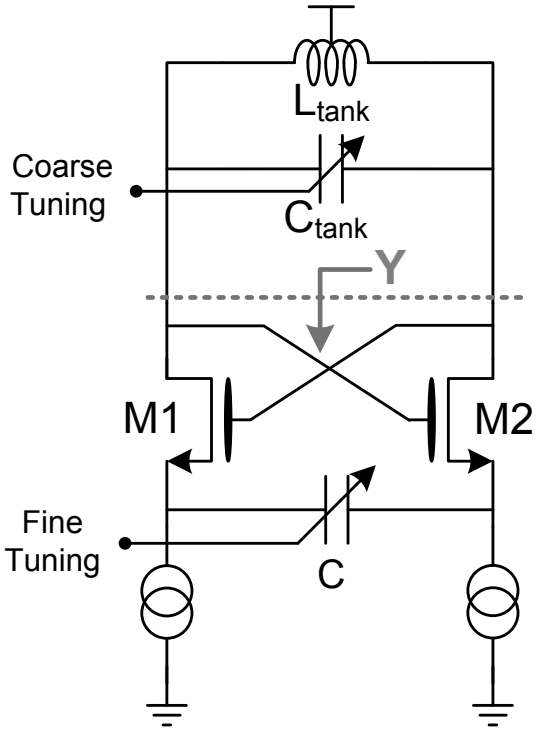

Figure 1.7: *Capacitive Degeneration DCO scheme.*

transconductance *gm* was averaged over a time interval equal to one period of the oscillation frequency $2\pi/\omega_{LO}$ (high order harmonics were neglected for simplicity).

Since the signal current which flows through the capacitance C is the same one of the transistor M1-M2, the capacitance C appears in series to transistor transconductances *gm* with an inversion of sign due to the gate-drain cross-connections that realize the positive feedback which sustains the oscillation. The effect of C on the DCO frequency tuning characteristic can be estimated evaluating the admittance Y (indicated in Fig. 1.8 as $gm_{eq} + C_{eq}$) using a series to parallel conversion in the circuit of Fig. 1.8. The admittance Y can be expressed as follows

$$Y = -\frac{gm}{2} \cdot \frac{4C^2\omega_{LO}^2}{gm^2 + 4C^2\omega_{LO}^2} - j\omega_{LO}C \cdot \frac{gm^2}{gm^2 + 4C^2\omega_{LO}^2} \tag{1.8}$$

where ω_{LO} is oscillation frequency of the DCO. For $C \gg gm/(2\omega_{LO})$ equation 1.8 can be rewritten as

$$Y = -\frac{gm}{2} - j\omega_{LO}C \cdot \left(\frac{gm}{2C\omega_{LO}}\right)^2 \tag{1.9}$$

where gm_{eq} becomes the classical negative conductance which compensates tank losses [8], while C_{eq} is equal to the capacitor C shrunk by a factor $gm^2/(2\omega_{LO}C)^2$. This factor is equal to Q_f^2 where Q_f is the quality factor of the impedance which

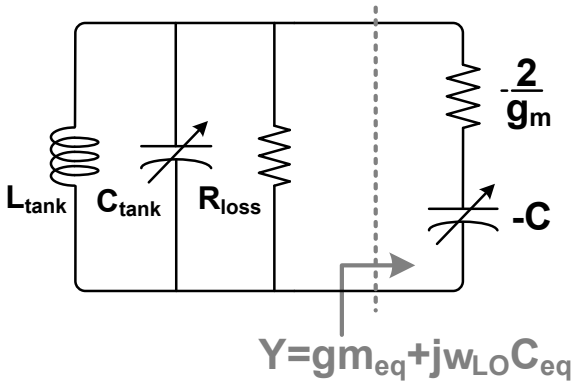

Figure 1.8: *Capacitive Degeneration DCO equivalent scheme.*

models the degenerated switching pair given by

$$Q_f = \frac{gm}{2\omega_{LO}C} \tag{1.10}$$

If the quality factor gets worse, the equivalent capacitance at the tank diminishes. As it will be shown in Section dedicated to Phase Noise analysis, although Q_f has to be lower than one to provide a shrinking effect, this does not have any adverse effect on phase noise or LO amplitude since the impedance in parallel to the tank is negative and restores DCO losses.

Starting from 1.8, gm_{eq} and C_{eq} have been plotted in Fig. 1.9 (assuming $gm = 10mS$ and $\omega_{LO} = 3.6GHz$). gm_{eq} shows a monotonic behavior that asymptotically tends to $gm/2$ while C_{eq} is not monotonic and starts to decrease for $C > gm/(2\omega_{LO})$.

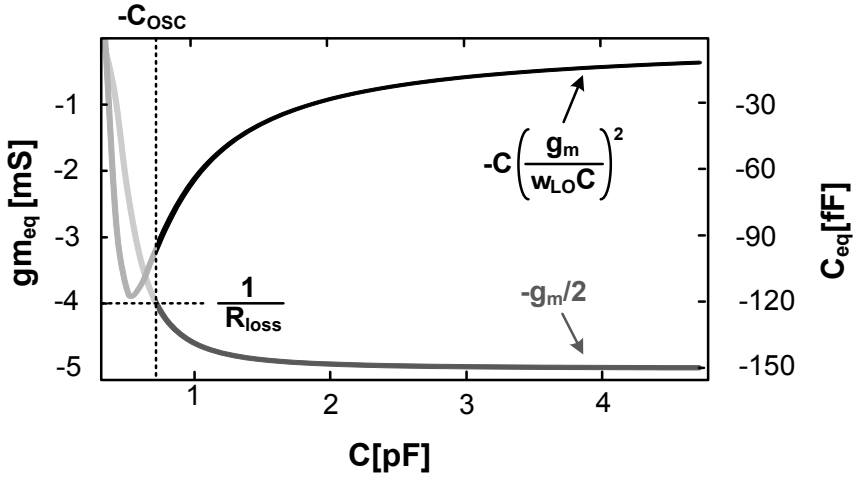

Figure 1.9: *Real and Imaginary par of admittance Y ($gm = 10mS$, $R_{loss} = 250\Omega$, $\omega_0 = 3.6GHz$).*

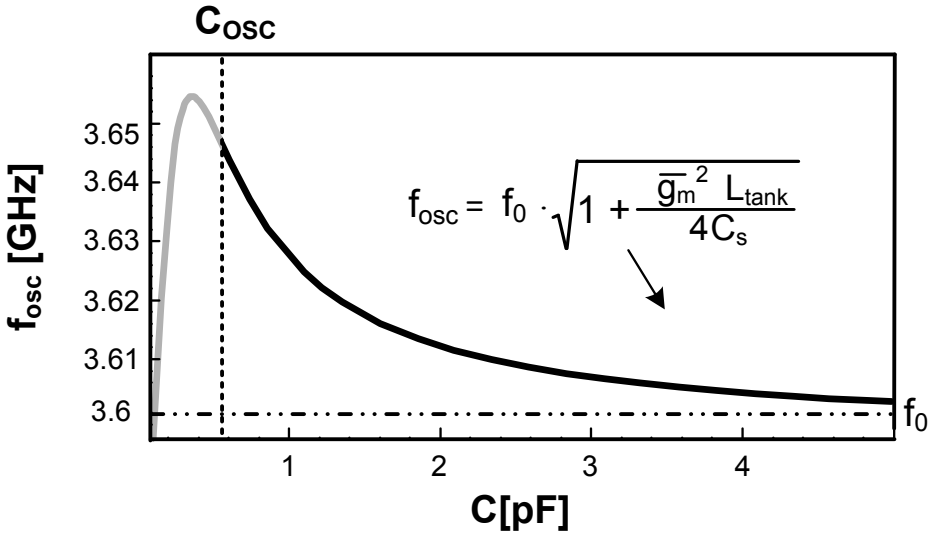

Figure 1.10: *DCO fine frequency tuning (gm = 10mS).*

Since the absolute value of the (negative) real part of Y has to be larger than $1/R_{loss}$ to sustain of the oscillations, the useful portion of the plot of Fig. 1.9 corresponds to C greater than C_{osc} that is the minimum value of C for which $gm_{eq} > 2/R_{loss}$. From the plot in Fig. 1.9 it can be seen that for the set of parameters used, a capacitor $C = 3pF$ is reflected in parallel to the tank into an equivalent capacitance $C_{eq} = 15fF$ with a shrinking factor of about 200.This means that switching on a capacitor of 5fF at the sources of M1-M2 produces the same effect as switching on a capacitor of 25aF in parallel to the oscillator tank.

1.3.1 Fine-Tuning Characteristic

The tuning characteristic of the oscillator as a function of the capacitance C (i.e. $\omega_{LO} = \omega_{LO(C)}$) can be found evaluating the resonance frequency of the scheme in Fig. 1.8 and is given by the following equation

$$\omega_{LO} = \frac{\omega_0}{\sqrt{2}} \cdot \sqrt{1 + Q_f^2 \left(\frac{C}{C_{tank}} - 1\right) + \sqrt{4Q_f^2 + \left(1 + Q_f^2 \left(\frac{C}{C_{tank}} - 1\right)\right)^2}} \quad (1.11)$$

where $\omega_0 = 1/\sqrt{C_{tank} L_{tank}}$ represents the resonant frequency of the classical LC oscillator and Q_f is given by 1.10 with ω_{LO} approximated to ω_0. Equation 1.11 was computed as a function of C and shown in Fig. 1.10. The curve has the same behavior as that of the capacitance C_{eq} showing a reduction of the slope for high value of C. In this zone the sensitivity of the output frequency to the capacitance C is small and consequently a very fine frequency tuning can be obtained. In partic-

ular, if $C \gg gm/(2\omega_0)$ the previous equation can be simplified as:

$$\omega_{LO} \approx \omega_0 \cdot \sqrt{1 + Q_f^2 \frac{C}{C_{tank}}} \tag{1.12}$$

from which it follows also that:

$$\frac{\delta\omega_{LO}}{\omega_{LO}} \propto -\frac{\delta C Q_f^2}{2C_{tank}} = -\frac{\delta C_{eq}}{2C_{tank}} \tag{1.13}$$

This expression has the same form as 1.6 which applies to the case in which the tuning is performed acting directly on the tank capacitance. The key difference is that in this case the frequency shift is magnified by a factor Q_f^2 that is generally much smaller than one (e.g. 1/200). This means that the amount of capacitance necessary to obtain the same frequency shift is $1/Q_f^2$ larger than δC_{tank}, overcoming technology limitations.

The frequency range is another key point in the design of the fine-tuning bank because in the real application, it has to be large enough to maintain the PLL locked. The coarse tuning in fact is used only to compensate process and temperature variations and performs the selection of the channel. The range of frequency-tuning achievable when the tuning is performed directly at the tank is limited by the parasitic capacitance in parallel with the tank and the quality factor used for the resonator [8]. On the other hand, using the capacitive degeneration, the tuning is limited by the range of the capacitance C_{eq} that can be synthesized in parallel to C_{tank}. From the equation 1.8 it can be found that the capacitance C_{eq} can vary between 0 (for C infinite) to a $-gm/4\omega_{LO}$ (when $C = gm/(2\omega_{LO})$) leading to a tuning range $\Delta\omega_{fine}$ given by

$$\frac{\Delta\omega_{fine,max}}{\omega_{LO}} = \frac{\Delta C_{eq,max}}{2C_{tank}} = \frac{gm}{8\omega_{LO}C_{tank}} \tag{1.14}$$

where $\Delta C_{eq,max}$ is the maximum variation of C_{eq}. For a given tank and ω_{LO} the only possibility to enlarge the fine tuning range is to increase gm and consequently the power consumption. However, an increment of gm has also the consequence to increase Q_f (according to equation 1.10), reducing the shrinking factor implemented by the circuit. This trade off can be highlighted expressing $\Delta\omega_{fine}$ as function of Q_f by the use of 1.10, obtaining

$$\frac{\Delta\omega_{fine}}{\omega_{LO}} = \frac{C}{C_{tank}} \cdot Q_f \tag{1.15}$$

In this form itâs clear that for a given shrinking factor, $\Delta\omega_{fine}$ can be enlarged only making C larger with a consequent increment of the design area. Assuming $C_{tank} = 3.5pF$ and $gm = 10mS$, the maximum tuning range results slightly greater than 50MHz, according to the plot in Fig. 1.10. However, the curve in Fig. 1.10 shows also that for values of C close to $gm/(2\omega_{LO})$, the characteristic becomes quite non-linear. In general this is not a problem and in the All Digital PLL presented

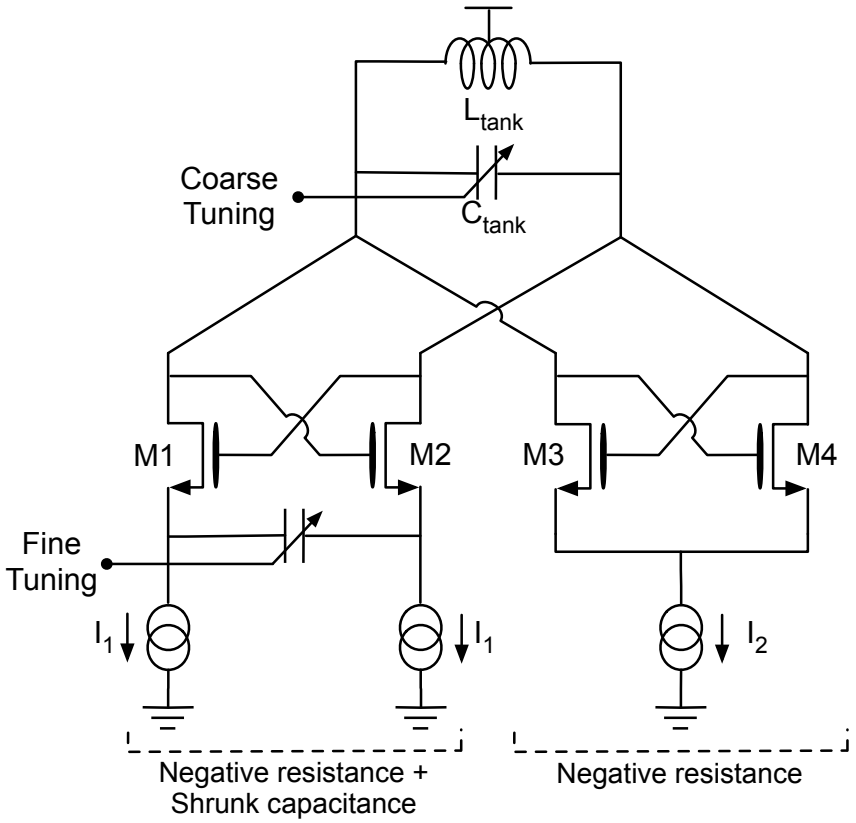

Figure 1.11: *Current calibration of the DCO capacitive degeneration.*

in the follower chapter a pre-distortion algorithm has been adopted. It increases the complexity the system, but allows to enlarge the tuning range. Alternatively, to keep the DCO characteristic sufficiently linear, the usable tuning range cannot exceed more than about 20% of $\Delta\omega_{fine}$ (e.g. in this case 10MHz).

1.3.2 Calibration Technique

Since the frequency resolution and the tuning range depend on Q_f, defined (equation 1.10) by the ratio between the transconductance of M1-M2 in Fig 1.7 and the capacitance C, a calibration is needed to compensate the process and temperature variation. Moreover, generally, the transconductance of M1 and M2 has to be large enough to sustain the oscillations but sufficiently small to give the required shrinking factor. This trade off does not allow an easy optimization of the structure since for a given *gm* (as required to compensate the tank losses) and shirking factor, C is univocally defined from 1.10, giving no degree of freedoms. For example, when the resonator quality factor becomes low, *gm* must become large leading to excessively large values for C.

Two different solutions have been used and tested: the former is the *Current*

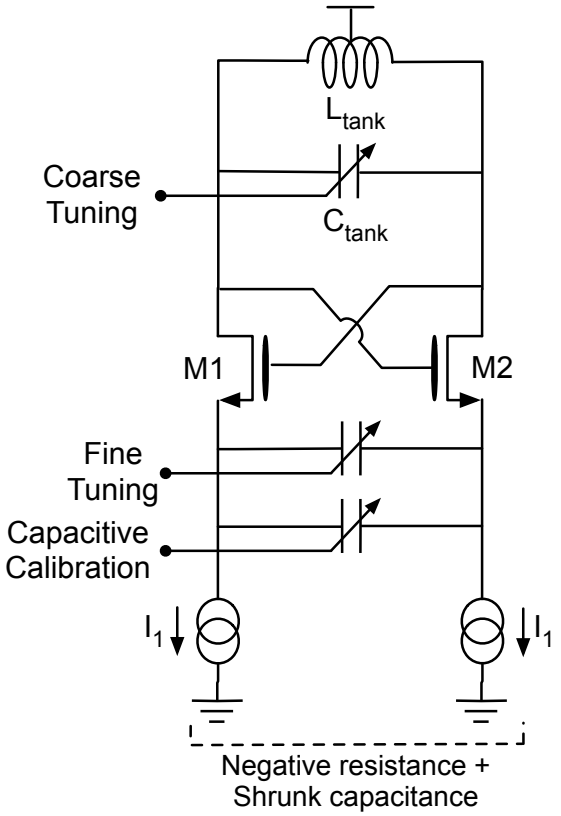

Figure 1.12: *Capacitive calibration of the DCO capacitive degeneration.*

Calibration based on acting the bias current of the switching pair controlling their transconductance; the latter is the *Capacitive Calibration* where the frequency resolution is changed varying the fixed capacitance between the sources of the transistors M1-M2. The both solution not only allow a better design optimization of the DCO, but at the same time offer an easy way to calibrate the fine tuning characteristic compensating process and temperature variations.

Current Calibration

The current calibration is shown in Fig. 1.11 and it is based on the use of a second cross-coupled transistors pair M3-M4 added in parallel to M1-M2. The role of M3-M4 is to add an extra degree of freedom in the structure that allows to choose the most suitable values for the transconductance *gm* of M1-M2 and C, without the constraint $gm_{eq} > 2/R_{loss}$ present in the scheme of Fig. 1.7. In this implementation, while the current I_1 controls the transconductance for M1-M2 defining Q_f and the DCO frequency resolution, the current I_2 keeps constant the total negative resistance defining the oscillation amplitude and the phase noise.

However, the two transistors M3-M4 add capacitive load to the tank, reducing

the frequency and particularly the tuning range. Moreover, the size of the current generator I_2 has to be large enough to reduce its flicker noise contribution to the output phase noise.

Capacitive Calibration

The capacitive calibration doesn't modify the traditional architecture of the LC tank adding an extra switching pair, but controls the frequency resolution changing the fixed capacitance between M1 and M2 as shown in Fig 1.12. The current and consequentially the transconductance of M1-M2 remain the ones that sustain the oscillation with the wanted amplitude without an extra capacitive load to the tank. The shrinking factor of equation 1.10 is controlled switching on or off the fixed capacitances. This solution doesn't affect the output phase noise and has the same advantages of the *Current Calibration* in term of reconfigurability.

1.3.3 Class-C operation

The transistors of the cross-coupled pairs can be biased to work always in saturation region (Fig. 1.13), operating in Class-C as proposed by Mazzanti *et. al*

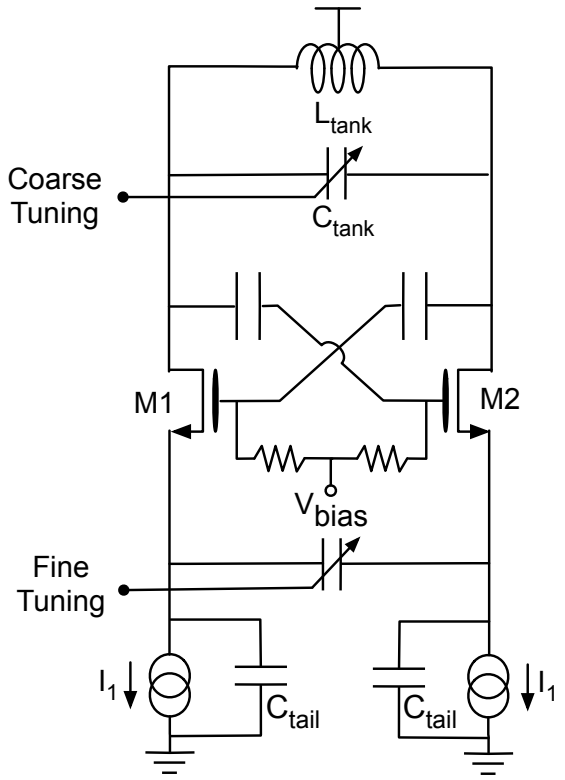

Figure 1.13: *Class-C architecture of the DCO.*

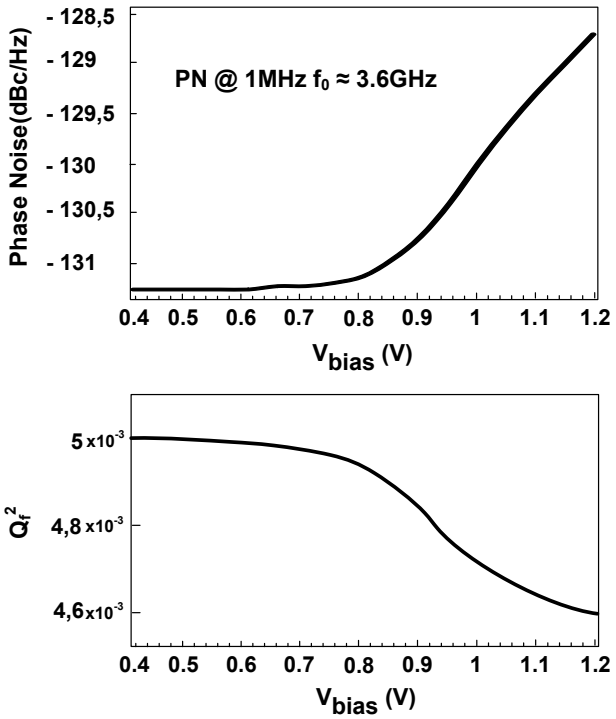

Figure 1.14: *Phase noise and tuning range versus V_{bias}.*

[17]. Although this condition is not mandatory, in this case the phase noise is minimized and at the same time the average transconductance of the differential pair increases, keeping down the current I_1 necessary for a given shirking factor. The class-C operation is guaranteed by the presence of a capacitances C_{tail} and a bias voltage V_{bias} set lower than the power supply voltage V_{dd}, through an RC filter that loads negligibly the tank. This leads short and tall current pulses, which maximize the oscillation amplitude leading to a minimization of the phase noise. Moreover, the capacitances C_{tail} naturally filters out the noise contribution from the current generator. It can be proved that, for the same power consumption, the theoretical phase noise improvement, compared to the standard differential-pair LC-tank oscillator (operating in class-B) is 3.9dB [17]. The inferior bound of the the bias voltage V_{bias} is related to the voltage drop reserved to the current generators I_1.

The plots in Fig. 1.14 confirms that for a given I_1, when V_{bias} is low (M1-M2 in saturation region) the phase noise reaches the minimum while Q_f^2 is maximized.

1.3.4 Phase Noise Analysis

The analysis of the *Capacitive Degeneration* has demonstrated that the shrinking effect exploited to perform the fine tuning, produces a negative capacitance in parallel to the tank with a quality factor Q_f much lower than one. The presence of

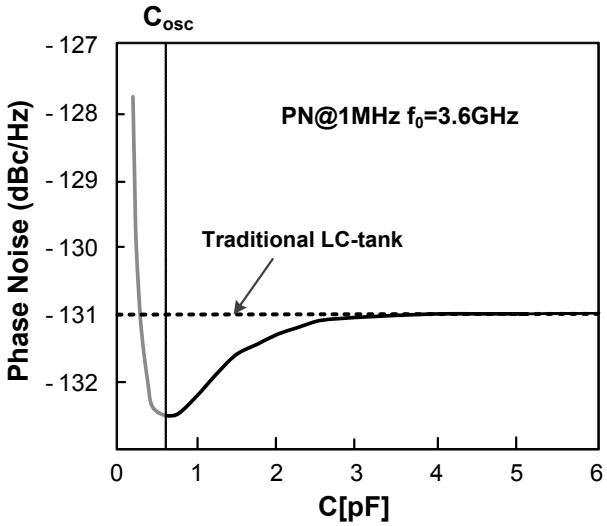

Figure 1.15: *Phase noise versus degenerating capacitance C.*

a capacitance with a poor quality factor would suggest a degradation in the phase noise of the oscillator. However it can be proved that if the capacitance C is sufficiently large, the oscillator operates as a traditional one without any penalty on the total output noise. This result has been verified simulating the phase noise at a fixed frequency offset for different values of C. From the plot of Fig. 1.15, it can be seen that when C is much greater than 2 pF (corresponding to the condition $C \gg gm/(2\omega_{LO})$), the phase noise obtained is almost exactly equal to the one without a capacitive degeneration. For lower values of C, the phase noise shows a slight improvement compared with the standard oscillator. However, no attempt was made to take advantage of this mechanism since it corresponds to a region that does not provide an adequate shirking factor. To prove how the capacitive degeneration doesn't have any impact on the phase noise, a quantitative analysis through the use of the impulse sensitive functions (ISF) [18] is reported, providing a comparison with the results obtained by Andreani et al. for the classic LC tank topology [19].

As described in the Hajimiri and Lee theory [18], the phase noise in $1/f^2$ region caused by a noise source, at the offset frequency $\Delta\omega$, depends on the ISF and it is given by:

$$L\{\Delta\omega\} = 10\log\left(\frac{\Gamma_{rms}^2}{q_{max}^2}\cdot\frac{i_n^2/\Delta f}{4\Delta\omega^2}\right) \tag{1.16}$$

where q_{max} is the maximum amount of dynamic charge loaded into the tank capacitance, $i_n^2/\Delta f$ is the white power spectral density of the noise current and Γ^2, rms is the square rms of *impulse sensitivity function* (ISF) $\Gamma(\phi)$.

Starting from the scheme in Fig. 1.16, the effect of the fine tuning capacitance C on the output phase noise is derived evaluating the ISF of the cross-coupled transistor (i.e. $\Gamma_{M1}(\phi)$ and $\Gamma_{M2}(\phi)$ with $\Gamma_{M1}(\phi) = -\Gamma_{M2}(\phi)$) and of the bias current

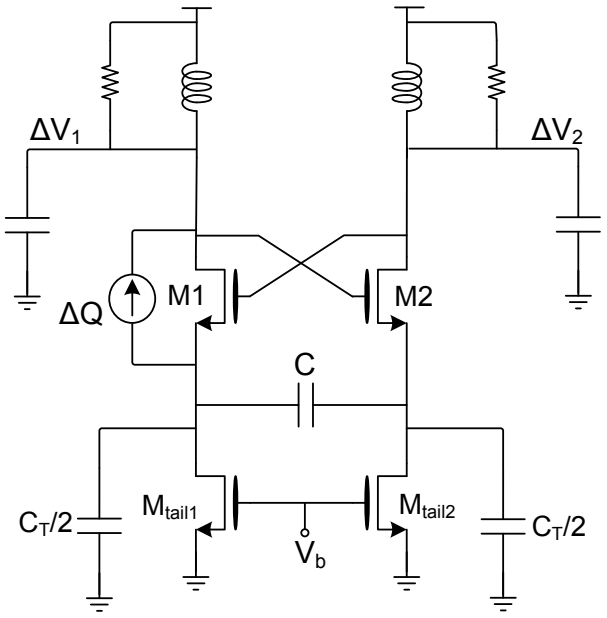

Figure 1.16: *ISF derivation in degenerate LC oscillator.*

generators (i.e. $\Gamma_{M_{tail}1}(\phi)$ and $\Gamma_{M_{tail}2}(\phi)$ with $\Gamma_{M_{tail}1}(\phi) = -\Gamma_{M_{tail}2}(\phi)$). The phase shift associated to the finite quality factor of the tank is not considered because it does not change with the capacitive degeneration of the switching pair.

Referring to the transistor M1 of Fig. 1.16, to find $\Gamma_{M1}(\phi)$, the analysis distinguishes three different cases related to the operation mode of the differential pair, each of which is associated with a different ISF: both transistors work in saturation or one of them is turn off. However, the phase noise contribution of M1 differs from the classical oscillator scheme only when both transistors lead current, because in the other cases the *impulse sensitivity function* is zero in both the oscillator architectures [19].

When the two transistors work in saturation region, the noise charge impulse ΔQ present between the drain and source of M1 produces a voltage difference between the DCO outputs that takes to the following Γ function

$$\Gamma_{M1}(\phi) = \frac{\cos(\phi)}{2} \cdot \frac{2gm_2(\phi)}{(1+C_T/C)gm_1(\phi)+gm_2(\phi)} \tag{1.17}$$

where C_T is the parasitic capacitance at the source of M1-M2.This result is very similar to the one obtained by Andreani et al, that for a the classical oscillator is given by

$$\Gamma_{M1}(\phi) = \frac{\cos(\phi)}{2} \cdot \frac{2gm_2(\phi)}{gm_1(\phi)+gm_2(\phi)} \tag{1.18}$$

Equation 1.17 differs from 1.18 for the presence at the denominator of the term $gm_1 \cdot C_T/C$ which reduces the effect of the switching transistors on the phase noise.

However, as explained in the beginning of this section, to sustain the oscillation and to achieve the desired resolution C should be much greater than C_T making the difference between 1.17 and 1.18 negligible.

An analogous approach can be used to find the ISF of the bias current generators ($\Gamma_{M_{tail}1}(\phi) = -\Gamma_{M_{tail}2}(\phi)$). Once again it can be proof that the new ISFs differ from the traditional one ($\Gamma_{M_{tail}}(\phi)$) only when both transistor are on, having

$$\Gamma_{M_{tail}1}(\phi) = \frac{\cos(\phi)}{2} \cdot \frac{(1+C_T/C)gm_1(\phi) - gm_2(\phi)}{(1+C_T/C)gm_1(\phi) + gm_2(\phi)} \tag{1.19}$$

and from [19]

$$\Gamma_{M_{tail}}(\phi) = \frac{\cos(\phi)}{2} \cdot \frac{gm_1(\phi) - gm_2(\phi)}{gm_1(\phi) + gm_2(\phi)} \tag{1.20}$$

Equation 1.19 contains once again the factor proportional to the radio of the two capacitances C_T and C, in this case both at the numerator and at the denominator. As explained before, this factor is irrelevant for the large value of C used.

When only one transistor of the cross-coupled pair is on, the large capacitance C ($C \gg gm_1/\omega_{LO}$) produces a short between M_{tail1} and M_{tail2} making the ISF equal to one like the classic case [19].

1.3.5 Positive vs Negative shrunk capacitance

The negligible effect of the shrinking capacitance technique on the total output noise could be erroneously justified by the fact that the added capacitance is small and thus, although it has a poor quality factor, does not significantly affect the tank losses. According to this reasoning, adding in parallel to the tank a capacitance C in series with a positive conductance $gm/2$ as in Fig. 1.17 (instead of negative one as in Fig 1.7) could appear to be another good way to exploit the capacitive degeneration principle. The impact on the DCO phase noise by the use of a positive conductance instead of a negative one can be evaluated staring from the expression of the phase noise of a traditional LC oscillator [19]:

$$L_{classic}\{\Delta\omega\} = 10\log\left[\frac{k_B T}{2A_{tank}^2 C_{tank}^2 R\Delta\omega^2} \cdot \left(\gamma + 1 + \frac{\eta}{2}\gamma g m_T R\right)\right] \tag{1.21}$$

where k_B is the Boltzmann constant, T is the absolute temperature, A_{tank} is the maximum amplitude of the output waveform, C_{tank} and R are the resonant capacitance and resistance of the tank, gm_T and η are the transconductance and the ISF_{rms} of the tail source [19]. For a given oscillator amplitude A_{tank}, the new phase noise expression can be derived by equation 1.21 assuming a conductance $gm/2$ in parallel to the tank resistance R, obtaining

$$L\{\Delta\omega\} = L_{classic}\{\Delta\omega\} + 10\log(1 + Rgm/2) \tag{1.22}$$

Contrary to the solution proposed, in this case the degradation of the phase noise is proportional to the conductance gm used to perform the capacitance shrinking.

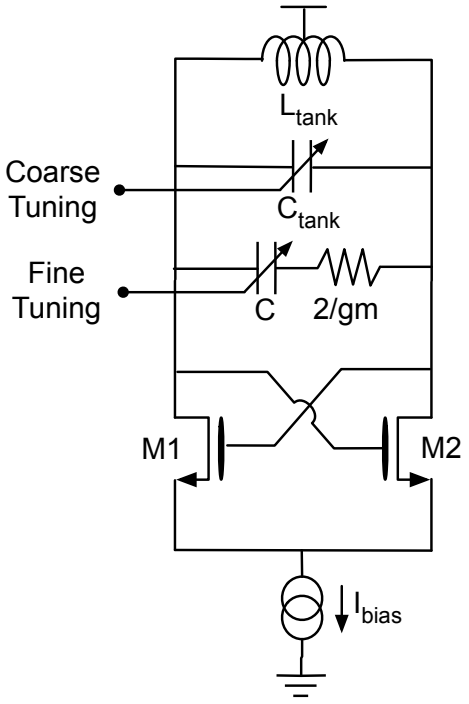

Figure 1.17: *DCO scheme with the positive shrunk capacitance.*

Since the value of *gm* sets a constraint on the maximum fine-tuning range available (equation (8)) it is better to rewrite 1.22 as follows

$$L\{\Delta\omega\} = L_{classic} + 10\log\left(1 + 4Q_T\frac{\Delta\omega_{fine}}{\omega_{LO}}\right) \tag{1.23}$$

where *gm* is given by the equation 1.14 and Q_T is the quality factor of the original resonator given by $R_{LO}C_{tank}$. From 1.23 it is clear that no penalty on the total outputs phase noise can be obtained only in the limit of a fine tuning range that approaches zero. In comparison with the solution proposed, assuming for the tank $Q_T = 18$, $\omega_{LO} = 3.6GHz$ and $\Delta\omega_{fine} = 50MHz$ (which correspond to a usable tuning range of 10MHz) the degradation of the phase noise is around 3dB. This penalty is even worse if the Q_T and/or the tuning range are increased.

Chapter 2

The All Digital PLL

Digital PLLs are usually obtained from analog ones splitting the loop into two domains, the analog one, which contains the oscillator, and the digital one, which typically includes the loop filter. The position and the characteristics of the A/D and D/A interfaces characterize the architecture of the digital PLL giving rise to several published topologies.

In the all digital PLL presented in this chapter, the D/A interface is placed at the DCO and the A/D interface is placed at the PFD level, using a high resolution TDC to perform phase comparison [29]. The DCO is based on the capacitive degeneration described in the previous chapter and it has enough resolution not to require $\Sigma\Delta$ dithering. The analog path from the RF output to the divided edge is exactly the same as in a classic PLL. The architecture af the frequency synthesizer is shown in Fig. 2.1 and implements a type II fractional-N loop. There is a straightforward analogy with the analog PLL. The main differences is that in the digital domain an accurate $\Sigma\Delta$ noise cancellation can be achieved and that the loop filter can be easily reconfigured. The latter possibility [9] allows not only reconfiguration to different standards but also the use of gear shifting to achieve very fast locking times.

An alternative approach to implement a digital PLL consists in placing the A/D interface directly at RF, using a counter at the output of the DCO (or after a few divider stages to decrease the counting frequency). This solution eliminates the need for a multi-modulus divider chain replacing it with an RF-counter [9][21][29][30]. The operation of a multi-modulus divider however does not differ in any fundamental way from that of an edge counter, even though some differences on power consumption and synchronous behavior might apply. The comparison between the two digital PLL topologies is further carried out in [29], where the conclusion is reached that for the same TDC and DCO dynamic ranges, the two architectures are completely equivalent when a 1st order $\Sigma\Delta$ modulator is used in the fractional-N divider. The ADPLL presented in this chapter uses a first-order $\Sigma\Delta$ modulator to control the fractional-N loop since it requires the smallest dynamics for the TDC. As for the D/A position, some solutions implement an analog VCO controlled through a DAC [22], thus shifting the interface at the filter output. Even though

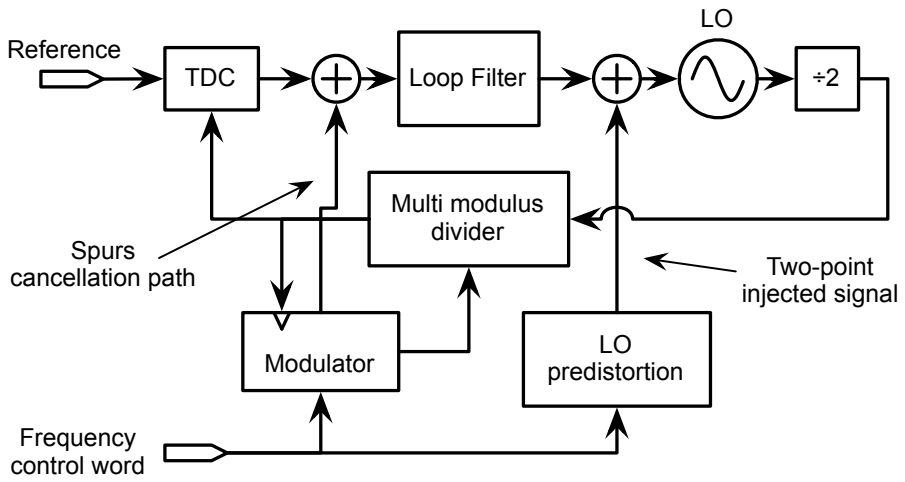

Figure 2.1: *Fractional-N, two-points modulation ADPLL architecture.*

conceptually straightforward, this solution maintains the same issues of coupling and sensitivity of an analog PLL and requires a very careful DAC design in terms of noise and supply rejection.

The ADPLL is targeted for a GMSK transmitter using direct phase modulation. The 2G transmission poses extreme challenges on the DCO phase noise profile. In the case of the GSM the required phase noise (PN) of -165dBc/Hz @ 20MHz demands also a DCO frequency resolution below 1KHz when a carrier of 900MHz is used [9]. At the same time, if an in-band phase noise below -105dBc/Hz is sought, a TDC time resolution close to 5ps is required for a 2GHz output carrier and a 26MHz reference clock.

The insertion of a direct modulation path leds to a two-points modulation scheme that ideally provides flat phase modulation response no matter which loop bandwidth (BW) is selected. Therefore, the PLL BW can be kept small to achieve low noise and spur into the adjacent channel. In principle this feature can also be leveraged to implement a polar transmitter for non-constant envelope standards (e.g. EDGE or WBCDMA).

As a final remark, it is easily understandable that the overall operation of the ADPLL must rely on multiple calibration loops. The most important one is TDC gain calibration to achieve accurate $\Sigma\Delta$ noise cancellation. Any gain mismatch here translates not only into phase noise degradation but also into possibly large fractional spurs. Another important calibration is DCO linearization, as the dither-less DCO used in this PLL [16] exhibits a systematic non-linear characteristic that would make accurate modulation unachievable.

The ADPLL design has involved more people both form the University of Pavia and from Marvell. The team was mainly formed by the author, Luca Vercesi (Marvell), Antonio Liscidini (University of Pavia) and Fernando De Bernardinis

(Marvell) under the supervision of Francesco Rezzi (Marvell) and Rinaldo Castello (University of Pavia). Also other people form Marvell were involved in particular steps of the project: Danilo Gerna, Luca Romanó, Antonio Milani, Enrico Sacchi, Paolo Rossi, Pierandrea Savo, Valeria Garofalo, Francesco De Paola, Patrizia Mastromatteo and Riccardo Straus. In particular, the TDC and the architecture of the frequency synthesizer has been deeply studied, developed and designed by Vercesi and De Bernardinis. The author gave his contribution to the develop of the ADPLL and he designed the DCO.

The first part of the chapter is focused on the time-to-digital converter and its quantization noise. Then the architecture of the DCO is presented and finally, the ADPLL is described.

2.1 Time to Digital Converter

The Time to Digital Converter (TDC) is a particular type of Analog to Digital Converter (ADC) where the analog input is the timing difference between two events. It replaces the analog Phase Detector (PD) and digitalizes the delay between the divider output and the reference signal. The TDC represents one of the key building blocks of the ADPLL since its resolution limits in-band noise, while its linearity sets a lower bound for the power level of fractional spurs [21]. In terms of resolution, independently of the ADPLL architecture (with or w/o divider), the TDC must provide a time quantization that is a small fraction of the DCO period to guarantee an acceptable in-band noise.
Assuming a random input signal, the TDC introduce a white noise with a power spectral density given by:

$$q_{TDC}(f) = \frac{\Delta\phi^2}{12}\frac{1}{f_R} = \frac{1}{12}\left(2\pi\frac{\Delta t}{T_R}\right)^2\frac{1}{f_R} \tag{2.1}$$

where Δt is the TDC time resolution, f_R and T_R are respectively the frequency and the period of the reference signal. Inside the loop of the ADPLL, the transfer function of the TDC noise is a low-pass function with the corner frequency equal to PLL bandwidth and the magnitude, at low frequency, equal to the square of the ratio N_{div} between the output frequency and the reference one. Consequently, the contribution of the TDC noise to the output phase noise is given by:

$$PN(f) = q_{TDC}\cdot N_{div} = \frac{1}{12}\left(2\pi\frac{\Delta t}{T_{DCO}}\right)^2\frac{1}{f_R} \tag{2.2}$$

where T_{DCO} is the period of the oscillation. In the case of the GSM, the required in-band phase noise is -100dBc/Hz, demanding a TDC time resolution of few ps. For example, assuming the f_{DCO} of 2GHz and f_R equal to 26MHz, the TDC time resolution of 5ps limits the in-band noise to -110dBc/Hz.

To overcome the limit set by the minimum delay available in the technology, several architecture were proposed in literature. Linear Vernier TDCs quantize

time differences exploiting the cumulative delay difference of two lines based on elements whose delay is greater than the target resolution [24]-[25]. This technique can overcome technology limitations as it separates minimum stage delay from resolution. However, its full scale is limited by the number of delay elements that grows exponentially with the number of bits. Multi-path approaches [10]-[11] perform interpolation between several parallel delay lines and, as for the linear Vernier, has a full scale that is severely limited by the number of delay stages required. A larger number of bits can be obtained adopting more complex architectures directly derived from voltage-to-digital converters as the GRO based TDCs [26]-[27], that provides a shaped quantization noise like in sigma-delta ADCs, and the two-steps TDC proposed in [28] based on a time amplifier. The main drawback of these approaches is that their power efficiency decreases reducing the number of quantization levels synthesized. From this point of view when 6 bits or less are demanded, other topologies like flash TDCs becomes competitive.

The TDC architecture adopted in the ADPLL prototype is the 2-dimension Vernier TDC, proposed in 2010 by Vercesi, Liscidini and Castello [23]. The TDC that was used in the prototype was entirely designed by Vercesi. The author has not taken part to the TDC ideation and design.

2.1.1 Two-Dimensions Vernier TDC

Linear Vernier TDCs are probably the simplest topology to implement high-resolution converters. However, the large number of delay stages required for moderate conversion ranges increases the integral non-linearity (INL) of the time-to digital conversion. In fact, in the classic linear Vernier, the time quantization is realized by taking only time differences only between taps located in the same position of the two delay lines (Fig. 2.2.a). Since a delay Δ is accumulated after each stage, a signal edge that lags a reference edge by $n\Delta$ at the input of the lines will lead it after n stages. Inserting one flip-flop for each delay line stage it is then possible to produce a digital thermometric code that represents the digitalization of the time difference [24]. This provides uniform quantization with N codes (N is the length of each delay line), each representing a time step Δ (the TDC resolution).

When all possible differences between the taps are considered, it is possible to define a plane (named *Vernier plane*) as the one reported in Fig. 2.2.b [23]. In this way, having two lines with N elements each, N^2 quantization levels are defined. This approach can significantly decrease the number of stages of the delay lines needed to achieve a given number of quantization steps with the same resolution Δ. The reduction of the number of stages not only reduces the complexity and the power consumption of the structure, but also significantly reduces the distortion of the TDC compared to linear Vernier topology [23]. Finally, it is easily recognizable that the structure proposed can be considered as an extension of the both single delay line and linear Vernier TDCs which lie respectively on the borders and on the diagonal of the Vernier plane (Fig. 2.2.b). However, in the Vernier plane only a part of the generated quantization levels is uniformly spaced and there are some

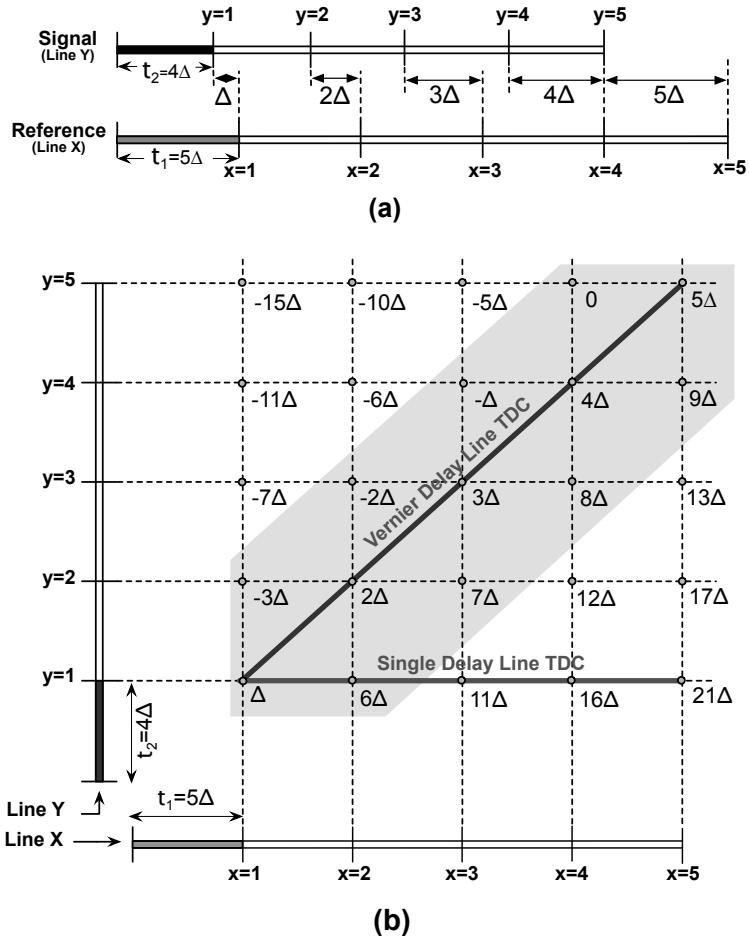

Figure 2.2: *(a) linear and (b) 2-dimension Vernier TDCs.*

missing delays (e.g. 10Δ, 14Δ). Top overcome this limitation one of the two delay lines need to be enlarged. This increases the part of the Vernier plane is taken into account and a wider range of uniformly spaced quantization levels is generated.

The realized 2-D Vernier TDC schematic diagram is shown in Fig. 2.3. The two delay lines define the Vernier plane that is completely covered by a matrix of SR latches used as a time comparators. The designed of the latch is critical and the most important parameter for the design of this block is the offset matching [23]. In fact, the offset matching among the comparators affects the TDC linearity with a direct impact on the DNL (its influence on INL is less significant since the error introduced is not accumulated during the quantization process). Each latch produces a 1 or a 0 depending if the rising edge of the reference leads or lags the rising edge of the signal. However, while a linear Vernier produces intrinsically a thermometric code, in this case the outputs must be ordered following the position of consecutive quantization levels [23]. To allow proper operation over process

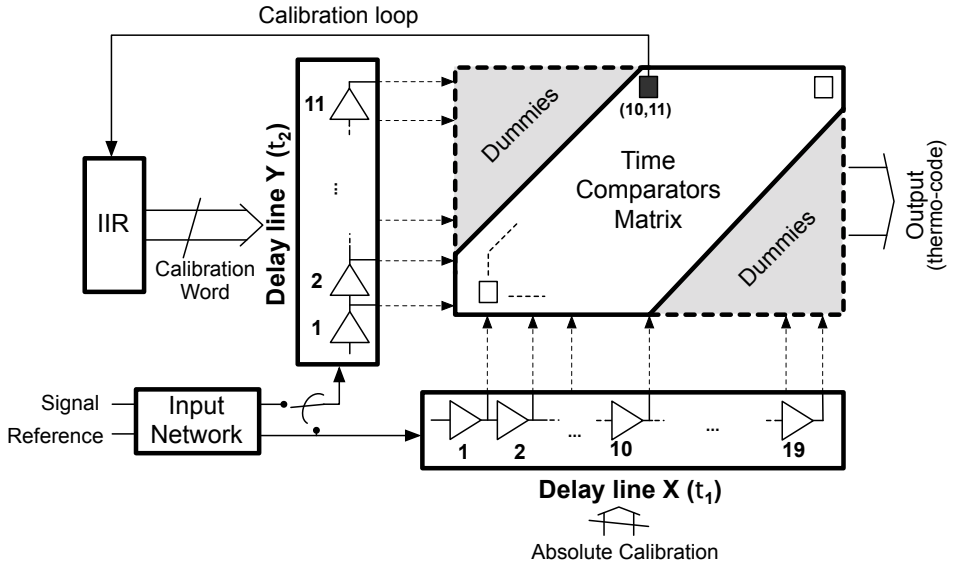

Figure 2.3: *TDC scheme*

and temperature change, a background DLL was used to enforce an equal length for the delay lines. This is achieved using tunable delay elements composed by a chain of two inverters. The tuning is performed acting on the capacitive load of the first inverter, generating a linear digital word-delay characteristic. Finally, the presence of two delays stage for tap offers isolation between the capacitor tuning bank and the latch, allowing to realize sharper edges in front of the latch.

In particular, the proper ratio between the delays $\tau 1$ and $\tau 2$ (in this case 11/10) is defined by a local calibration loop closed on line Y (Fig. 2.3). In the calibration phase, the reference feeds both the lines and the loop forces the delay accumulated after $10\tau 1$ on the X line and after $11\tau 2$ on the Y line to be equal. The tuning elements present in the line X are controlled at the PLL system level defining the TDC gain as described in the following Section.

Overall, the TDC is a 7-bit structure with 119 quantization levels. For line X and line Y, 19 and 11 stages are respectively used. The target resolution of $\Delta = 5ps$ is obtained choosing $\tau 1 = 55ps$ and $\tau 2 = 50ps$, achieving a full scale of 590ps, from -45ps to 545ps. Notice that a linear Vernier approach for the same full-scale and resolution would have required two delay lines of 119 elements each (i.e. 238 stages instead of 30).

2.1.2 TDC gain calibration

The proposed ADPLL architecture is based on the cancellation of $\Sigma\Delta$ noise whose accuracy is completely dominated by the gain of the time-to-digital conversion [29]. Therefore an accurate background calibration scheme to track gain variations was adopted. This scheme is widely used in ADC calibrations and has

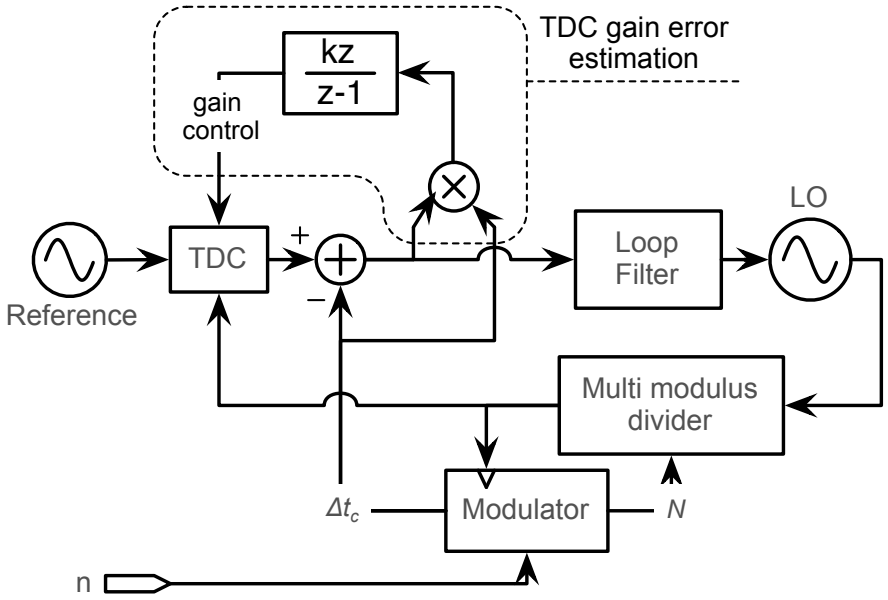

Figure 2.4: *TDC gain calibration loop*

been extended to TDCs as well [6]. Background operation is achieved correlating the signal after cancellation with the incoming signal, as in Fig. 2.4. When convergence is reached, the signals become uncorrelated. If a gain mismatch is present, the sign of the correlation can be used to feed a filter and drive gain correction. The bandwidth of the filter determines the accuracy of the correction and can be changed during operation. On the other end, the accuracy of calibration is limited by the granularity of the correction that is implementable around the TDC. The TDC gain is controllable in the analog domain with 10ps resolution. This is not enough and the TDC output is further corrected in the digital domain to achieve a finer resolution. The calibration machine implements the necessary logic to merge coarse analog with fine digital calibration. It is important to note that the TDC gain calibration loop has to be disabled when the fractional spur falls in band as it alters the correlation mechanism and decreases the calibration accuracy.

2.1.3 TDC linearity calibration

In a PLL implementing first-order ΣΔ residue cancellation, the TDC linearity has a deep impact on the fractional spurs that are generated in the PLL. Therefore, TDC linearity has to be trimmed to achieve INL well below 1 LSB. Because of this, we achieve linearity calibration with a foreground process which is aimed at identifying individual threshold non discrepancies and correcting them (Fig. 2.5). Threshold identification is achieved through a histogram method as from converter literature. Once the actual thresholds have been estimated, the mismatch on the X and Y delay lines are estimated as well. This is optimally achieved averaging

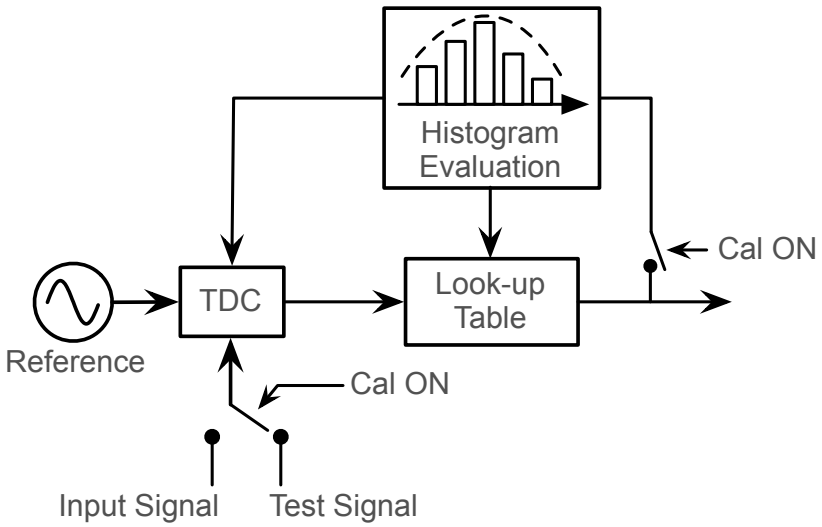

Figure 2.5: *TDC linearity calibration loop*

through least squares fitting of measured thresholds with inverted delays. In more implementable terms, the delay increments on the X and Y axes are used to estimate inverter delays and compute analog correction adjustments. This process is reiterated until convergence is achieved. Then, a digital fine correction step is performed where each individual threshold is digitally shifted to minimize INL. This results in uneven quantization steps, but correct INL. Because of a digital limitation in the current silicon, the amount of fine correction is limited to 0.5 LSBs which nonetheless provide 5 to 10 dB improvement in the lab on the spurs level. Simulation results with 6 bit digital correction indicate a margin of improvement of at least 10 dB, which would take spurs below -60dBc.

2.2 Digitally Controlled Oscillator

In the ADPLL, the DCO with the capacitive degeneration was adopted due to its fine frequency resolution that minimizes the contribution of the quantization noise to the out-of-band noise of the frequency synthesizer. As deeply described in the chapter 1 the the fine-tuning bank is moved from the tank to the sources of the switching pair of the LC oscillator exploiting an intrinsic shrinking effect present in this architecture. Fig. 2.6 reports the topology of the DCO, obtained starting from an existing VCO architecture which the dither-less tuning scheme was applied to. It was designed using the *Current Calibration* technique to trim the fine frequency tuning range and resolution. This topology differs from the original one proposed in mioDCO, since in this case the oscillator was biased through a current genera-

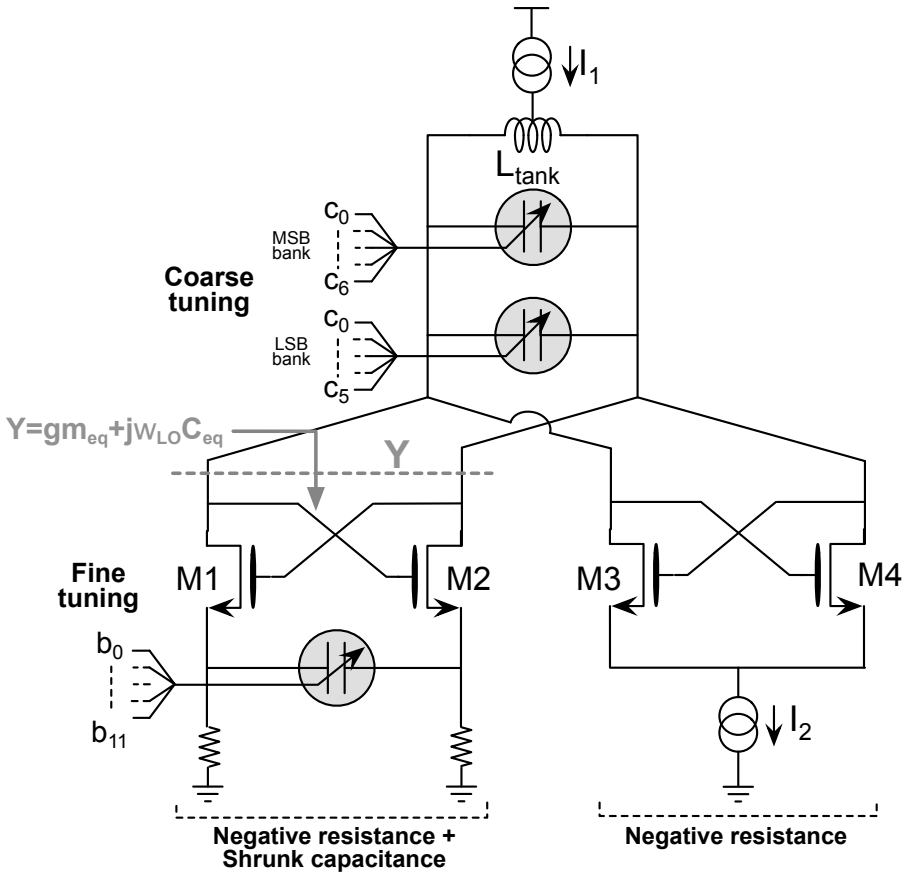

Figure 2.6: *ADPLL digitally controlled oscillator scheme*

tor connected between the voltage supply and the center the tap of tank inductor. Placing the current source between the power supply and the DCO improves the Power Supply Rejection (PSR) of the noise associated with the voltage regulator that supplies the oscillator. The current generator I_1 biases the whole DCO, setting the amplitude and the phase noise of the oscillator. The second generator I_2 biases the cross coupled pair M3-M4, controllung the current $I_1 - I_2$ that flows in the degenerated switching pair. This solution allows to control the transconductance of the degenerated switching pair (defining Q_f and the DCO frequency resolution) and to minimize the parasitic capacitive load at the sources of M1- M2 that reduces the fine-tuning range. The coarse tuning of the frequency, used to compensate the process and temperature variation and to select the channel is still performed at the resonant load through two capacitive banks (MSB and LSB banks) of 7 and 6 bit respectively that tune the frequency over a range of 33% across 7.2GHz. The fine-tuning bank placed between the sources of the switching pair M1 and M2 is realized as reported in Fig. 2.7. The frequency is controlled by 12 bit. The 8 most significant bits (MSB) are used to control a matrix of 16x16 varactors. All elements

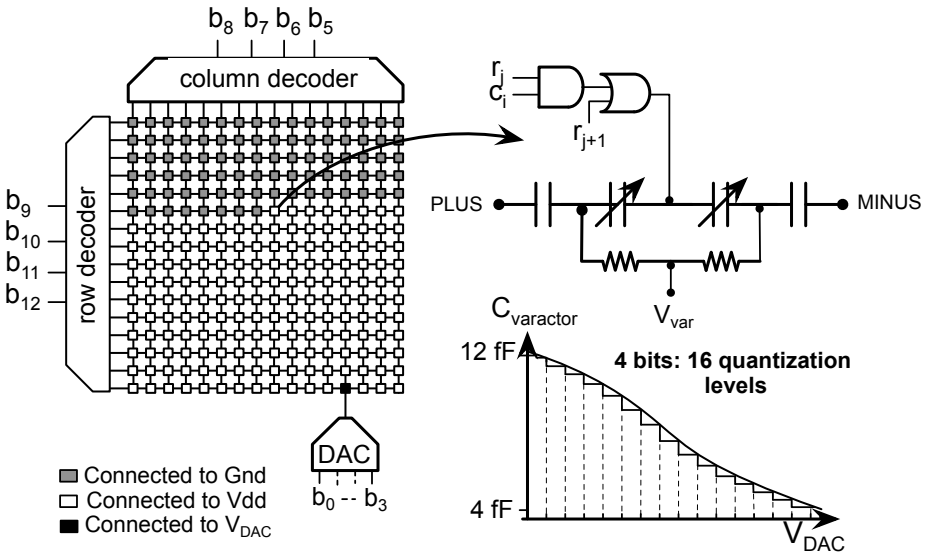

Figure 2.7: *Fine-tuning bank of the ADPLL digitally controlled oscillator scheme*

except one are connected either to the voltage supply (V_{dd}) or to ground generating a thermometric filling of the matrix. The remaining varactor is connected to the output of a 4-bits digital-to-analog converter (DAC) which provides 16 additional voltage levels between VD_{dd} and ground. Since only one varactor is biased in the high-gain region of its characteristic, the sensitivity of the oscillator to noise and spurious signals coupled at the DAC output is negligible.

2.2.1 DCO calibration

Accurate 2-point modulation relies on reliable DCO gain. However, the k_{DCO} gain is subject to process and environmental factors and it cannot be known precisely. Moreover, in the presented PLL, as shown in chapter 1, the DCO fine-tuning characteristic is non-linear and the oscillator is the only component of the two-points modulation that, acting outside the loop band is not linearized by the loop. During 2-point modulation, the instantaneous frequency deviation is presented as a control word to the DCO assuming a linear relationship. Therefore, it is of uttermost importance calibrating not only gain, but also non-linearity so as to provide a "nominal" DCO to the modulation engine. We also remark that during modulation the DCO input signal cannot be regarded as a "small" signal since large portion of the DCO input range may be explored.

In all digital PLL, the DCO gain is generally calibrated with a digital normalization based on a background algorithm function of the phase error present in the loop [9]. The same approach could be extended to provide the pre-distortion of the entire DCO characteristic. However this operation is not trivial and inside the PLL loop would result to costly in term of computation. The solution proposed

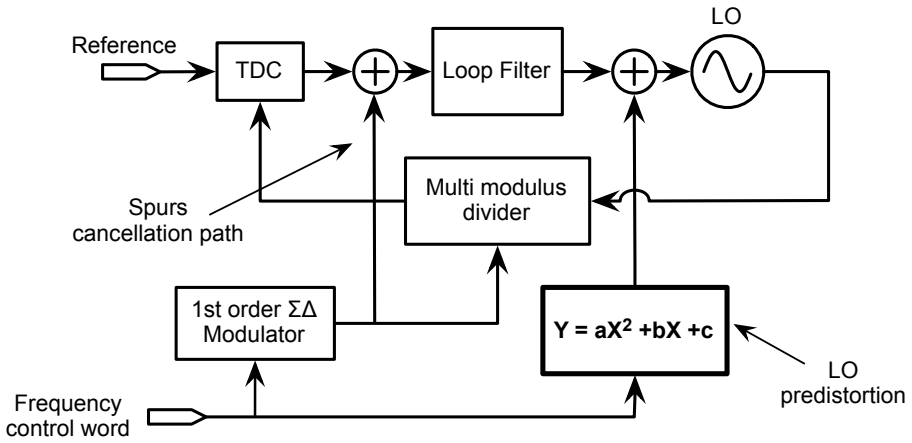

Figure 2.8: *Predistortion calibration*

in this ADPLL (developed in collaboration with L. Vercesi and F. De Bernardinis from Marvell) is shown in Fig. 2.8. The idea is to perform the pre-distortion not within the loop but on the two-point modulation signal. The main advantage of this solution is to reduce the computational complexity on the most critical path of the system.

A polynomial equation was used for the LO pre-distortion. The higher is the order of the polynomial equation, the more accurate is the approximation of the

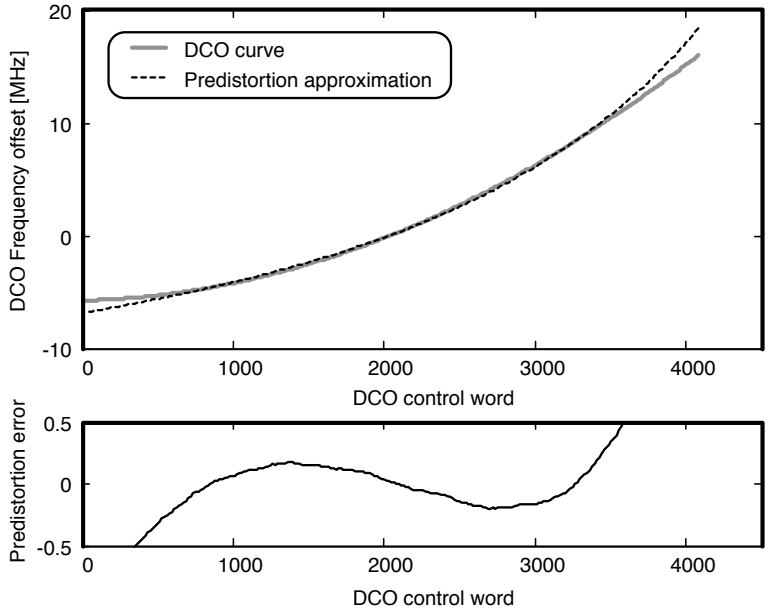

Figure 2.9: *Predistortion approximation*

nonlinear function. However, the accuracy trades off with the implementation complexity that grows with the polynomial order. A second order approximation was chosen for the LO pre-distortion. Polynomial coefficients are efficiently computed measuring the DCO control word variations when a given frequency is shift imposed through the sigma-delta modulator. As it will be shown in the measurements of the ADPLL, the DCO calibration step adds 17μs to the calibration time. The Fig. 2.9 reports the comparison between the fine-tuning characteristic and the approximation of the 2^{nd} order polynomial showing a very good agreement.

2.3 Frequency and phase locking acquisition

PFD based PLLs whose linear tuning range is less than the required one usually achieve locking in 2 steps, first a coarse frequency tuning is performed re-centering the LC tank and then the real phase locking acquisition is achieved acting on the linear control node. The TDC adopted in this work does not provide the equivalent of a PFD for locking purposes. it estimates the delay between the reference and the divider output edges whatever their frequencies are. Even if multiple signal cycles could occur in one reference period, the TDC would not detect them. Frequency detection is therefore required. Moreover, the linear range of the TDC (600ps) is limited to one DCO period, thus very small compared with the reference period (2%). The initial phase error can be as big as the reference period and the information that the TDC can provide during phase locking is quite limited. During phase locking, the TDC saturation is a highly nonlinear phenomena, which is highly undesirable. Therefore, a bridge is needed between coarse frequency calibration (AFCAL-Amplitude and Frequency CALibration) and PLL operation. Two calibration steps are thus added, an FLL phase to compensate for the PD-only behavior of the TDC and an Edge-Search phase to compensate for the very small linear range of the TDC. Finally, linear locking is accelerated through gear shifting. In fact, the ADPLL loop filter design has a great impact on phase locking acquisition. Wider loop bandwidth benefits the locking process, but narrow bandwidth benefits the LO spectral purity. The gear shifting approach starts the ADPLL with a wide acquisition bandwidth and it narrows it down once locking has been acquired.

2.3.1 Frequency Locked Loop

The first step of the locking procedure is to lock the ADPLL frequency to the desired value (Fig. 2.10). Since the TDC does not provide any frequency information, a frequency detector is required to be used in an auxiliary Frequency Locked Loop (FLL). The FLL is realized through the use of an RF counter that counts the number of LO periods that occurs in one reference period. The counter output is compared to the FCW and the resulting frequency error is fed to the loop filter, which consists of a simple integrator. The filtered frequency control word act

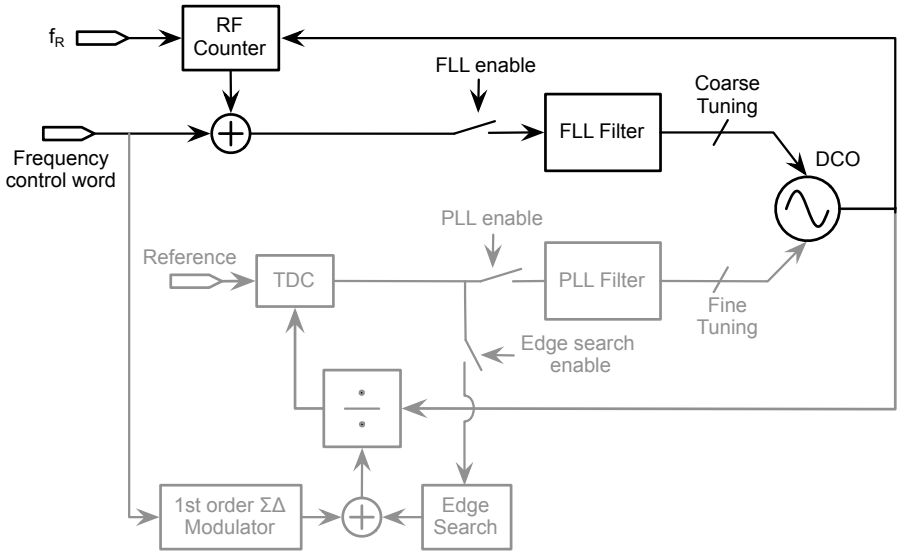

Figure 2.10: *ADPLL frequency locked loop*

on the coarse tuning bank of the DCO looking its frequency. The resulting system has only one integrator in the loop, resulting unconditionally stable.

The ADPLL stays in FLL mode until the frequency errors falls within the linear range of acquisition.

2.3.2 Edge Search Loop

The narrow TDC linear range requires that the divided LO edge and the reference edge are closer than one T_{LO} from each other to operate linearly. If not, the TDC saturates and the loop dynamics become highly non linear and much slower. This problem can be solved with a certain elegance keeping the system in FLL mode and controlling the multi-modulus divider to make it swallow LO edges until the TDC enters the linear region. The Fig. 2.11 reports the diagram block of the ADPLL when the edge search is active. Acting on the multi modulus divider control, only the divider state variable is manipulated without affecting the frequency loop that is kept active. In practice, if the TDC output is upper saturated the divider control is reduced, while if TDC output is lower saturated the divider control is increased.

The edge searching can be classified as a type one phase locked loop: the TDC still acts as a phase detector while the divider acts as a local oscillator.

A linear search algorithm was implemented in the prototype; this solution is capable of bringing the TDC within its linear region within at most N-1 reference cycles, depending on the initial phase offset. This can be easily improved with more sophisticated search algorithms, but in this prototype simplicity was given priority, as the overall improvement on locking was not critical.

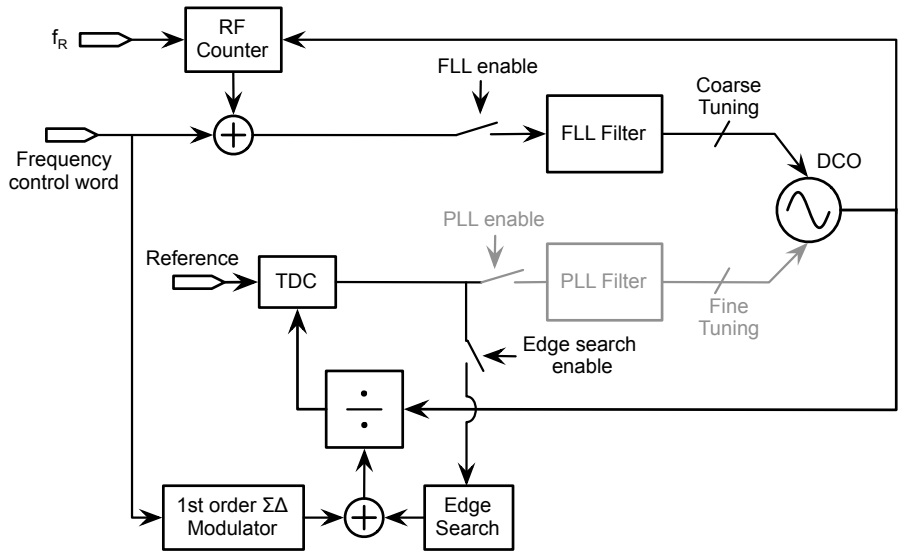

Figure 2.11: *ADPLL edge search*

2.3.3 Phase locking and Gear Shift

After the Edge Search phase is completed, the FLL is disabled and the PLL is activated with maximum bandwidth. The Fig. 2.12 reports the schematic representation of the proposed PLL. A maximum of 4 gear shift steps can be programmed to achieve the final bandwidth. This technique has been propose for analog PLL ([31]). However it is generally difficult to perform a PLL gear shifting in analog circuits because of the imperfect matching and voltage or charge losses during switching. Due to the fully digital implementation, the manipulation of filter coefficients and state variables is very simple. When gear shift is performed, the loop filter coefficients are changed to the values of the new filter transfer function.

The first gear shift is triggered as the DCO input variation becomes smaller than a programmable threshold, thus indicating steady state operation. However, the following gear shifts are time triggered to avoid the long observation time required to detect the steady state condition. Gear shift intervals are then chosen according to their respective time constants. The overall locking process is reported in Fig. 2.13 and the relative locking time in Table 2.1. Since the locking procedure is adaptive, it depends on the initial locking conditions, with a variation of 10% over the mean locking time. The greatest part of the locking time is required by the AFCAL, which is the most conservative part of the locking process and whose time duration is almost constant taken by the previous analog PLL. On the contrary, the FLL, the Edge Search and the PLL Gear Shift sections show the highest variability due to the high sensitivity to the initial conditions. The simulation refers to a multiple Gear shift performed in three steps. The fine tuning signal calms down. The absence of spikes in the spurs compensation error highlights the effectiveness

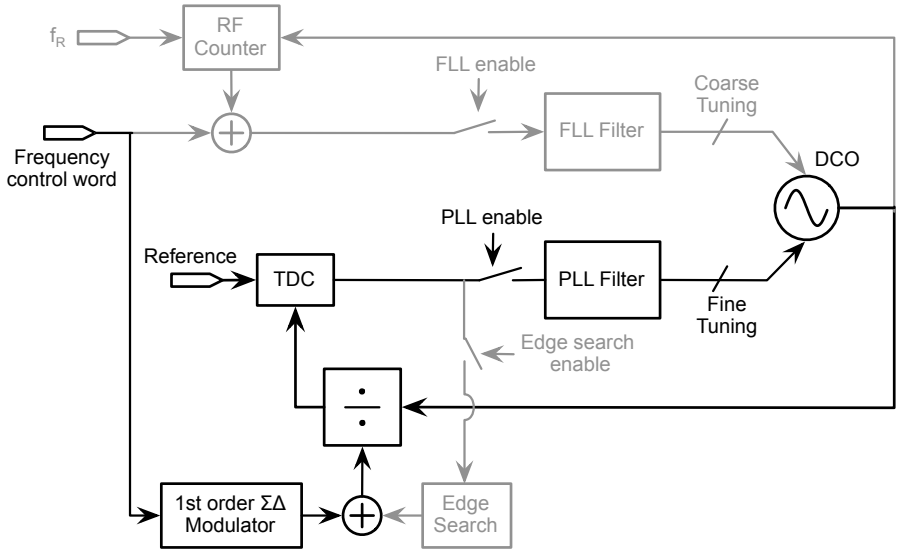

Figure 2.12: *Phase locking and Gear Shift*

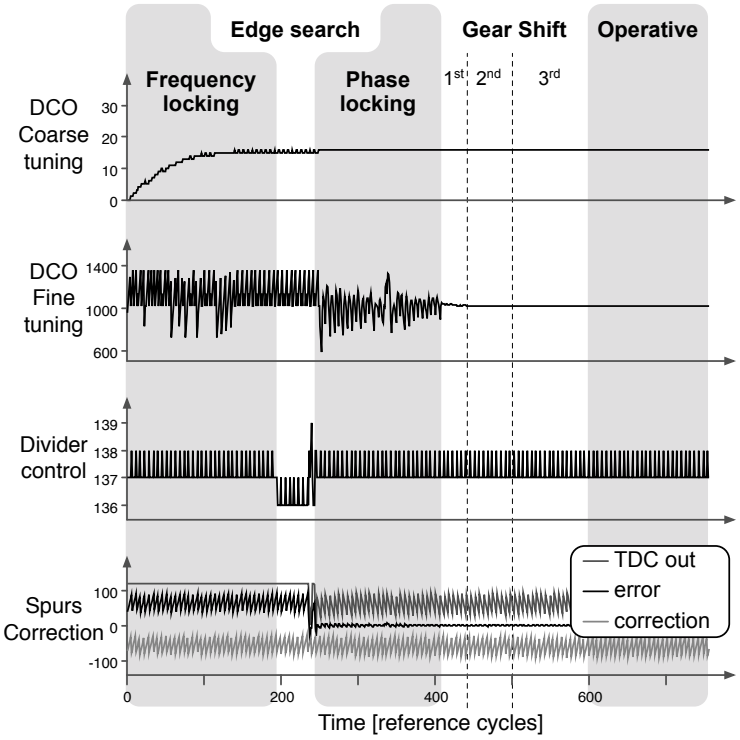

Figure 2.13: *ADPLL locking procedure simulation*

of the gear shift.

Once the gear shift is finished, the PLL is in an operative state and the DCO spectral purity is optimal.

	Time duration			average fraction of locking time	maximum end time
	Minimum	**Average**	Maximum		
AFCAL	42.5μs	**42.6**μs	42.7μs	57%	42.7μs
FLL	2.6μs	**2.9**μs	3.8μs	4%	46.5μs
Edge Search	0.2μs	**2.4**μs	4.7μs	3.3%	50.5μs
PLL WB	1.3μs	**5.4**μs	9.3μs	7.4%	59.1μs
Gear Shift	3.5μs	**3.5**μs	3.5μs	4.7%	62.6μs
DCO calibration	17μs	**17**μs	17μs	23%	79.6μs

Table 2.1: *ADPLL locking time.*

Chapter 3

High Power Efficiency Oscillators

The continuous growth of personal wireless communications demands low-cost low-power solutions in the design of wireless systems. Wireless transceivers for many standards including GSM, Bluetooth, WLAN, Wireless Personal Area Network (WPAN), and PicoRadios Wireless Sensor Network require low-power design techniques to enhance their battery lifetime and to improve their portability.

Low-voltage design is one of the choice that may save the power consumption of the analog circuits. However, this approach limits the signal amplitude and degrades the signal-to-noise ratio affecting the system performance. This is especially true for voltage controlled oscillators (VCOs) in wired and wireless communication systems due to the low phase noise required by the cellular standards. To satisfy the phase noise mask, the oscillator still represents one of the most element power-hungry elements of the transceiver. Existing techniques for low-power VCO design derive from differential-pair LC tank oscillator that ensures the best spectral purity for a given power consumption and employ either nonstandard processes or external tank components with high quality factor.

Among all the solution reported in literature, the class-C harmonic VCO, is the one that offers the best phase noise performance with the respect the same topology operating in class-B. In this oscillator the better conversion of bias current into fundamental current harmonic increase the output swing reducing the current consumption for the same phase noise performance.

In this chapter different techniques are presented to reduce the power consumption. The power scalable n-pn DCO changes the topology of the oscillator at the bands where an higher phase noise is tolerated containing the current consumption. The three other solutions, detailed in the second part of the chapter are based on class-C topology and solve the start-up problem of this architecture.

3.1 Power scalable n-pn DCO

The newest RF front-end are becoming more complicated as newer standard are introduced (e.g. LTE). Reconfigurability can be used to reduce their size, pro-

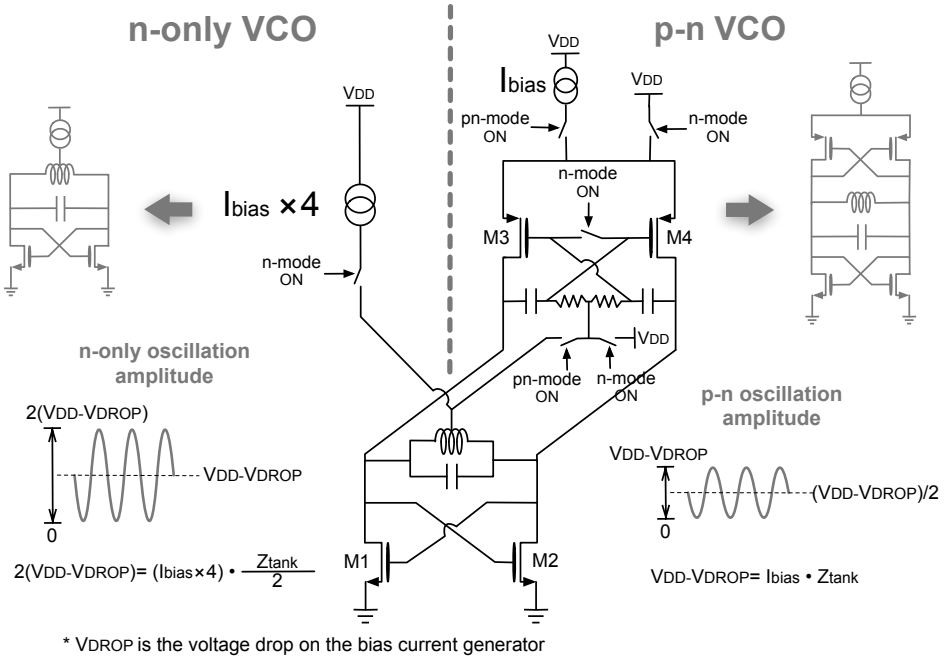

Figure 3.1: *Power scalable n-pn DCO*

vided that power consumption is not adversely affected. For 2G/3G transceivers, local oscillator (LO) generation requires significant area and power. Reconfigurable voltage-controlled-oscillators (VCOs) are generally used to maximize the achievable tuning range to reduce their number in the presence of many supported bands. However, no VCO capable to support both WCDMA and GSM has been reported that is competitive with the power consumption achieved using the traditional approach based on two different oscillators. In fact, the very demanding GSM phase noise specs require a current up to four times higher (depending on the duplexer selectivity) than that used in the WCDMA case. In the design of an LC-tank harmonic oscillators, phase noise normalized to power consumption (i.e. the figure-of-merit, FoM), reaches its optimum value at the maximum oscillation amplitude compatible with the supply voltage V_{dd} [**?**]. This condition impairs power reconfigurability of VCO since, once the tank is chosen, there is only one value of current that gives the best FoM. On the other hand, making the tank reconfigurable invariably results in a degradation of its Q, i.e. a reduced FoM.

The idea of a power scalable n-pn DCO is to keep the same (optimized) tank while switching the VCO topology from n-only to p-n. This allows to reconfigure the power consumption maintaining an almost constant FoM for both topologies. The Fig. 3.1 shows the DCO architecture and reports the equivalent schemes when the n-only and p-n configuration are selected. As theoretical derived in [**?**], for the same tank and the same supply voltage V_{dd}, n-only and p-n VCOs have the same maximum FoM, which, however, is reached using 4 times more current for the

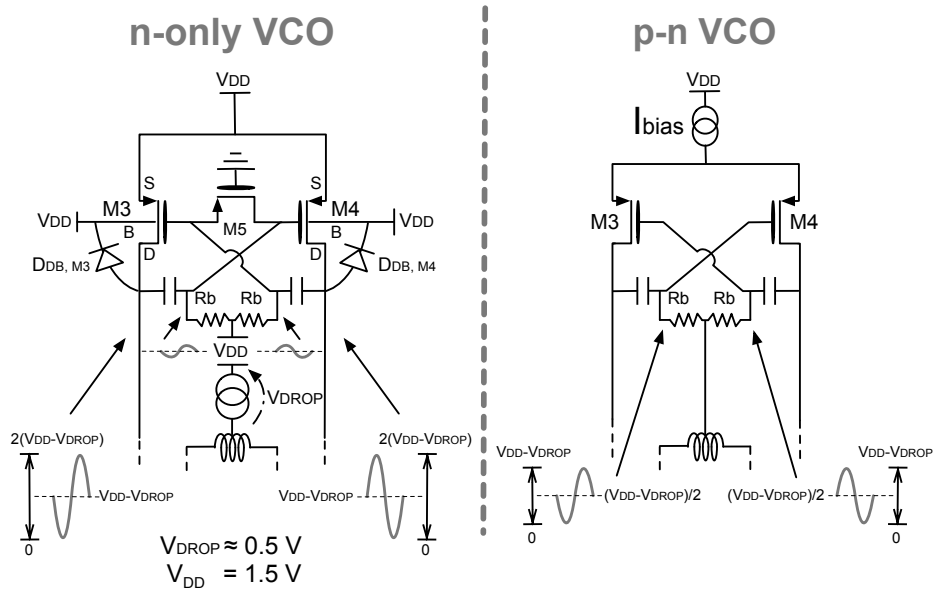

Figure 3.2: *P-MOS bias scheme*

n-only VCO. However, in the former case, the bias current is 4 times larger, the oscillation amplitude is twice as large and the phase noise is 6dB lower. This can be intuitively understood observing that, on the one hand, the FoM increases with the LO swing, and this can be twice as large for an n-only VCO, compared to a p-n one; on the other hand, a p-n VCO has a current efficiency twice that of an n-only VCO (Fig. 3.1). These observations indicate a clear path to power reconfiguration: using an n-only VCO when a very low phase noise must be achieved and switching to an n-p VCO when a higer phase noise can be accepted, saving power at the same time. More specifically, a very attractive scenario is to reduce the p-n VCO current to 1/4 of the n-only VCO configuration current: if the maximum peak amplitude is reached in both VCOs, the theoretical phase noise deterioration in the p-n configuration is exactly 6dB, keeping constant the FoM and with it the power efficiency.

Although, in principle, a reconfigurable n-only to p-n VCO seems straightforward, its implementation is not trivial. In fact, the p-MOS transistors must be completely switched off in the n-only case or the tank Q becomes seriously degraded. This affect the phase noise performance, especially when the specifics are stricter. Ensuring that this is true over a full oscillation period is difficult, since the VCO output voltage swings well above V_{dd}. As reported in Fig. 3.1, in the n-only configuration, the voltage of the output nodes swings between 0 and 2(V_{dd} - V_{DROP}), where $V_{DROP} \simeq 0.5V$ is the voltage drop on the current generator. Reported at the gate of the p-MOS cross coupled pair, it could switch on M3-M4 degrading the phase noise. This problem is solved adopting the bias scheme depicted in Fig. 3.2 for the p-MOS transistors. Drains and gates are ac-coupled through a

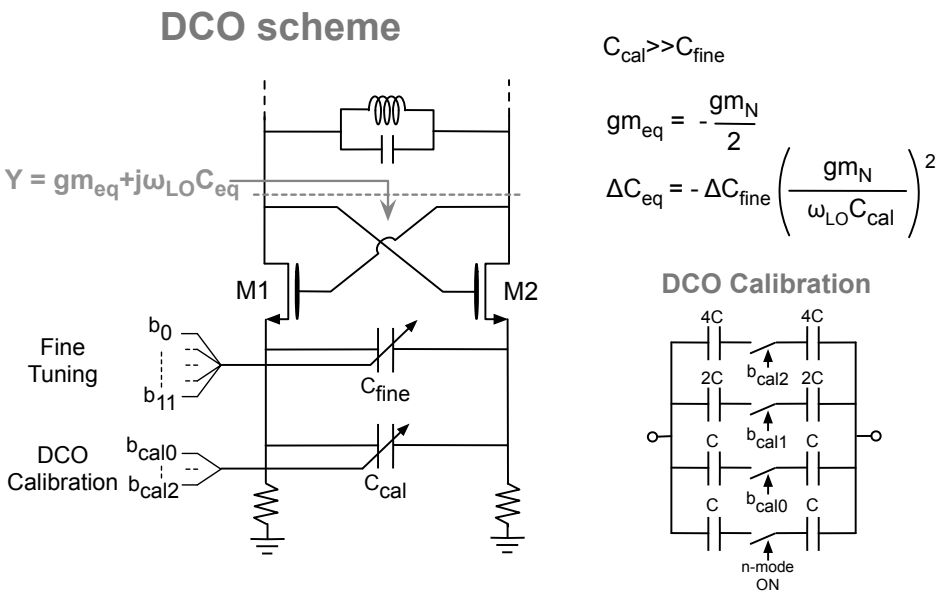

Figure 3.3: *DCO scheme and calibration*

tunable RC network, whose cut-off frequency is re- configured acting on switch M5. The ac-coupling has two purposes: to easily reconfigure the dc bias of the p-MOS gates, and to connect/isolate them to/from the VCO outputs. In the n-only VCO, both sources and gates are biased to V_{dd} and M5 is switched on (Fig. 3.2.a). In this case, the ac-coupling network has a high-pass cut-off frequency given by $2/(CR_{on})$, where R_{on} is on-resistance of M5. R_{on} is chosen small enough to guarantee a sufficient attenuation between the VCO outputs and the gates of M3 and M4, thereby keeping them off. Notice that minimizing R_{on} also maximizes the Q of the series connection of C and M5, making negligible its impact on the overall tank Q. An additional issue is that the voltage across the drain-to-bulk diodes of the turned-off p-MOS transistors should never exceed the activation voltage V_D=0.7V. This is achieved with margin, if we consider a 0.5V voltage drop (V_{DROP} in Figure 2) across the current source (carrying a maximum of 24mA), together with a V_{dd} of 1.5V.

For the p-n VCO, the sources of the p-MOS devices are connected to the bias current, while the dc voltage at their gates is equal to the common-mode voltage at the VCO outputs. This is achieved by connecting the center tap of the p-MOS bias resistors (Rbias) to the center tap of the tank inductor (Fig 3.2.b). Transistor M5 is now turned off, making the new high-pass cut-off frequency equal to $1/(CR_b)$. Choosing an R_b large enough to decrease the high-pass cut-off frequency well below ω_{LO} ensures proper operation of the p-MOS pair without introducing extra tank losses.

In the proposed VCO, power reconfigurability has been combined with the flexibility of a digitally-controlled-oscillator (DCO). The scheme adopted is the

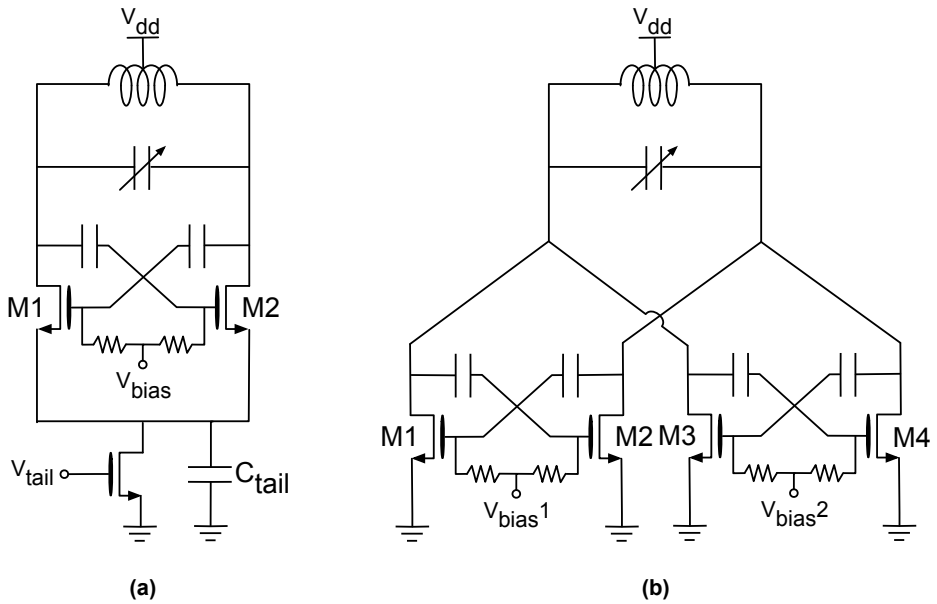

Figure 3.4: *Original class-C oscillator [17]; b) dual-conduction oscillator [35]*

dither-less one proposed in [16], which consists of a capacitively-degenerated n-MOS pair. As reported in Fig. 3.3, the capacitance C_{fine} is reflected in parallel to the tank shrunk by a factor proportional to $gm_N/(\omega LOC_s)$, where gm_N is the n-MOS transistor transconductance averaged over one LO period, while C_s is the total capacitance between the n-MOS sources ($C_{fine}+C_{cal}$). The scheme of Fig. 3.3 differs from the one reported in [16] with respect to the trimming of the shrinking factor. The DCO is based on the Capacitive Calibration and, as depicted in Fig. 3.3, the frequency resolution and tuning range are tuned acting on C_{cal} as opposed to the n-MOS bias current (i.e. gm_N). In this way, DCO frequency resolution and current consumption can be scaled independently.

In the chapter 4 the prototype and the measurements are explained.

3.2 Hybrid Class-C/Class-B VCO

The design of very-wide-band CMOS voltage-controlled oscillators (VCOs) compliant with the phase noise specifications of cellular transmitters is non-trivial, especially considering the GSM standard, where the phase noise exhibited by the local oscillator (LO, generated by the cascade of VCO, buffers, and usually frequency dividers) should be several dB below -162dBc/Hz at 20MHz frequency offset from the carrier. As shown in [34], challenging phase noise requirements can embrace the WCDMA transmitter as well (e.g. -166dBc/Hz at 45MHz frequency offset for WCDMA band VIII), if cheap antenna duplexers are chosen to minimize costs. High spectral purity at low power consumption is one of the more challenging targets in the design of a frequency synthesizer for wireless communication

handsets. In such scenarios, and particularly in the very relevant case of WCDMA transmitting at moderate power levels, the LO power efficiency is still one of the limiting factors for a long-lasting battery life, motivating the ongoing quest for VCO power optimization. In the last decade both academy and industry investigated and proposed several techniques to improve the phase noise performance of the voltage-controlled oscillator (VCO). The most relevant solutions derive from the differential-pair LC tank oscillator, which ensures a very high spectral purity for a given power consumption.

Besides improving the quality factor (Q) of the LC-tank, which is of fundamental importance but represents a technological rather than a circuital limitation, the class-C oscillator of Fig. 3.4.a is an attractive candidate for power reduction. In fact, as demonstrated in [17], class-C operation results (ideally) in a 36% lower bias current, compared to the commonly used class-B oscillator, for the same oscillation amplitude and phase noise. This is because the conversion of bias current into fundamental current harmonic is more efficient in class-C (with an ideal conversion factor αC equal to 2) than in class-B (ideal conversion factor $\alpha B = 4/\pi$). The class-C determines short and tall current pulses, which maximize the oscillation amplitude leading to a minimization of phase noise.

There are, however, issues that must be solved before a low-phase-noise class-C oscillator can be used efficiently. The primary concern is that the oscillator should indeed work in class-C, which entails that the drain-to-source voltage of M1/M2 should not drop below their overdrive voltage. This is accomplished with the shift of the dc bias voltage V_{bias} at the gate of M1/M2, which works very well in a low bias current scenario, where V_{bias} may be as low as the threshold voltage V_t of M1/M2 [17]. This, in turn, allows the oscillation amplitude to be a large fraction of the available supply voltage V_{dd}, before M1/M2 are pushed into the linear region. Thus, the oscillator figure of merit (FoM) may be extremely high, and at the same time the phase noise performance may be inadequate for cellular standards [17]. If we now decrease the LC-tank impedance and increase the bias current, in an attempt to achieve a much lower phase noise, we are forced to increase V_{bias} as well, with the adverse consequence of decreasing the maximum allowed oscillation amplitude.

It should be noted, however, that the value of V_{bias} needed to ensure startup is in this case much higher than its steady-state value [17], since the oscillation begins in class-A, but settles in class-C. This key observation was used in [35] to design a composite oscillator made of a class-C oscillator core with a very low V_{bias}, together with an additional transistor pair working much closer to class- B, whose task is to start up the class-C pair (Fig. 3.4.b). The approach in [35], itself targeting an ultra-low-voltage, high-phase-noise application, can be modified to achieve a low phase noise as well, by introducing suitable bias networks for the two transistor pairs (in fact, in the absence of an explicit current-limitation mechanism [35], current consumption is in practice checked only by the class-C transistors entering the linear region, defeating the goal of class-C operation itself).

Fig. 3.5 shows the schematic diagram of the proposed hybrid class-B/class-C

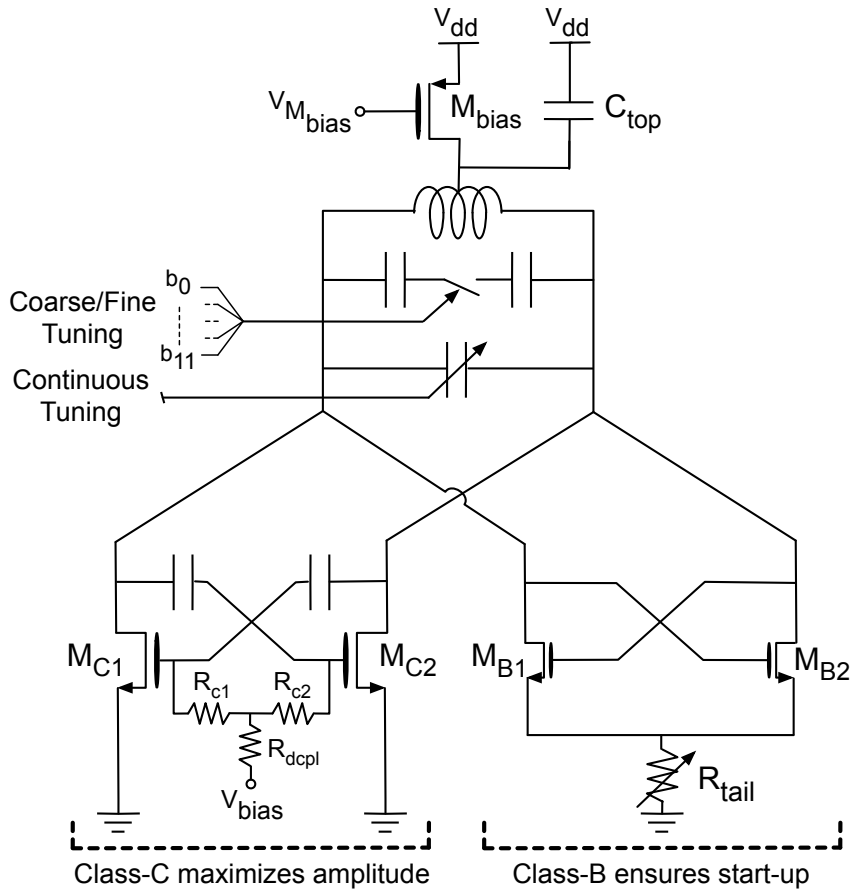

Figure 3.5: *Proposed hybrid class-B/class-C oscillator.*

oscillator. The bias current is injected into the LC tank by M_{bias}, while the amount of current drained by the class-B core (M_{B1}/M_{B2}) is set by the switchable resistance R_{tail}. The large capacitor C_{top} is instrumental for operating M_{C1}/M_{C2} in class-C, in the same fashion as C_{tail} in Fig 3.4.a. Since the role of M_{B1}/M_{B2} is primarily to ensure a reliable startup of M_{C1}/M_{C2} across PVT variation, only 20% of the (maximum) bias current is diverted into M_{B1}/M_{B2} and their sizes are less than the cross coupled pair biased in class C. At the same time, V_{bias} is allowed to be as low as the threshold voltage of M_{C1}/M_{C2}, i.e. approximately 500mV. It should be noted that the lack of source feedback pushes M_{C1}/M_{C2} slightly out of the saturation region when carrying the maximum current; however, the current waveforms are still effectively class-C for all operational current levels. Assuming conservatively that the class-C conversion factor αC is 1.8 (instead of 2), while αB stays at $4/\pi$, a 25% bias current reduction is achieved, compared to a purely class-B oscillator with identical performance. In fact, a lower bias current results in a more ideal design as well; furthermore, the impact of bias current noise is lower in the hybrid

oscillator, where most of it is filtered by C_{top} [17]. The phase noise expression for the hybrid oscillator in the 1/f2 region is found employing the theory in [17], and is given by:

$$L(\Delta\omega) = 10\log(\frac{\kappa_B T}{A^2 C^2 R(\Delta\omega)^2} \cdot (1+\gamma_n)) \tag{3.1}$$

where κ_B is the Boltzmann constant, T the absolute temperature, $\Delta\omega$ the angular offset frequency from the carrier, C and R the capacitance and the parallel resistance of the tank and A is the differential peak oscillation amplitude:

$$A = \frac{1}{2}(\alpha_C I_{bias,C} + \alpha_B I_{bias,B})R \tag{3.2}$$

$I_{bias,C}$ ($I_{bias,B}$) is the bias current in class-C (class-B) transistor pair.

As already mentioned, an important difference between the oscillator of Fig 3.4.a and the proposed one is that M_{C1}/M_{C2} in Fig. 3.5 lack source feedback. As a consequence, in the absence of R_{dcpl}, the low-frequency noise from R_{C1}/R_{C2} finds a straightforward path to the tank, where it is converted into phase noise by unavoidable AM-to-PM conversion mechanisms. A 5MΩ R_{dcpl} pushes such noise at low (offset) frequencies, where it is easily removed by the phase-locked loop where the VCO is going to work.

3.3 Dynamic Bias Schemes for Class-C VCOs

As presented in the previous Section, the class-C VCO (Fig. 3.4.a) offers the best phase noise performance compared to the same topology operating in class-B. In this oscillator, the increase in oscillation amplitude is not paid with a noise growth from the active devices, which operate always in the saturation region (or are turned off). The class-C operation is guaranteed by the bias voltage V_{bias}, set lower than the power supply voltage V_{dd} and by the presence of the capacitance C_{tail} that determines short and tall current pulses, which maximize the oscillation amplitude leading to a minimization of phase noise. Moreover, the capacitance C_{tail} naturally filters out the noise contribution from the current generator.

The main drawback of the class-C architecture is the limit set by the value of V_{bias} to the oscillation amplitude, since the switching pair must be kept working in the saturation region. Lowering V_{bias} allows a larger output voltage swing, but at the same time affects adversely the oscillator start-up [17]. Consequentially, the demand that the differential pair M1 and M2 should not work in the triode region throughout the oscillation period imposes a limit to the oscillator amplitude A_{osc} whose theoretical maximum value is [17]:

$$A_{osc} = \frac{V_{dd} - V_{bias} + V_{th}}{2} \tag{3.3}$$

where V_{th} is the threshold voltage of the transistor. For example, assuming V_{bias} approximately equal to V_{th}, the maximum achievable amplitude is only half of the

voltage supply. This condition limits implicitly also the current consumption, and with it the minimum achievable phase noise.

The need of a higher oscillation amplitude negates the improvement of current saving provided by the class-C solution, and thus the classical LC-tank oscillator is still generally preferred. In fact, when the core transistors operates in class-B the maximum value of the oscillation amplitude $A_{tank} < V_{dd}V_{sat}$ depends only on the power supply ($V_{dd]}$) and the saturation voltage (V_{sat}) of the tail current source. Under this condition, the classical architecture allows a maximum amplitude almost twice as large as the class-C oscillator, with a fixed V_{bias} set close to the V_{th}.

To improve the oscillator swing, it is necessary to reduce the bias voltage V_{bias}. In [39], V_{bias} was set slightly lower than V_{th}, since the sub-threshold transconductance of the switching pair was large enough to satisfy the start-up condition. However, even assuming a good sub-threshold conductance, such a low V_{bias} may force the current generator to work in the triode region, impairing once again the oscillator start-up. A possible solution is to remove the current generator altogether [35] (Fig. 3.4.b) . This leads to a reduction of the voltage at the two gates of the differential-pair. Nevertheless, this approach would require in practice a constant oscillation amplitude that has to be controlled acting on the total current consumption.

A more reliable solution is to adapt the bias voltage to the output amplitude as in [40], where an architecture is proposed that uses an amplitude detector followed by a comparator, which selects between the start-up voltage that ensures start-up, and the operative voltage that allow the best performance. Anyway, the hard switch between the two voltages determinates a transient that potentially can cause the oscillation to stop [40]. To avoid this problem, a low-pass filter smoothes the variation of the gate voltage of the differential pair, but simultaneously increases the settling time of the oscillator. Moreover, the amplitude detector loads the resonant load, lowering the quality factor of the tank [40].

To break the trade off between start-up issue and output amplitude, two different dynamic bias schemes were investigated . Both solutions use a negative feedback to set dynamically the proper bias voltage at the gates of the switching pair. In particular, at start-up the loop guarantees a V_{bias} high enough to guarantee oscillation build-up, while during the operative condition V_{bias} is lowered to the minimum value that allows the current generator to deliver the current required to sustain the oscillation. In this way, the output swing can be increase with the respect to a static bias obtaining a phase noise improvement sufficient to satisfy also the strictest mobile communication standards like GSM.

3.3.1 Class-C dynamic bias with current tail generator

Fig. 3.6 shows the simplified proposed architecture of the feedback VCO derived from the conventional class-C oscillator. M_{tail} sets the bias current sustaining the oscillation. The negative feedback loop senses the voltage V_{CM} at the common source of M1 and M2 and controls the voltage at their gates, keeping at the same

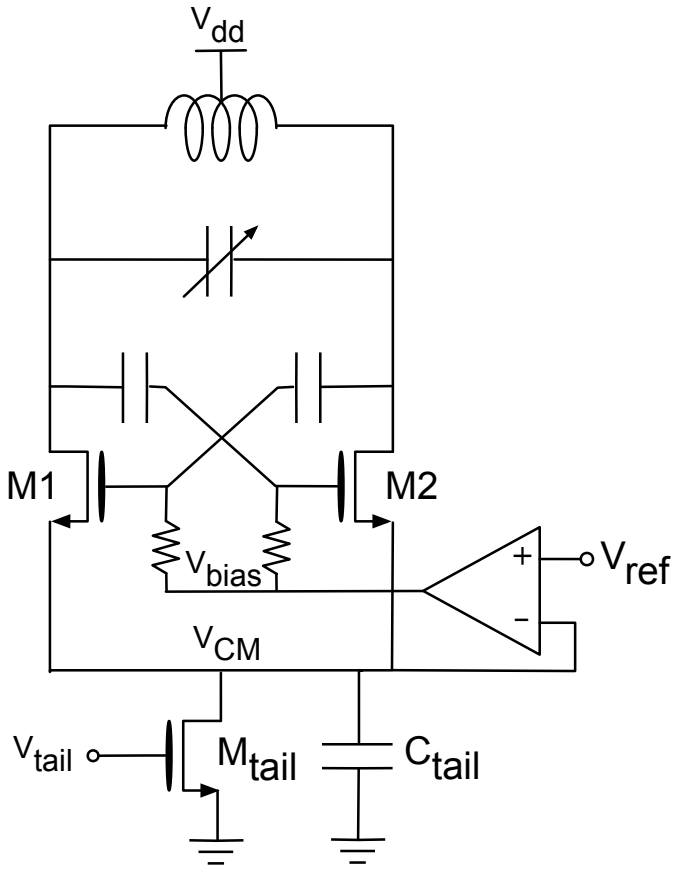

Figure 3.6: *Schematic of the proposed class-C VCO with current generator*

time the current generator in the saturation region. The loop forces the drain voltage of transistor M_{tail} to become almost the same as V_{ref}, which is chosen somewhat greater than the saturation voltage ($V_{d,sat}$) of M_{tail}. Typically, this value is between 100-150mV, depending on the size of M_{tail} and the current it must deliver.

Fig. 3.7 plots the relevant transient voltage waveforms for this oscillator. At the initial state, the drain voltage of M1 and M2 is at V_{dd} and the output of the operational amplifier is high enough to allow the switching pair to carry the total current delivered by M_{tail}, ensuring an easy start-up. With the increasing of the oscillator amplitude, the common-mode voltage at the sources of M1 and M2 rises rapidly, due to the rectifying action of the tail capacitor. The feedback compensates this effect reducing the voltage V_{bias} biasing the differential-pair to work deeper and deeper in class-C. At the end of the transient, the loop ensures the minimum voltage at the gates of M1 and M2 that allows the current generator to deliver the required current. The oscillation amplitude is therefore maximized. Simulation results indicate an oscillation amplitude (peak, single-ended) of 790mV.

The setting time and the error between reference V_{ref} and gate voltage V_{CM}

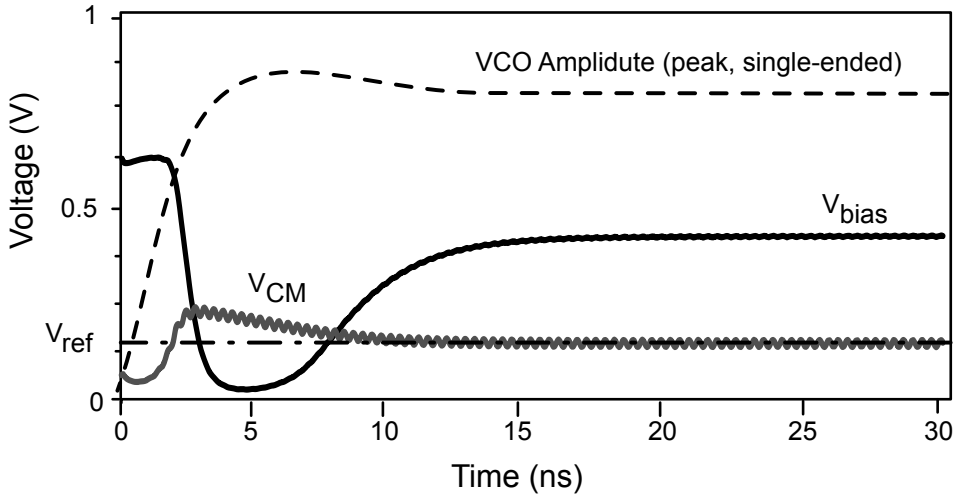

Figure 3.7: *Schematic of the proposed class-C VCO with current generator*

depend respectively on the bandwidth and the DC gain of the operational amplifier (op-amp). The op-amp adopted in the simulation of Fig. 3.7 has the dominant pole at 25MHz and a DC gain of 20. The resulting settling time is about 25ns, which satisfy the requirement of any communication standards. Moreover, the gain guarantees the correct $V_{[}d,sat$ value with an accuracy of some tens of mV, which is sufficient not to affect the performance of the current generator.

3.3.2 Class-C dynamic biasing with resistive tail

The architecture presented in 3.6 requires a bias current generator to work properly. Capacitor C_{tail} filters out the noise added by $M_{[}tail$ only at high frequency offset from the carrier, while flicker noise is totally up-converted. Moreover, the reference voltage V_{ref} is only an estimation of the saturation voltage required by the current generator.

Fig. 3.8 shows another architecture overcoming these limits. The resistance Rtail replaces Mtail, and the bias current is controlled by setting the voltage across such resistor. In particular, Ibias determinates Vref, which the op-amp copies at the sources of the switching pair as VCM. The ratio N between the two resistances sets the current in the oscillator core. In this architecture, VCM can assume a lower value than VCM in Fig. 2. Consequently, the operational amplifier lowers further Vbias, increasing the output swing and improving the phase noise. On the other hand, the op-amp needs a larger bandwidth and a higher gain to compensate the fluctuations at the VCM node, which could change the bias current of the oscillator. However, simulations show that a DC gain of 30dB and a bandwidth of 50MHz are sufficient to ensure the correct operation of the VCO, limiting also the noise introduced by the operational amplifier.

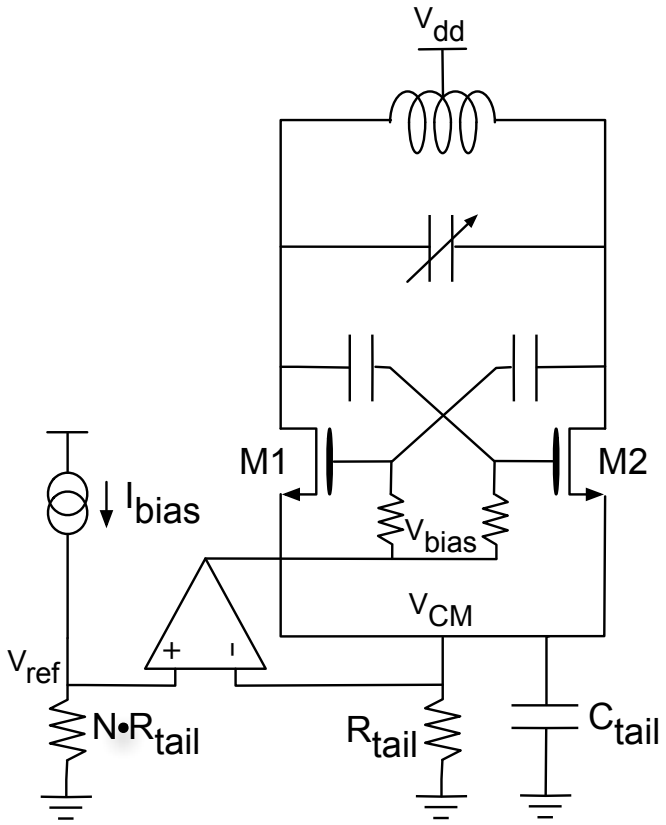

Figure 3.8: *Schematic of the proposed class-C VCO with tail resistor*

3.3.3 Simulation results

The architectures of Fig. 3.6 and Fig. 3.8 have been simulated in a standard 65nm CMOS technology. Simulations were run in Spectre RF using PSS, PAC, SP and PNOISE analysis.

For comparison purposes, the two oscillators have the same resonant load with center frequency equal to 7.2GHz. The tank is realized using a differential inductance of 250pH with a simulated quality factor of 17 at 7.2GHz. Two different banks of switched capacitors allow a discrete frequency tuning of 2.5GHz (33%), with an average frequency resolution of 1.4MHz.

The continuous frequency tuning is performed by an AMOS varactor having a tuning range of 15MHz.

Fig. 3.9 shows the simulated phase noise of both VCOs. To reach the phase noise performance required by the GSM standard (i.e. -109dBc at 400kHz), the bias current was set to 11mA and the voltage supply to 1.2V. The oscillations amplitude (peak, differential) was 1.4V. The phase noise for the current-generator VCO and the resistive-tail VCO at 1MHz from the 7.2GHz carrier is -125.85dBc/Hz and -126.45dBc/Hz respectively.

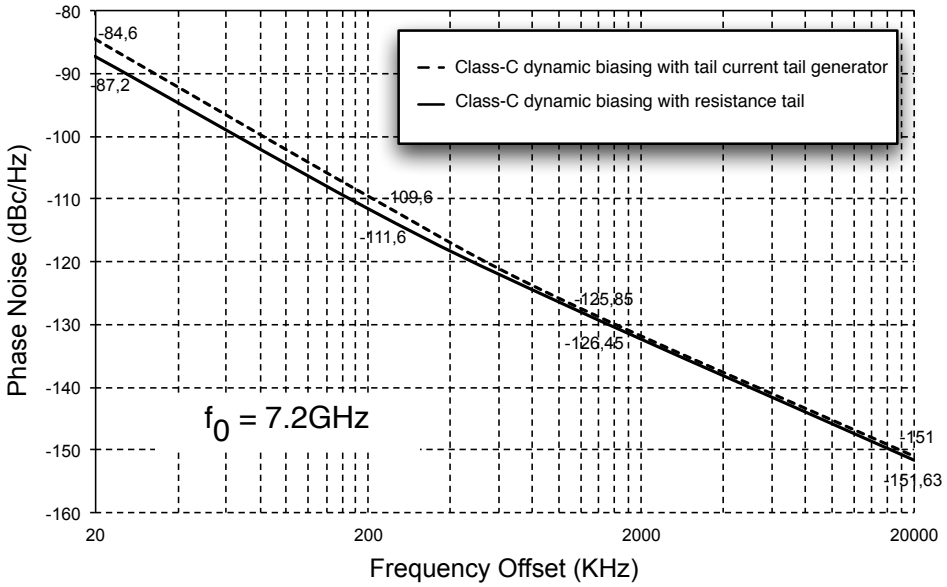

Figure 3.9: *Schematic of the proposed class-C VCO with tail resistor*

Considering the total power consumption of 12mW, the VCO figure-of-merit (FoM) of both oscillators is equal to -191dBc/Hz.

Chapter 4

Prototypes

The research activity presented in this dissertation has produced some different prototypes: a DCO which allowed to verify the principle of the capacitive degeneration; the dither-less All Digital PLL which adopted the DCO to satisfy the out-of-band phase noise performance thanks to its fine frequency resolution; a power scalable DCO for multi-standard application that has a high reconfigurability in term of power consumption and phase noise; finally a hybrid class-C/class-B oscillator which exploits the class-C principle overcoming the limitation described in [17] and presented in the previous chapter.

The first DCO prototype was mainly designed and characterized by the author, in collaboration with Antonio Liscidini and Rinaldo Castello (both from the University of Pavia). The measurements results were presented at the *2010 IEEE International Solid-State Circuits Conference* ([20]) and published on I*EEE Journal of Solid-State Circuits ([16])*.

The ADPLL prototype was designed in collaboration with the Italian design center of Marvell. As already described in chapter 2, the ADPLL design involved more people both form the University of Pavia and from Marvell. The team was mainly formed by Luca Vercesi, the author, Antonio Liscidini (University of Pavia) and Fernando De Bernardinis (Marvell) under the supervision of Francesco Rezzi (Marvell) and Rinaldo Castello (University of Pavia). The measurements results were presented to the 2011 IEEE Custom Integrated Circuits Conference ([38]).

The multi-standard, power scalable DCO and the Hybrid Class-C/Class-B prototypes were designed and characterized by the author in collaboration with Piero Andreani (University of Lund, Sweden), Antonio Liscidini and Rinaldo Castello (both from the University of Pavia). The measurements results of both oscillators will be presented at the *IEEE International Solid-State Circuits Conference* next February.

In this chapter the prototypes are presented and measurements results are discussed in comparison with the state of the art. At the end this is a table that summaries the performance of all VCO and DCO prototypes.

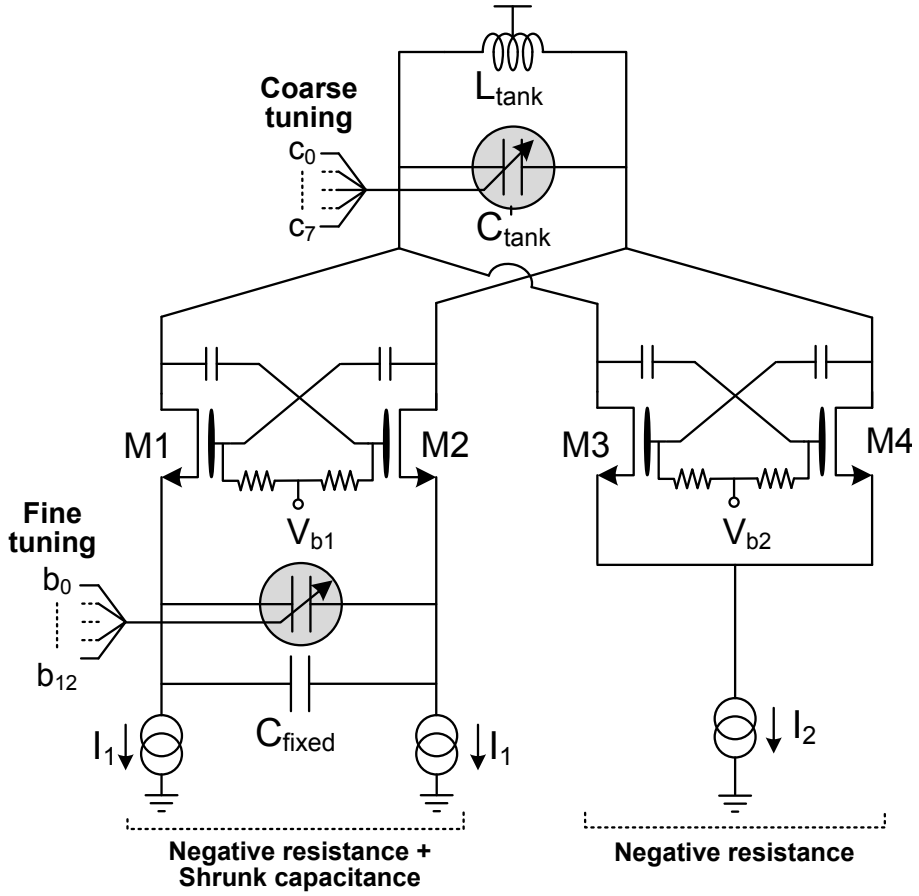

Figure 4.1: *DCO prorotype scheme.*

4.1 DCO Prototype

In chapter 1, the *Capacitive Degeneration* principle was introduced and discussed. To validate the presented theory, a DCO based on the current calibration (scheme in Fig. 4.1) and class-C operation was realized with an 8 bits coarse array and a 13 bits fine array. The DCO prototype was fabricated in a 65nm CMOS process using only standard devices provided by the technology. It has been tailored to GSM application, with a center frequency of 3.6GHz in order to provide the quadrature signals at 1.8GHz through a frequency divider that is not integrated in the chip.

The tank was realized using a differential inductor of 500pH with a simulated quality factor of 18 at 3.6GHz. For the coarse tuning bank a switch Metal-Oxide-Metal (MoM) capacitor matrix was implemented. The 3 LSBs of this bank were substituted by a varactor in order to close the DCO in an analog PLL, soldered on a PCB, during some testing phases. This was necessary since the prototype was not

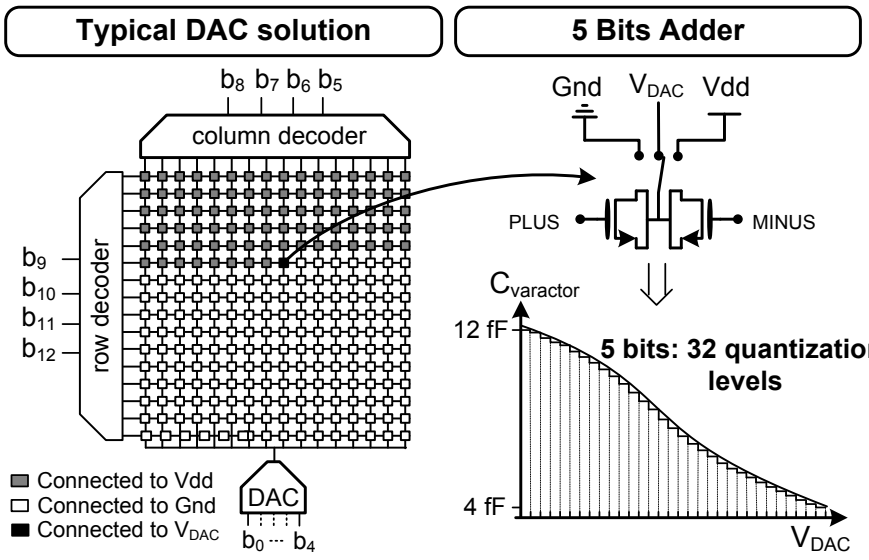

Figure 4.2: *Fine-tuning bank.*

inserted in any ADPLL. However the capacitive load required by the fully-digital implementation was preserved.

The two pairs of cross-coupled transistor were both biased to operate in class-C. The voltage reference connected to the gates was filtered both in the chip and on the board to avoid any additional noise injected by the bias.

The fine tuning bank was realized as reported in Fig. 4.2. Its unitary elements are nMOS varactors with a capacitance that varies from a minimum of 4fF to a maximum of 12fF. The 8 most significant bits (MSB) were used to control the matrix of 16x16 varactors. All elements except one are connected either to the voltage supply (V_{dd}) or to ground generating a thermometric filling of the matrix (gray and white units). The remaining varactor (black element in Fig. 4.2) is connected to the output of a 5-bits digital-to-analog converter (DAC) which provides additional 32-voltage levels between V_{dd} and ground. Since only one varactor is biased in the point of its characteristic with a high voltage-to-frequency gain, the sensitivity of the oscillator to noise and spurious signals is minimized. Although the quantization of the varactor characteristic is not strictly required to reach the target fine frequency resolution, this approach was adopted to simplify the routing of the matrix.

Finally, the oscillator signal is carried out the chip through a open-drain buffer, designed to minimize the capacitive load at the output of the DCO avoiding to affect the output frequency and coarse tuning range.

The design of the prototype was performed with a full custom approach both to the oscillator core and the digital elements like the DAC and the logic which controls all bits.

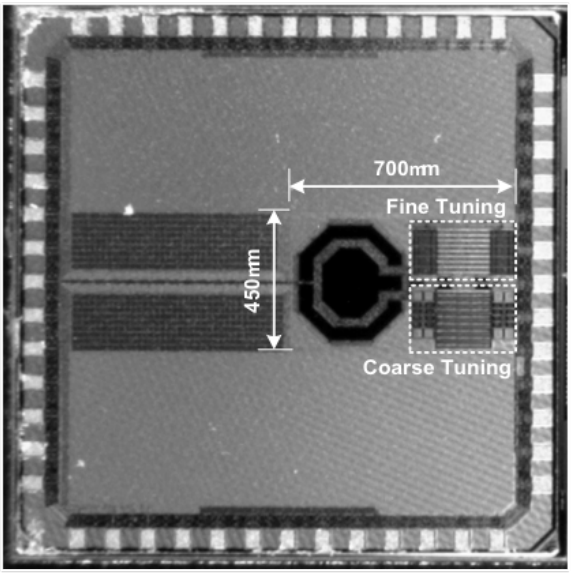

Figure 4.3: *Chip Photograph of the DCO.*

The obtained chip is depicted in Fig 4.3, where it is also possible to distinguish the different building blocks. The DCO occupies an area of $0.32mm^2$, dominated by the inductor and the two capacitors banks. The shrinking factor is underline noting that the coarse tuning bank sizes equal to the fine one although they realize

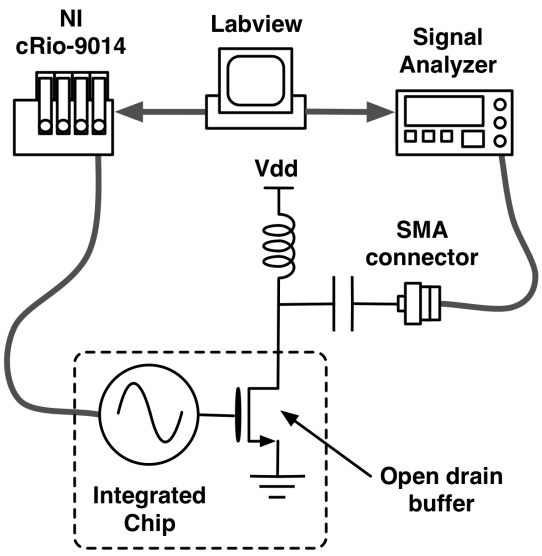

Figure 4.4: *Environment setup*

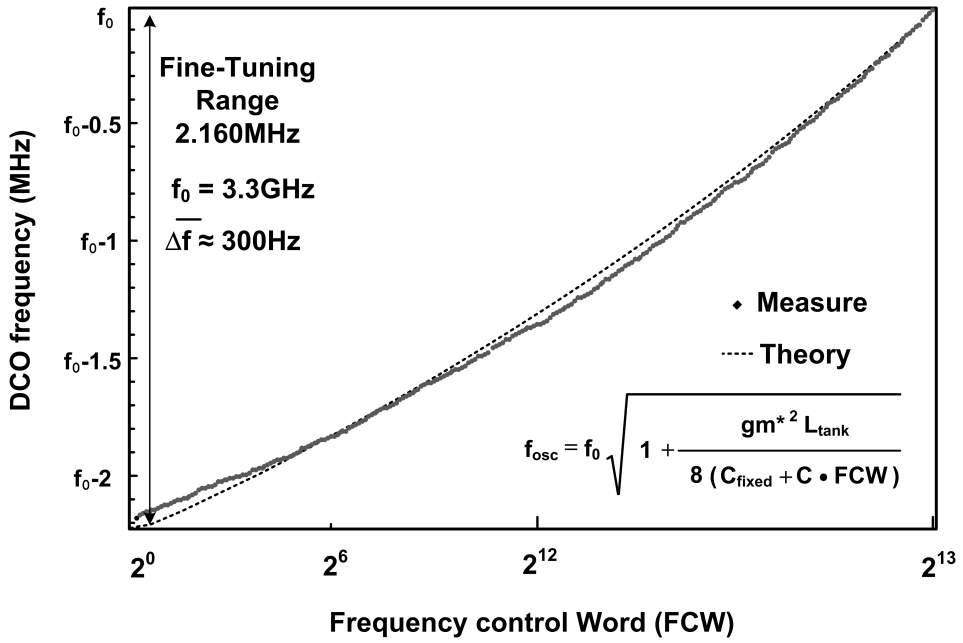

Figure 4.5: *Fine-Tuning characteristic*

a different tuning range (780MHz for the coarse bank and below 10MHz for the fine bank).

The die was tested using a dedicated RF board. The figure 4.4 shows the environment setup used to test the DCO. All measurements were performed using the software LabVIEW, a very flexible tool used both to drive the DCO through a real-time controller NI cRio-9014, and to process the data provided by the measuring instruments, in particular the spectrum analyzer. The delivered power to the signal analyzer was around -6dBm.

The oscillator has a voltage supply of 1.8V and, with a total current consumption which varie between 16mA and 20mA at the bounds of the coarse tuning range. The frequency can be tuned over a range of about 780MHz around 3GHz. It is lower than the simulated one due to a greater values of the integrated inductance and capacitances. The current is divided between the two cross coupled pairs and the ratio between the two currents I_1 and I_2 depends upon the desired shirking factor. In Fig. 4.5 the measured fine-tuning characteristic is reported, showing a very good agreement with the theory. The shrinking factor is around 200 with a fine-tuning range of 2.160MHz and an averaged resolution of 300Hz (minimum 150Hz). In this case the current drawn by the fine-tuning branch (I_1) is around $500\mu A$.

As stated in chapter 1, the current calibration obtained using the two switching pairs enables to act on the current I_1 leading an agile calibration of the fine-tuning resolution. In addition to this, the possibility to change the DCO resolution keeping constant the number of bits allows to re-use the same oscillator for different

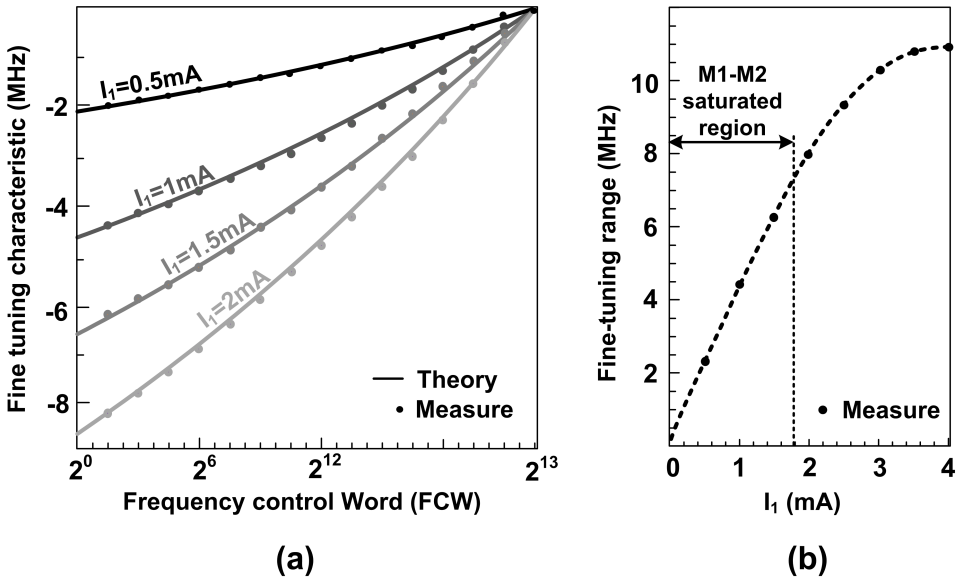

Figure 4.6: *Fine-Tuning characteristic versus* I_1

standards that required the same number of bits but different tuning range and frequency resolution (e.g. GSM and UMTS).
The DCO fine-tuning characteristics for different values of the bias current I_1 are reported in Fig. 4.6.a. The plots show a very good agreement with the theory also in this case. The tuning range varies from 2MHz to 12MHz with the frequency resolution that can be tuned from a minimum of 150Hz to a maximum of 800Hz. The plot in Fig. 4.6.b shows that the tuning range depends almost linearly on the bias current I_1 until 8MHz. This is due to the fact that the transistor transconductance gm in the saturated region is almost proportional to $\sqrt{I_1}$ and consequently the shirking factor grows linearly with I_1 (being Q_f proportional to gm^2). The tuning range versus frequency starts to becoming non linear for a current level that puts the auxiliary switching pair out of the saturation region during part of the oscillation period (no more class-C operation).

The DCO phase noise measured by a Rhode-Schwarz FSQ8 signal analyzer is reported in Fig. 4.7. Due to the relatively low quality factor of the tank, estimated to be around 10 due to parasitic resistance in the tank layout, the phase noise at 1MHz far away from the carrier is -127.5dBc/Hz at 3.3GHz (in line with the state of the art for GSM applications [10]). It was measured at the upper bound of the tuning range which typically represents the worst condition. Considering the total power consumption around 28.8mW, the DCO figure of merit (FoM) is equal to 183dBc/Hz.

All other measurements results compared with the state of the art are reported in Tab. 4.2. The DCO with the capacitive degeneration achieves the finest frequency resolution when no dithering is used. Furthermore the solution presented

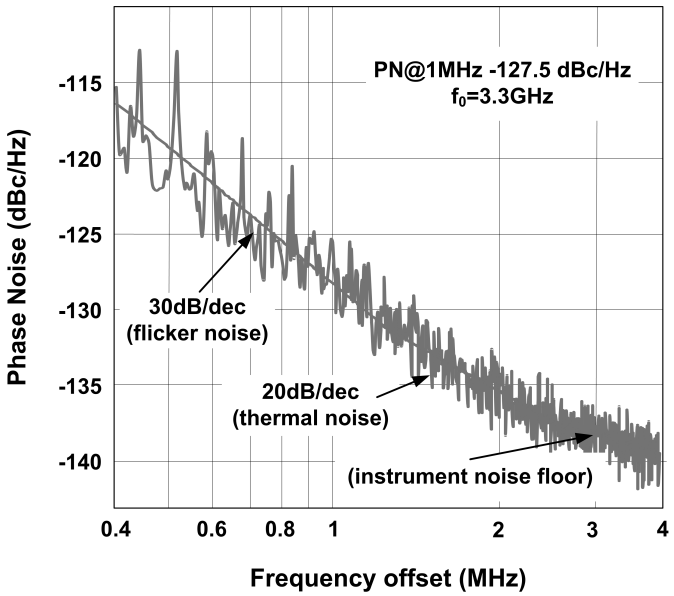

Figure 4.7: *Output phase-noise measure*

is the first one which allows re-configurability of the frequency resolution over a wide range. This property can be very attractive not only for an easy calibration of the DCO but also for the use in multistandard frequency synthesizer.

	this work	[9]	[10]	[11]	[12]	[13]
Center Freq. [GHz]	**3**	3.6	7.75	1.7	4	3.35
Tuning Range [MHz]	**780 (26%)**	900 (25%)	2800 (36%)	132 (8%)	1000 (25%)	600 (18%)
Fine Freq. Resol. [KHz]	**0.15-1.5**$^{(a)}$	12$^{(b)}$	0.8	150	200	5
Fine Freq. Range [MHz]	**2-12**$^{(a)}$	0.8	0.6	132	200	10
Voltage Supply [V]	**1.8**	1.4	1.2	0.5	2.5	1.2
Current Consump. [mA]	**16**	18	16	0.372	3.2	2
PN@1MHz [dBc/Hz]	**-127.5**	-126	-118	-109	-114	-118
FoM [dBc/Hz]	**183**	183	183	181	177	185
Techn. [CMOS]	**65nm**	90nm	65nm	130nm	130nm	90nm

(a) Tunable acting on I_1

(b) Without dithering

Table 4.1: *Summary results and comparison with the state of the art*

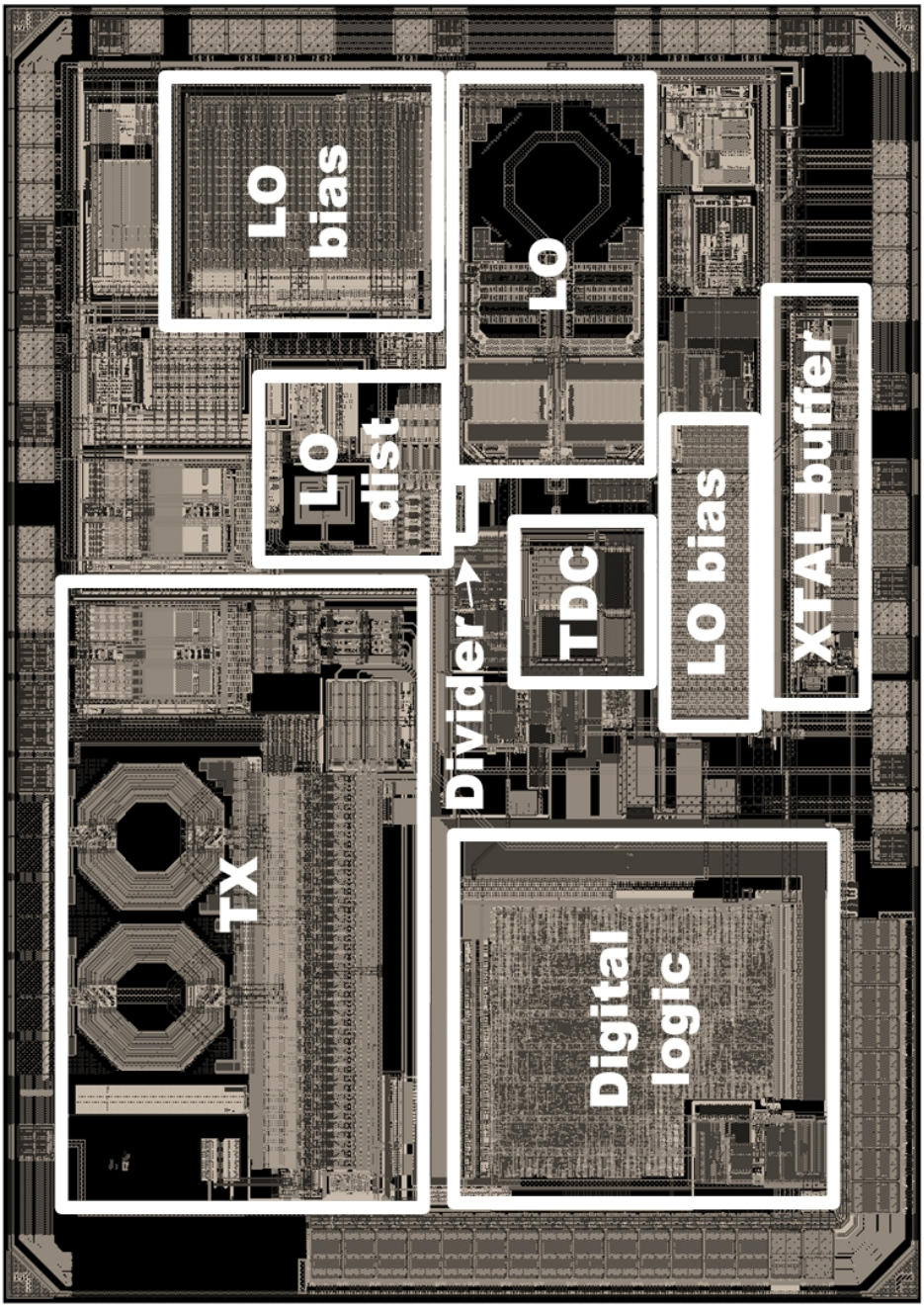

Figure 4.8: *ADPLL prototype layout snapshot*

4.2 ADPLL Prototype

The ADPLL prototype, fabricated in 55nm low power CMOS TSMC process was inserted in a complete transmitter for GSM application (Fig. 4.8). The 55nm

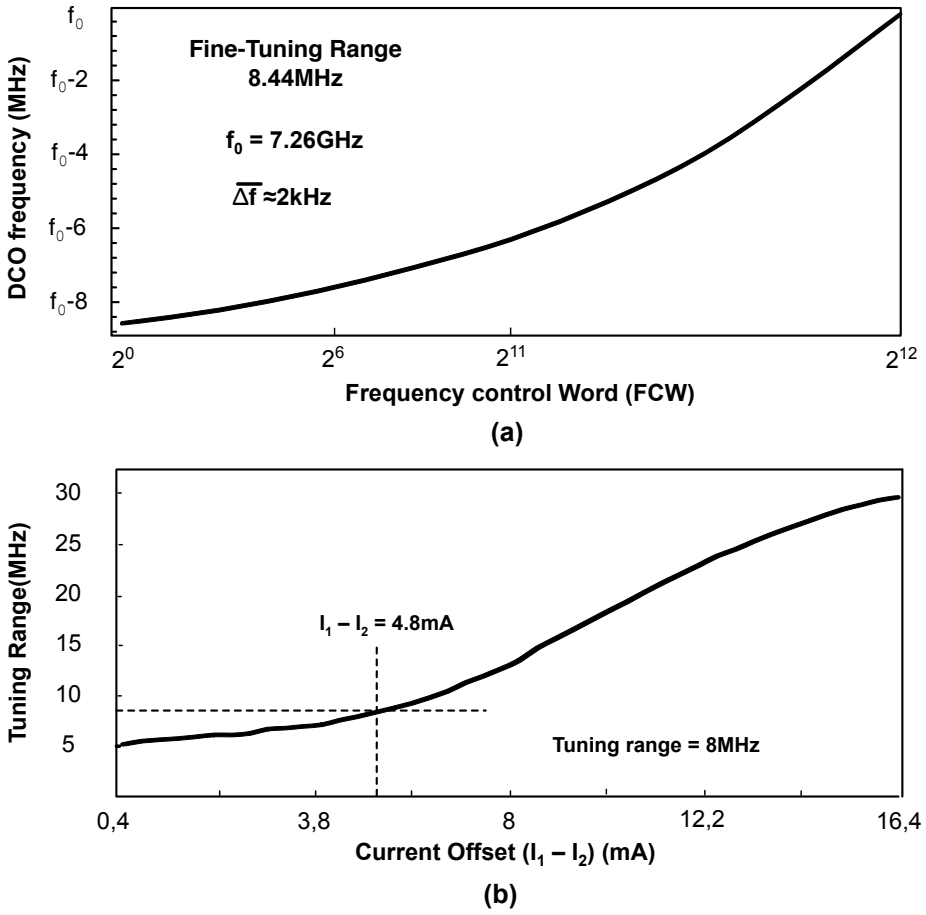

Figure 4.9: *DCO characteristics*

process is just a 10% optical shrink of the 65nm process used for the TDC prototype. The entire transmitter occupies an area of $3.5mm^2$ while the total active area reserved to the ADPLL is $0.7mm^2$. The output carrier frequency correspond to 1.8GHz/900MHz after a division by 4/8 of the DCO oscillation frequency. The use of a 7.2GHz DCO core was motivated at the system levels to minimize the pulling with other oscillators when integrated in a full transceiver, at the cost of increased power consumption for a given phase noise performance. The total power consumption of the frequency synthesizer is 41.6mW, where 32.5mW are consumed the DCO, 5.4mW by the dividers, 0.75mW by the TDC and 3mW by the digital processor.

4.2.1 DCO measurements

The frequency of the DCO can be change between 5.8GHz and 8.1GHz with a tuning range of 2.3GHz (33%). The tank is realized using a differential inductor of

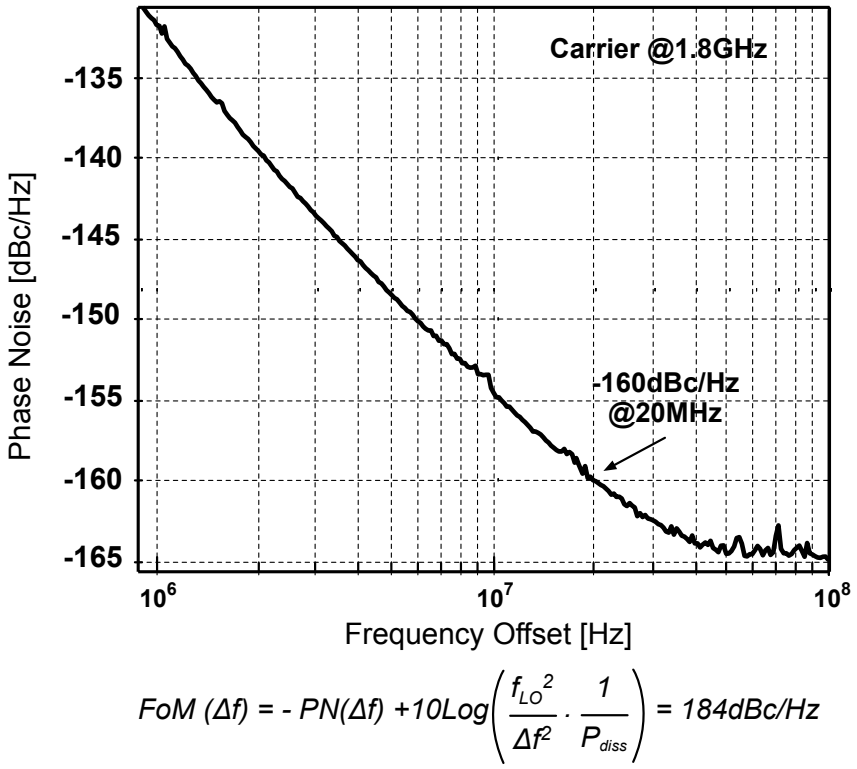

Figure 4.10: *Phase noise open loop DCO*

250pH with a simulated quality factor of 20 in the middle of the frequency characteristic and the coarse tuning is performed at the tank.
The ADPLL controls the fine-tuning bank of the capacitive degeneration architecture whose characteristics, at the center frequency (7.2GHz), is shown in Fig. 4.9.a. The current in the degenerated switching pair (i.e. $I_1 - I_2$) was set to have an average resolution of 2KHz with a tuning range of 8MHz (Fig. 4.9.a). This value made negligible the effect of the frequency discretization since the quantization noise laid more than 10dB below the intrinsic phase noise of the DCO. Acting on the current I_2 allows to calibrate the DCO tuning range that can be changed between 5MHz and 30MHz with the frequency resolution which varies between 1KHz and 6KHz as reported in Fig. 4.9.b. The capability to change the shrinking factor allows to reuse the same oscillator for different standards that may require the same number of bits but different tuning range and frequency resolution (e.g. GSM and UMTS).

The open-loop DCO phase noise measurement, reported in Fig. 4.10, was taken with an Agilent HPE5052B-M1 phase noise meter. With the current consumption of 21mA, the phase noise at 20MHz away from the carrier is -160dBc/Hz at 1.8 GHz that satisfies the specifics required by the GSM standard. The FoM of the DCO is 184dBc/Hz.

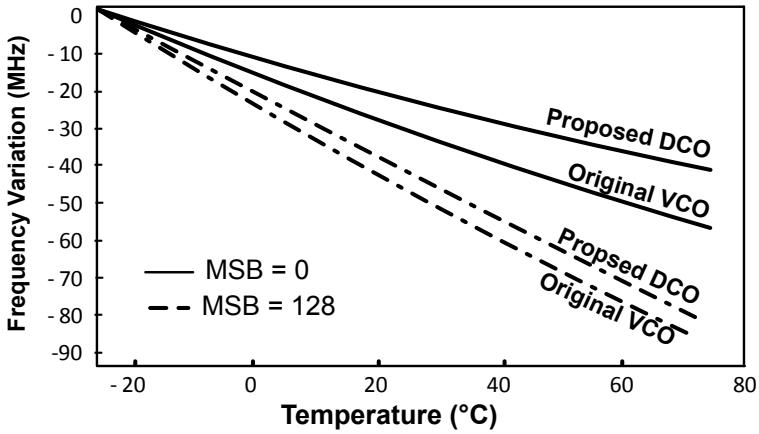

Figure 4.11: *DCO characteristics*

Finally, the Fig. 4.11 shows the comparison of the frequency drift due to the temperature between the previous VCO (where the capacitive degeneration was applied), from $-25°C$ to $75°C$. In particular, the plot reports the variations of the coarse-tuning range at the edges of the characteristic when the MSB are 0 (f_0 = 5.8GHz) and 127 (f_0 = 8.1GHz). Accordingly to the theory, the drift of the frequency grows whit the digital control word in both oscillators: at high frequency

	Results
Center Frequency	7.2GHz
Tuning Range	2.3GHz (33%)
Fine Frequency Resolution	1KHz-6KHz$^{(a)}$
Fine Frequency Range	5MHz-30MHz$^{(a)}$ (12 bits)
Voltage Supply	1.5 V (provided by integrated LDO)
Current Consumption	16mA-24mA
PN @ 1MHz	-131dBc/Hz$^{(b)}$
PN @ 20MHz	-160dBc/Hz$^{(b)}$
FoM	184dBc/Hz
Technology	CMOS 55nm

(a) Tunable acting on I_2

(b) At 1.8GHz

Table 4.2: *Summary results of the DCO*

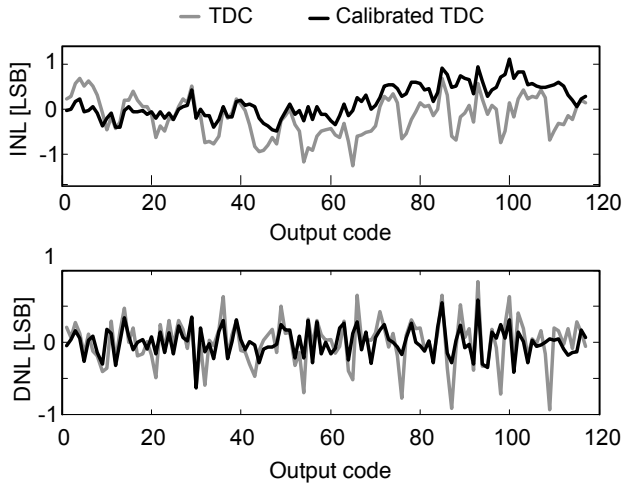

Figure 4.12: *Linearity measurements*

the capacitive load of the tank is mostly composed by the parasites of the switch whose temperature variation is more non linear than the classical capacitances. Anyway, the capacitive degeneration reduces the thermal drifts, especially at lower frequency where the reduction is 27% smaller than the classical oscillator. At the higher frequency the difference between the two architecture is less significant and the DCO drift is only 6% smaller than the VCO. These results confirms that the differences of the performances of the DCO and VCO are negligible and that the digital approach in the design of the oscillator does not introduce any drawback.

The 4.2 summaries the performance of the DCO.

4.2.2 ADPLL measurements

Before showing the measurements of the ADPLL, the Fig. 4.12 reports the linearity measurements of the TDC. Both DNL and INL are always less the one LSB, showing its good linear performance. Since the matrix of the 2-D Vernier is explored by diagonals, the INL is folded with a periodicy equal to the number of stages in line Y.

Fig. 4.13.a shows the phase noise spectrum of the ADPLL with a carrier at 1.8 GHz and a loop bandwidth of 800 kHz. The measurement was taken with an Agilent HPE5052B-M1 phase noise meter. In-baad phase noise is dominated by the TDC and the reference oscillator (which itself dominates for frequencies lower than 10 kHz) while the DCO has a negligible impact. The measured -108dBc/Hz in-band phase noise is only 2dB away from the theoretical quantization noise floor for the given TDC resolution of 5ps and a reference of 26MHz [32]. Since it was measured with a wide PLL bandwidth to better identify the in-band plateau, the slope of the out-band noise is greater than -20dBc/Hz. It doesn't represent the phase noise of the oscillator, but it shows the TDC noise filtered by the transfer

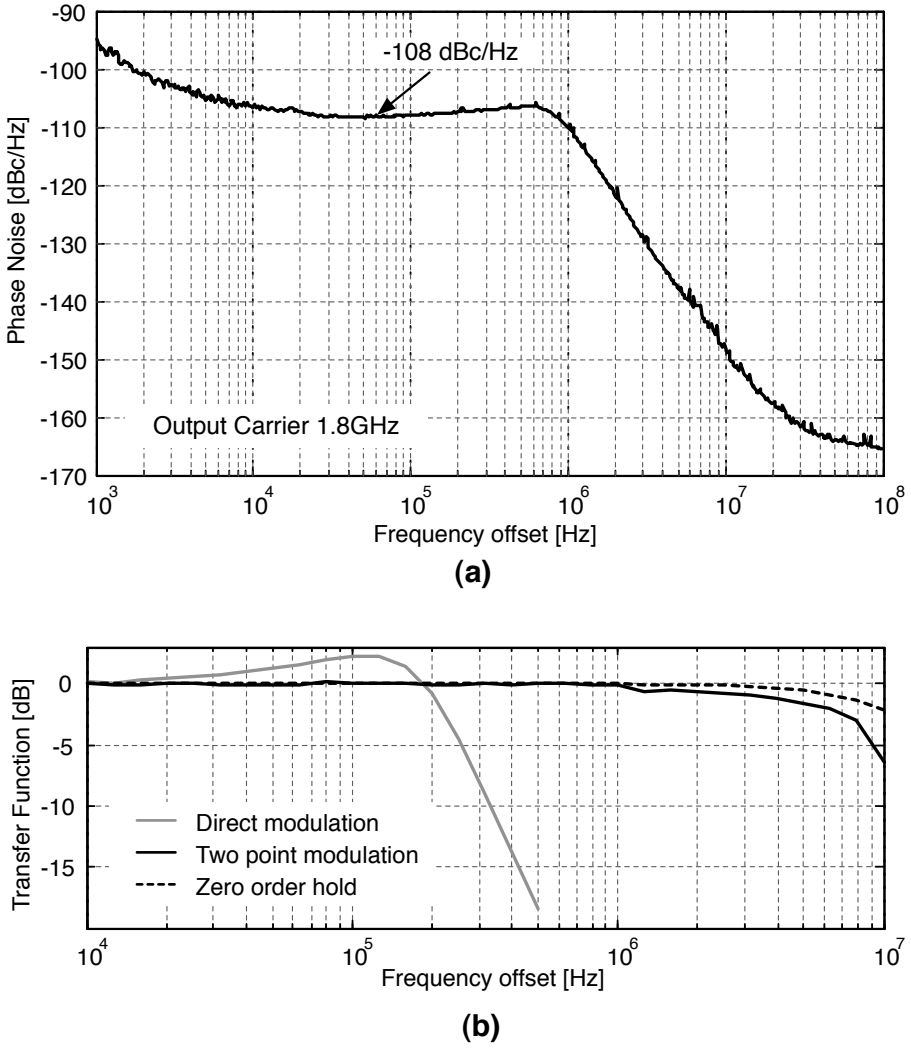

Figure 4.13: *(a) Phase noise and (b) PLL transfer function*

function of the loop filter.

In Fig. 4.13.b the ADPLL transfer functions with and without the two-points modulation are reported. When the two-points is activated, the modulation bandwidth is limited by the zero order hold transfer function due to the reference clock of 26MHz. This curve represents the ultimate limit to the two-point modulation bandwidth. The two-points modulation transfer function is remarkably flat also in the surroundings of the ADPLL bandwidth, where an inaccurate signal injection at the input of the DCO could produce a discontinuity in the signal transfer function.

Fractional spurs are an issue for all frequency synthesizers. The choice of a first order Sigma Delta modulator (without any dithering) that was taken to minimize the required TDC full-scale has the fractional spurs augment as its major drawback.

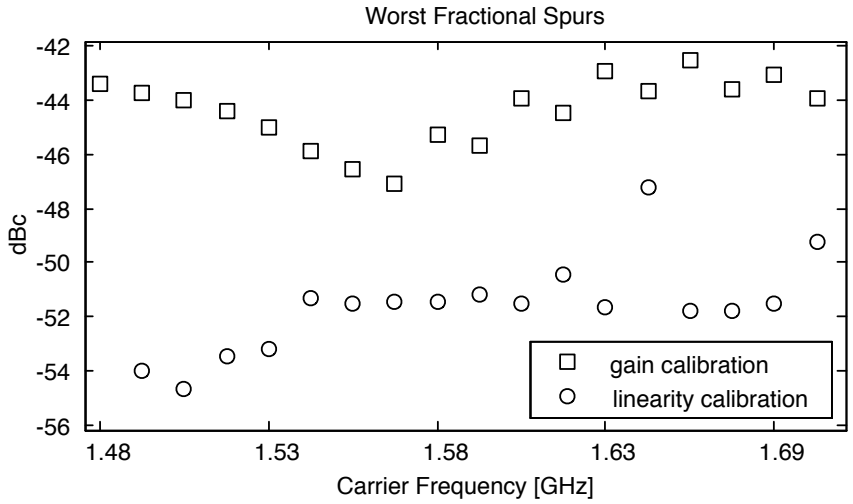

Figure 4.14: *Fractional spurs*

A spurs cancellation approach was used that rely on the TDC gain calibration. Since the fractional spurs are injected in the system at the TDC input they are processed by the low pass system transfer function. The fractional spurs were measured in band for different values of the carrier frequency. The measurement results are depicted in Fig. 4.14. The TDC gain calibration algorithm resulted in a -42dBc worst case spurs level while a worst case spur level of -50dBc was obtained after linearity calibration.

The main characteristics of the proposed ADPLL are summarized in Table 4.3. The out-of-band phase noise must be normalized to the output carrier frequency while the in-band noise also to the reference frequency [26]. Different implementation are compared using the following figure of merit (FOM) [25]:

$$FoM = 10\log\left(\frac{\sigma_T^2}{1s}\cdot\frac{P_{PLL}}{1mW}\right) \tag{4.1}$$

where σ_T is the RMS jitter and PPLL the total power consumption of the PLL. The proposed solution shows the best FoM together with [27]. Expression 4.1 assumes the same power consumption for the DCO and the rest of the PLL. In this condition the FoM reaches its minimum value. For the PLL reported the DCO consumes about 80% of the total power consumption to satisfy the stringent GSM out-of- band emission mask. This situation slightly penalizes the proposed solution with the respect to the one reported in [27].

	this work	[9]	[10]	[11]	[12]	[13]
Reference [MHz]	**26**	N/A	50	40	25	48
Carrier Freq. [GHz]	**1.8**	7	3.7	3.2	3.5	5.3
Tuning Range	**33%**	83%	N/A	32%	29%	34%
In-band Noise [dBc/Hz]	**-108**	-90	-108	-101	-101	-97
Out-of-band Noise [dBc/Hz]	**-160 @20MHz**	-144 @20MHz	-150 @20MHz	-121 @3MHz	-123 @3MHz	-114 @1MHz
Max PLL Bandwidth [MHz]	**3**	2	0.5	0.3	3.4	N/A
In-band spurs [dBc]	**-50**	N/A	-42	-42	-58	-45
RMS Jitter [fs][(a)]	**138**	255	120	426	N/A	303
Power Dissip. [mW]	**41.6**	30	39	4.5	9	20
FoM [dB]	**-241**	-237	242.4	-241	N/A	-237.5
Area [mm^2]	**0.7**	0.3	0.9	0.2	0.4	1.3
Techn. [CMOS]	**55nm**	40nm	130nm	65nm	65nm	65nm

(a) Estimated assuming optimal bandwidth for FoM

Table 4.3: *Summary results and comparison with the state of the art*

4.3 Power scalable n-pn DCO Prototype

In chapter 3, the Power scalable n-pn DCO architecture was introduced. To validate the the idea, a reconfigurable DCO has been integrated in a standard 55nm CMOS process using only standard devices provided by the technology. It has been tailored to GSM/WCDMA standards with a center frequency of 7.75GHz. The tank has been realized using a differential inductor of 250pH with a simulated quality factor of 15 at 7GHz.

Coarse tuning is the same for both n-only and p-n VCOs, and is performed at the resonant load using two capacitor banks with different resolutions, controlled by 7 and 6 bits respectively. The two banks are implemented with switch Metal-Oxide-Metal (MoM) capacitor matrices and they tune the frequency at the output of the divider-by-2 between 3.25GHz and 4.5GHz, with a frequency resolution of 700kHz.

The fine-tuning bank, placed between the sources of M1 and M2, is controlled by a 12bits digital word, whose 8 MSBs control a matrix of 16x16 nMOS varactors with a capacitance that varies from a minimum of 4fF to a maximum of 12fF, connecting them either to V_{dd} or ground, while the 4 LSBs control the output voltage

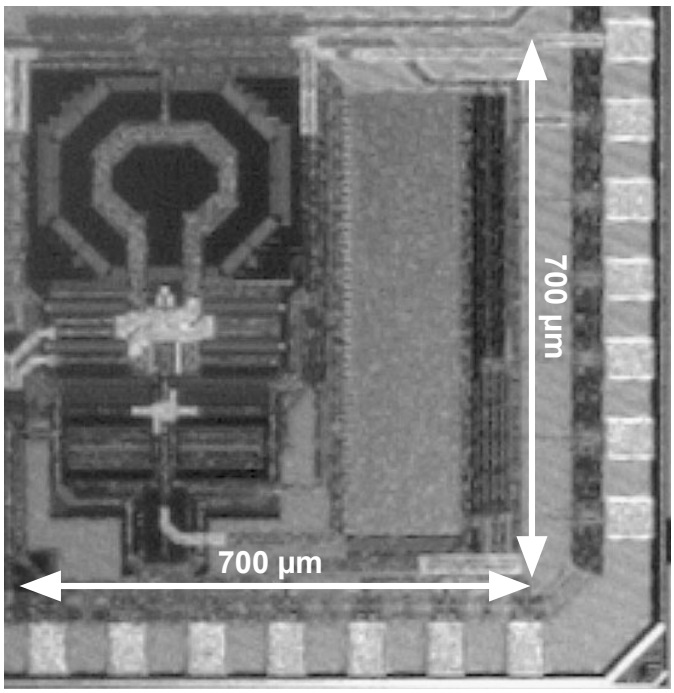

Figure 4.15: *Coarse-tuning characteristic*

of a DAC that acts on the control node of a varactor [16]. The capacitive calibration is controlled by 3 bits which change the capacitive load at the sources of the cross coupled pair between 0.1pF and 2.4pF.

Finally, the DCO is buffered with a integrated divider-by-2 that uses the topology proposed in [33], designed to minimize the capacitive load at the output of the DCO.

Also in this case, the design of the prototype was performed with a full custom approach both to the oscillator core and the digital elements like the DAC and the logic which controls all bits.

The obtained chip is depicted in Fig 4.15, where it is also possible to distinguish the different building blocks. The DCO occupies an area of $0.49mm^2$, dominated by the inductor, the two capacitors banks and the two current generators. The measurements were performed using LabVIEW exploiting its capability to drive and elaborate the data provided by the instruments. The delivered power to the signal analyzer was around -2dBm.

The Fig. 4.16.a shows the coarse tuning range, common for both n-only and p-n topologies. At the output of the divider-by-2, the DCO covers a tuning range of 1.25GHz eith a frequency resolution of 700kHz.

The Fig. 4.16.b and 4.16.c report the fine-tuning characteristics of the p-n and n-only DCOs for different values of the capacitance C_{cal}. The fine-tuning range can be programmed from 2.5MHz to 7.5MHz in p-n mode, with a frequency resolution

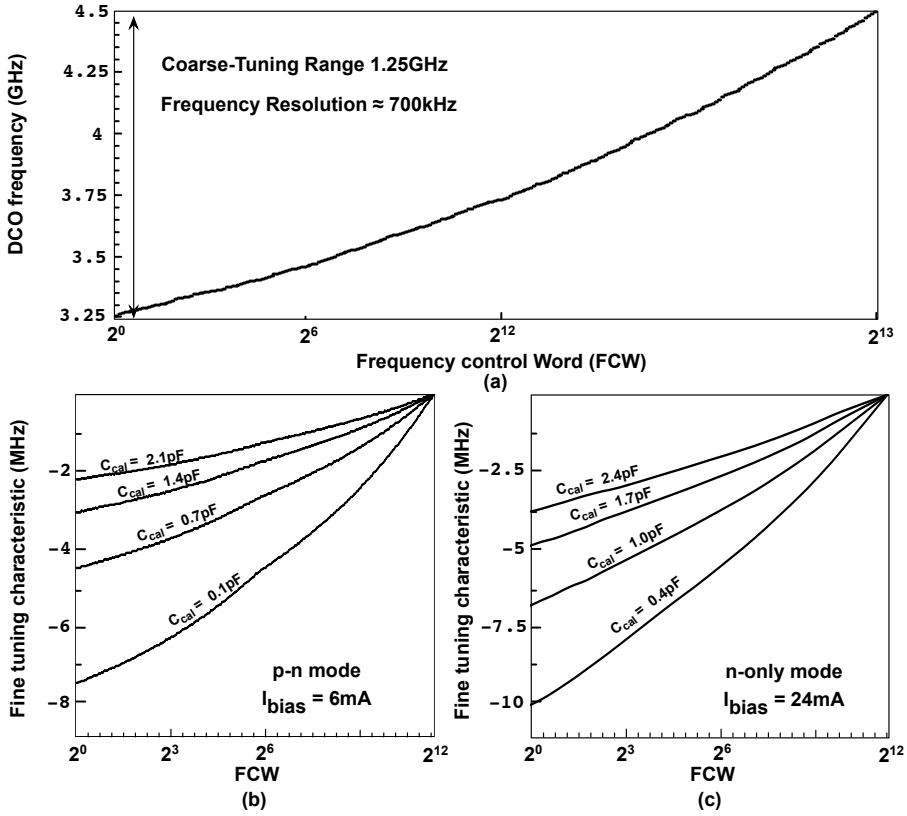

Figure 4.16: *(a) Coarse tuning characteristic. Fine tuning characteristics for p-n mode (b) and only-n mode (c)*

of 0.6-2kHz, and between 4MHz and 10MHz in n-only mode, with a resolution of 1-2.5kHz. It is lower in the p-n configuration due to the lower current that biases the oscillator. It reduces the transconductance of the switching pair, decreasing the maximum tuning range achievable by the capacitive degeneration architecture (equation 1.14).

The DCO phase noise at the output of the divider-by-2, measured with a phase noise meter, is reported in Fig. 4.17. In the middle of the tuning range (3.92GHz), the phase noise at 2MHz offset from the carrier is -129.3dBc/Hz for the p-n DCO and -134.7dBc/Hz for the n-only DCO, for a bias current of 6mA and 24mA respectively and V_{dd} equal to 1.5 V. The phase noise difference between the two DCOs is 5.4dB, very close to the theoretical value of 6dB. The p-n DCO achieves a FOM of 185.6Bc/Hz, only marginally better than the n-only DCO FOM of 185.0dBc/Hz. The higher current provided by the current generator increases its noise which marginally affects the phase noise performance of the n-only configuration.

The Fig. 4.18 shows the phase noise measurements at the minimum, center and maximum frequencies of the tuning range for both the configurations. At higher frequency, the phase noise worses due to the less capacitive load at the resonant

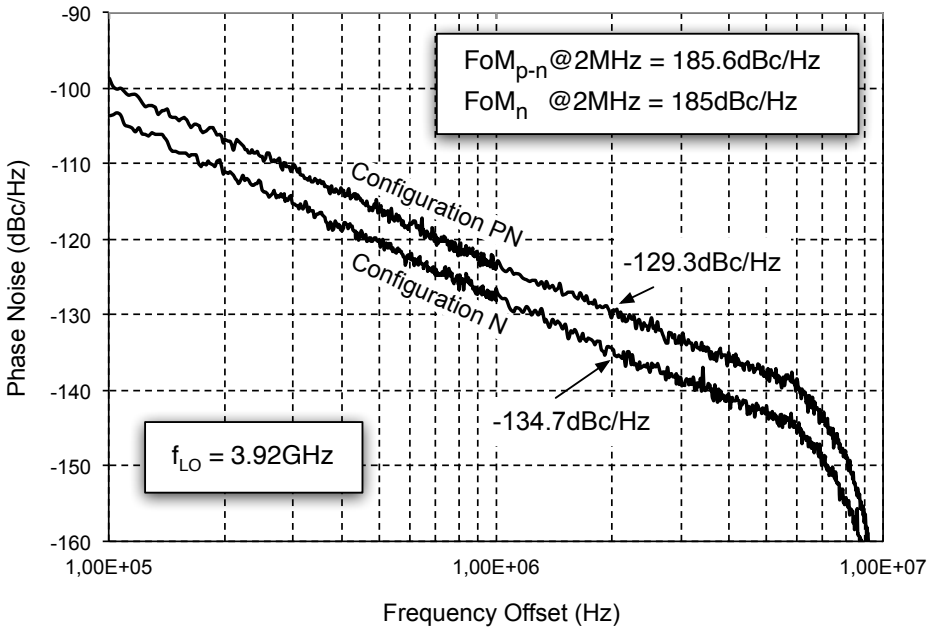

Figure 4.17: *Phase noise measurements of the two DCO configurations*

load, but the FoM, which considers also the power consumption, remains constant.

Finally, the Tab. 4.4 summaries the performance of the DCO.

	p-n mode	n-only mode
Center Frequency	7.75GHz	
Tuning Range	2.5GHz (33%)	
Coarse Frequency Resolution	1.4MHz	
Fine Tuning Range$^{(a)}$ (12 bits)	5MHz-15MHz	8MHz-20MHz
Fine Frequency Resolution$^{(a)}$	1.2KHz-4KHz	2KHz-5KHz
Voltage Supply	1.5 V	
Current Consumption	6mA	24mA
PN @ 2MHz$^{(b)}$	-129.3dBc/Hz	-134,7dBc/Hz
FoM$^{(b)}$	185.6dBc/Hz	185dBc/Hz
Technology	CMOS 55nm	

(a) Programmable by the capacitance C_{cal}

(b) After an on-chip divider by 2

Table 4.4: *Summary results of the DCO*

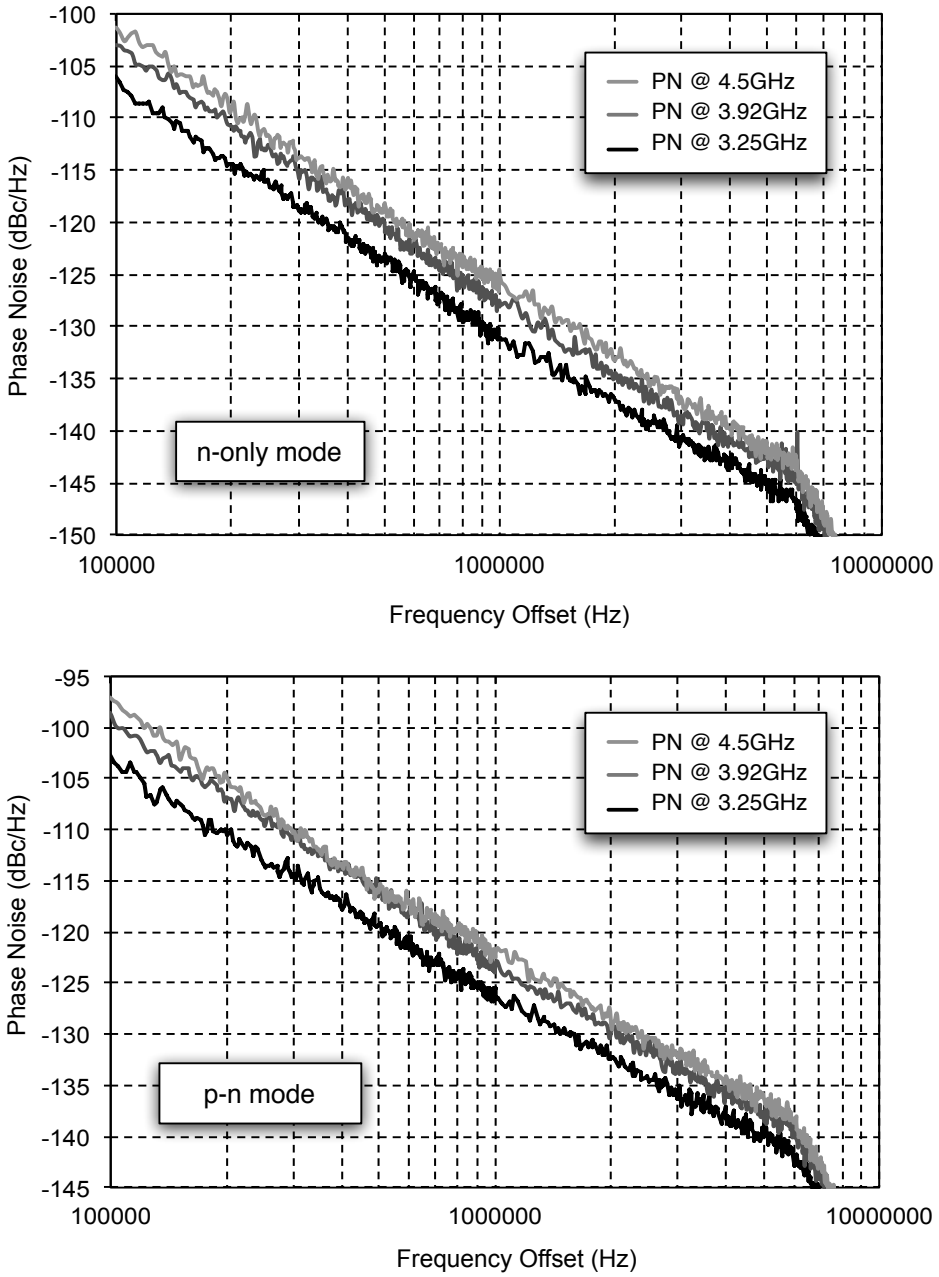

Figure 4.18: *Phase noise measurements of the two DCO configurations at the minimum, center and maximum frequencies.*

4.4 Hybrid Class-C/Class-B VCO Prototype

The Hybrid Class-C/Class-B VCO has been designed in a standard 55nm CMOS process and tested. The tank has been realized using a differential, single-turn in-

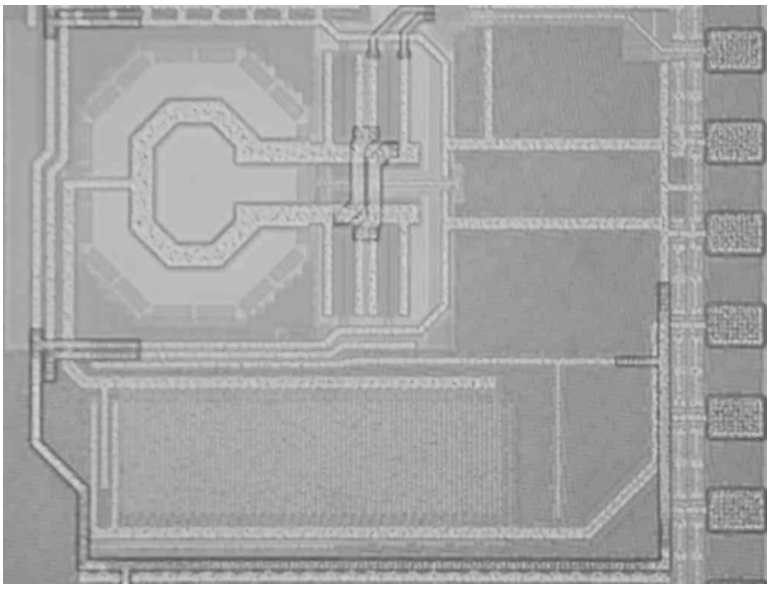

Figure 4.19: *Die photograph of the VCO*

ductor of 0.25nH with an estimated Q of 15 at 7GHz. Since M_{B1}/M_{B2} carry a small fraction of bias current, their width is only 1/8 of that of M_{C1}/M_{C2}, which minimizes the parasitic capacitances. All transistors are thick-oxide devices with a length of 200nm.

The VCO is tunable from 6.7GHz to 9.2GHz with a 7-bit course switch Metal-Oxide-Metal (MoM) capacitor bank, a 6-bit fine MOM capacitor bank, and an AMOS varactor for continuous tuning having an average range of 15MHz. After division by 4/8, all GSM bands and several WCDMA bands are covered. The value of V_{bias} at the gates of the class-C pair M_{C1}/M_{C2} was set to 500mV, and it was checked that increasing it to 600mV did not deteriorate appreciably the VCO performance. The voltage reference of the two gates was filtered both in the chip and on the board to avoid any additional noise injected by the bias. Finally, the VCO is buffered with a integrated divider-by-2 that uses the topology proposed in [33].

The Fig. 4.19 reports the die photograph of the VCO whose core dimensions are $700\mu m \cdot 700\mu m$, dominated by the inductor and the current generator.

All the measurements were performed using LabVIEW. Fig. 4.20 shows the phase noise plot at minimum, middle, and maximum frequency, for a power supply of 1.5V and a current consumption of 18mA, after on-chip frequency division by 2 (using the divider presented in [33]) to ease measurements. The notch at 10MHz offset is an artifact of the measurement system. The phase noise at 2MHz offset for the middle plot (with a carrier frequency of 3.95GHz) is -137dBc/Hz, which extrapolates to -157dBc/Hz at 20MHz offset, and to -169dBc/Hz after further frequency division by 4. This shows that the GSM/WCDMA phase noise

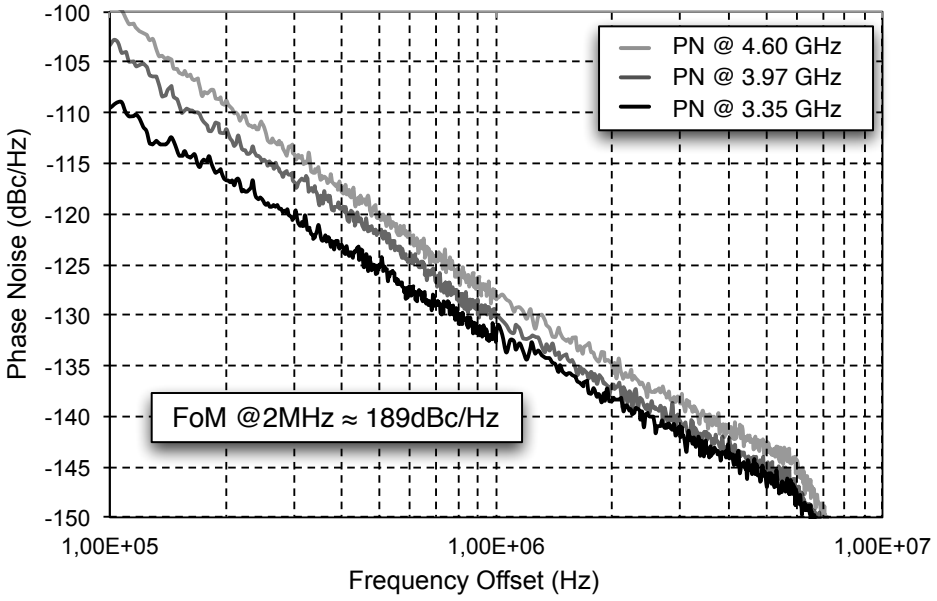

Figure 4.20: *Phase noise measurements at the minimum, middle, and maximum oscillation frequency*

specifications mentioned in the introduction are met with margin. The $1/f^3$ noise corner varies between 100kHz and 300kHz.

The phase noise performance worses at higher frequency, but the FoM of the VCO does not change. In fact, Fig. 4.21 displays the phase noise at 400kHz/2MHz

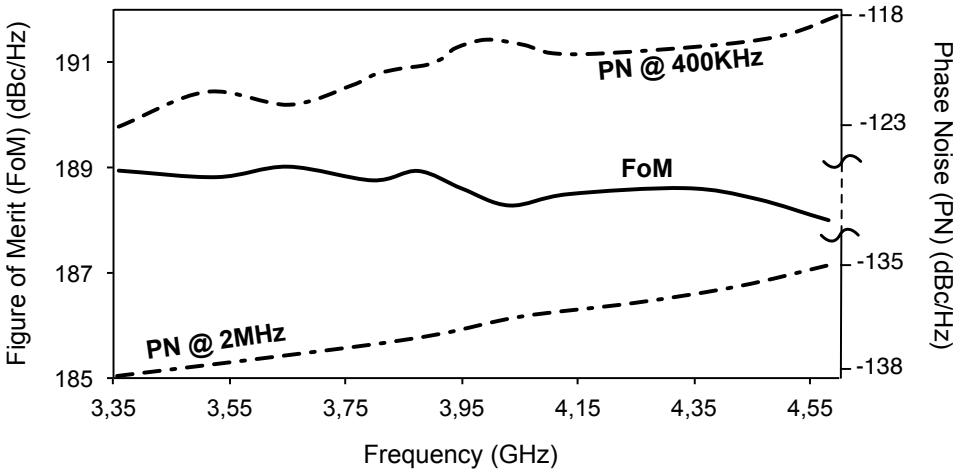

Figure 4.21: *Phase noise measurements at the minimum, middle, and maximum oscillation frequency*

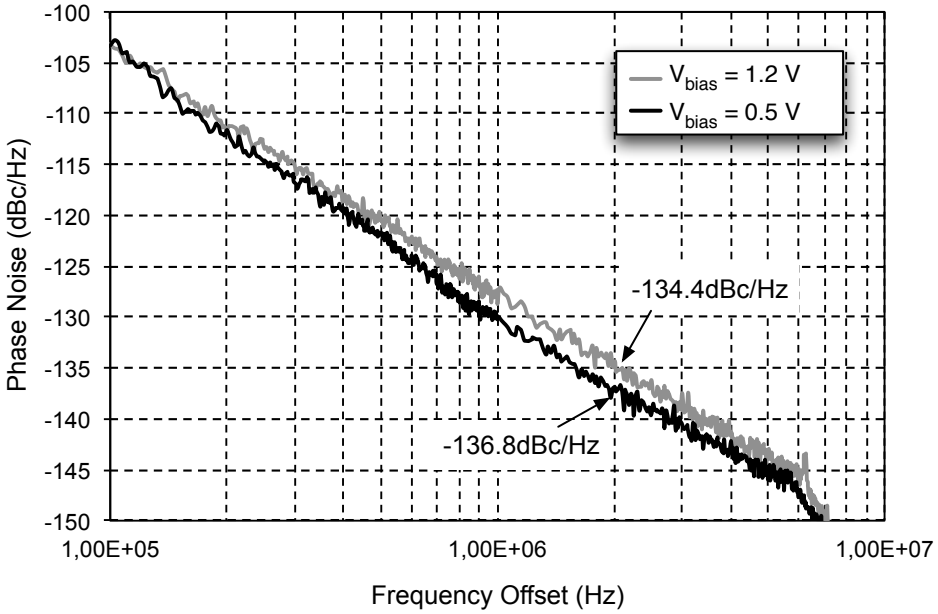

Figure 4.22: *Phase noise measurements at mid-band, for V_{bias} = 1.2V (M_{C1}/M_{C2} operating in class-B), and V_{bias} = 0.5V (M_{C1}/M_{C2} operating in class-C), keeping a constant power consumption*

offset and figure-of-merit (FoM) vs. oscillation frequency (divided by 2). The maximum FoM is above 189dBc/Hz, and varies approximately 1dB across the tuning range. This is comparable to the FoM of the VCO in [34], which was designed in an RF CMOS process.

Fig. 4.22 shows a phase noise plot when M_{C1}/M_{C2} operate in class-B, obtained by raising V_{bias} to 1.2V. The penalty compared to class-C operation is slightly higher than 2dB at 2MHz. From another point of view, the Fig. 4.23 reports the phase noise plotted at mid-band, for V_{bias} = 1.2V M_{C1}/M_{C2} operating in class-B), and V_{bias} = 0.5V (M_{C1}/M_{C2} operating in class-C), with class-B bias current increased by 25% to obtain the same phase noise in both cases. This confirms the more efficiency achieved biasing he switching pair M_{C1}/M_{C2} in the class-C.

The phase noise measurements for different value of the current I_{bias} are reported in Fig. 4.24. It improves as the current increases, but with a current consumption of 8mA, the VCO would be able to satisfy the requirements of the GSM standards. In fact, the extrapolated phase noise at 20MHz offset, after further frequency division by 4 is -163.8dBc/Hz, with a margin of 2dB respected to the GSM specs.

Finally, the Tab. 4.5 summaries the performance and compares the Hybrid Class-C/Class-B VCO with the state of the art.

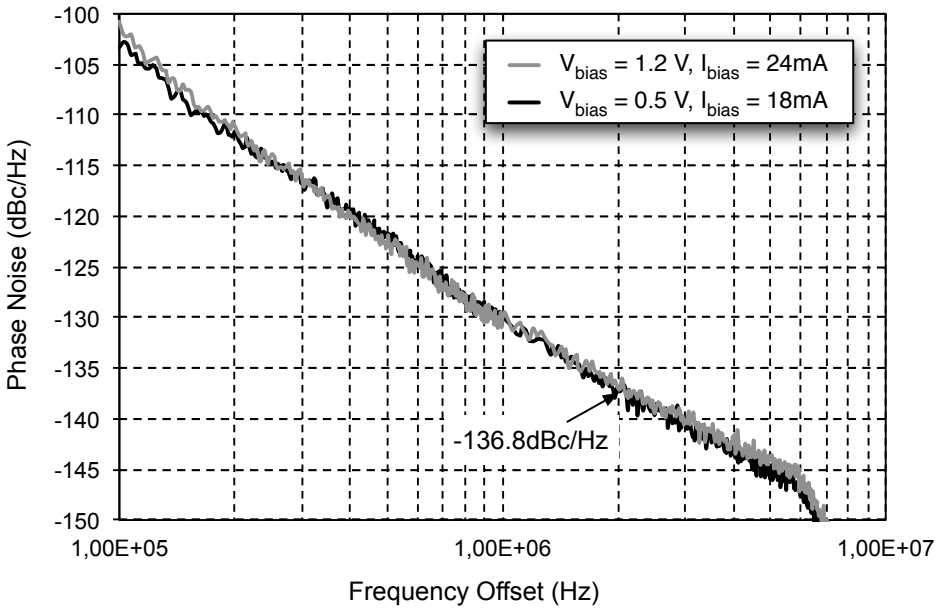

Figure 4.23: *Phase noise plots at mid-band, for V_{bias} = 1.2V and V_{bias} = 0.5V with different current consumptions*

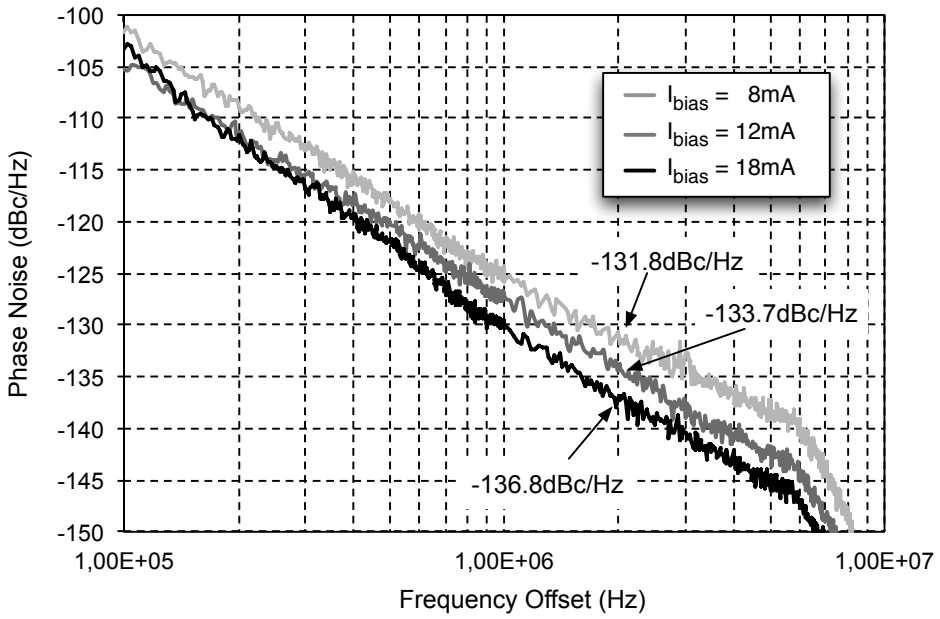

Figure 4.24: *Phase noise measurements at mid-band, for different values of bias current I_{bias}*

	this work	[11]	[34]	[36]	[37]
Center Frequency [GHz]	**7.95**	3.64	3.32	14	4.15
Tuning Range [GHz]	**2.5 (31%)**	0.69 (19%)	1.53 (46%)	2.0 (15%)	2.5 (60%)
PN at mid-band [dBc/Hz]	**-137 @2MHz**$^{(a)}$	-149 @3MHz$^{(b)}$	-156 @20MHz	-133 @3MHz$^{(b)}$	-126 @1MHz
Estimated PN @20MHz from 915MHz [dBc/Hz]	**-169**	-167	-168	-162	-164
Power Supply [V]	**1.5**	1.4	1.2	1.2	1.8
Current Consumption [mA]	**18**	18	19	7	7.5
FoM [dBc/Hz]	**188-189**	186	188	185	185-190
Techn. [CMOS]	**55nm**	90nm	RF 90nm	65nm	130nm

(a) After division by 2

(b) after division by 4

Table 4.5: *Summary results and comparison with the state of the art*

4.5 Summary Results

The table 4.6 reports the measurement results of all the DCO and VCO prototypes. The DCO, designed in 2009, is the only one that uses the CMOS 65nm technology with the voltage supply of 1.8V. It was realized to verify the capacitive degeneration theory and was tailored to GSM standard. The DCO shows good phase noise performance, but the resulting FoM is only 183dBc/Hz due to the underestimated parasitic resistance in the tank layout that reduced the Q of the tank.

The ADPLL was realized in 2010. The DCO of the frequency synthesizer exploits the capacitive degeneration and its fine-tuning was designed to be able to cover a large range of frequency (30MHz), allowing multi-standard applications. Its FoM is 184dBc/Hz in line with the state of the art.

Finally, the power scalable DCO and the Hybrid Class-C/Class-B VCO were integrated in 2011. The former save current keeping the same tank and switching the DCO topology from n-only to p-n. The phase noise difference between the two DCOs is 5.4dB, very close to the theoretical value of 6dB. The latter is based on the class-C principle that improves the conversion of bias current into fundamental current harmonic, saving current for the same oscillation amplitude and phase noise. In fact, the VCO reach the best phase noise performance and FoM.

	DCO	DCO (ADPLL)	Power-Scalable DCO p-n (n-only) mode	Hybrid Class-C/Class-B VCO
Center Frequency [GHz]	3	7.2	7.75	7.95
Tuning Range [GHz]	0.78 (26%)	2.3 (33%)	2.5 (33%)	2.5 (31%)
Fine Tuning Range [MHz]	2-12[a] (13 bits)	5-30[a] (12 bits)	5-15 (8-20)[a] (12 bits)	15MHz (Varactor)
Fine Frequency Resolution [KHz]	0.15-1.5[a]	1-6[a]	1.2-4 (2-5)[a]	-
Power Supply [V]	1.8	1.5	1.5	1.5
Phase Noise [dBc/Hz]	-127.5 @1MHz	-160 @20MHz[b]	-129.3 (-134.7) @2MHz[c]	-137 @2MHz[c]
Estimated PN @20MHz from 915MHz [dBc/Hz]	-164	-166	-161.3 (166.4)	-169
Current Consumption [mA]	16	20	6 (24)	18
FoM [dBc/Hz]	183	184	185.6 (185)	188-189
Technology [CMOS]	65nm	55nm	55nm	55nm

(a) Tunable (b) After division by 4 (c) After division by 2

Table 4.6: Summary results of all prototypes

Conclusions

The design of the Phase Locked Loop (PLL) is one of the most important topic on which the research activity is focused, due to the wide range of applications where they are applied. The All Digital PLL (ADPLL) is the last step of the frequency synthesizers evolution and is the result of the digital intensive approach to the PLL design. It exploits all the advantages of the digital design and the new CMOS technologies that improve the reconfigurability, the speed, the reliability of the system together with the reduction of the cost, the area and the power consumption.

One of the key blocks of the ADPLL is the Digital Controlled Oscillator (DCO). It defined the out-of-band phase noise performance and represent the most power-hungry element of the system.

In the first part of my research activity I was committed to the design of a DCO with high frequency resolution, studying a new architecture that didn't affect the output phase noise and avoided the use of dithering. The result is the capacitive degenerated DCO which achieves the high frequency resolution controlling a capacitive bank placed between the sources of the switching pair of a classical LC-tank oscillator that restores the energy losses sustaining the oscillation. Exploiting the shrinking effect of this architecture, the proposed DCO has the fine frequency resolution small enough to keep the quantization noise much lower than the analog noise, using only standard devices provided by the technology. The capacitive degenerated DCO potentialities were demonstrated through both a theoretical approach and a prototype characterization.

In the second part of my activity I contributed to the design of a fractional-N ADPLL and I designed the DCO exploiting the capacitive degeneration. The digital frequency synthesizer combines noise performances of the best analog PLLs with the flexibility of digital circuits, allowing wideband two point modulation and fast locking. Measurements and FoM classification confirm the soundness of the proposed solution.

Finally, I researched some techniques to reduce the power consumption of the oscillator, resulting in three different solutions: the Power scalable n-pn DCO, the Hybrid Class-C/Class-B VCO and the Dynamic Bias Class-C VCO. The basic idea of the power scalable DCO is to keep the same tank while switching the oscillator topology from n-only to p-n depending on the phase noise specs for each band. This allows to reconfigure the power consumption maintaining an almost constant

FoM for both topologies. The hybrid class-C/class-B VCO exploits the advantages of the classical class-C oscillator, overcoming its the trade-off between the maximum output amplitude and start-up condition. Those two solution were demonstrated and the two prototypes confirm the theories. The power scalable DCO has the same FoM for both the topologies, while the hybrid class-C/class-B oscillator increases the FoM greater than 2dB compared to the classical architecture. The dynamic bias class-C VCO uses a negative feedback to set dynamically the proper bias voltage at the gates of the switching pair. In particular, at the start-up the loop guarantees the bias voltage able to get up the oscillation while during the operative condition the it is lowered to the minimum value, maximizing the output swing. The idea was proved only by simulations, while the layout is still in progress.

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