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ANALOG TO DIGITAL CONVERTERS FOR SWITCHING POWER SYSTEMS

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Introduction

In an "electronic" world, where portable devices have become the driving force of the consumer market, new challenges are emerging to increase the performance, while maintaing a reasonable battery life. Thanks to the fast improvement of CMOS fabrication technology, which is pushing toward deep sub-micron integration level, the digital domain looks like the best solution to implement signal processing functions. Indeed, the reduction of the voltage headroom introduces severe constraints for achieving an acceptable dynamic range in the analog domain. Lower cost, lower power consumption, higher yield, and higher re-configurability are the major advantages of using digital signal processing. In recent years, several typically analog functions have been moved in the digital domain. This evolution means that the Analog-to-Digital (A/D) Converters (ADCs) are becoming the key components in many electronic system. They are, indeed, the bridge between the analog and the digital worlds, and, therefore, their efficiency and accuracy often determine the overall system performance. However, not all of the analog signal processing functions can be implemented in the digital domain. For example, signal amplification and power supply voltage regulation are two functions that are inherently analog, thus requiring analog power-efficient solutions, such as the switching-mode technique. This technique is based on the manipulation of the power supply voltage through a switching system, in order to produce a signal or a specific constant voltage value, with maximum efficiency. All the switching-mode systems, however, require some sort of control circuit, which often consumes a significant amount of power. It is obvious that moving the control functions of switching-mode analog circuits into the digital domain would inherently be the best solution, since it would benefit of the advantages of digital signal processing, while implementing high-efficiency analog functions. However, such switching systems with digital control require high-performance low-power ADCs.

This thesis focuses on the design of two different ADCs, used in two digitally controlled switching-mode systems. The first system is a digitally controlled Switched-Mode Power Supply (SMPS), in which a multi-function Successive Approximation Register (SAR) ADC is used to achieve the required performance with minimum power consumption and area. The device, realized with a 65 nm CMOS technology, is designed for portable applications, where silicon area is critical. The second design is focused on the implementation of a third-order low-pass hybrid continuous-time (CT) multi-bit $\Sigma\Delta$ modulator, implemented with a 45nm CMOS technology. This ADC is included in a fully-digital class-D amplifier for closing the feedback loop, ensuring high linearity and an intrinsic anti-aliasing filter. Class-D audio amplifier are the most efficient audio power

stages. Likewise a SMPS, a class-D amplifier is based on the duty cycle regulation of the switched power supply.

Before describing in detail the two designs, we will introduce the switching-mode systems in general, focusing in particular on class-D amplifiers and SMPS, in order to determine the best ADC topologies for these applications. In Chapter 1 the general aspects of switching-mode power systems and the main benefits with respect to linear solutions will be analyzed. Chapter 2 will focus on the digital solutions to control the switching-mode power systems. Analog and digital solutions will be compared considering the evolution toward deep sub-micron technologies. In Chapter 3 the SAR ADC designed in 65nm CMOS technology will be described, showing the results of the complete SMPS system. In Chapter 4 the CT $\Sigma\Delta$ modulator in 40nm CMOS technology will be presented, together with the first measurements of the ADC stand alone. Finally, the conclusions will be discussed in Chapter 5.

Chapter 1

Switching-Mode Systems

In a complex electronic system there are many cases where it is necessary to increase or reduce the voltage level. According to the nature of the signal, it possible to distinguish two main cases: DC-DC or AC-AC converters. In the first case we talk about voltage regulators, while in the second case of signal amplifiers.

In many cases it is necessary to adjust a constant voltage to achieve the power supply levels required by different components. These components may be digital or analog, and both of them have different requirements in terms of supply voltage levels, supply voltage tolerances and current consumption levels. In this case DC-DC converters are required. A DC-DC converter provides a constant DC output voltage, which is steadily maintained at the designed value.

On the other hand it is often necessary to increase the power of a time variant signal, increasing its voltage level. In this case we need a signal amplifier able to follow the input signal variations without introducing distortion. A typical case are audio amplifiers, used to amplify the voltage signal to drive the inductive speaker load. Unlike the voltage regulator, the signal amplifier typically works with variable signals in a given frequency range, and, therefore, it is an AC-AC converter.

In both cases there are many solutions to optimize the performance in the appropriate scope. In this chapter we will examine the common theory used to regulate the DC voltage and to amplify an AC audio signal increasing the efficiency.

1.1   Linear Voltage Converters

DC-DC and AC-AC converters have similar circuit topology even though they operate in different current regime (direct and alternative). In both cases we can distinguish two main topologies: linear and switching system. In a linear solution generally the output voltage is obtained by varying a resistance trough a control signal. The output voltage is a percentage of the input voltage (or power supply) and the residual voltage is lost on the control resistance. This make the linear systems very inefficient.
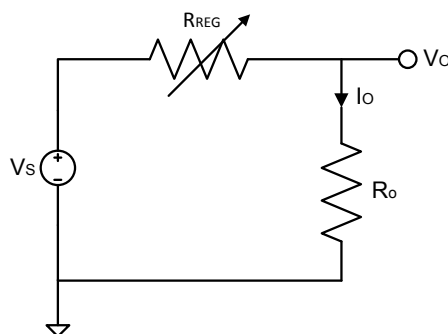
Figure 1.1: General linear regulator

1.1.1 Efficiency Considerations

When considering portable devices, power dissipation should be minimal both for achieving the longest possible battery life time and for minimizing heat generation. Obviously, the less energy is lost during normal operation of a system, the better it is. The parameter that defines the effectiveness of a system it is called efficiency. The efficiency η of a generic system is defined as the ratio between the output power P_{OUT} and the input power P_{SUP} of the system:

$$\eta = \frac{P_O}{P_{SUP}} = \frac{P_O}{P_O + P_{DISS}}.$$ (1.1)

In particular, we can specify more in detail P_{SUP} as shown in (1.1), in which P_{DISS} includes all the power losses. In applications where power consumption is not particularly important, a constant quiescent current is used in the active devices. This current, also called "operating current" or "ground current", is never delivered to the load, but it flows from the power supply to ground. Since the load current often varies widely, the net effect of the quiescent current also varies. The question is, which load occurs for the greatest amount of time? If load currents are small for most of the time, then the quiescent current has to be low to achieve high efficiency. This caveat is especially critical in designs that never actually turn off. This is the case of linear regulators and linear amplifiers.

1.1.2 Linear Regulators

In a linear regulator power is transferred continuously from the input supply to the output load. The control circuitry must monitor (sense) the output voltage, and adjust the current by changing the voltage on the gate (or base) of a transistor used as a resistor. The transistor size defines the maximum load current which the regulator can provide while maintaining a stable output voltage. Typically, the linear regulator offers small physical size and low noise operation, but, on the other hand, it has low efficiency and it is able to provide only output voltages lower than the supply voltage. As shown in Figure 1.1, a
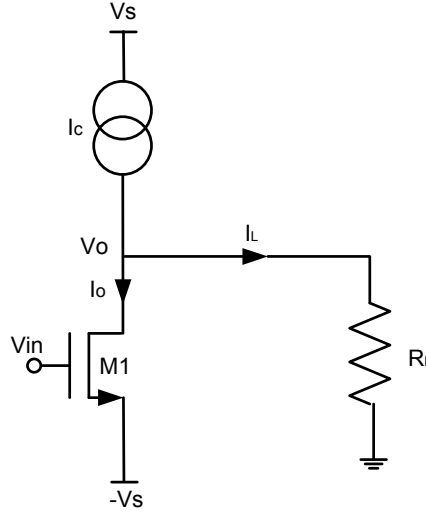
Figure 1.2: General class-A amplifier

linear regulator is similar to a variable resistor. The wasted power is then given by:

$$P_{DISS} = I_O \cdot (V_S - V_O).\qquad(1.2)$$

A linear regulator may be preferred for light loads (small I_0) or when the desired output voltage approaches the source voltage (small $\Delta V = V_S - V_O$). Indeed all linear regulators require an input voltage at least some minimum amount higher than the desired output voltage. That minimum amount is called the dropout voltage. If the dropout decreases, the efficiency increases and we have a so-called Low-Dropout (LDO) regulator.

1.1.3 Linear Amplifiers

Power amplifiers can be divided in different categories, depending both on the topology and how the amplifier delivers the power to the load: each category is called class and features different characteristics. The linear amplifiers belong to class A, B, AB, and C. In the class-A amplifier, shown in Figure 1.2, the input signal is applied to the gate of transistor M1 that is biased by the current source I_0. Even in the absence of input signal, a bias current I_0 is always absorbed from supply voltage V_S, producing a fixed and significant power loss. Considering a sinusoidal input signal:

$$V(t) = A \cdot \sin(2\pi f t),\qquad(1.3)$$

as shown in Figure 1.3, the power transferred to the load is given by:

$$P_L = R \cdot I_{Leff}^2 = R \cdot \frac{V_0^2}{(2 \cdot R^2)} = \frac{V_0^2}{2 \cdot R},\qquad(1.4)$$
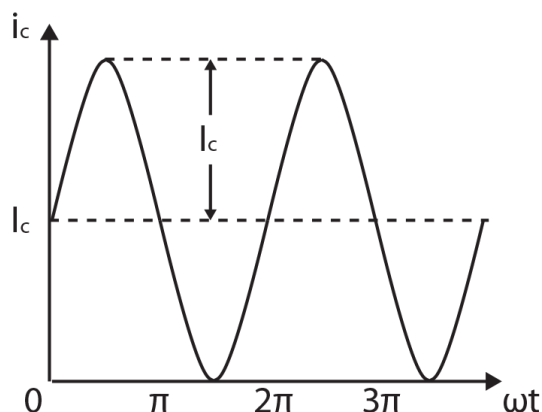
Figure 1.3: Current in a class-A amplifier

while the power delivered by the supply is:

$$P_S = 2 \cdot \frac{V_S{}^2}{R}. \tag{1.5}$$

Therefore, the efficiency becomes:

$$\eta = \frac{P_L}{P_S} = 0.25 \cdot \frac{V_0^2}{V_S} \rightarrow \eta_{max} = 25\%. \tag{1.6}$$

According to (1.6), the theoretical efficiency is poor and, therefore, the use of class-A amplifiers can be tolerated only when neither power consumption nor thermal dissipation causes problems. Nevertheless, this class of amplifiers ensures very high linearity and it is easy to design due to the small number of components, thus making this configuration very popular in many non portable applications.

Class-B, AB and C amplifiers feature better efficiency than class-A stages, reaching values of the order of 50%, but at the expense of worse linearity performance.

1.2   Switching-Mode Voltage Converters

To increase the efficiency, the most common technique is to use a switching converter topology, based on the pulse code modulation, which transforms the input signal in a rail-to-rail switching square-wave that can drive in a very efficient way the output load. An output filter is then introduced, in order to demodulate the amplified signal (or the DC value) and filter out all the high frequency spurs introduced by the modulation. The pulse code modulation is adopted both to regulate a DC voltage supply, in a Switching-Mode-Power-Supply (SMPS), or to amplify an audio signal, in a class-D amplifier, as show in Figure 1.4.
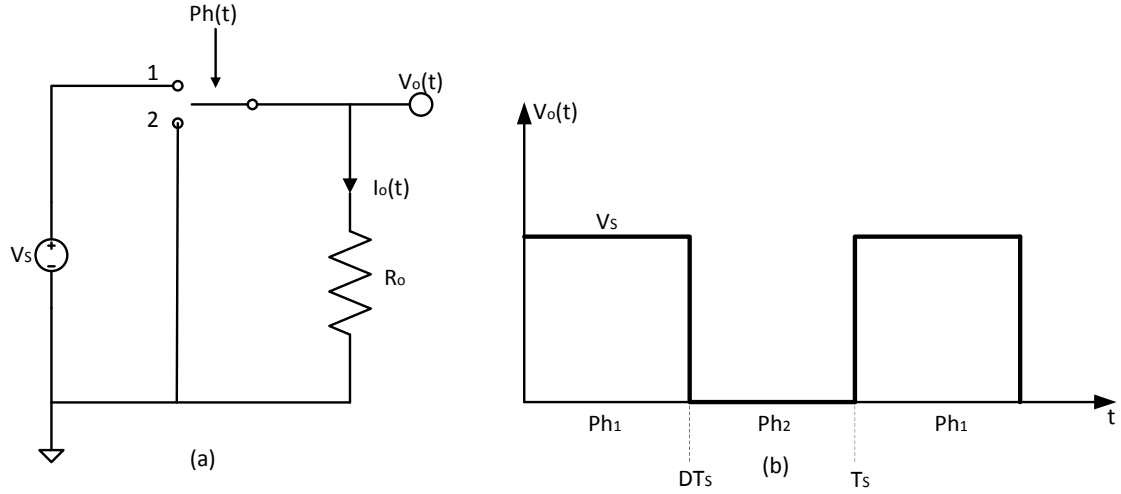
Figure 1.4: Ideal switching system (a) and output voltage waveform $v_s(t)$ (b)

Considering the ideal circuit illustrated in Figure 1.4(a), the switch produces a rectangular voltage waveform $v_o(t)$, as shown in Figure 1.4(b). Voltage $v_o(t)$ is equal to the DC input voltage V_S when the switch is in position 1, while it is equal to zero when the switch is in position 2. The inverse of the switching period T_S is called switching frequency, f_s. The duty ratio D is defined as the fraction of the switching period that the switch spends in position 1. The complement of the duty ratio, D', is defined as $(1 - D)$. This kind of modulation is called Pulse Width Modulation (PWM). Integrating $v_o(t)$ over the period T_S, we obtain the average value:

$$\langle v_o(t) \rangle = \frac{1}{T_S} \int_0^{T_S} v_o(t) dt. \tag{1.7}$$

The integral in (1.7) is given by the highlighted area under the curve, as shown in Figure 1.5. Therefore, the average value $\langle v_o(t) \rangle$ is:

$$\langle v_o(t) \rangle = \frac{1}{T_S} \int_0^{T_s} v_o(t) dt = \frac{1}{T_S} (DT_s V_S) = DV_S. \tag{1.8}$$

The average output voltage is, therefore, a function of D. In order to obtain the average output voltage, a low-pass filter has to be introduced. In DC regulators the filter will be designed to extract the DC components, but to reject the components of $v_o(t)$ at the switching frequency and its harmonics. The PWM signal is periodic and its duty cycle can be fixed or change very slowly with respect to T_S, as shown in Figure 1.6(a). By contrast, in a class-D amplifier, the PWM signal is the product between a carrier (generally a triangular wave) and the audio signal to be amplified. Then, $v_o(t)$ is filtered to extract the signal in the audio band, as shown Figure 1.6(b), and to reject the high frequency spurs introduced by the modulation.
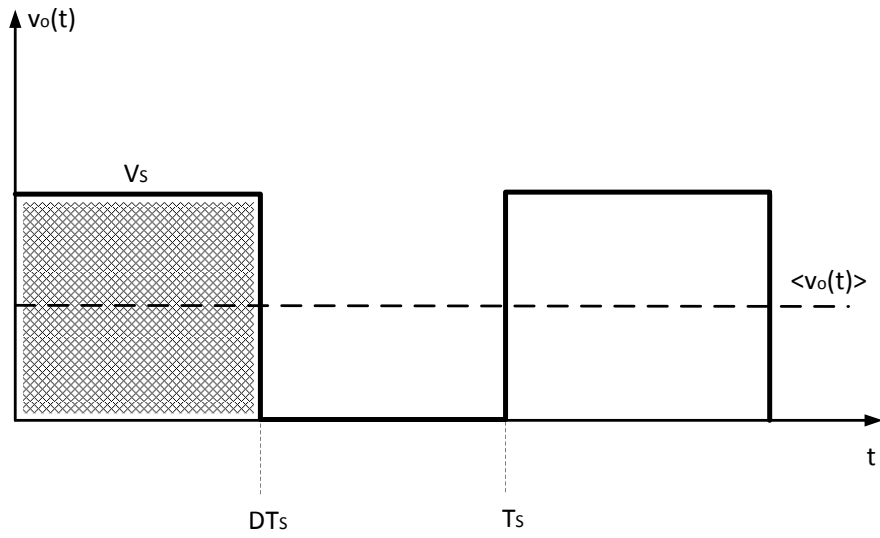
Figure 1.5: Average output voltage
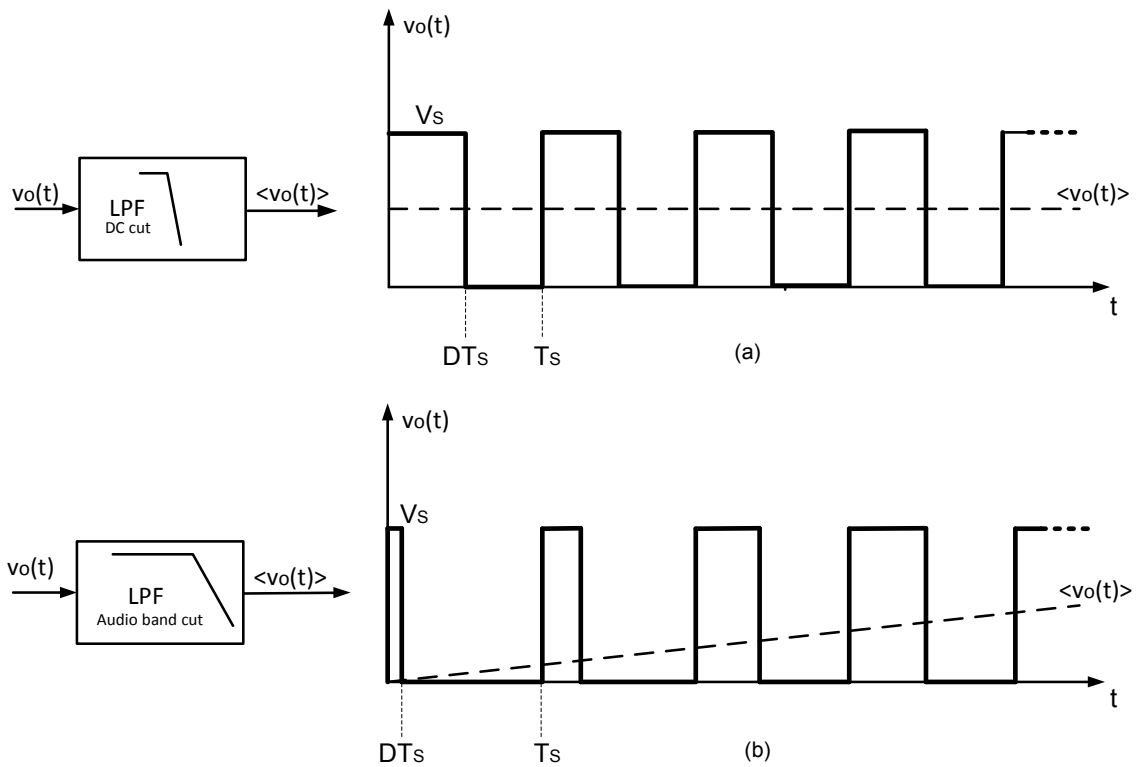
Figure 1.6: PWM modulation with constant duty-cycle (a) and variable duty-cycle (b)

1.2.1 Pulse Code Modulation

Pulse code modulation is the key feature of a switching-mode converter. Two are the main existing pulse code modulation techniques: the Pulse Density Modulation (PDM) and the Pulse Width Modulation (PWM). For both modulations the output signal consists of trains of pulses with variable density in the time domain, as shown in Figure 1.7. With PDM, especially for large input signal amplitudes, the output transistors are switched on and off quite often, thus introducing significant switching losses. Moreover, PDM requires a more complex modulator implementation with respect to PWM, which normally requires just a comparator. For these reasons class-D amplifiers and DC-DC converters normally use PWM modulation, which can be implemented in two main versions.

The first PWM version is called Natural Sampling (NS). As shown in Figure 1.8(a) it is obtained from the comparison between the modulating signal and a periodic carrier signal, that usually is a triangular or saw-tooth waveform. Figure 1.9(b) shows an example of NS signal behavior: due to the absence of any form of sampling, this modulation is completely analog and features an ideally null distortion. For this reason this type of modulation is preferred in the class-D amplifiers.

The second PWM version is called Uniform Sampling (US) and it is represented in Figure 1.9(c). In this case a sample-and-hold circuit is inserted in front of the comparator, in order compare the carrier with a fixed input value, as shown in Figure 1.8(b). This kind of modulation introduces a delay time that cannot in general be neglected and represents the most significant difference between uniformly sampled and naturally sampled modulators. This delay causes a phase lag, which introduces many in band harmonics, but is often used in mixed analog-digital systems, where a very good interface between digital part (input) and analog part (power output) is needed. In these cases, PWM with US does not worsen the system linearity performance, since the digital input signals are already sampled, while the performance mainly depends on quantization and sampling frequency.

1.2.2 SMPS Regulator Topologies

The basic premise behind the operation of SMPS is the use of switches to charge an energy storage element from the input power source and then discharge the same element to the load. Since charging and discharging occur in separate time intervals, it becomes possible to decouple the energy transfer from the input to the output. The switching process to accomplish this decoupling produces a periodic waveform with a DC component and harmonic components at multiples of the switching frequency, which have then to be filtered.

Starting from these assumptions, it is possible to design different DC-DC converter topologies. It is possible to distinguish three main switching-converter families, from which stem all the other topologies.
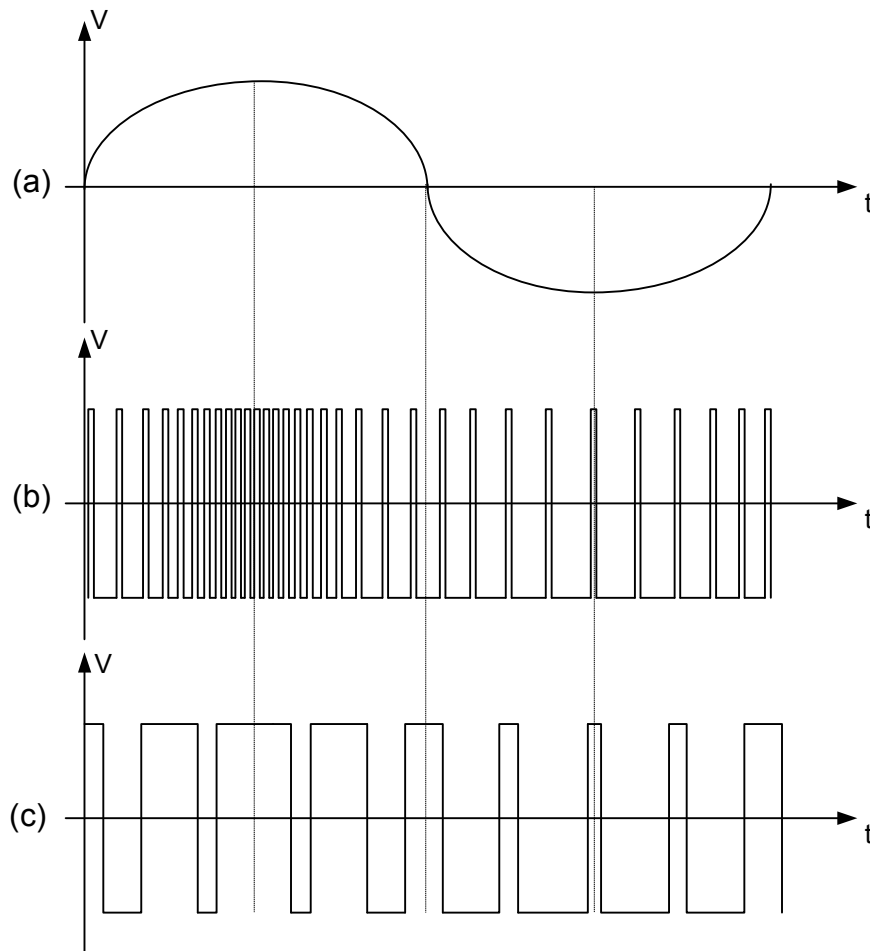
Figure 1.7: Pulse modulations examples: input signal (a), PDM (b) and PWM (c)
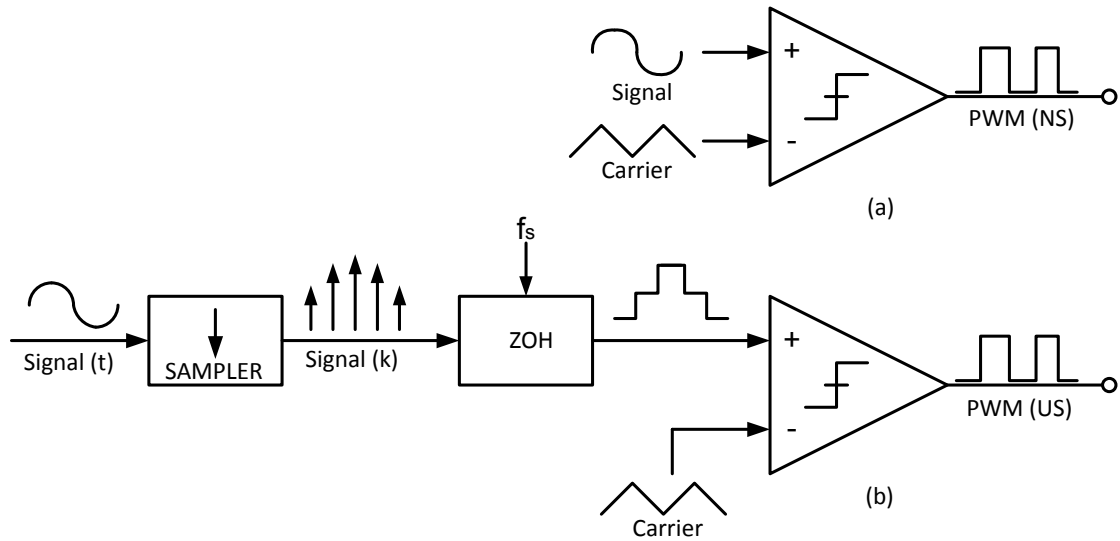
Figure 1.8: PWM modulators: Natural Sampling modulator (a) and Uniform Sampling modulator (b)

Synchronous Buck Converter

In a synchronous Buck converter, the DC output voltage can only be smaller than the supply voltage. This topology is defined as synchronous because the on/off period is controlled by the switch driving phase in contrast with other configurations where the discharging of the inductance takes place through a diode. As shown in Figure 1.10(a), in an ideal buck converter, there are two time intervals during each switching period: one in which the inductor is charged through the up-switch and one in which the inductor is discharged through the down-switch. Such operation is called Continuous Conduction Mode (CCM) and is characterized by a two-level switch-node voltage and a continuous inductor current. The switching process generates a rectangular voltage waveform at the switch node, with peak value equal to the input voltage and duty-cycle set by the gate-drive signal, which is then low-pass filtered to remove the harmonics at multiples of the switching frequency. This produces a DC output voltage with superimposed ripple (due to non-ideal filtering). The magnitude of the DC component of the output voltage V_O depends on the input voltage V_S, as well as the duty-cycle D, according to:

$$V_O = D \cdot V_S. \tag{1.9}$$

Boost Converter

The basic principle of a Boost converter is illustrated in Figure 1.10(b). The inductor is charged when the switch is on and is discharged when the diode is on. Such a converter can only increase the voltage, but not reduce it. When the switch is on, the current flows
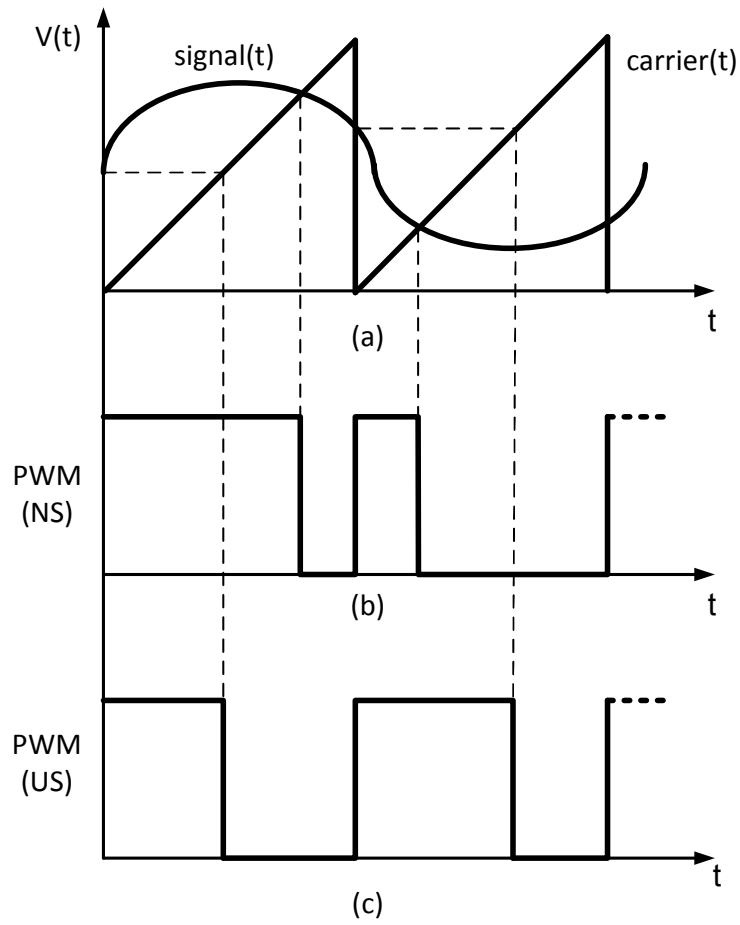
Figure 1.9: PWM waveforms: carrier and input signal (a), Natural Sampling output signal (b) and Uniform Sampling output signal (c)

through the inductor charging it. In this phase the diode is open and the current on the load is supplied by the output capacitor. When the switch is turned off, the inductor discharges on the capacitor through the diode. If the discharging inductor current reaches zero before the end of the switching period, a third time interval is introduced, during which both the switch and the diode are off and the inductor is in steady-state at zero current, resulting in a discontinuous inductor current waveform. This mode of operation is known as Discontinuous Conduction Mode (DCM) and can occur during low load conditions for any SMPS employing a diode, but does not occur if the diode is replaced with an active switch, as in the synchronous Buck converter. The output voltage in DCM can be calculated as:

$$V_O = \frac{1 + \sqrt{1 + \frac{4D^2}{K}}}{2} \cdot V_S, \tag{1.10}$$

where

$$K = \frac{2L}{R_L T_s}. \tag{1.11}$$

The operation in DCM or CCM depends on the inductance value. The limit between the two modes is determined by:

$$L_0 = \frac{R_L T_s \cdot D (1 - D)^2}{2}. \tag{1.12}$$

If $L > L_0$, the circuit operates in CCM and V_O is equal to:

$$V_O = \frac{1}{1 - D} \cdot V_S. \tag{1.13}$$

However, operating the Boost converter in CCM is difficult because of stability issues and, therefore, it is preferable to use it in DCM.

Buck-Boost Converter

The last topology is the Buck-Boost converter, show in Figure 1.10(d). This converter can either increase or decrease the voltage with polarity inversion. The inductor is charged when the switch is on and the diode is off. When the switch turns off, the inductor forces the current through the diode changing the polarity of V_O. The output voltage can be larger or smaller than the supply voltage depending on the value of D, according to:

$$V_O = \frac{D}{1 - D} \cdot V_S. \tag{1.14}$$

1.2.3 Analogy between Class-D Amplifiers and Buck Converters

Class-D amplifiers and Buck DC-DC converters are actually quite similar both in terms of topology and of operating principle, as illustrated in Figure 1.11, although the functional scope, the variables involved, and the qualitative factors are different.
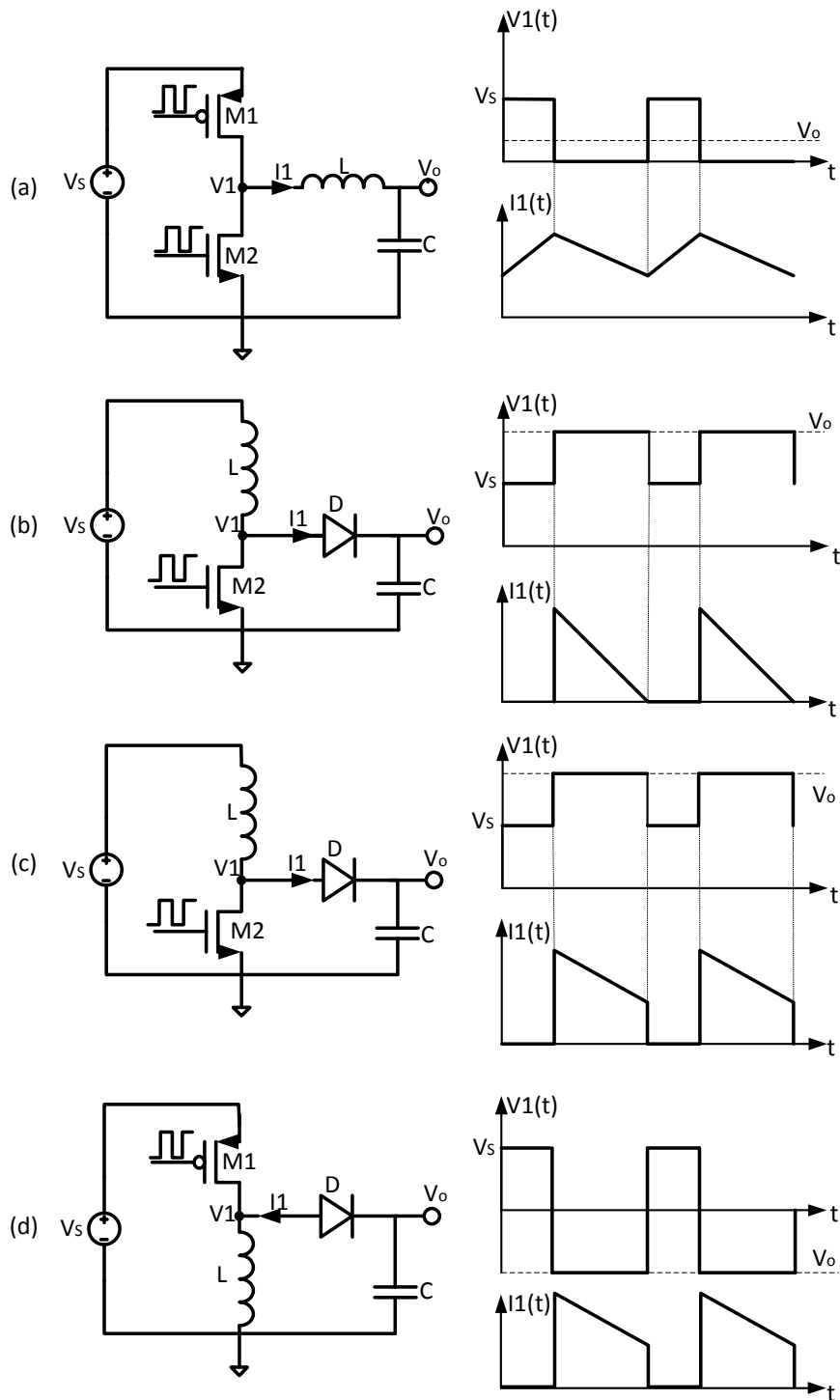
Figure 1.10: SMPS regulators: synchronous Buck converter (a), Boost converter in DCM (b), Boost converter in CCM (c), and Buck-Boost converter (d)
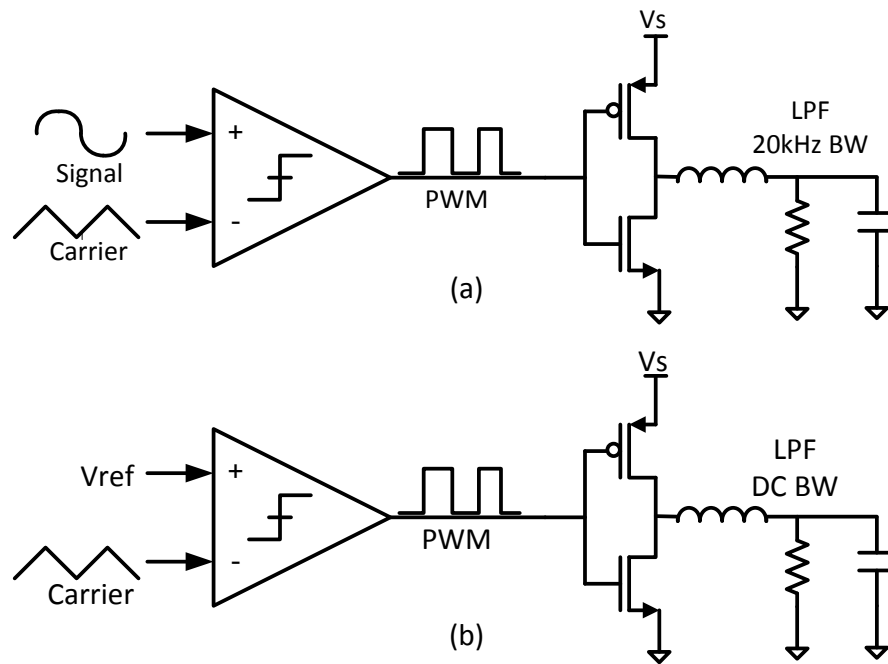
Figure 1.11: Analogy between ClassD signal amplifier (a) and SMPS Buck converter (b)

The main differences between the two system are summarized in Table 1.1. Firstly, the reference signal in a synchronous Buck converter is constant (or changes very slowly), while in a class-D amplifier it is an audio signal, which is continuously changing. This means that the duty cycle is relatively fixed in the Buck converter, whereas it varies in the class-D amplifier. Moreover, the output filter in the Buck converter is designed to obtain a DC output voltage with low ripple and the inductor is sized to deliver a constant current towards to the load. By contrast, in a class-D amplifier, the inductor is included in the speaker (the load) and the current flows in both directions. Finally, the MOS power transistors are optimized differently: in the Buck converter the main target is to maximize the efficiency, while in a class-D amplifier the main goal is to achieve good linearity.

Table 1.1: Comparison between class-D signal amplifier and SMPS Buck converter

Parameter	Buck Converter	Class-D Amplfier
Input format	Fixed	Variable (audio signal)
Output current	Positive	Negative and positive
Output filter constraints	Small ripple	Audio signal band, linear phase
Quality criteria	Load transient, line transient	Distortion, noise, power-supply rejection ratio
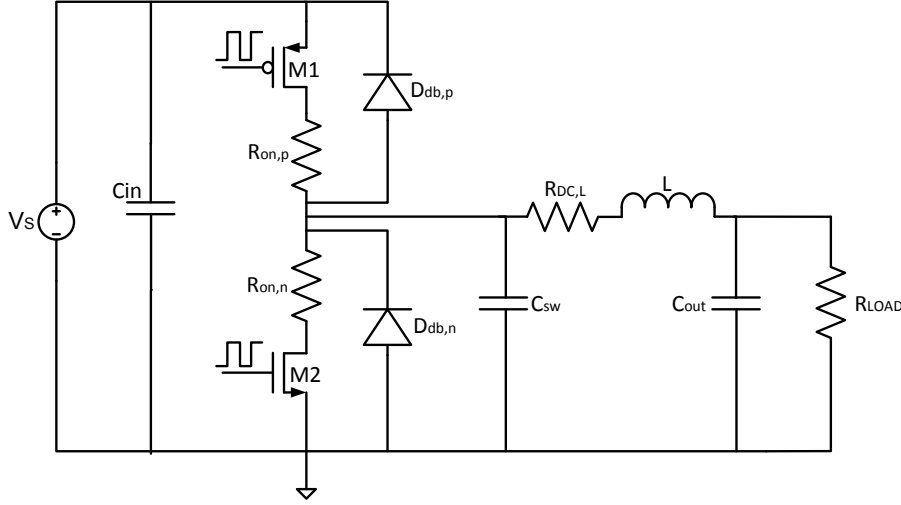
Figure 1.12: Switching-mode system including the main parasitic components

1.2.4 Efficiency

Theoretically, due to the behavior of switching-mode systems, no power stage bias current is needed. All the power drained from the supply is delivered without losses to the load, leading ideally to 100% efficiency. In the real world, however, there are anyway sources of power loss. Then, it is important to evaluate the impact of each component on the overall losses. Each loss component can be allocated into the two following categories:

- DC losses (conduction losses and quiescent current);
- AC losses (switching losses).

Figure 1.12 shows the circuit parasitic elements that are the main source of power dissipation in a switching-mode-system. The equivalent circuit includes the switch on-resistances ($R_{on,p}$ and $R_{on,n}$) and the inductor winding resistance ($R_{DC,L}$), the switching node parasitic capacitance (C_{SW}), and the parasitic drain-body diodes ($D_{db,p}$ and $D_{db,n}$) of the MOSs power transistors.

Conduction Losses

The current flowing through non-ideal power transistors, filter elements, and metal interconnections results in a power dissipation in each component equal to:

$$P_{COND,i} = I_{RMS,i}^2 \cdot R_i, \tag{1.15}$$

where I_{RMS} is the root-mean-square value of the current flowing through the ith component, and R_i is the parasitic resistance of the ith component. In PWM mode, the I_{RMS} has DC and AC components:

$$I_{RMS,i}^2 = I_{RMS,DC,i}^2 + I_{RMS,AC,i}^2. \tag{1.16}$$

In a class-D amplifier the AC components (harmonic losses) are larger, due to intermodulation between the input signal and the carrier frequency. In the DC-DC converters, the losses are mainly due to the DC current, while the AC components are caused by the ripple. In both of cases the performance depends strongly on the load and filter quality. The conduction losses are proportional to the signal level.

Gate-Drive Switching Losses

Pulling up and down the gate of a power transistor in each switching cycle dissipates a dynamic average power given by:

$$P_{GATE} = E_{GATE} \cdot f_S, \tag{1.17}$$

where E_{GATE} is the energy required for off-to-on-to-off gate transition (which can include some energy due to the Miller effect), and includes the power dissipation in the driver circuitry. Since the gate-drive loss is independent of the load current, it degrades the light-load efficiency.

Gate-Drive Timing Error

There are tree mutually exclusive mechanisms of losses due to timing errors which can occur in the switching of the power MOSFETs, all independent of the output current:

- *Cross-Conduction Loss* — A short-circuit path may temporarily exist between the input rails during power MOSFET switching transitions. To avoid potentially large short-circuit losses, it is necessary to provide dead-times in the conduction of the MOSFETs with local digital feedback, to ensure that the two devices never conduct simultaneously. Cross-conduction losses are given by:

$$P_{SW,CC} = \frac{1}{2}\left(t_{SW,on} + t_{SW,off}\right) \cdot f_S \cdot \frac{V_S}{R_{DS,on}}, \tag{1.18}$$

  where $t_{SW,on}$ and $t_{SW,off}$ are the conduction time during the on and off states, f_S is the switching frequency, V_s the supply voltage and $R_{DS,on}$ the transistor on-resistance.

- *Body Diode Conduction* — If the dead-times are too long, the parasitic body diode of the low-side NMOS power transistor may be forced to pick up the inductor current for a fraction of each switching cycle. Since the forward bias diode voltage V_{DIODE} is around 700 mV, in low-voltage applications it can be comparable to the output voltage and its conduction loss may be significant:

$$P_{DIODE} = 2 \cdot (I_{LOAD}V_{DIODE}t_{ERR}f_S), \tag{1.19}$$

  where t_{ERR} is the timing error between complementary power MOSFET conduction intervals and I_{LOAD} is the output current. Furthermore, when the PMOS device is
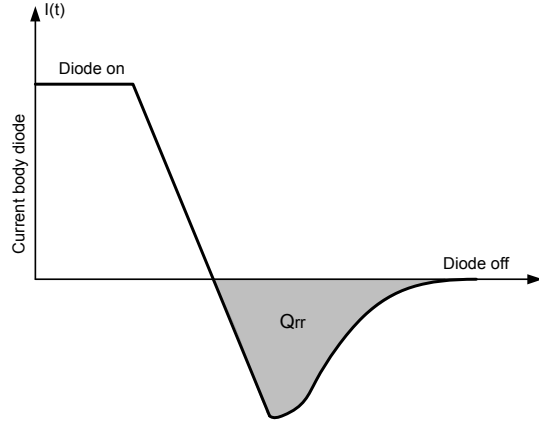
Figure 1.13: Body diode reverse recovery charge

turned on, it must remove the excess minority carrier charge from the body diode, thus dissipating an energy given by:

$$E_{ERR} = Q_{RR}V_S,\tag{1.20}$$

where Q_{RR} is the charge stored in the parasitic body diode shown in Figure 1.13.

- *Capacitive Switching Loss* — The PMOS transistor *MP* charges the parasitic capacitance C_{SW} to V_S during each switching cycle, thus dissipating an average power given by:

$$P_{SW,LH} = \frac{1}{2}C_{SW}V_S^2 f_S,\tag{1.21}$$

where C_{SW} includes the reverse-biased drain-body junction diffusion capacitance C_{db} and some or all of the gate-drain overlap (Miller) capacitances C_{gd} of the power transistors, the wiring capacitance from their interconnection, and the stray capacitance associated with bonding wires and pads.

Quiescent Power Consumption

The PWM generator and the other control circuits consume static power (P_Q). In low-power applications, this power consumption term may contribute substantially to the total losses, even at full-load.

Global Efficiency

Taking into account all the loss contributions, the overall efficiency of a switching-mode system is given by:

$$\eta = \frac{P_{LOAD}}{P_{LOAD} + P_Q + P_{SW,CC} + P_{SW,LH} + P_{DIODE} + P_{COND} + P_{GATE} + P_J},\tag{1.22}$$
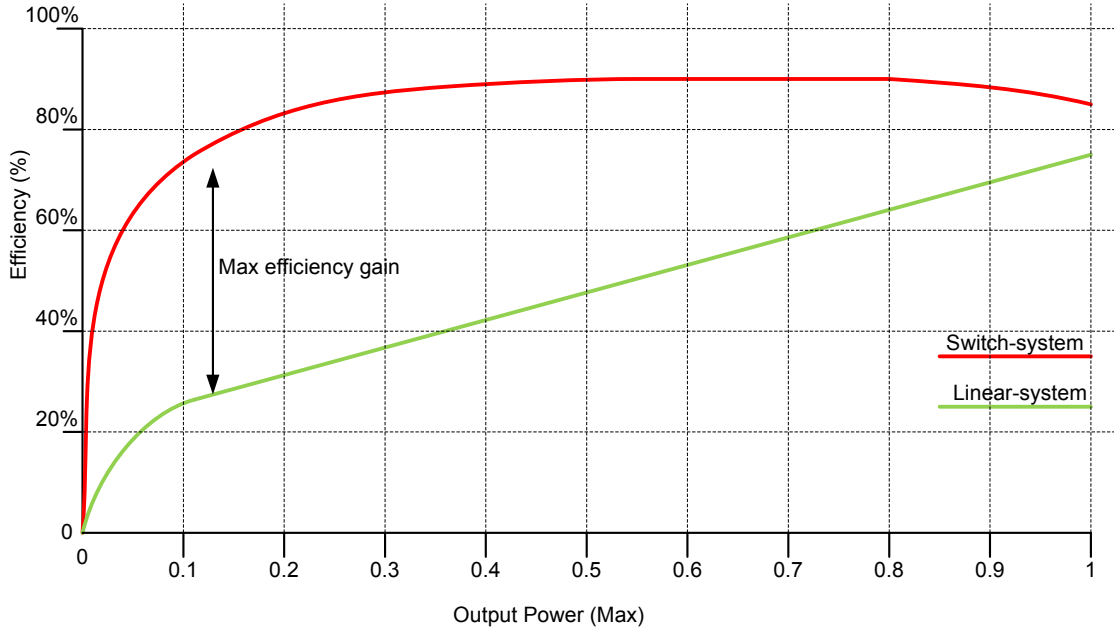
Figure 1.14: Comparison of the efficiency of linear and switching-mode systems

where P_J are the losses due to Joule effect, significant especially with large output signal levels.

Figure 1.14 shows a comparison of the efficiency between a linear and a switching-mode system. The difference between the two solution is quite large, especially for low output power, where the output signal is much lower than the supply voltage. In this case, in a linear system the power loss on the regulator resistance is large, while a switching system is efficient at low output power too, where only switching losses and quiescent power losses are significant, as shown in Figure 1.15.

1.2.5 Linearity

Unlike in SMPS DC-DC converter which works with constant output voltage, the output signal linearity is the most important parameter for signal amplifiers. Total Harmonic Distortion (THD) is the parameter used to define the linearity performance of the system. When a sine-wave is applied to a non-linear amplifier, at the output we obtain an amplified sine-wave at the base frequency of the signal, plus higher-order components with frequencies multiple of the base frequency. The THD is defined as:

$$THD = \frac{\sum_{n=2}^{\infty} P_n}{P_1}, \tag{1.23}$$

where P_1 is the power of the fundamental harmonic with frequency equal to the frequency of the input signal (base frequency) and $\sum_{n=2}^{\infty} P_n$ is the power of the higher-order harmon-
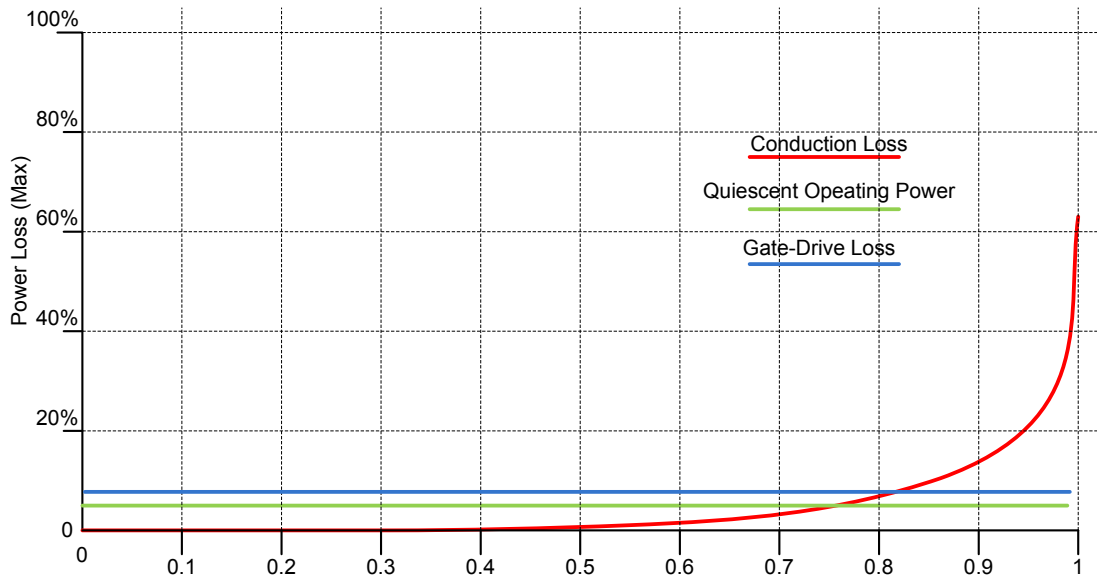
Figure 1.15: Losses as a function of the output power in a switching-mode system

ics.

A class-D amplifier, unlike the amplifiers belonging to the linear classes, is intrinsically a non-linear system, since it involves both non-linear blocks and timing error components. As a matter of fact, after the PWM modulator the input signal information is transferred from the voltage domain to the time domain (pulse width), where, unfortunately, it can be easily effected (distorted) by uncorrelated delays introduced by the different system blocks. The main contribution in this sense is introduced by the so called "dead-time" control. Such control is introduced to overcome the cross-conduction problem: basically a suitable digital logic within the class-D amplifier output drivers ensures that each transistor of a branch is turned on only when the other if completely off, as illustrated in Figure 1.16.

In practice, during a certain time interval (the dead-time), both transistors of the output branch are off, thus preventing cross-conduction. However, although the dead-time introduction improves significantly the efficiency, it also worsens the linearity because, changing the PWM timing, it effects the input signal information. For this reason, a trade-off between efficiency and THD has always to be considered in the design of the dead-time control circuit.

Another very important aspect, always related to the PWM timing, is the carrier linearity. As shown in Figure 1.17, a non linear carrier introduces time errors on each switching edge, with respect to the linear case, thus producing distortion contributions observable as in-band harmonics after the demodulation.

Other non-linearity contributions are due to asymmetries in rise/fall time of the power transistor driving signals, hysteresis and delays of the PWM comparators, non-idealities in
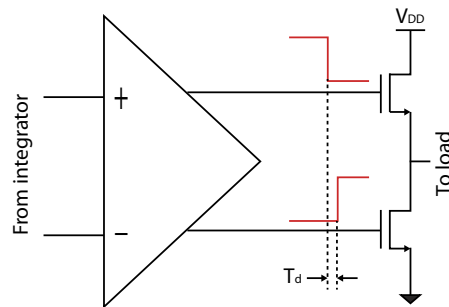
Figure 1.16: Dead-time control in the power transistor driving signals

the bridge drivers (e. g. saturation), and mismatches among the power bridge transistors.

1.2.6 Open-Loop and Closed-Loop Structures

A simple example of generic switching-mode system is shown in Figure 1.18. Depending on the reference signal and the output filter it can operate as DC-DC or AC-AC converter. This structure is very easy to implement, features high input impedance, and is intrinsically stable. However, the performance is limited by the quality of the supply voltage. Indeed, noise, disturbances, and drift of the power supply voltage affect both the gain, regulation, and linearity features. To overcome this limitation quite often both DC-DC and AC-AC converters are implemented with a closed-loop topology.

Closed-Loop Class-D Amplifier

In an open-loop class-D amplifier the overall gain depends on the supply voltage, which has to be accurate. Moreover, the output power transistors are directly connected to the power supply and, hence, any noise or disturbance on the power rails (ΔV_S) is transferred to the load (ΔV_O), leading to a degradation of the Power-Supply Rejection Ratio (PSRR), defined as:

$$PSRR = \frac{\Delta V_S}{\Delta V_O} \qquad (1.24)$$

Every non ideality introduced by the PWM modulator, the drivers, or the output stage influences directly the quality of the output signal. To overcome these limitations, most class-D amplifiers are used in a closed-loop configuration [1], as shown in Figure 1.19, where the PWM modulator is driven by difference between the input and the output signals amplified by an integrator. Due to the closed-loop topology, all the non-idealities occurring after the integrator (like distortion, and PSRR) are referred to the input divided by the integrator gain, which is large in the signal band, and their importance is then strongly reduced. Moreover, the overall (closed-loop) gain is well determined by the resistor ratio R_{FB}/R_{IN}.
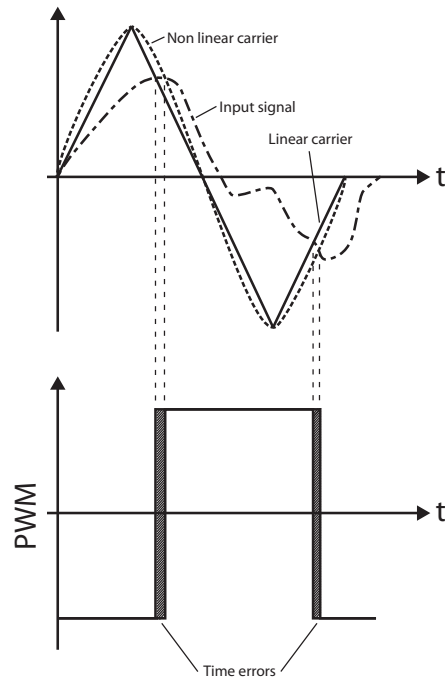
Figure 1.17: Time errors due to carrier non-linearity
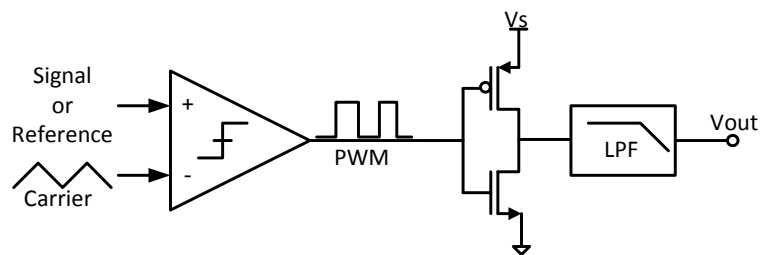
Figure 1.18: Generic open-loop switching-mode system
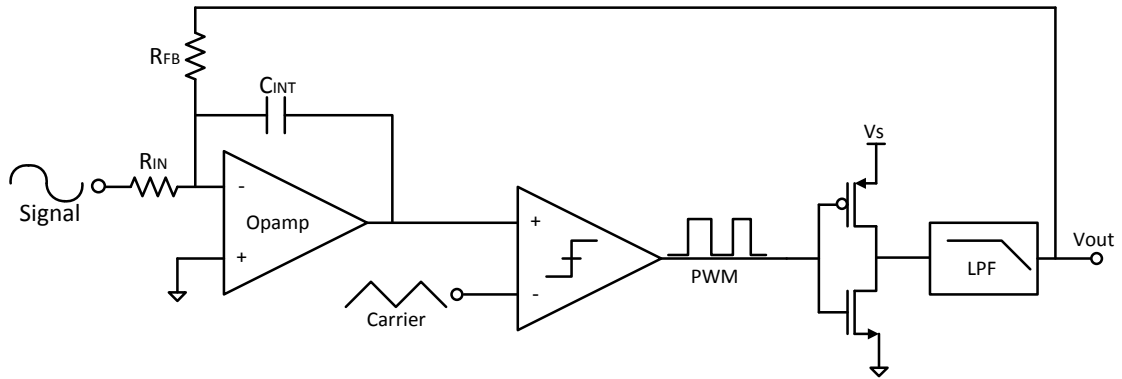
Figure 1.19: Closed-loop class-D amplifier
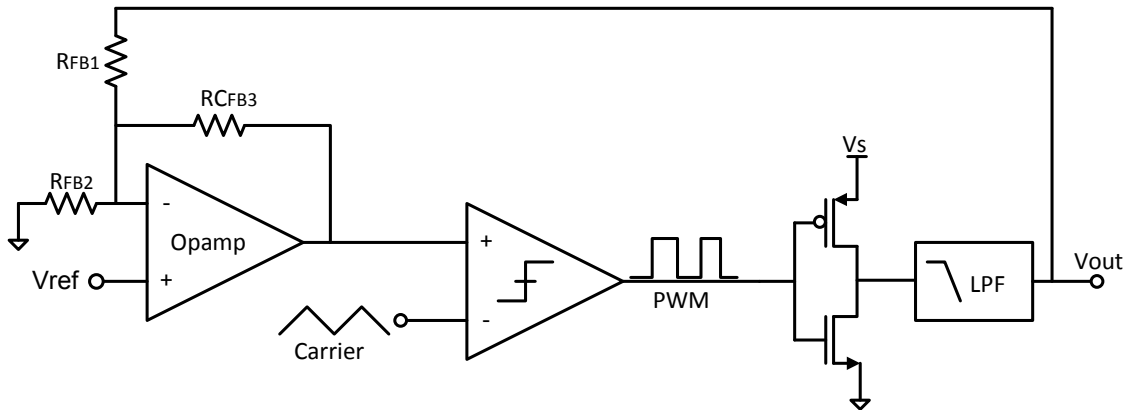
Figure 1.20: Closed-loop Buck SMPS

Closed-Loop Buck SMPS

In a Buck SMPS closed-loop operation is required to achieve the desired regulation performance. Indeed, the goal of a voltage regulator design is to realize a system whose behavior is as close as possible to an ideal voltage-controlled voltage source, with the highest power efficiency and highest immunity against input and output disturbances. This is obtained again by regulating the duty-cycle of the PWM waveform on the basis of the difference between the reference and the output signals, suitably amplified. In most voltage-mode regulators the loop gain is provided by an operational amplifier, as shown in Figure 1.20.

Chapter 2

Digital Control of Switching-Mode Systems

Power electronics for consumer applications represents a typical example of engineering tradeoff among costs, performance, system complexity, efficiency and robustness. In this context, the control circuits for SMPS and class-D amplifiers have been traditionally achieved through analog techniques with dedicated integrated circuits (ICs). Analog compensation is well known among power electronics engineers and provides the designer with an excellent tool for maximizing the performance/cost ratio. However, as switching-systems are becoming increasingly complex and often composed of smaller interacting units, the classical concept of control has gradually evolved into the more general problem of subsystems management, used to increase the performance and the efficiency. Besides the basic control function, a number of additional features are often required, such as smart power management for increasing the efficiency of a SMPS system depending to the load, or control of the output dynamics of class-D amplifiers, in order to improve the linearity and reduce the power consumption. These control circuits often allow a certain degree of programmability of the compensation characteristics. Implementing the control circuits in the digital domain could potentially meet the aforementioned requirements very effectively, due to the versatility and programmability inherent in the digital approach. On the other hand, a digital controller finds its major weakness in the achievable closed-loop dynamic performance. The time required for A/D conversion, the computational delays, and the sampling-related delays strongly limit the small-signal closed-loop bandwidth of a digitally controlled SMPS or class-D amplifier. For a digital class-D amplifier, in addition to the time considerations, A/D conversion linearity and resolution are of paramount importance, leading to system complexity. For these reasons, intensive scientific research activity is addressing the problem of making digital controller stronger competitors against their analog counterparts in terms of achievable performance.

After reviewing in Chapter 1 the general features and performance of switching-mode systems, in Chapter 2 we will focus on the implementation of digital control in such systems. We will firstly discuss some typical SMPS architectures with analog control from a system-level point of view. Then some digital control implementation will be

illustrated and, finally, we will describe the realized digital Buck SMPS. Likewise, for class-D amplifiers, we will describe introduce basic analog and digital solutions before describing the designed prototype.

2.1   Analog Control of SMPS Regulators

As mentioned in Chapter 1, closed-loop regulators require a control circuit, which has to monitor the output voltage, change the operating mode according to the load current, and in general optimize the efficiency. In commercial low-power SMPS, on-chip integrated analog controllers are mostly used. Low-cost, high-efficiency, design simplicity, and a relatively good dynamic response are the main reasons for their popularity. In this section, two of the most common analog solutions are reviewed.

2.1.1   PWM Voltage-Mode Controllers

Voltage-mode compensation is the most straightforward control strategy used to maintain the output voltage at the desired value. The PWM signal is generated using the voltage feedback information only (i. e. the difference between output and reference voltage). Because of their simplicity, Voltage-Mode Controllers (VCM) are the dominant solution in low-power low-cost systems. The controllers are used in miniature battery powered devices and are also widely employed in higher power systems that are produced in large volumes.

A typical VCM implementation is shown in Figure 2.1. It consists of two main blocks: a pulse-width modulator and a combined compensator subtraction network. The modulator consists of a comparator and a sawtooth waveform generator. The PWM comparator compares the sawtooth waveform (whose frequency is equal to the switching frequency) with error voltage. The modulator gain depends on the sawtooth peak-to-peak amplitude. The comparator provides a constant-frequency, variable-pulse-width signal that drives the power stage. The whole control circuit structure is very simple and cost effective, since it can be implemented with just two operational amplifiers, two comparators (an additional amplifier and a comparator are needed for the sawtooth generator), and few passive components.

The circuit of Figure 2.1 is based on a typical type-III/lead-lag compensation network, which offers good voltage regulation in steady state and fast dynamic response. However, in the analog implementation it is difficult to control the compensator transfer function [2], i. e. the compensator control law. The law depends on the values of a large number of resistors and capacitors, which have tolerances, change with temperature, and are influenced by aging. Because of these considerations a slower compensator ensuring system stability for all operating conditions is typically used [3] and the control bandwidth is usually limited. Consequently, the LC components of the power stage are over designed, to reduce the magnitude of the output voltage deviations.
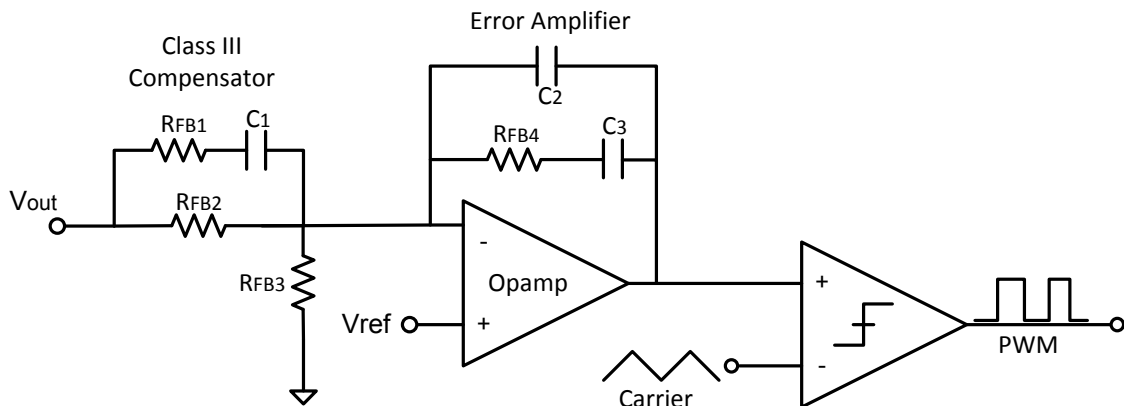
Figure 2.1: Typical analog voltage-mode PWM controller

2.1.2 PWM Current-Mode Controllers

Current-Mode Control (CMC) architectures may help to realize voltage regulators with good dynamic performance when the input supply voltage is susceptible to fast and sharp transient variations. Figure 2.2 shows the block diagram of a CMC Buck regulator.

While in a VMC regulator a sawtooth waveform, separately generated, is compared with the error voltage, in a CMC regulator the inductor current is converted to a voltage signal and replaces the sawtooth waveform. Therefore, the CMC involves two loops. An inner loop, realizing a form of feed-forward, and an outer voltage loop, realizing a classical output voltage feedback. Nowadays, the most popular type of CMC is the so called peak-current-mode control. In peak CMC, the high-side switch is turned-off when the inductor current reaches a threshold level, determined by the difference between the control signal (provided by the voltage error amplifier from feedback loop) and a compensation ramp signal. Without entering in details, the compensation ramp is necessary to avoid sub-harmonic oscillations in applications requiring duty-cycle values higher than 0.5.

The first advantage of CMCs is that the control-to-output transfer function has a single pole at low frequency, since the inductor is controlled by the current loop. This improves the phase margin and requires only first-order compensation circuits. Secondly, since the inductor current rises with a slope determined by the difference between the input and output voltages, the regulator immediately responds to line variations. On the other hand, the main disadvantages are the large susceptibility to switching node noise and the cost represented by the additional power dissipation of the current sensing circuit.

2.2 Digital Control of SMPS Regulators

The rapid advances in CMOS and VLSI technology have enabled the development of high-performance, practical, cost-effective, and low-power digital SMPS controllers [4]. Figure 2.3 shows the block diagram of an advanced digital controller that closes the feed-
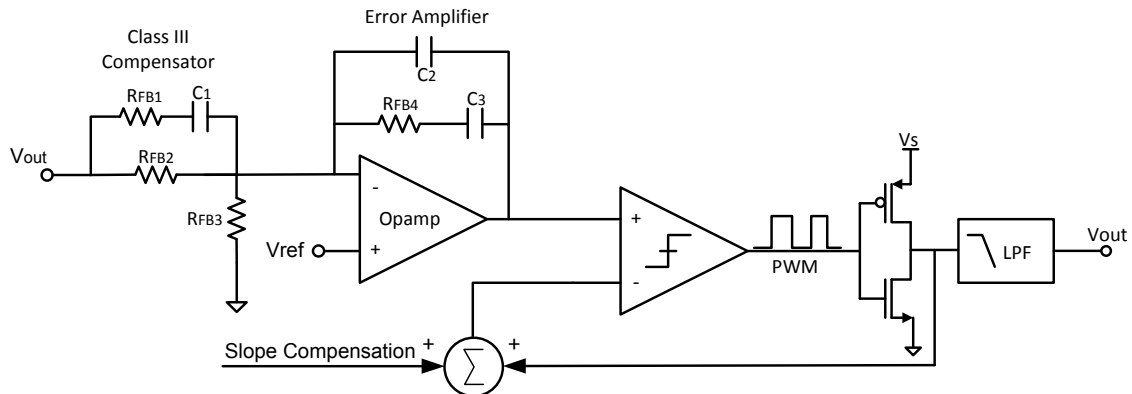
Figure 2.2: Block diagram of a current-mode PWM controller

back loop around a SMPS.

In a digital control loop one or more state variables are sampled and quantized by means of A/D Converters (ADCs). Adequate signal sensing and analog conditioning circuitry is usually required before the A/D conversion. The discretized information is processed by the digital compensator through its control algorithm, which calculates the discrete-time control signal $D[n]$ on a sampling cycle basis. As in analog control schemes, the PWM modulator plays a key role in interfacing the control system to the switching converter. In a digitally controlled power converter, the Digital Pulse-Width Modulator (DPWM) acts as a D/A Converter (DAC), as its function is to translate the digital sequence $D[n]$, produced by the compensator, in an analog PWM signal $D(t)$ suitable for driving the SMPS power switches. Since modern power switches require large sourcing/sinking current capability from the gate signal during the switching transitions, gate drivers are usually present as an interface between the DPWM and the power converter. The function of the gate drivers is to enhance the driving capabilities of the PWM signal $D(t)$ by increasing its power level, as well as to perform proper voltage level conversion. Beside its control function, the digital system may include diagnostics, communication, and self-tuning capabilities. The result is that a digital controller not only regulates the output voltage, but can also perform complex sequencing and can monitor key parameters, like average current and power for the host system.

2.2.1 Basic Digital Control

In the scheme shown in Figure 2.3, three specific blocks are of paramount importance to achieve the high regulation performance required: the ADC, to sample the error voltage (and an associated set-point reference DAC), the digital filter to compensate the feedback loop (i. e. Compensator), and the Digital Pulse-Width Modulator (DPWM) to generate the gate-drive signals.
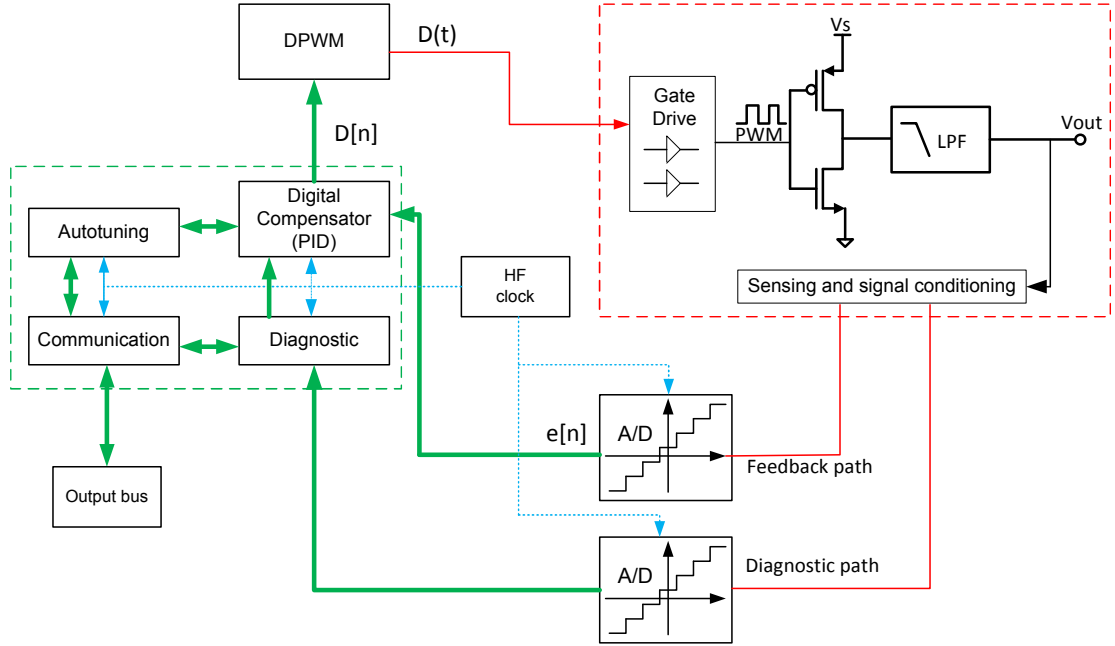
Figure 2.3: Digital controller for a Buck SMPS

A/D Converter (ADC)

The sampling and quantization of the DC-DC converter state variables, once sensing and conditioning is performed, serves the purpose of both providing feedback signals for the compensator and the necessary monitoring function for other features of the digital system, like diagnostics or auto-tuning. From a system-level point of view, there are two main aspects to be considered in selecting the A/D converter, namely its resolution n_{AD} (i. e. the length of the output binary word) and its conversion time Δt_{AD}. The ADC resolution can be selected once the Dynamic Range (*DR*) required for the sampled signal in the digital domain is known. For an input signal uniformly distributed between 0 and a the resulting Signal-to-Noise Ratio (*SNR*) is:

$$SNR\ [dB] = 6.02 \cdot n_{AD} - log_{10}\left(\frac{FSR}{a}\right), \tag{2.1}$$

where FSR is the Full-Scale Range. From the condition $SNR > DR$ the required ADC resolution is found.

Digitally controlled SMPS usually require high conversion rate ADCs in spite of the relatively low sampling rate of the converter state variables, which may be equal to the switching frequency or few times higher. In fact, the A/D conversion time Δt_{AD} is of extreme importance when the ADC is operated within a feedback loop, as any delay time translates into a phase lag that limits the achievable closed-loop bandwidth:

$$\Delta\phi_{AD}(f) = -2\pi f \Delta t_{AD}. \tag{2.2}$$

The term of comparison is represented by the converter switching period T_S, as discussed for gate driving delays: at a given closed=loop bandwidth f_C, defined as some fraction α of the converter switching frequency f_S, evaluation of (2.2) yields:

$$\Delta\phi_{AD}(f_C) = -2\pi\alpha f \frac{\Delta t_{AD}}{T_S}. \tag{2.3}$$

Negligible values of $\Delta\phi_{AD}(f_C)$ are achieved for conversion rates in the order of tens of mega-samples per second.

Beside these system-level discussions, additional application-specific considerations have to be made in order to identify the most suitable A/D converter. In fully-integrated digital controllers the use of area efficient ADCs is usually mandatory. Power consumption is also of primary concern especially in portable applications and it limits both the ADC sampling rate and the ADC resolution.

Digital Pulse-Width Modulator (DPWM)

In any digital control scheme, a control algorithm or control law is employed to process data sampled from the analog plant and produce the discrete-time control signal $D[n]$ used to achieve the desired control action. In pulse-width modulated SMPS this action is obtained by modulating the duty-cycle of the power switch driving signal. Thus, $D[n]$ inherently represents the desired duty-cycle value. However, the information carried by $D[n]$ has to be delivered to the power converter switches as an on/off signal $D(t)$. The DPWM thus acts as the necessary interface between the digital compensator and the power converter.

Strictly speaking, the DPWM performs a D/A conversion from the digital input $D[n]$ to the modulated analog waveform $D(t)$. It is characterized by its resolution, i. e. the number of bits n_{DA} of the input digital word. Each of the possible $2^{n_{DA}}$ values of the digital input is mapped by the DPWM to a unique duty-cycle value. Thus, once the switching period is specified, a time quantization can be associated to a particular DPWM:

$$\Delta q_{t,DA} = \frac{T_S}{2^{n_{DA}}}, \tag{2.4}$$

which represents the smallest turn-on time variation that the DPWM is able to generate. High-resolution, high-frequency DPWMs are required to achieve high-bandwidth, precise voltage regulation in digitally-controlled switching converters. Although dithering or sigma-delta modulation approaches can be applied to improve the effective DPWM resolution to some extent, it is very desirable to achieve high-hardware resolution using relatively minimal hardware resources. As in the case of ADCs, the choice of a particular DPWM architecture in an integrated digital controller is affected by both area and power consumption constraints. An interesting survey of DPWM architectures and trade-offs among resolution, silicon area, and power consumption is reported in [5].

Digital Compensator

In both analog and digital control of SMPS the compensator objective is to perform a signal processing function on the sensed converter state variables, in order to produce a control action on the plant. The basic operation of a digital compensator works on a sampling-cycle basis, starting from the acquisition of an input digital sample $e[n]$ (often recognized as the error between the regulated variable and the control set-point) and terminating with the computed digital control sample $D[n]$, available after a certain computational delay Δt_{calc}, which depends on the control law complexity as well as on its hardware implementation.

Linear control laws represent the most important class of signal processing functions employed in digital control of SMPS. They relate $D[n]$ to $e[n]$ by means of a linear, constant coefficients difference equation of the type:

$$D[n] = -\sum_{i=1}^{N} a_i D[n-i] + \sum_{j=0}^{M} b_j e[n-j], \quad M \leq N. \tag{2.5}$$

Control laws of this type are of particular importance because they simply involve additions and multiplications. These operations are readily available in micro-controller or DSP-based platforms, or can be implemented as hardwired logic in an integrated digital controller using standard adder and multiplier blocks. Equation (2.5) includes the important sub-class of Proportional-Integral-Derivative (PID) digital compensators, described by [6]. Nonlinear control actions can also be performed [7], generally aimed to achieve better dynamic performance in closed-loop operation. These may include anti-windup provisions, as well as nonlinear proportional and integral actions.

More generally, a digital compensator presents programmability and versatility features not usually found in analog control, that allow different control laws to be implemented and adopted as a function of particular boundary conditions, opening the possibility of intelligent control strategies. A typical example has been proposed in [8], where efficiency maximization in a low-power application was obtained by changing the control strategy when switching from heavy-load to light-load conditions and viceversa. For these reasons, the action of a digital compensator can be better described by a control algorithm rather than by a simple linear or non-linear signal processing operation.

Diagnostics, Communication and Auto-Tuning

Beside the control function, a digital SMPS may be provided with a number of features aimed to enhance the robustness of the power conversion, as well as its integration and interfacing capabilities with the surrounding world.

Diagnostic functions are common in high-reliability applications. Examples are given by distributed power systems for server applications, aircraft and spacecraft power systems and military applications. The need for high-reliability always requires fault detection features, if not fault prediction capabilities. Diagnostics is the set of monitoring
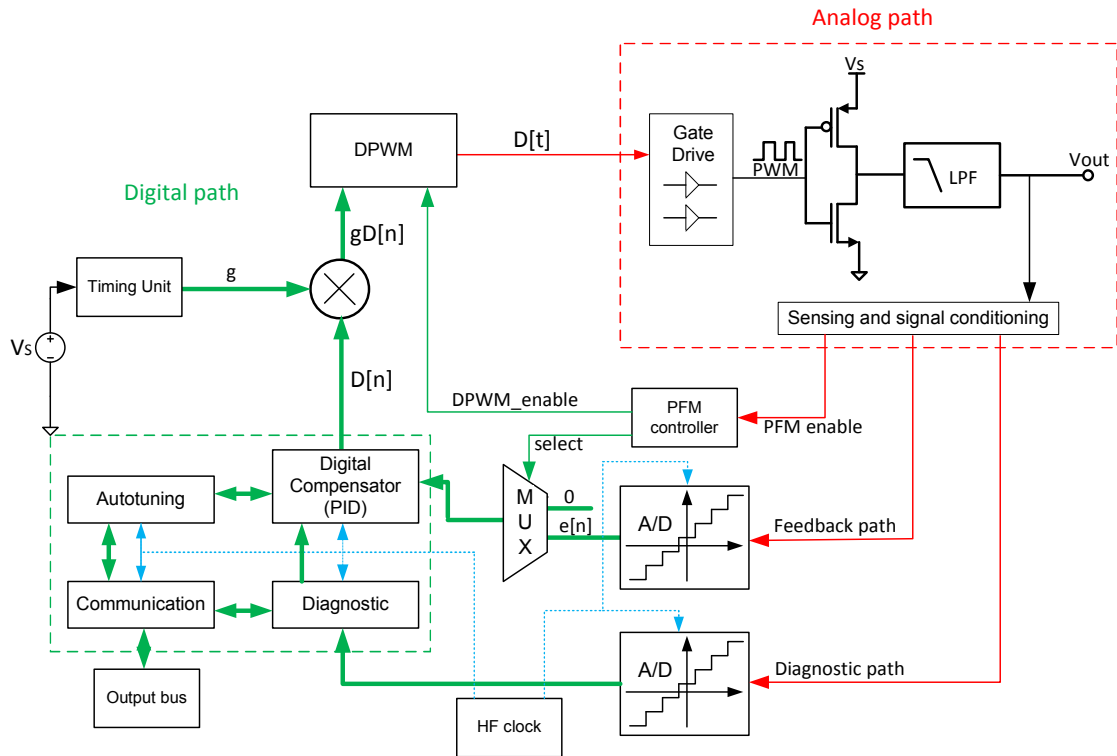
Figure 2.4: Improvements in the digital controller for a Buck SMPS

activities aimed to periodically check the health of the power system and, eventually, activate signaling mechanisms when the onset of critical situations is detected.

Communication functions allow the digital SMPS to interact with the surrounding world, exchanging information about the converter status, as well as receiving commands and programming instructions. Whenever a centralized diagnostic monitor is present in a distributed power system, communication buses allow the collection of health information of different sub-systems. In some cases the communication may occur between the converter and the load, as it happens between modern microprocessors and VRM modules.

Auto-tuning is a feature that allows a digital SMPS to automatically tune its digital compensator parameters. This function is one of the most interesting possibilities offered by digital techniques and allows for great performance optimization. Beside optimizing the SMPS control from a dynamic point of view, by determining the most suitable compensator for a given power plant, self-tuning features greatly enhance the versatility of a digital control system and its robustness with respect to process parametric variations, these being well known weak points in conventional analog controllers.

However, low-cost and low-control complexity requirements dictated by the market of consumer applications make these provisions by no means widespread.

2.2.2 Improved Digital Control

In addition to the functions previously described, several solutions are adopted to increase the efficiency and improve the control strategy in digital SMPS. Figure 2.4 summarizes two of the most important improvements:
- PWM/PFM control;
- input voltage feedforward.

Digital PWM/PFM Controller

From Figure 1.14 the AC losses and quiescent operating power become increasing significant when the load scales downward. A PWM converter which is 95% efficient at full load is roughly 50% efficient at one percent of the full load. In portable applications, if the converter is used at full load only for a short time, the energy loss at light load becomes the dominant limitation on the battery life. Therefore, improving the efficiency at light load would become essential.

One control scheme which achieves high light load power efficiency is the Pulse-Frequency-Modulation (PFM), with this control strategy the converter operates only in short bursts at light load. The PFM mode can be implemented with single-burst per cycle or multiple-bursts per switching cycle. Between bursts, both power MOSFETs are turned off and the circuit idles with zero inductor current. Then, the output filter capacitor sources the load current. When the output is discharged to a certain threshold below a reference voltage, the converter is activated for another burst, returning charge to the output capacitor. Therefore, the load-independent losses in the circuit are reduced and the light-load power efficiency is sustained. As the load current decreases, the idle time increases. Thus, regulation is achieved when the charge delivered through the inductor is equal to the charge consumed by the load.

To change the operating mode from PWM to PFM, the system needs to sense when the inductor current becomes zero. This can be achieved by measuring the voltage drop across the on-resistance of the NMOS power switch when it switches on, as shown in Figure 2.5. When the signal PFM_{enable} is activated the system switches to PFM mode, setting the PID error $e[n]$ to zero, and shutting down the PWM generator.

Such technique is also widely available in "multi-mode" analog controllers (e.g. [9]), where the mode of operation (e. g. PWM or PFM) depends on the load and it is automatically switched. Digital multi-mode control techniques have recently received increased attention. For example, it has been shown that custom digital multi-mode integrated circuits (ICs) can achieve very low light-load power consumption [10]. In addition, digital realizations open possibilities for further efficiency improvements through on-line efficiency optimization, or predictive control of segmented power stages [10].

Input Voltage Feedforward

A technique to increase the benefit of PFM modulation is to introduce an Input Voltage Feedforward (IVFF). The IVFF improves the rejection of input voltage disturbances and
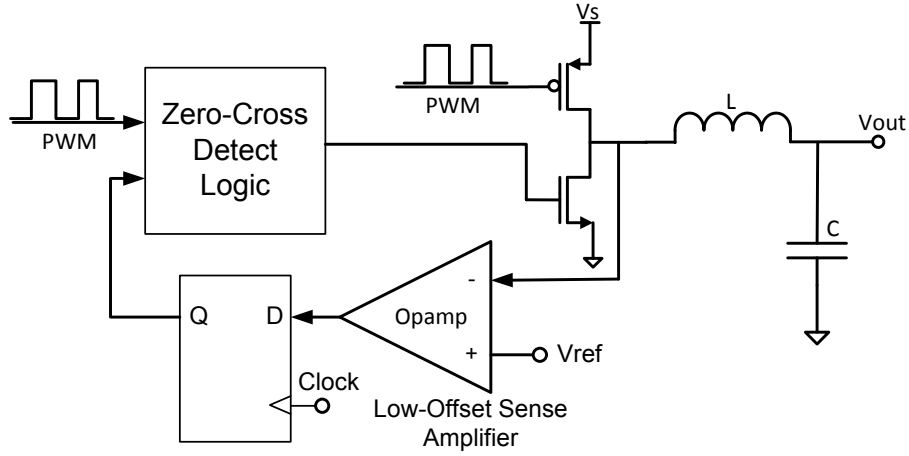
Figure 2.5: Inductor current zero-cross detection with micro-power low-offset operational amplifier

the dynamic response of the voltage control loop, since the loop gain becomes independent of the input voltage.

The PFM techniques operate well for a fixed input voltage V_S, but not over a wide range of input voltages. For example, if V_S changes when in PFM mode, the T_{on} and T_{off} timing based on D previously obtained in PWM mode becomes incorrect, reducing the efficiency. The IVFF proposed in [9] is shown in Figure 2.4: the phase command $D[n]$ from the PID compensator is multiplied by a feedforward gain g, in order to adjust the DPWM duty-cycle. A simple, single-comparator counter ADC, shown in Figure 2.6, senses the input voltage to generate the digital signal g. A current proportional to V_S charges a capacitor to a fixed threshold voltage V_{REF} and the required time T_C is measured by a counter. The counter output g is then proportional to $V_{S,NOM}/V_S$:

$$g = \frac{T_C}{T_S} = \frac{RCV_{REF}}{T_S V_S} = \frac{V_{S,NOM}}{V_S}, \tag{2.6}$$

where $V_{S,NOM}$ is the nominal input voltage (typically in the middle of the input voltage range) and T_S is the nominal switching period. Signal g is the IVFF gain that scales the duty-cycle command $D[n]$, as shown in Figure 2.4. In addition to properly adjusting T_{on} and T_{off} in PFM mode, the benefits of IVFF include improved dynamic performance [9].

2.3 Implemented Digital SMPS

Tho verify the potential of digital control in SMPS, we developed a 1-A, 6.4-MHz switching frequency DC-DC converter with embedded digital controller, implemented in 65-nm CMOS technology. The proposed DC-DC converter, exploiting a customized, multi-function SAR ADC (described in detail in Chapter 3) and a non-linear PID controller, can
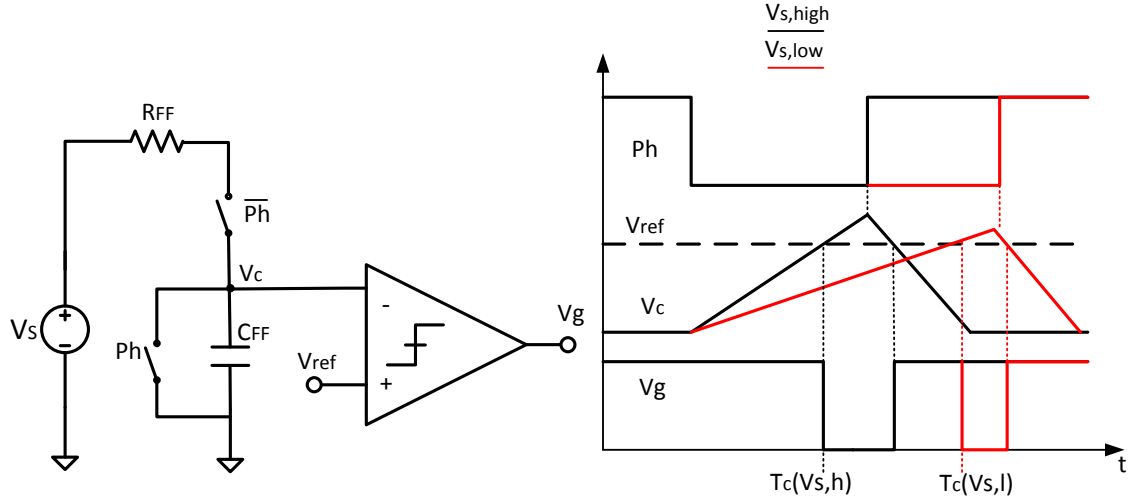
Figure 2.6: Operation of the counter ADC for input voltage feedforward (IVFF)

switch automatically between Continuous-Conduction Mode (CCM) and Pulse-Skipping (PSK), thus maintaining a fairly large efficiency also for light loads. Moreover, a feed-forward path in the digital control loop, implemented using the SAR ADC for converting also the battery voltage V_{BAT}, significantly improves the line transient performance. Other solutions presented in the literature, such as [9], which exploit the information on V_{BAT}, include an additional dedicated ADC for this purpose, that requires extra area and power consumption.

The development of the proposed device is based on "real-life" specifications of an SMPS for portable application, and, therefore, it does not focus solely on transient performance optimization, as most of the other digital SMPS ICs described in the literature. Indeed, the proposed SMPS involves a complete optimization of the system, including support for a wide range of power supplies (thanks to the V_{BAT} feedforward), introduction of a digital variable reference, and automated-mode switching between PSK and CCM. All these features are available (for the controller part) with a silicon area almost one order of magnitude smaller than the state-of-the-art.

2.3.1 Architecture

Figure 2.7 shows a simplified block diagram of the proposed digital SMPS, showing both CCM and PSK mode control loops, while Figure 2.8 shows a simplified timing diagram for the system operating in CCM. A single 7-bit SAR ADC embedded in the system is used in time-sharing to digitize both V_{OUT} and V_{BAT} with different timings. The larger V_{OUT} bandwidth requires that V_{OUT} is digitized with a higher sampling frequency ($F_s = 6.4$ MHz). On the other hand, the lower V_{BAT} bandwidth allows us to digitize V_{BAT} at a data rate equal to $F_S/8 = 0.8$ MHz, thus reducing the ADC and clock generator power consumption of about 50% with respect to the case in which V_{BAT} is digitized with
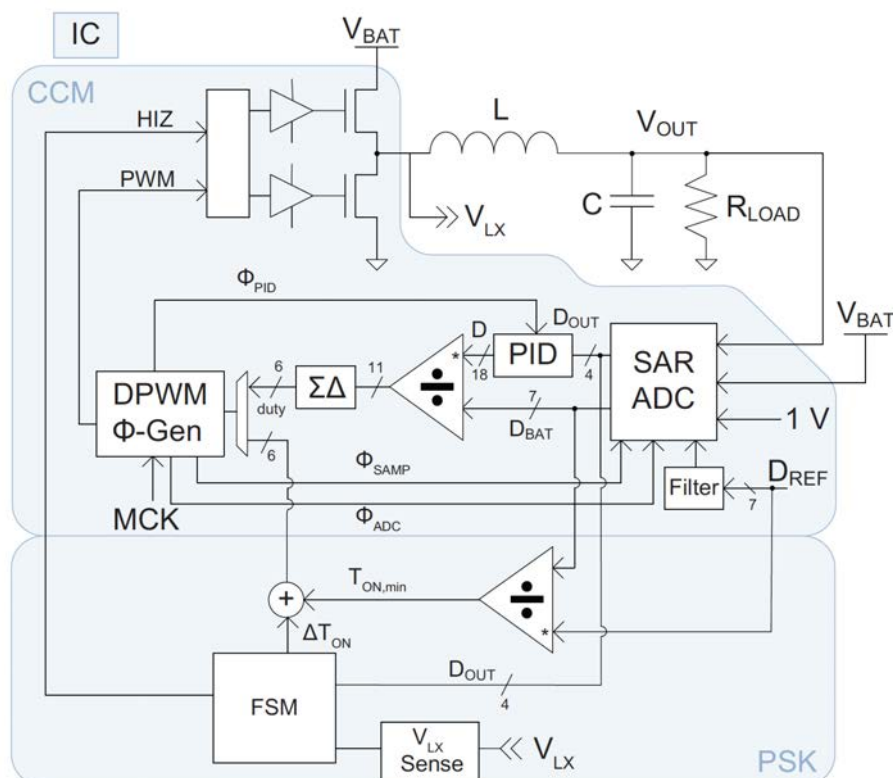
Figure 2.7: Simplified block diagram of the digital Buck SMPS

sampling rate equal to F_s, without degrading the system performance.

Continuous-Conduction Mode (CCM)

In CCM, a closed-loop mixed-signal system controls the output voltage (V_{OUT}). Bandwidth, stability, and accuracy are optimized by exploiting the 65-nm CMOS high-speed capability, for operating the digital SMPS with a 307.2-MHz master clock. The digital word representing V_{OUT} is subtracted from a 7-bit set-point (D_{REF} corresponding to the desired voltage level V_{REF}), to obtain a digital representation of the error $D_{OUT} \propto V_{REF} - V_{OUT}$. Reference D_{REF} is digitally filtered, to smooth the dynamic voltage scaling behavior. On the other hand, the digital word relative to V_{BAT} (D_{BAT}) allows the implementation of a feedforward path in the control-loop for optimizing the system response and stability. Both digital words are fed to a digital controller, whose block diagram is shown in Figure 2.9, including a non-linear PID and a divider, which calculate the next 11-bit duty-cycle value. A multi-bit $\Sigma\Delta$ modulator dithers the 11-bit signal into a 48-level signal (*duty*), coded on 6 bits, fed into a simple counter-based DPWM. This generates the 1-bit signal which drives the integrated power stage buffers, as well as the clock signals for the ADC and the PID controller. The DPWM and clock generator consists of a sim-
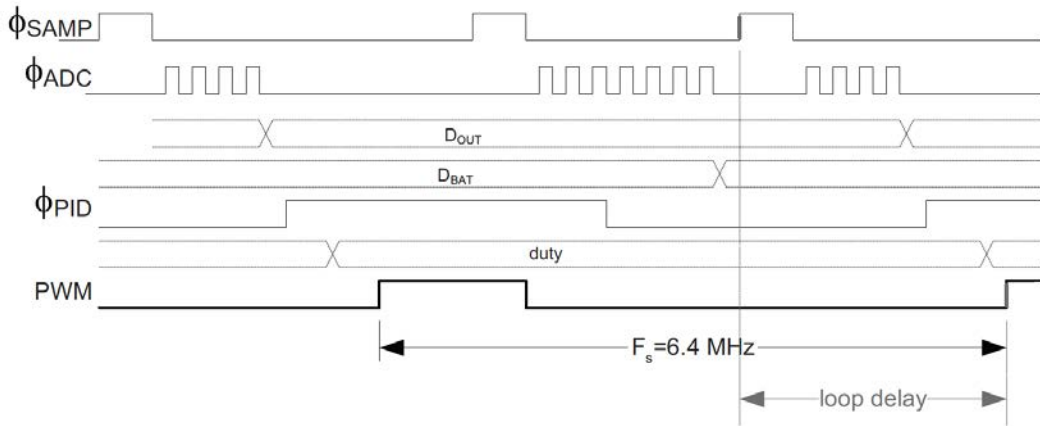
Figure 2.8: Simplified timing diagram of the digital Buck SMPS in CCM
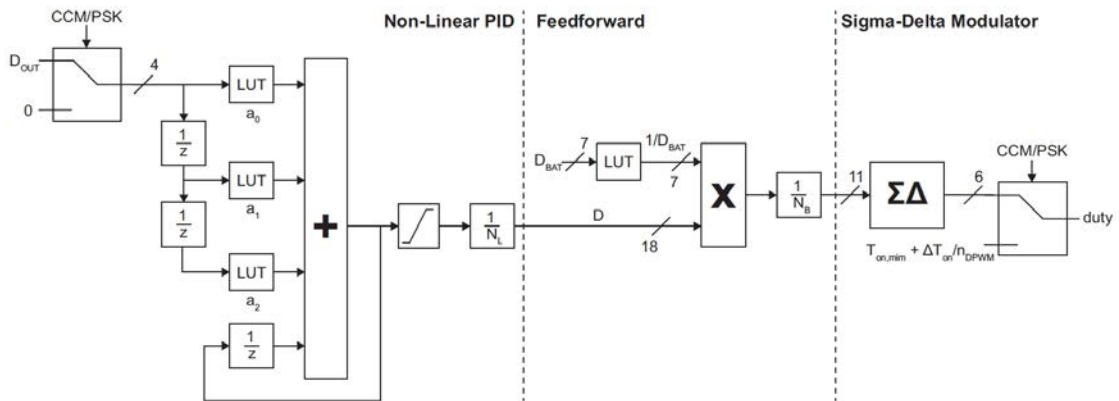
Figure 2.9: Block diagram of the digital controller

ple 48-level ripple-counter operated at 307.2 MHz. From the counter output (*counter*), several signals are obtained:

- the PWM signal, which is rising to "1" when *counter* = 0 and falling back to "0" when *counter* = *duty*;
- the SAR ADC conversion clock (ϕ_{ADD}), obtained by gating with the counter the 307.2 MHz clock divided by 2, so that ϕ_{ADC} is only present for 7 periods for V_{BAT} and 4 periods for V_{OUT};
- the SAR ADC sampling clock (ϕ_{SAMP}), directly generated from *counter*.

An additional 5-bit counter operated at 6.4 MHz (307.2/48 MHz) is gating the V_{BAT} related clocks (ϕ_{ADD} and ϕ_{SAMP}), allowing the V_{BAT} sampling frequency to range from F_s (i. e. the same rate as V_{OUT}) to $F_s/32$.
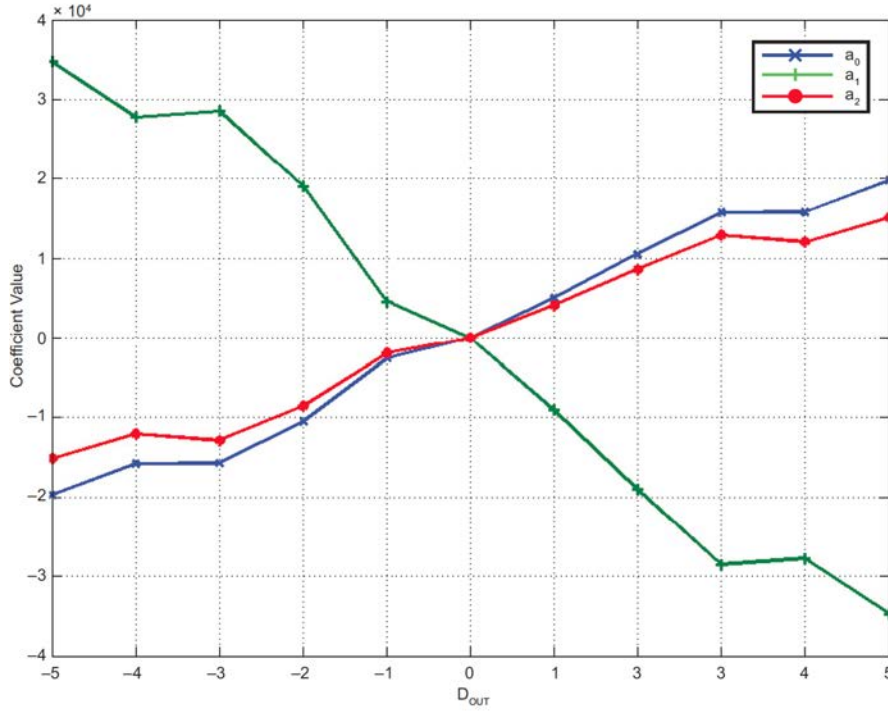
Figure 2.10: Digital controller coefficient values as a function of the error signal

The PID controller implements the classical discrete-time transfer function:

$$\frac{D(z)}{D_{OUT}(z)} = \frac{a_2 z^2 + a_1 z + a_0}{z(z-1)}, \tag{2.7}$$

where $D_{OUT}(z)$ is the signal coming from the ADC, coded with four signed bits, and $D(z)$ is the duty-cycle, coded with 18 bits, as required to avoid saturation. As proposed in [11], coefficients a_0, a_1, and a_2 are implemented as lookup tables (LUTs). The coefficients depend on the value of D_{OUT}, thus making the response non-linear and allowing a faster transient response, while maintaining stability. The coefficient values as a function of D_{OUT} are plotted in Figure 2.10. Unlike in [6], where coefficients are analytically chosen, the proposed approach starts from a manually-designed compensator, which is then fed into an optimization loop, aiming at minimizing the over-voltage and maximizing the phase margin, over the whole range of V_{BAT}, D_{REF}, transistor on-resistance (R_{on}), inductance (L), capacitance (C), and equivalent series resistance (ESR).

The feedforward path in the digital controller introduces an additional static term $1/V_{BAT}$ in the classical open-loop control-to-output transfer function of a Buck converter based on the "average" model, given by:

$$G(s) = \frac{\frac{V_{BAT}}{D_0}}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}}, \tag{2.8}$$

where D_0 is the steady-state duty-cycle, $\omega_0 = 1/\sqrt{LC}$ and $Q = R\sqrt{C/L}$, in which the DC gain is actually proportional to V_{BAT}. The additional term $1/V_{BAT}$, introduced by the feedforward path, effectively cancels this dependency and leads to a constant DC gain in the transfer function, thus allowing the use of a more aggressive compensation over the whole V_{BAT} range. It can also be shown that with such a scheme, at least at first order, $dV_{OUT}/dV_{BAT} = 0$ at DC. This is actually not completely true when second-order and quantization effects are considered, but it clearly shows the benefits of the feedforward path in the digital controller on the line regulation performance.

In order to preserve the phase margin, the digital SMPS must minimize the loop-delay, i. e. the time spent between sampling V_{OUT} and applying the correction to the system. To optimize this timing, a 153.6-MHz burst clock signal is used for the ADC, derived from the master clock, allowing a fixed latency. Moreover, as already mentioned, the calculations in the digital PID are done with mere lookup tables, adders and multipliers, only needing a single clock edge to determine the duty-cycle. The DPWM is sampling this result 16.2 ns later, in order to account for worst-case signal propagation in the control circuit.

Pulse-Skipping (PSK) Mode

The SMPS power stage and switching frequency are designed to offer maximum 85% efficiency at minimum drop-out for high currents, but this efficiency degrades very steeply when the load is such that the current in the inductance is inverting, adding extra losses to the already dominant switching losses. In order to alleviate this issue, a Pulse-Frequency Modulation (PFM) scheme can be used. A fixed-duration (fixed T_{on}) pulse is applied to the output stage, which then goes to high-impedance state until the output voltage drops below the set-point. An alternative solution is synchronizing the output voltage tracking with a clocked comparator [4]. However, while this scheme offers excellent efficiency performance, its reduced bandwidth, due to the lower clock frequency, makes it a good candidate only for dedicated ultra-low current modes, but it cannot be used for medium to low current modes (i. e. below critical conduction), where transient performance requirements are expected to be similar to CCM.

The solution implemented in the proposed SMPS, called Pulse-Skipping (PSK) mode, is a synchronized fixed-on-time (T_{on}) PFM scheme, which exploits the same ADC as in CCM to compare the output voltage with a digital set-point. In order to generate a value of T_{on} which minimizes losses, a digital adaptive scheme is used. An initial digital value $T_{on,min} = n_{DPWFM} \cdot D_{REF}/D_{BAT}$, where n_{DPWFM} is the number of DPWM levels, is calculated using look-up tables for fast and efficient implementation of the required division. The value of $T_{on,min}$ corresponds to the time required for the current to reach zero after a conduction period for a lossless power stage. Because of losses, the actual value of T_{on} will be necessarily larger. Therefore, at the end of each conduction cycle, a current sensing circuit detects if the inductance current is negative. If this is the case, T_{on} is increased by 1 LSB, until a positive inductance current is detected. After a conduction period, if the ADC detects that the output voltage is still below the set-point, another pulse

is generated, or, otherwise, the output stage goes in high-impedance state, until the output voltage drops again below the set-point.

Automatic Mode Switching

A key feature for a SMPS is the ability to automatically select the optimal operating mode for efficiency: if the load current (I_{LOAD}) is such that the current in the inductance (I_L) is inverting before the end of the switching period, PSK mode must be used, whereas CCM is required for higher values of I_{LOAD}. The transition between the operating modes is managed by the Finite-State Machine (FSM) shown in Figure 2.11. Two variables are used for choosing the operating mode: the output code of the SAR ADC ($\varepsilon = D_{OUT}$), which is a digital image of the output voltage error, and the digital signal $I_L[T_S]$, provided by the current sensing circuit, whose function is to sense whether the current in the inductance is positive or negative at the end of every conversion period. The current sensing circuit runs at the power stage frequency, using ϕ_{PID} as clock. The SMPS is starting in open-loop configuration, by progressively incrementing the internal value of the PID accumulator, while the saturated output of the ADC remains disconnected from the digital compensator. When the output voltage approaches the set-point ($\varepsilon < 3$), the output of the ADC is connected to the PID input and the system starts operating in closed-loop configuration, always in CCM mode. In order to avoid oscillation between modes, because of potential wrong decisions taken during transients, the FSM waits until $\varepsilon = 0$ for N_{PER} consecutive periods (i. e. the SMPS is in stable condition), before allowing entering PSK mode, if needed (in a low-load condition). Moreover, the decision to eventually enter PSK mode is taken when the inductance current is inverted ($I_L[T_S] < 0$) for N_{PER} consecutive periods. The value of N_{PER} is chosen so that the system is settled ($\varepsilon = 0$) in worst-case conditions.

The state "PSK – Open SW" corresponds to the situation in which both power transistors are open, leading to high impedance at node V_{LX}. When entering this state (always after a conduction period of the bottom power transistor), the value of $I_L[T_S]$ is detected and the value of T_{on} for the next conduction period is calculated. The state P"SK – Close SW" corresponds to a full conduction period, with duty-cycle given by $T_{on} = T_{on,min} + T_{on}$.

To be less sensitive to the offset of the current sensing circuit and provide hysteresis, the condition to quit PSK mode is based on the ADC output value: as long as the output voltage remains within 1 LSB around the set-point ($|\varepsilon| \leq 1$), the system stays in PSK mode, otherwise it switches back to CCM ($|\varepsilon| \geq 2$). In case of fast load transients, which create an important output voltage drop, the SMPS switches back at once to CCM and can quickly react to the transient. In case of slow increase of the load current, the system switches back to CCM only when needed. Indeed, if the load current is slightly larger than the maximum current that the system can supply in PSK mode, the output voltage slowly drops and reaches the condition $|\varepsilon| = 2$), for which it switches back to CCM.

A necessary condition for the FSM to be stable is that $(I_{DET})_{max} < I_{CRIT}$, where I_{DET} is the threshold value, for which the current sensing circuit detects that the inductance current is inverted, and I_{CRIT} is the critical output current (the steady-state output current for which the inductance current becomes negative during the conduction period). If
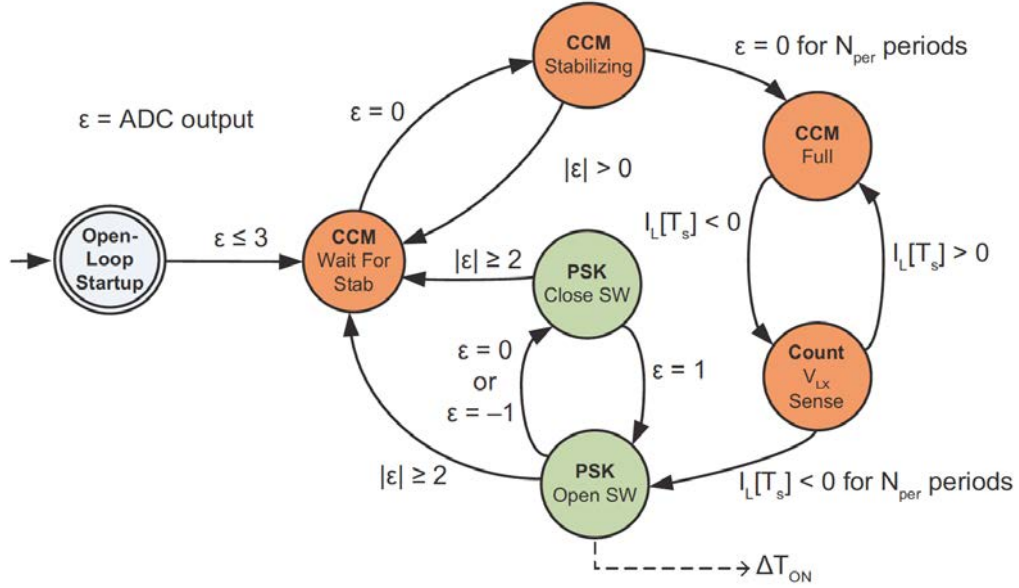
Figure 2.11: Simplified automatic-mode switching finite-state machine

$I_{DET} > I_{CRIT}$ and the output current I_{LOAD} is such that $I_{DET} > I_{LOAD} > I_{CRIT}$, the system will enter PSK mode, not being able to provide enough current. Therefore, the output voltage drops and the FSM continuously oscillates between the two modes. Although the transient and regulation characteristics of the SMPS are not affected by this situation, unwanted low frequency oscillations with period larger than $2 \cdot N_{PER}$ will occur.

In order to avoid this condition, an offset is added in the current sensing circuit, such that $I_{DET} < I_{CRIT}$, even for worst-case process variations. As a consequence of this offset, when $I_{CRIT} > I_{LOAD} > I_{DET}$, the system still remains in CCM, although the current in the inductance is inverting, as a result the efficiency slightly drops in this zone.

Current Sensing Circuit

The operating principle and the schematic of the current sensing circuit are shown in Figure 2.12 and Figure 2.13, respectively. The function of this circuit is to determine, at the end of each conduction period, whether the inductance current I_L is inverted and is flowing back to ground. This information is used in CCM, to determine if the system should switch to PSK mode, and in PSK mode, to evaluate if the applied T_{on} is too short.

The inductance current detection is performed indirectly, by sensing the voltage $V_{LX} = V(LX) - V(GNDP)$. As shown in Figure 2.12, if I_L is inverting before the end of the conduction period of transistor M_{BOT}, then voltage V_{LX} is becoming positive, because the current is now flowing from node V_{LX} to node GNDP. On the other hand, if I_L remains positive, the sign of voltage V_{LX} is not changing and V_{LX} remains negative. Moreover, since after M_{BOT} is turned off, either diode D_{TOP} or diode D_{BOT} is conducting, in both
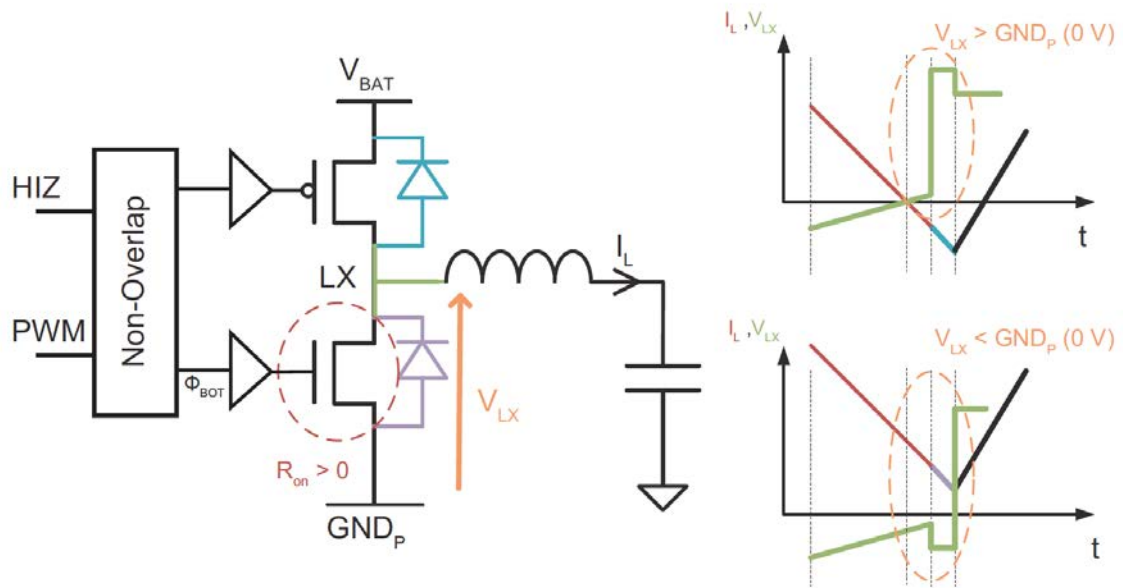
Figure 2.12: Operating principle of the current sensing circuit
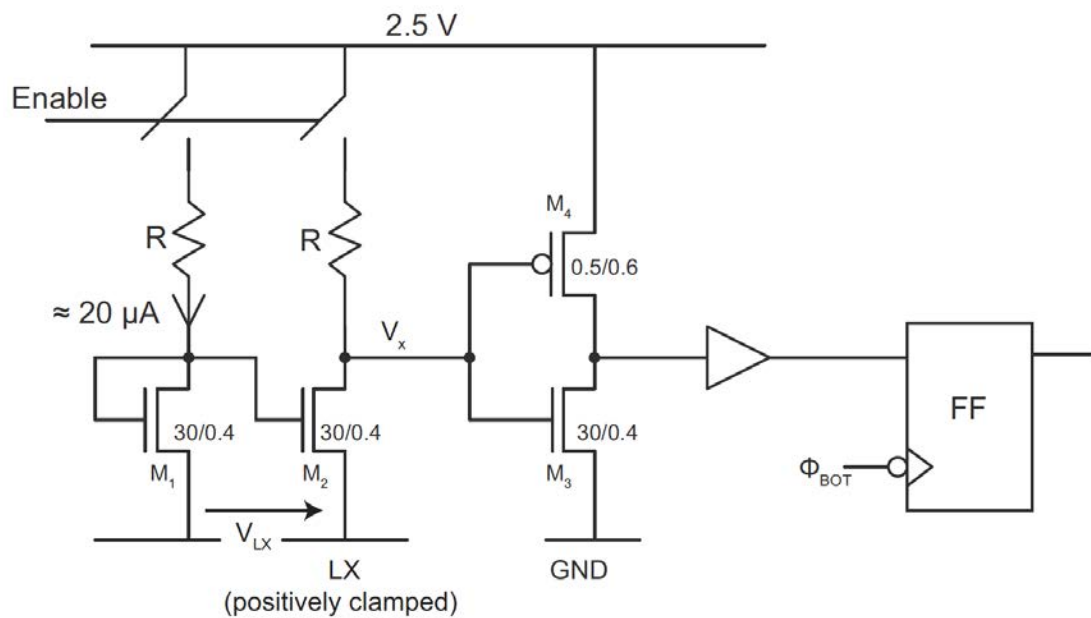
Figure 2.13: Schematic of the current sensing circuit

cases the sign of voltage V_{LX} is actually reinforced.

The sensing circuit shown in Figure 2.13 basically amplifies voltage V_{LX} ($V_{LX} = g_m R V_{LX}$, g_m being the transconductance of transistors M_1 and M_2), which is then further amplified by a chain of inverters and sampled by a flip-flop (FF) on the falling edge of the driving signal of M_{BOT}. Since the clock signal of the sampling flip-flop (ϕ_{BOT}) is then buffered to generate the driving signal of the power transistor itself, it is guaranteed that switching always occurs after sampling, thus not disturbing the measurement.

The drawback of this structure is that the PWM duty-cycle has to be such that conduction occurs in transistor M_{BOT} (i. e. the duty-cycle has to be lower than 95%, considering digital clamping). However, in actual portable applications, where the input voltage is provided by a battery and the output voltage is lower than 1.8 V, a duty-cycle value larger than 95% never occurs in steady-state.

The speed of decision impacts the precision of the threshold current I_{DET}, which is important to avoid oscillation between modes. Therefore, a fairly significant current ($\approx 20\ \mu$A) in each branch of the circuit shown in Figure 2.13 is required. However, the current sensing circuit is only activated during conduction periods and, therefore, its power consumption leads to less than 0.1% efficiency loss at the limit between PSK mode and CCM, while in PSK mode the average power consumption scales linearly with the output current, thus not impacting significantly the overall efficiency even for smaller currents.

2.3.2 Experimental Results

The proposed digital SMPS circuit has been fabricated in a 65-nm CMOS technology. Figure 2.14 shows a microphotograph of the chip. The load and line regulation measurements are illustrated in Figure 2.15. The achieved performance is limited by the ADC LSB (10 mV), as expected. Figure 2.16 and Figure 2.17 show the measured line and load transients, respectively. The line transient is significantly improved by the introduction of the feedforward path that can be implemented thanks to the availability of the information on V_{BAT}, guaranteed by the multi-function SAR ADC, which will be described in Chapter 3.

The behavior of the system during the automatic transition from CCM to PSK mode, resulting from a steep drop of I_{LOAD}, is illustrated in Figure 2.18. When I_{LOAD} drops, V_{OUT} rises, since there is an excess of charge, coming from the inductance, that cannot be evacuated by the load and, hence, accumulates on the capacitance ($C_L = 10\ \mu$F). When I_L has been detected to be steadily inverted, the system enters in the "PSK — Open SW" state, leaving the output in high-impedance condition, until V_{OUT} and, hence, the ADC output reaches the value ($\varepsilon = 1$, corresponding to $V_{OUT} = V_{REF} - 5$ mV) for which the normal PSK sequence starts.

The mode-transition overshoot, in this case, is around 25 mV. Figure 2.19 shows the automatic transition from PSK mode to CCM, resulting from a load current step of 400 mA. The system is leaving PSK mode when the output voltage drop is more than 15 mV ($|\varepsilon| \geq 2$) and the non-linear PID takes over. The resulting undershoot is limited to
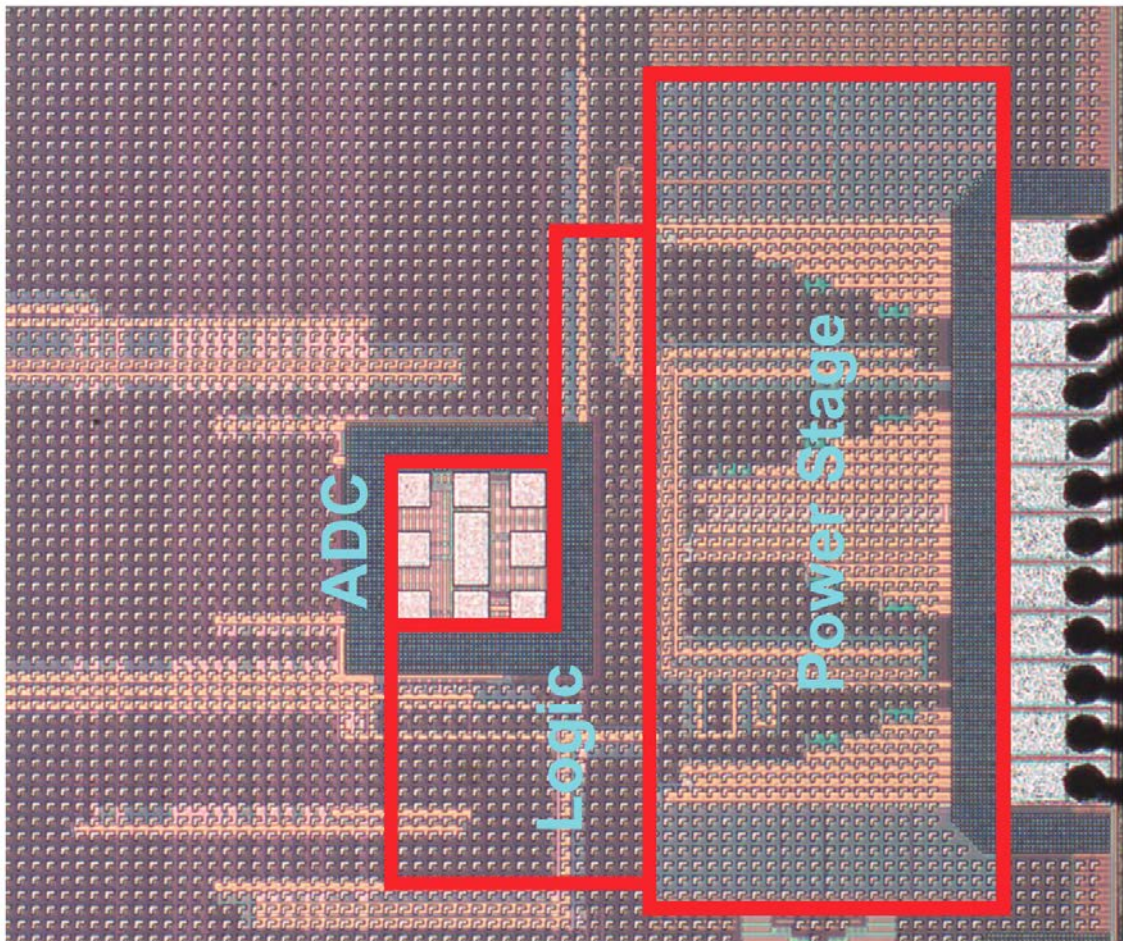
Figure 2.14: Microphotograph of the chip.
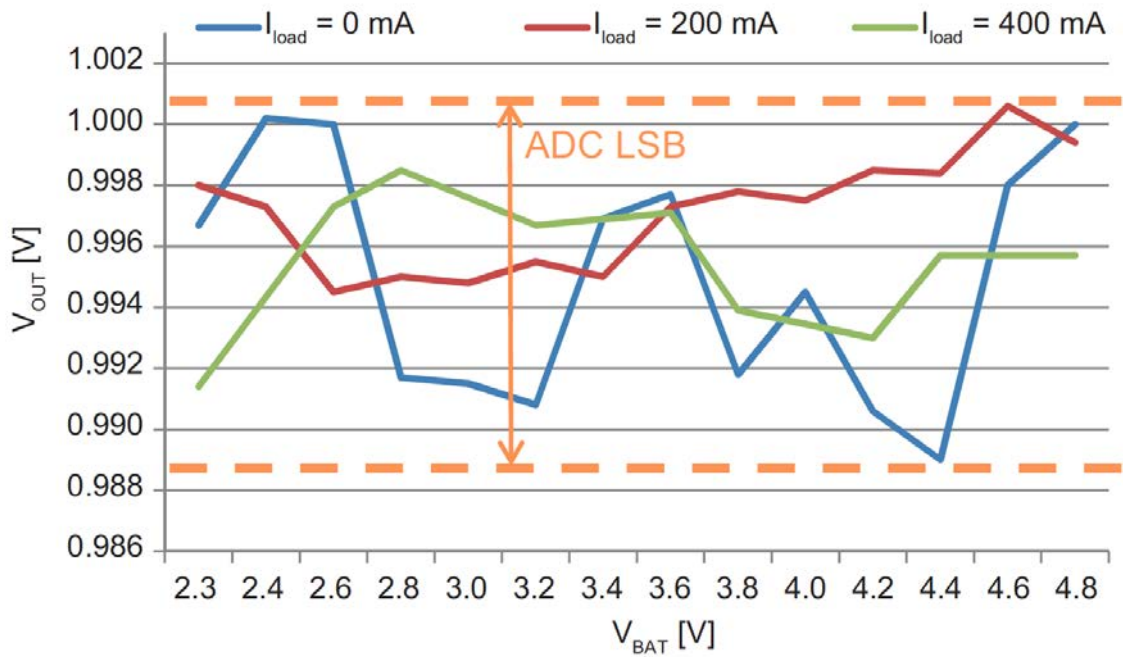
Figure 2.15: Line and load regulation measurement.
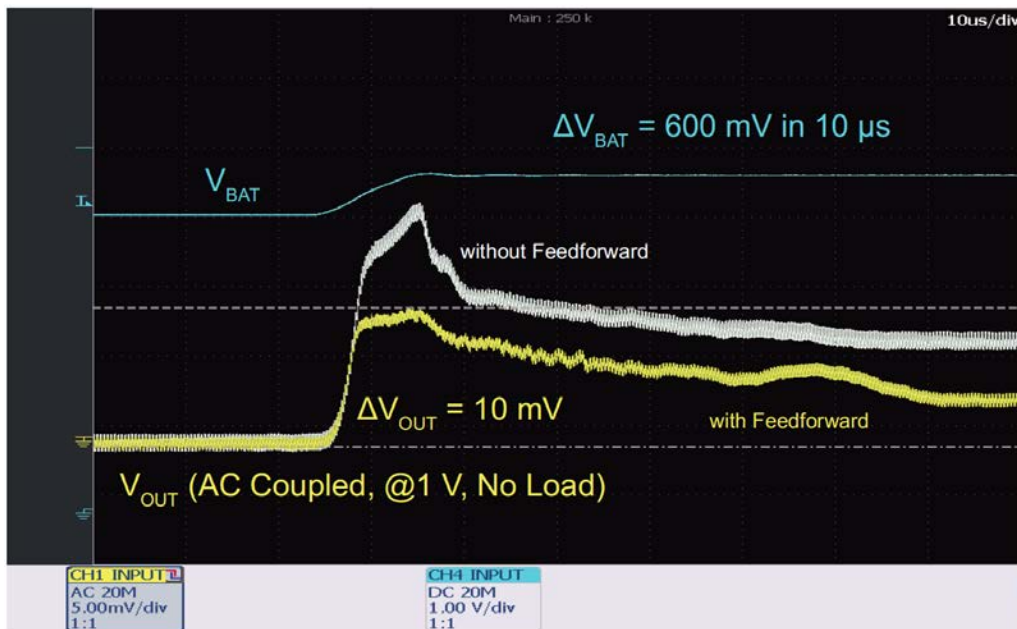
Figure 2.16: Line transient measurement
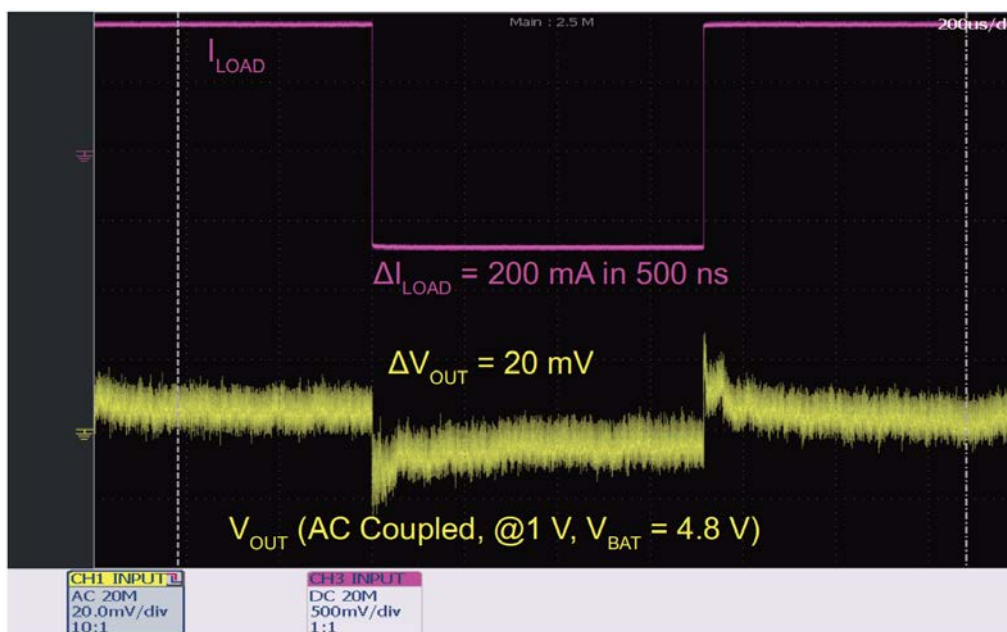
Figure 2.17: Load transient measurement

about 20 mV, in line with the load transient measurement shown in Figure 2.17.

Figure 2.20 shows the efficiency measurement. The maximum efficiency achieved, equal to 85%, is in line with expectations. This efficiency value could appear fairly low compared to [12] and [9], but the high switching frequency, with the associated switching losses, explains most of the difference. The high switching frequency, on the other hand, allows a small inductance value ($L = 470$ nH) to be used, which is important in portable applications. The automatic mode switching allows us to maintain the efficiency higher than 70% down to $I_{LOAD} = 5$ mA, while, considering CCM only, at $I_{LOAD} = 5$ mA the efficiency would be around 13%.

The main features of the proposed digital SMPS are summarized in Table 2.1 and compared with the state-of-the-art, [12–14]. The adopted system and circuit solutions achieve similar performance as [15], with smaller die area (1/3 factor) and lower power consumption (1/8 factor), while using a 6.4-MHz switching frequency, which allows the use of a small inductor, in line with the continuous trend of shrinking portable devices PCB sizes [14].

2.4 Analog Control of Class-D Amplifiers

As discussed in Chapter 1, switching-mode techniques can be used also to amplify an audio signal, trough the class-D amplifier. Audio signal amplification entails different problems and characteristics compared to the control of a voltage regulator. Performance optimization is not focused on efficiency and regulation, but on linearity and dynamic
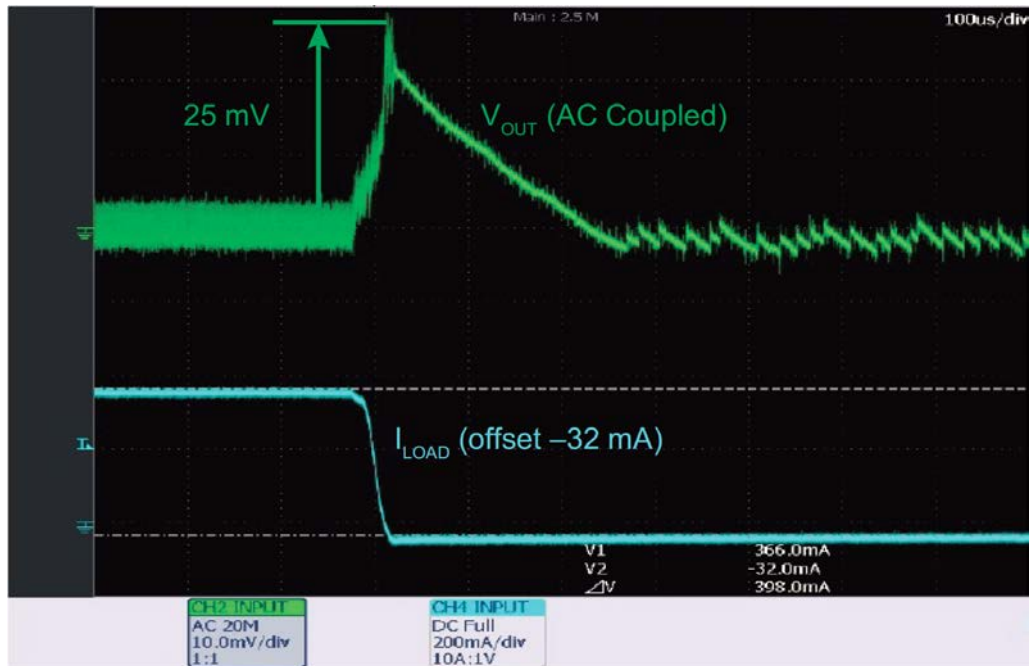
Figure 2.18: Transient measurement during automatic mode switching from CCM to PSK
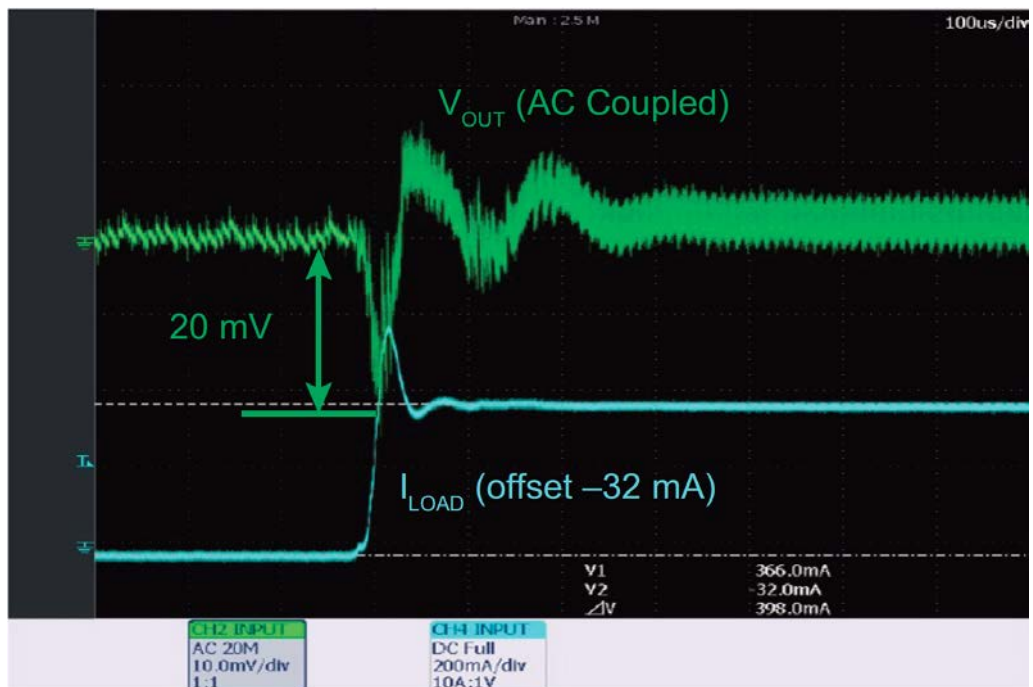
Figure 2.19: Transient measurement during automatic mode switching from PSK to CCM
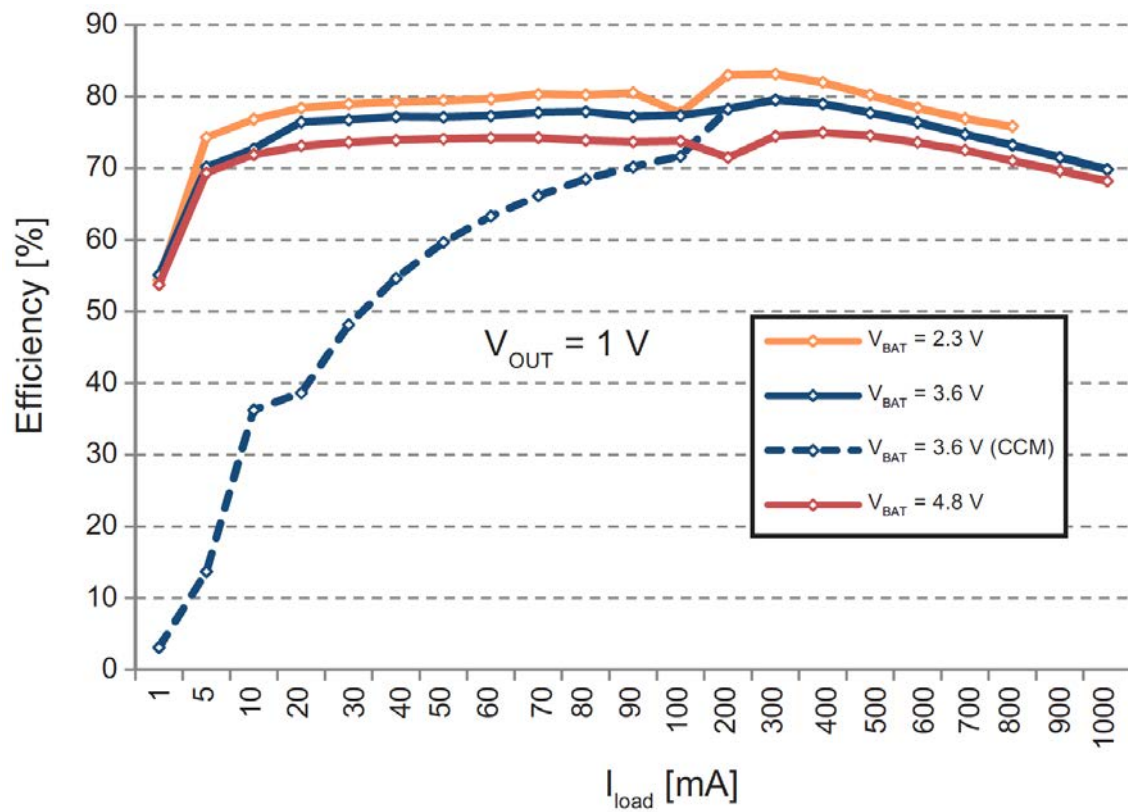
Figure 2.20: Efficiency measurement.

Table 2.1: Performance summary

Parameter	This Work	ISSCC 2010 [5]	ISSCC 2011 [9]5
Process	CMOS 65nm	CMOS 40nm	CMOS 45nm
Battery voltage	2.3 V ÷ 4.8 V	0 V ÷ 3.3 V	2.8 V ÷ 4.2 V
Output voltage	0.6 V ÷ 1.35 V	0.1 V ÷ 3.3 V	0.6 V ÷ 1.2 V
Output current	0 A ÷ 1 A	0.1 A ÷ 1 A	$20\,\mu$A ÷ 100 mA
Inductance	470 nH	$2.2\,\mu$H	$10\,\mu$H
Load capacitance	$10\,\mu$F	$10\,\mu$F	$2\,\mu$F
Line transient (V_{OUT} = 1 V)	10 mV ΔV_{BAT} = 600 mV	15 mV ΔV_{BAT} = 200 mV	–
Load transient (V_{OUT} = 1 V)	20 mV ΔI_{LOAD} = 200 mA	20 mV ΔI_{LOAD} = 250 mA	20 mV ΔI_{LOAD} = 40 mA
Line and load regulation (limited by ADC resolution)	≤ 10mV without limit cycles	≤ 1 mV with limit cycles	–
Switching frequency	6.4 MHz	3.125 MHz	–
Maximum efficiency	85%	90%	87%
Out ripple	≤ 10 mV	5 mV	10 mV
ADC power supply voltage	1.2 V	1.1 V	1.2 V
Active area (w/o power transistors) ADC DPWM + Phase generator PID + Control + $\Sigma\Delta$	0.038 mm^2 0.024 mm^2 0.0015 mm^2 0.0125 mm^2	0.1 mm^2 – – –	0.21 mm^2 – – –
Current consumption (w/o power transistors) ADC DPWM + Phase generator PID + Control + $\Sigma\Delta$	115.5 μA 18 μA 82.5 μA 15 μA	1.05 mA – – –	19 μA – – –

range. The best way to increase the class-D amplifier linearity is the use of feedback, as shown in Figure 1.19. Since a class-D amplifier is a very non-linear system, also with a feedback loop, the achievable THD values are not very impressive ($THD \approx 65 \div 70$ dB) and, hence, for a long time class-D amplifiers have been used in low-end applications only. Recently, a lot of research has been performed in order to find new solutions able to achieve the usual class-D high efficiency together with a linearity suitable for Hi-Fi applications. Many solutions have been tried in order to improve performance [16–18], but among all these attempts the best solution seems to be increasing the loop order [2,3], In fact, the higher is the loop order, the higher is the loop gain and, hence, the non-ideality attenuation. However, increasing the loop order increases also the circuit complexity and introduces critical stability issues. Therefore, a very well defined design methodology is needed for designing class-D amplifiers with loop order higher than two and, as usual, depending on the specifications, a trade-off between order, circuit complexity, and achievable linearity has to be considered.

2.4.1 High-Order Analog Class-D Amplifiers

In order to find stability criteria for high-order class-D amplifiers, we can start from a useful observation: a closed-loop class-D amplifier is quite similar to a Sigma-Delta ($\Sigma\Delta$) modulator. Both are based on a feedback loop with a number of integrators as large as their order, both contain a non-linear element (the PWM modulator in the class-D amplifier and the quantizer in the $\Sigma\Delta$ modulator), and both have zeros and poles introduced by feedback and feedforward paths. On the other hand, a class-D amplifier, using an analog PWM, is ideally able to represent an infinite number of levels by changing the duty-cycle of the carrier in each period, while a $\Sigma\Delta$ modulator, because of the quantizer, can represent only a finite number of states ("0" and "1" for a single-bit quantizer, with 50% duty-cycle), as summarized in Figure 2.21.

In other words, a class-D amplifier does not perform any quantization of the signal, unlike a $\Sigma\Delta$ modulator. In practice, the loop filter in a $\Sigma\Delta$ modulator suppresses the in-band quantization noise, whereas the loop filter in a class-D amplifier attenuates spurs and errors (mainly harmonic distortion), introduced by the PWM modulator and the power stage. For a given order, the linearized equivalent model of a $\Sigma\Delta$ modulator is the same as that of a class-D amplifier, as shown in Figure 2.22, where ε denotes the quantization error in a $\Sigma\Delta$ modulator or the PWM and power transistor bridge errors in a class-D amplifier. The output voltage V_{OUT} is given by:

$$V_{OUT} = V_{IN}\frac{H(s)}{1 + H(s)} + \varepsilon\frac{1}{1 + H(s)} \tag{2.9}$$

where, with a proper choice of $H(s)$, the contribution of ε can be attenuated as required, while leaving V_{IN} unchanged [19]. The higher is the order of $H(s)$, the higher is the attenuation of the spurs.

These concepts will be analyzed in Chapter 4 when we will introduce the $\Sigma\Delta$ ADC based on the noise-shaping theory.
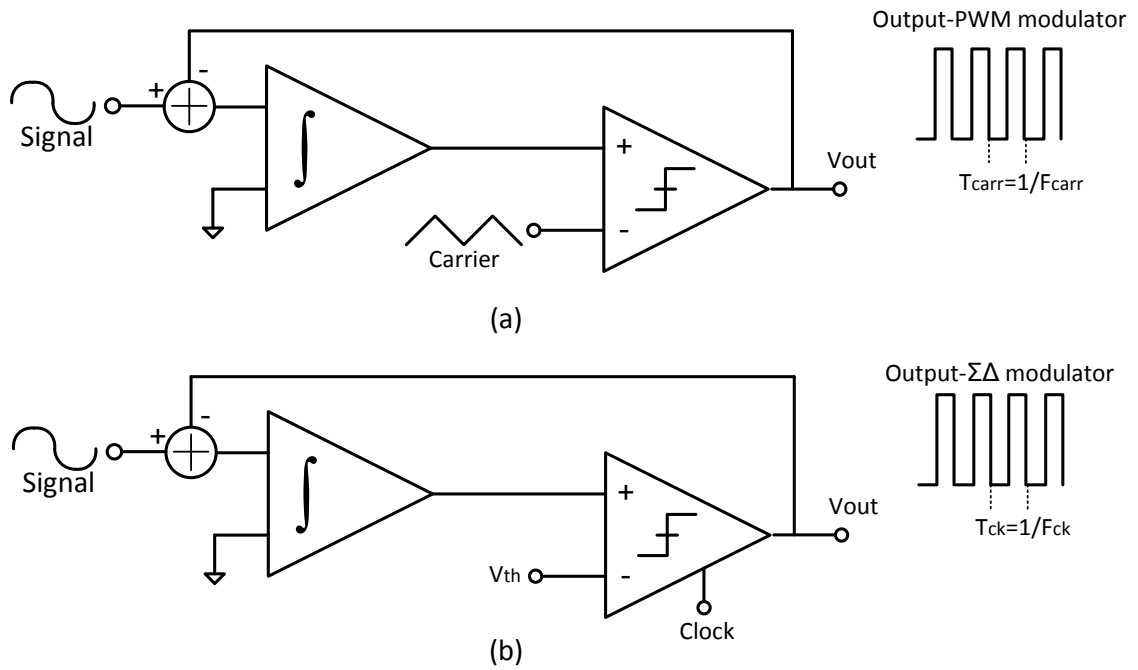
Figure 2.21: $\Sigma\Delta$ modulator versus class-D amplifier
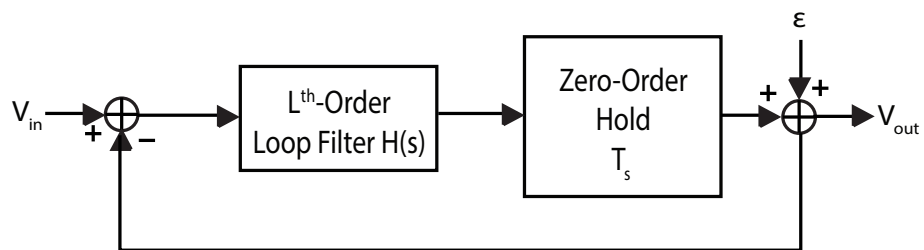
Figure 2.22: $\Sigma\Delta$ and class-D amplifier equivalent circuit
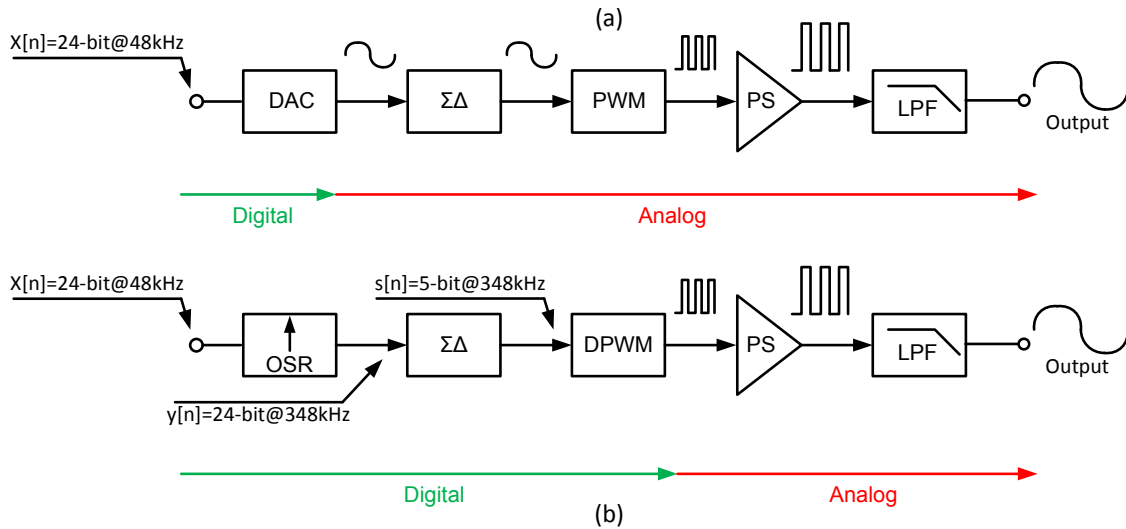
Figure 2.23: Analog and digital solutions for class D amplifiers.

2.5 Digital Control of Class-D Amplifiers

Recent developments make use of fully digital class-D amplifiers, in the sense that the digital input is not converted anymore into the analog domain, but it is directly interfaced to the digital processor, thus eliminating the need of a DAC, as shown in Figure 2.23. This solution offers better programmability, easier interface to digital processors, and a higher immunity to noise. As in the case of SMPS regulators the operating principle is based on high frequency digital PWM modulation (DPWM).

However, in this case, it is more complicated to add a feedback network, because we have to deal with digital input and analog output signals. As a result, due to the lack of a feedback network, open-loop digital class-D amplifiers typically feature worse performance than closed-loop analog class-D amplifiers. On the other hand, digital class-D amplifiers are more robust to process variations, more cost-effective, and easier to scale in advanced technologies.

2.5.1 Digital PWM Modulator for Class-D Amplifiers

To generate the PWM signal to drive the power stage, as in the case of SMPS, digital technology allows us to improve the performance and increase the linearity. Two approaches are commonly used: the direct approach and the indirect approach.

Direct Approach

The classical direct approach, illustrated in Figure 2.24(a), is the same used for SMPS regulators. In the case of class-D amplifiers, the input is a 24-bit digital word $x(n)$ sampled

Figure 2.24: Direct digital PWM generation: topology (a) and quantization (b)

at F_S and modulated by a Digital Pulse With Modulator (DPWM), in order to create a bit stream waveform to drive the power stage (PS). The PWM reference sawtooth signal have to sweep all the $x(n)$ levels during the sample time, as shown on Figure 2.24(b). In this case an accurate digital PWM can be obtained using high-speed logic and power devices.

However, there are two problems associated to direct DPWM generation. Firstly, the minimum frequency of the digital sawtooth quantum, which allows to sweep correctly all the levels at 48 kHz, can be expressed as:

$$F_{PWM} = 2^n \cdot F_S = 2^{24} \cdot 48 \text{ kHz} = 805.3 \text{ GHz}. \tag{2.10}$$

Obviously, such a frequency is not reachable in CMOS technologies.

Secondly, to reduce the switching stage power losses, the switching frequency hould be as low as possible. The finite switching time degrades the time-domain properties of the signal, leading to non-linear distortion, as discussed in Section 1.2.4.

Indirect Approach

The indirect approach, illustrated in Figure 2.25 [20], allows the digital input signal to be represented with fewer bits. The 24-bit input signal, indeed, is interpolated by $OSR = 8$, increasing the sapling frequency to $8F_S$, and truncated to 5 bits. The resulting truncation
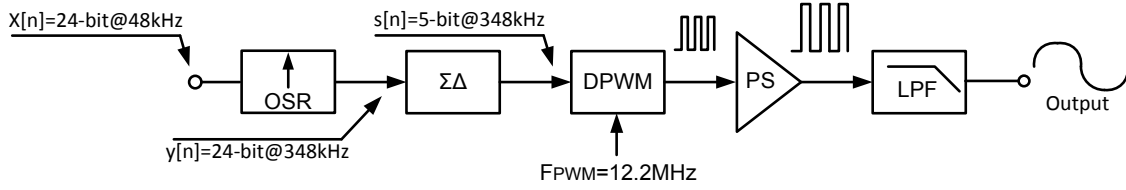
Figure 2.25: A class-D amplifier with digital signal processing.

noise is shaped by a $\Sigma\Delta$ modulator. The 5-bit signal then drives the DPWM. The value of F_{PWM}, in this case, can be expressed as:

$$F_{PWM} = 2^n \cdot OSR \cdot F_S = 2^5 \cdot 8 \cdot 48 \text{ kHz} = 12.2 \text{ MHz}, \tag{2.11}$$

which represents a more realistic frequency value.

2.5.2 Local Feedback for Digital Class-D Amplifiers

The major drawback of the open-loop digital class-D amplifiers is the reduced PSRR, as mentioned in Section 1.2.6. Indeed, the output voltage is not controlled and any disturbance on the power supply voltage is directly coupled to the output signal. Therefore some sort of feedback is necessary to obtain acceptable audio performance and to control the gain, which otherwise would vary with the supply voltage.

Because of the different nature of the input and output signals, it is difficult to implement a simple feedback path. To overcome this problem some solutions based on local feedback have been published. These feedback circuits are placed after the digital modulator or combine hybrid analog/digital circuits.

Pulse Edge Delay Error Correction (PEDC)

In the Pulse Edge Delay Error Correction (PEDEC) [21], an algorithm compares the input and output bitstreams and add a suitable time delay, in order to compensate the error. This is a pulse referenced control system, which cancel errors by re-timing the edges fed to the output switches, as illustrated in Figure 2.26. No matter the type of error, the PEDEC control system cancels error by pulse re-timing. Since both the reference signal and the feedback signal are PWM modulated, the PEDEC control system makes an absolute comparison and includes no quantization error. If there is no error the difference is zero.

The inputs of the Edge Delay (ED) unit are an error signal V_{ERR} and a reference signal V_{REF}. The output of the ED unit is an edge corrected signal V_C. The ED unit can be implemented as sown in Figure 2.27. To realize the ED signal V_C, the reference signal V_{REF} is integrated and clamped. The ED signal is compared to the error signal V_{ERR}. The pulse width will then increase or decrease if $V_{ERR} > 0$ or $V_{ERR} < 0$, respectively. The
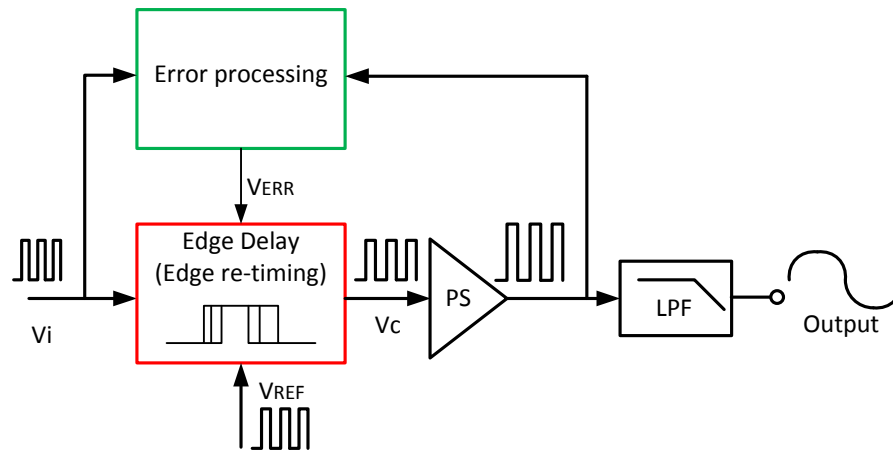
Figure 2.26: Block diagram of the Pulse Edge Delay Error Correction (PEDEC) control system

performance achieved with this solution is good ($THD > 80$ dB, $PSSR > 60$ dB), but the power consumption is too large for embedded systems.

Hybrid Analog/Digital Correction

The hybrid analog/digital correction [22] exploits a mixed analog/digital control loop. Figure 2.28 shows an overall block diagram of the digital class-D amplifier with hybrid correction. The difference (error) between the clean input PWM reference and the PWM output is amplified using an integrating error amplifier in the analog domain. This signal is converted into the digital domain with a small (6–7 bits) flash ADC, operated at twice the switching frequency. Then, exploiting the information available at twice the switching frequency, the PWM signal is corrected by independently adjusting both the rising and falling edges of the waveform. The digital PWM input, the digital correction signal, and the clock are used to produce the corrected digital PWM signal, which is then fed to the power stage.

This solution is suitable for high-power amplifiers. In mobile phones, the output power is too low to use such a control circuit.

Phase-Controlled Loop (PLC)

The Phase-Controlled Loop (PLC) solution [23] is based on an analog local feedback on the PWM phase, as shown in Figure 2.29(a). The local feedback loop, illustrated in Figure 2.29(b), consists of an integrator followed by a comparator. Signals V_{IN}, V_{OUT}, and V_i in steady-state are reported in Figure 2.30.

The behavior of such a loop can be divided in four distinct phases, due to the pseudo digital nature of signals V_{IN} and V_{OUT}. During a single phase, V_{IN} and V_{OUT} are constant
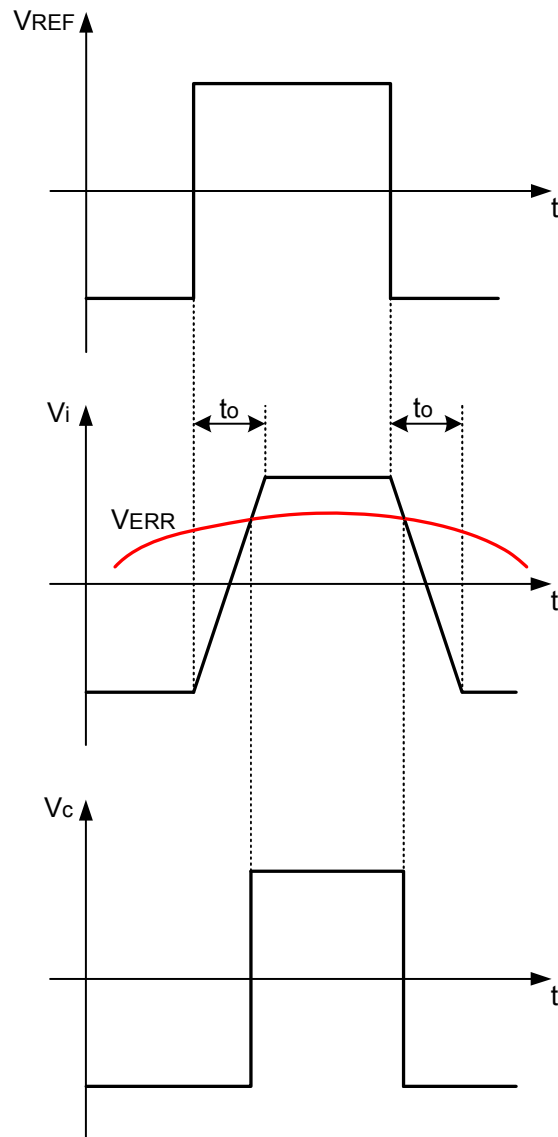
Figure 2.27: Implementation of the Edge Delay (ED) unit
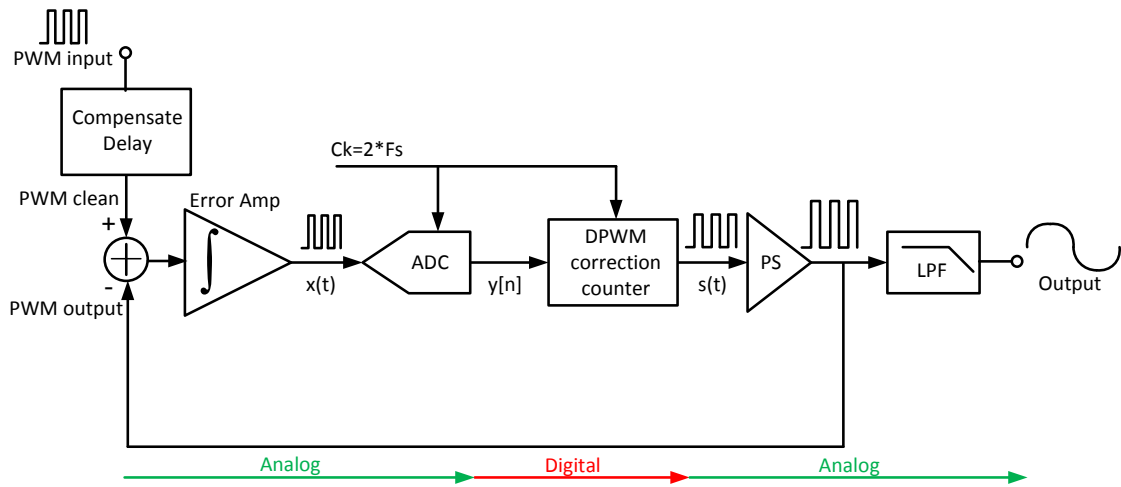
Figure 2.28: Hybrid analog/digital correction of PWM
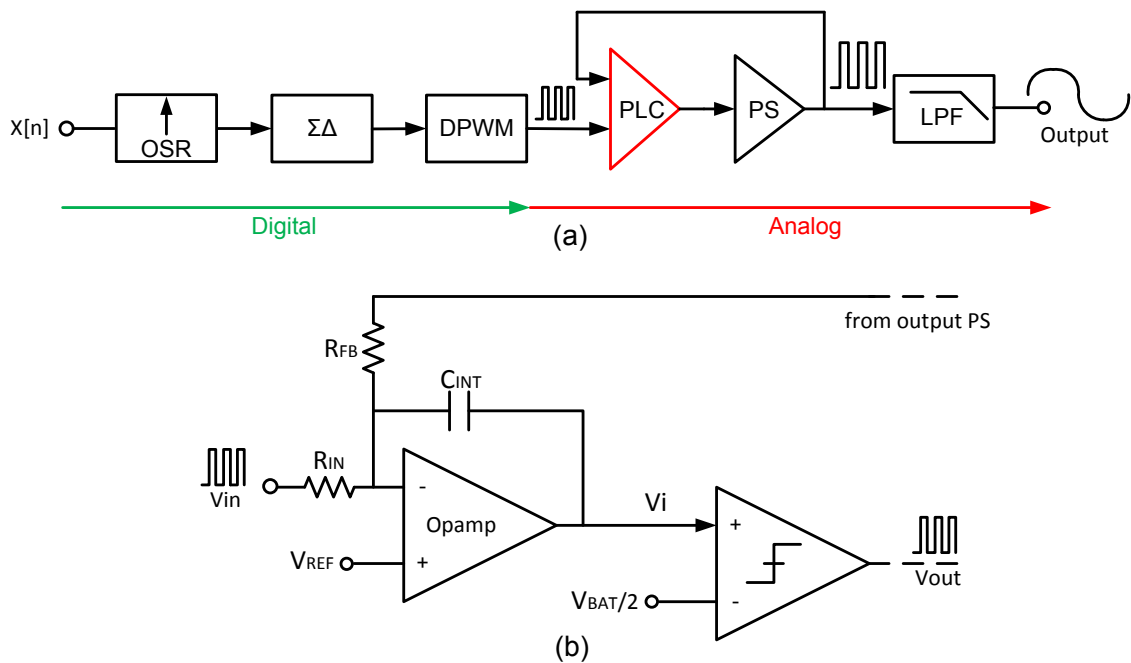
Figure 2.29: Class-D amplifier with Phase-Controlled Loop (PLC) (a) and PLC implementation (b)
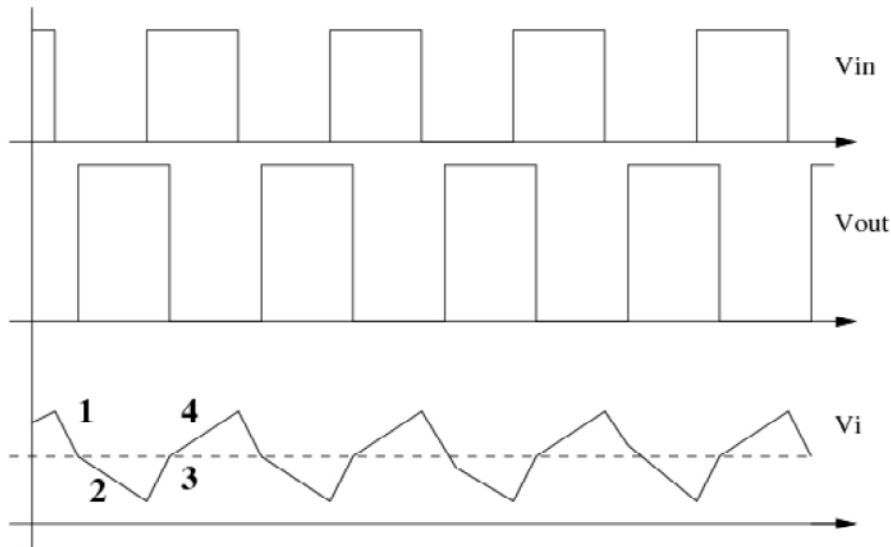
Figure 2.30: Input, output and control signals in the Phase-Controlled Loop (PLC)

and, hence, resistors R_{IN} and R_{FB} behave as current sources, which charge or discharge capacitor C. For example, in phase 1, both R_{IN} and R_{FB} are current sources, so U_C is increasing linearly and V_i is decreasing linearly, according to $U_C = V_{REF} - V_i$. Phases 1 and 3 are called working phases because the output voltage is different from the input voltage, whereas phases 2 and 4 are called waiting phases because the loop is waiting for a new input event. The simulated audio performances in this case are similar to those of analog class-D amplifiers ($THD > 80$ dB, $PSRR > 60$ dB, $SNR > 100$ dB).

2.6   Implemented Closed-Loop Digital Class-D Amplifier

To further increase the performance a local feedback is not enough: it is necessary to act upstream with the feedback loop, modifying the digital modulation as a function of the output signal. In this case an ADC is required to create a feedback path. The overall objective of this system is to control the interface between the digital modulator and the power stage to allow the realization of a class-D amplifier with a SNR as large as 100dB. This class-D amplifier topology, called DD3, is shown in Figure 2.31 [20]. The circuit consists of a feedback ADC preceded by an Anti Aliasing Filter(AAF), a Power Stage (PS), a Digital Modulator (DM), and a digital control ($C[n]$).

There are three possible configurations for the DD3 structure. In the basic configuration, called BF1 and illustrated in Figure 2.32, the input signal is sampled at 48 kHz. This configuration requires a decimation by $DSR = 3.072$ MHz/48 kHz $= 64$ of the ADC output. If the interpolation block required by the DPWM is moved outside the feedback loop, we achieve the BF2 configuration, shown in Figure 2.33. In this case the decimation

Figure 2.31: Closed-loop digital class-D amplifier
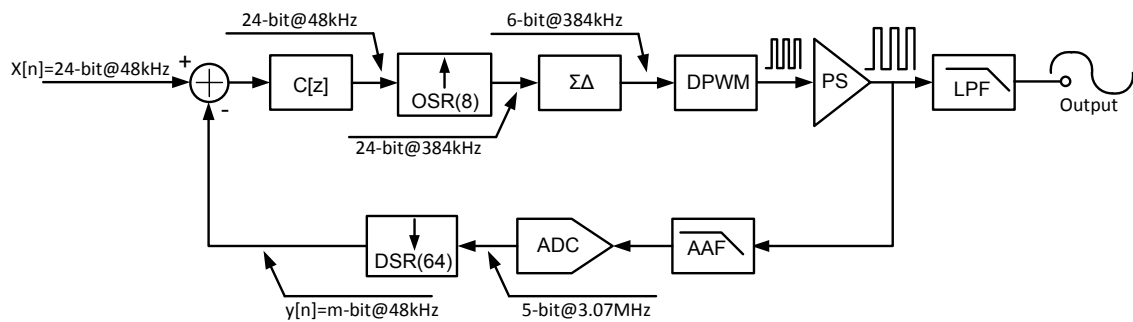
Figure 2.32: Closed-loop BF1 structure
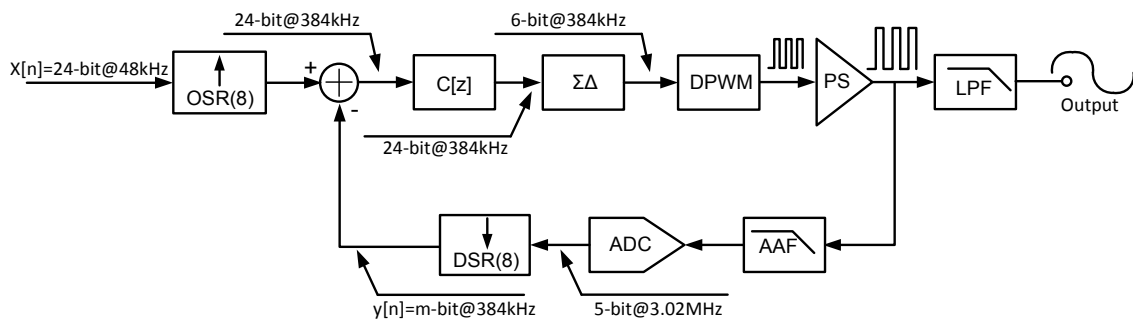
Figure 2.33: Closed-loop BF2 structure
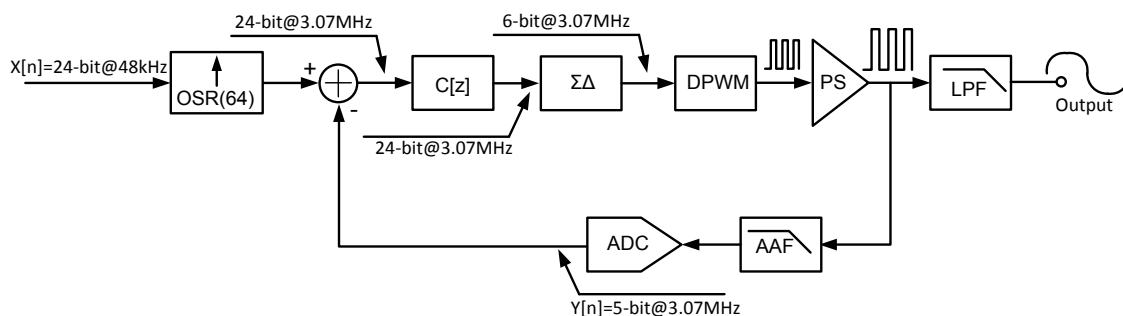
Figure 2.34: Closed-loop BF3 structure

factor required is $DSR = 3.072 \text{ MHz}/384 \text{ kHz} = 8$. If all the decimation and interpolation operations are removed and the whole circuit operates at $f = 3.072$ MHz, we obtain the BF3 configuration, shown in Figure 2.34. Configuration BF1 has strong drawbacks and cannot be practically used:

- high latency due to the decimation and interpolation operations, which strongly reduces the phase margin of the loop;
- low frequency sampling in the controller, which significantly limits the control circuit bandwidth.

Configuration BF2 has the disadvantage of having a decimator within the loop, but has the advantage that the $\Sigma\Delta$ modulator noise at high frequency ($f > 100$ kHz) is filtered. By contrast, configuration BF3 has no latency, but the $\Sigma\Delta$ modulator noise is not attenuated in the loop. Moreover, in configuration BF3 the switching frequency of the power stage is increased by 8 with respect to BF2, thus increasing the switching losses. In view of these considerations, configuration BF2, whose detailed block diagram is shown in Figure 2.35, represent the most convenient trade-off.

This DD3 class-D amplifier contains a discrete-time correction block $C[z]$, which samples the error signal at frequency $OSR \cdot F_S = 384$ kHz, followed by a digital $\Sigma\Delta$ modulator and DPWM. The power stage is based on a differential topology (H-bridge) designed to operate without an output filter.

The most important block in such a closed-loop class-D amplifier is the ADC in the feedback path, which has challenging requirements, such as:

- *Resolution* — A resolution of 5 bits is required at a sampling frequency of 3.07 MHz, thus leading to an oversampling ratio equal to $OSR = F_S/(2F_{BW}) = 3.07 \text{ MHz}/48 \text{ kHz} = 64$, where $F_{BW} = 24$ kHz.
- *Noise* — A high SNR is required. Basically, the ADC has to feature the same noise performance of the whole class-D amplifier ($SNR > 100$ dB).
- *Power consumption* — A low power consumption is essential to obtain an efficiency comparable to analog solutions.
- *Filtering* — It is necessary to filter the PWM signal coming from the power stage, in order to avoid the aliasing effect.
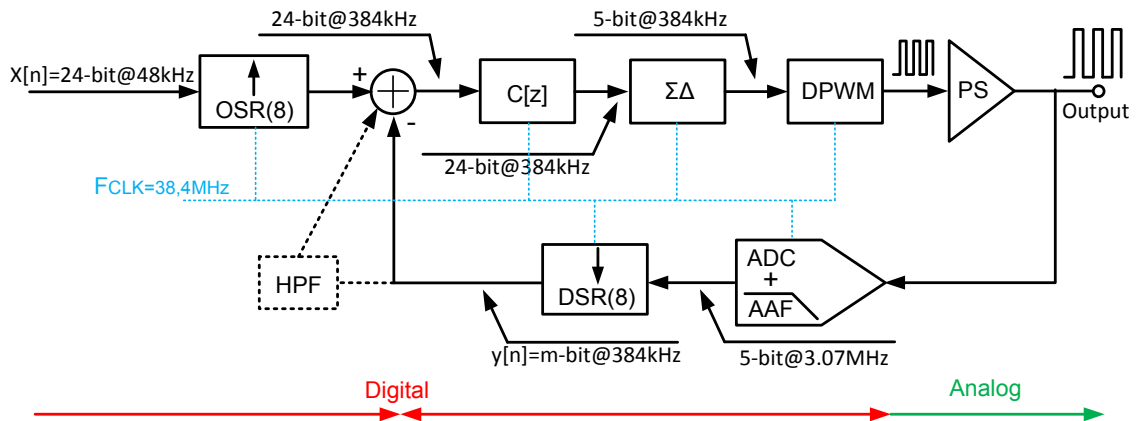
Figure 2.35: Implemented DD3 class-D amplifier architecture

- *Latency* — Time delay must be as small as possible to increase the phase margin of the loop and avoid instability.

All these features determine the overall system performance, which has to be comparable or better than conventional analog solutions. A Continuous-Time (CT) $\Sigma\Delta$ ADC is the best candidate to fulfill these requirements. In the Chapter 4 will describe in detail the motivation of the ADC topology choice, as well as the circuit design and measurements. The ADC output is processed by a decimator in order to reduce the sampling frequency and increase the effective resolution. In the feedback path it is also possible to include a simple offset cancellation filter (HPF), compatibly with the time latency tolerated. The available master clock frequency is 38.4 MHz.

Chapter 3

Multifunction SAR ADC for Digital SMPS

In Chapter 2 we analyzed the potential of digital control in the switching-mode systems and we introduced the implemented digital SMPS, reporting some design details and the achieved performance. The main device which enables the implementation of the digital SMPS with high efficiency is a multifunction Successive Approximation register (SAR) A/D Converter (ADC). In this chapter, after a short introduction on ADCs in general, we will focus on this specific circuit, describing all of the design details, as well as the measured performance.

3.1 Introduction to A/D Converters

The A/D converter (ADC) represents the interface between the world of humans, which is purely analog and the world of computers, which is definitely digital. In other words, the A/D converter transforms a continuous-time, continuous-value variable into a discrete-time, discrete-value variable. This conversion is partially reversible by using a D/A converter (DAC), with which the original analog signal can be reconstructed, eventually with some loss of information due to the discretization process. Before introducing the designed ADC, it is useful to illustrate the operation principle of A/D converters and the most important ADC architectures, specifying the key aspects which are used to quantify their performance.

3.1.1 ADC Operation

An ideal A/D converter performs three main functions, as shown in Figure 3.1: sampling, quantizing and coding.
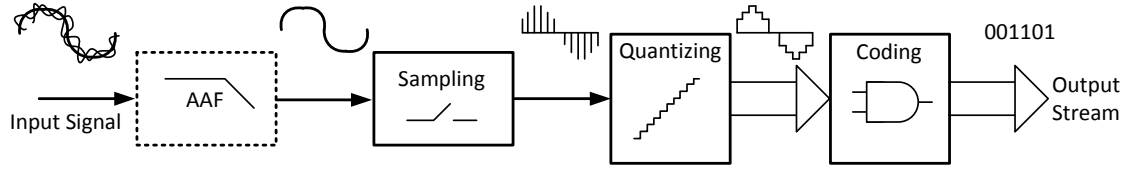
Figure 3.1: A/D conversion process
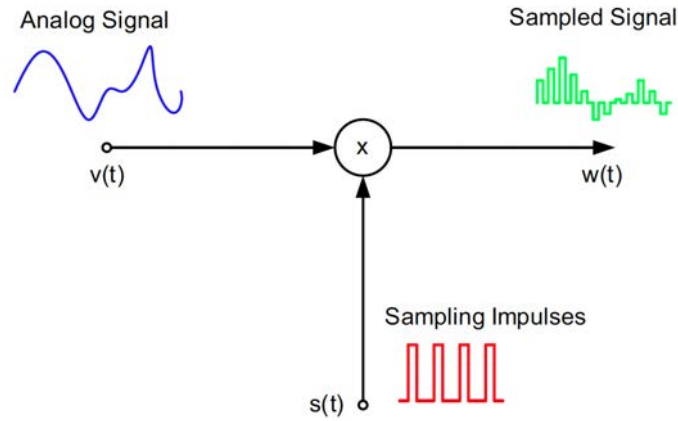
Figure 3.2: Sampling

Sampling

The sampling process transforms a continuous-time signal into a discrete-time signal. Ideally, the sampler takes the values of the signal amplitude with a fixed time step $T_S = 1/F_S$, F_S being the sampling frequency. Thus, the sampled signal $w(nT_S)$ is equal to:

$$w(nT_S) = \sum_{+\infty}^{-\infty} v(t)\delta(t - nT_S),$$ (3.1)

where $v(t)$ is the continuous-time input signal, as shown in Figure 3.2.

The sampling signal is periodic with period T_S. Therefore, using the Fourier series, it can be written as:

$$s(t) = \frac{a0}{2} + \sum_{n=0}^{\infty} a_n \cos(2\pi nF_S t) + \sum_{n=0}^{\infty} b_n \sin(2\pi nF_S t),$$ (3.2)

where a_n and b_n are given by:

$$a_n = \frac{2}{T_S} \int_{-T_S/2}^{T_S/2} s(t) \cos(2\pi nF_S t)dt,$$ (3.3)

$$b_n = \frac{2}{T_S} \int_{-T_S/2}^{T_S/2} s(t) \cos(2\pi n F_S t) dt. \tag{3.4}$$

The sampling signal $s(t)$ is an even function. Therefore, the integral defining b_n is null and (3.2) becomes:

$$s(t) = \frac{a0}{2} + \sum_{n=0}^{\infty} a_n \cos(2\pi n F_S t). \tag{3.5}$$

Assuming that the input signal is a sinusoid $v(t) = \cos(2\pi f_m t)$, with frequency f_m, the sampled signal is given by:

$$w(t) = v(t)s(t) = \cos(2\pi n f_m t) \left[\frac{a0}{2} + \sum_{n=0}^{\infty} a_n \cos(2\pi n F_s t) \right]. \tag{3.6}$$

With some calculations, (3.6) becomes:

$$w(t) = \frac{a0}{2} \cos(2\pi f_m t) + \sum_{n=0}^{\infty} \left\{ \frac{a_n}{2} \cos\left[2\pi\left(n F_S - f_m\right) t\right] \right\} +$$
$$+ \sum_{n=0}^{\infty} \left\{ \frac{a_n}{2} \cos\left[2\pi\left(n F_S + f_m\right) t\right] \right\}. \tag{3.7}$$

Therefore, the spectrum of the sampled signal contains infinite replicas of the input signal, centered at frequencies equal to $n F_S \pm f_m$, as shown in Figure 3.3(a).

The sampling process transforms a band-limited signal into a band-unlimited signal. This confirm once more the non-linear nature of the sampling process. The result obtained with (3.7) is easily applicable to the case, more common, of an aperiodic signal with bandwidth equal to f_{max}, as shown in Figure 3.3(b).

Figure 3.4 shows what happens if the sampling frequency is less than twice the maximum frequency of the input signal f_{max} and the Nyquist sampling theorem is not fulfilled. The replicas of the input signal spectrum partially overlap (red region of Figure 3.4) and modify the base-band spectrum. Therefore, there is distortion (aliasing) during the sampling process and the original analog signal can not be faithfully recreated from the sampled one. Indeed, the sampling frequency must be at least twice the maximum frequency in the spectrum of the signal to be sampled. For this reason, often, before sampling, the signal has to be filtered with an anti-aliasing filter (AAF), as shown in Figure 3.1.

In the case of the SAR ADC for SMPS this arrangement is not necessary because the input signal is practically constant, with very narrow bandwidth. Viceversa, we will see in Chapter 4 that in the case of the $\Sigma\Delta$ ADC designed for the class-D amplifier this problem has to be considered, because the input signal is PWM modulated.

Quantization

The quantization process assigns a number to each sample of the input signal. In other words, it changes a sampled data signal from continuous-amplitude to discrete-amplitude.
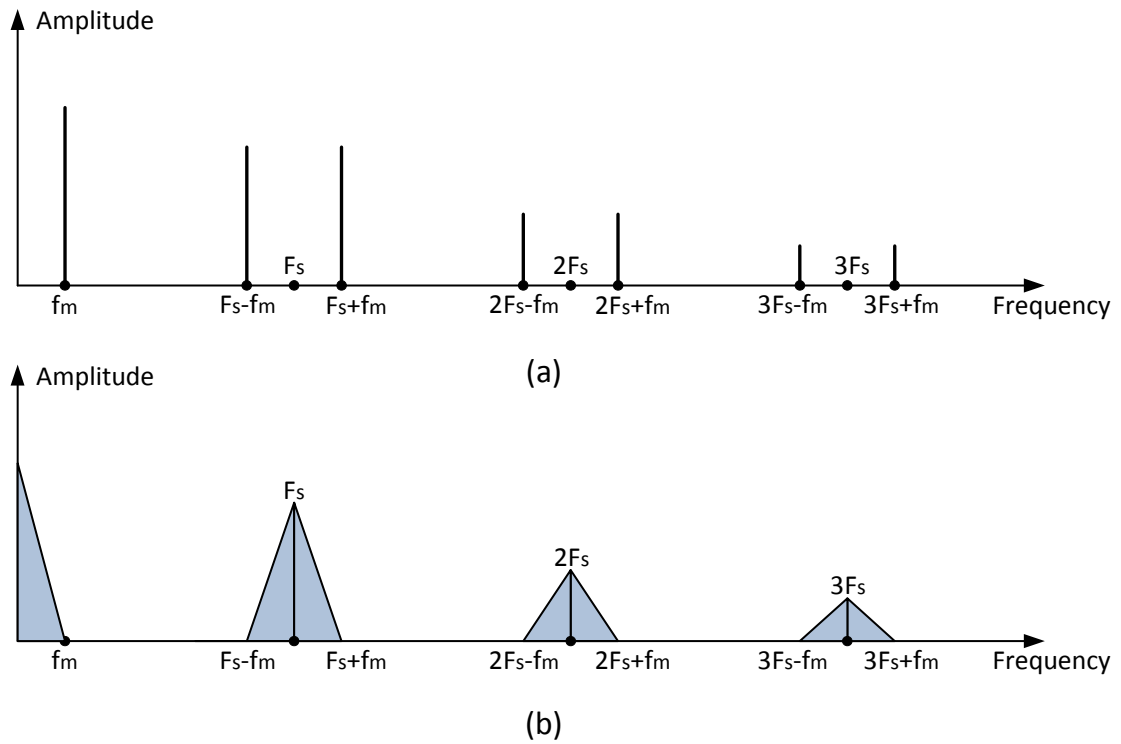
Figure 3.3: Spectrum of a sampled sinusoid (a) and spectrum of a sampled aperiodical signal (b)
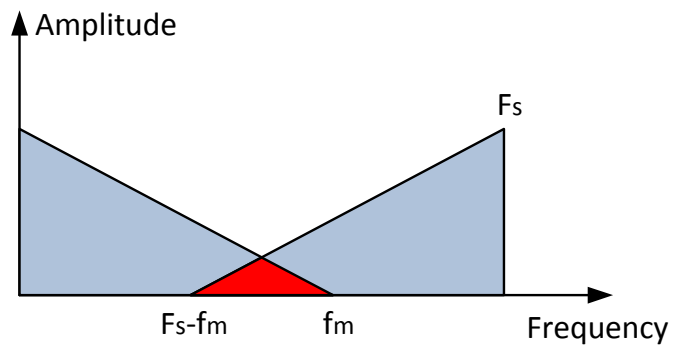
Figure 3.4: Aliasing effect
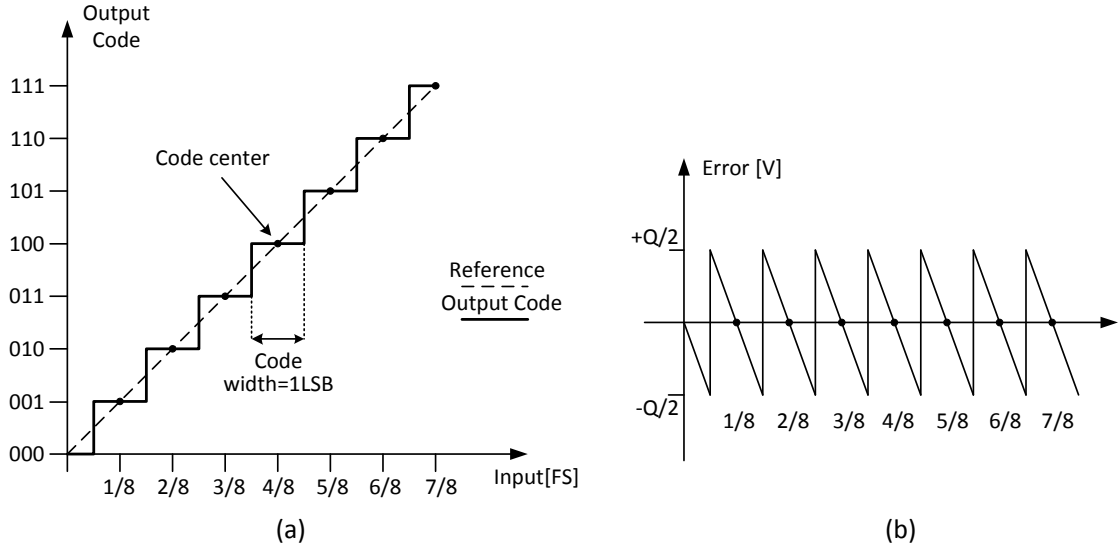
Figure 3.5: Quantization error of an ideal ADC

The input range of the quantizer is divided into a finite number of quantization intervals, normally equal (although there are some cases in which the steps are logarithmic). The quantizer assigns each sample of the input signal to one of these intervals, producing a value (number) that is the quantized level of the sampled analog input signal.

Assuming that V_{ref} is the input range of the quantizer with N levels, the quantization step is given by:

$$\Delta = \frac{V_{REF}}{N}. \tag{3.8}$$

Since a continuous-amplitude signal is quantized into a discrete-amplitude signal, an error is unavoidable. This error is called quantization error ϵ_Q and it is intrinsic in the quantization process. The output Y of the quantizer is then given by:

$$Y = X_{in} + \epsilon_Q, \tag{3.9}$$

where $n\Delta \leq X_{in} \leq (n+1)\Delta$ and $\epsilon_Q \leq \frac{1}{2}\Delta$, assuming that the mid point of the nth step represents all the amplitudes within the step itself. The quantization error goes to zero only with an infinite number of quantization levels, which is unfeasible in reality. Figure 3.5 shows the quantization error for an 8-level quantizer.

The quantization error, obviously, is related to the resolution of the ADC. The Signal-to-Noise Ratio (SNR) is defined as:

$$SNR_{dB} = 10\log\frac{P_{SIGNAL}}{P_{NOISE}}, \tag{3.10}$$

where P_{SIGNAL} is the power of the signal and P_{NOISE} is the power of the noise in the band of interest.

There is a relation between the SNR obtained by the quantization error and the number of bits of the quantizer:

$$SNR_{dB} = (6.02 \cdot n + 1.76). \tag{3.11}$$

Every additional bit of resolution:

- increases the SNR of 6.02 dB;
- reduces by a factor of 4 the power of the quantization noise.

Additional noise source, besides the quantization noise, degrade the performance of the ADC. For this reason, using (3.11), it is possible to define the effective number of bits (ENOB) given by:

$$ENOB = \frac{SNR_{dB,TOT} - 1.76}{6.02}, \tag{3.12}$$

where $SNR_{dB,TOT}$ is the signal-to-noise ratio accounting for all the noise sources.

Coding

The coding is the last operation performed by the A/D converter. Normally this operation is performed by combinatorial logic or by read-only-memory (ROM) cells. Encoding commonly used to represent the sampled data are:

- *Thermometric* — It is normally generated by a full flash ADC and it uses a set of $(2^N - 1)$ binary levels to represent N bits. For this reason it is not used for coding an ADC final output.
- *Unipolar Straight Binary (USB)* — It represents the first quantization level, $-V_{REF} + \frac{1}{2}V_{LSB}$ with the code (...000). As the analog signal increases by one LSB, the output code increases by one, until it reaches the full-scale code (...111), when the analog signal is above $V_{REF} - \frac{1}{2}V_{LSB}$.
- *Complementary Straight Binary (CSB)* — It is the opposite of USB coding. It represent the full scale code with (...000) and the first quantization level with (...111).
- *Binary Two's Complement (BTC)* — This coding scheme allows to perform subtractions. The most significant bit MSB indicates the sign (0 for positive inputs and 1 for negative inputs). The BTC coding scheme is very suitable for microprocessor based systems or to implement mathematical algorithms.

3.1.2 ADC Topologies

The three blocks described above can be realized with different design techniques. Several key aspects allow to classify the A/D converters topologies. The trade-off between speed and power consumption is one of the most important [19]. In order to choose the most suitable ADC architecture for the SMPS application, it is useful to review the most common topologies:

- *Flash ADC* — Sometimes called parallel ADC, it is the fastest type of converter. It is used to sample high-frequency signals, up to several GHz, but has limited resolution, high power dissipation, and relatively large area. The main reason for the

high power consumption is the large number of comparators. For an N-bit converter, we need $(2^N - 1)$ comparators, which means that the number of comparators increases exponentially with the number of bits. For this reason it seldom exceeds a resolution of 8 bits. This converter requires a single clock cycle per conversion.

- $\Sigma\Delta$ *ADC* — As we shall see in Chapter 4, the oversampling $\Sigma\Delta$ ADCs are very common in digital audio systems, featuring a limited bandwidth. They exploit oversampling and noise shaping to achieve high SNR and linearity.

- *Time Interleaved ADC* — Typically used for very-high-speed applications, time interleaving increases the overall sampling speed of an ADC by using two or more sub-ADCs in parallel. Operating M ADCs in parallel increases the system sampling rate by a factor of M. Each sub-ADC is operated with a clock signal phase-shifted by $360°/M$, with respect to the previous one. However, mismatches in gain, offset, and sample time among the time-interleaved ADCs generate undesired spectral components and make the system very sensitive to non-idealities.

- *Pipeline ADC* — It is a multi-stage system, consisting of multiple conversion stages working in series on groups of bits. In practice each stage quantizes the "residue" (quantization error) of the previous stage, increasing the effective resolution. This solution is used to obtain high resolution with relative low power consumption at high speed. This converter, after an initial latency of M clock cycles, where M is the number of stages, produces one output sample per clock period.

- *Successive Approximation Register (SAR) ADC* — It uses a comparator and a DAC to implement the successive approximation search method. This converter resolves a bit per conversion cycle, thus requiring N cycles to achieve N bits. The resolution is limited only by the component matching in the DAC. The greatest merit of this topology is a very low power consumption, typically dominated by the single comparator and the digital logic.

Considering the low power consumption, reduced area, and the high conversion accuracy required, the SAR ADC is the best candidate to obtain a robust, high-efficiency SMPS.

As shown in Figure 3.6 the SAR ADC is a medium resolution ADC and has typical low sampling rate. In fact, increasing the number of bits increases the number of iterations needed to obtain the output code, thus increasing the time delay and reducing the sampling rate for a given clock frequency. Thanks to the sub-micron technology adopted in this project, the sampling frequency can be pretty high (19.2-MHz maximum).

3.1.3   ADC Static and Dynamic Performance Metrics

In order to evaluate the performance of ADC, it is useful to introduce the most important metrics used, either static and dynamic.

ADC Static Performance Metrics

The main ADC static parameters are:
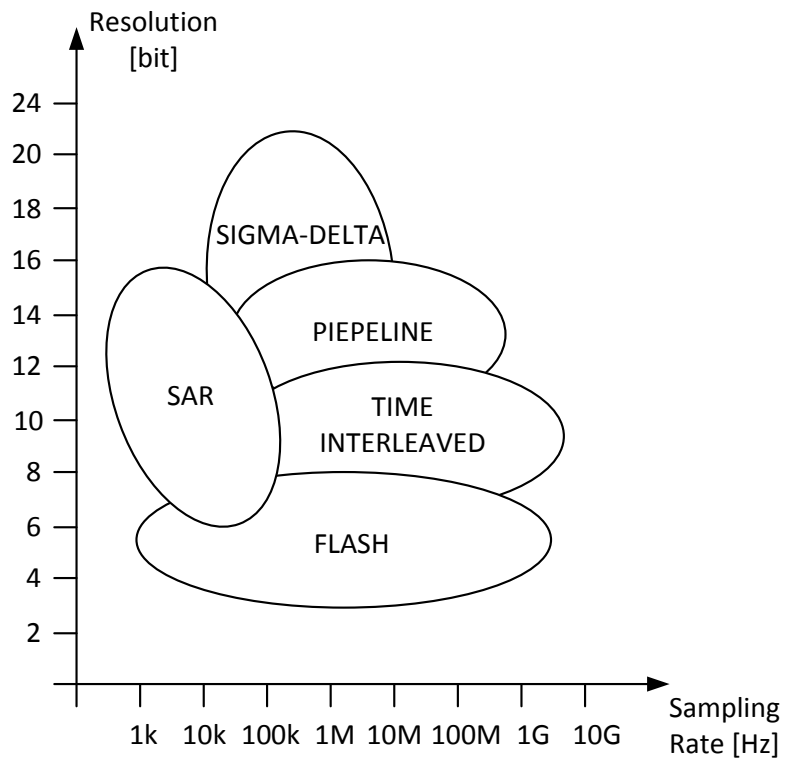
Figure 3.6: A/D converter topologies as a function of resolution and sampling rate
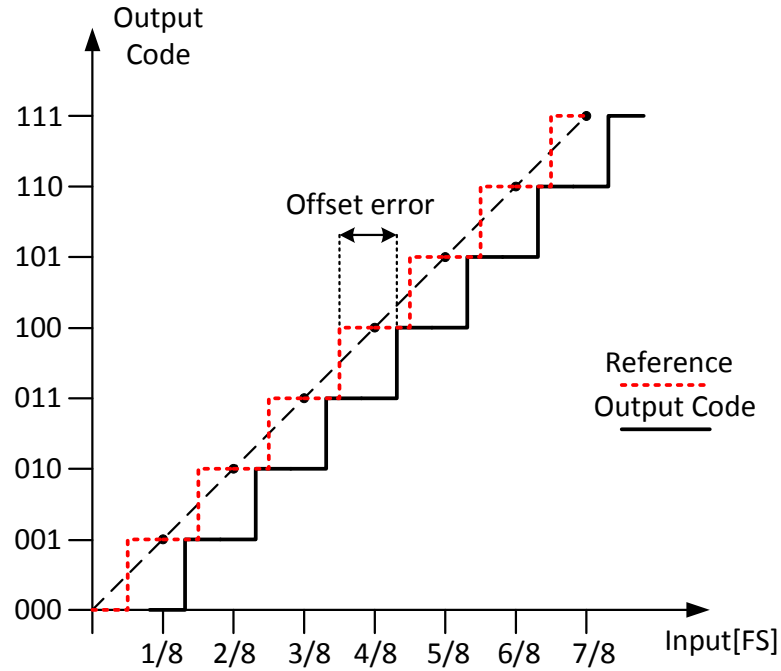
Figure 3.7: Offset error in A/D conversion

- *Analog Resolution* — The analog resolution is the smallest analog input variation which produces a variation of 1 LSB in the output code and it is given by $\frac{V_{REF}}{2^N}$, where V_{REF} is the input range and N is resolution.
- *Analog Input Range* — The analog input range is the peak-to-peak input signal (voltage or current) which generates, as output, a full-scale response.
- *Offset* — The offset is the difference between the ideal and real input signal value required to achieve a null output signal (it can be expressed in Volt, Ampere, LSB, or percentage of the full scale). The offset shifts all the quantization steps by the same quantity as shown in Figure 3.7.
- *Gain Error* — The gain error is the error on the slope of the straight line interpolating the transfer curve, as shown in Figure 3.8, which differs from a straight line of slope 1 (ideal A/D converter).
- *Differential Non-Linearity (DNL)* — The DNL measures the deviation of the ADC transfer characteristic from the ideal input-output curve with step Δ_i. Assuming that x_k is the transition point between two successive steps, then the width of the kth step is equal to $\Delta_k = (x_{k+1} - x_k)$. The DNL is then given by:

$$DNL(k) = \frac{\Delta(k) - \Delta_i}{\Delta_i}. \tag{3.13}$$

As shown in Figure 3.9, the DNL can be positive or negative.
- *Integral Non-Linearity (INL)* — The INL is the deviation of the transfer characteristic from a straight line of slope 1 (ideal A/D converter), as shown in Figure 3.10.
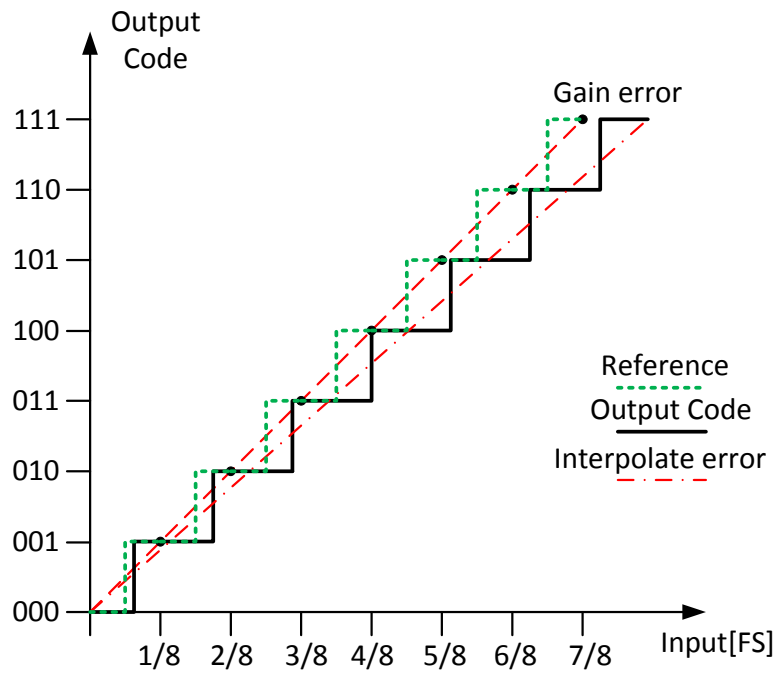
Figure 3.8: Gain error in A/D conversion
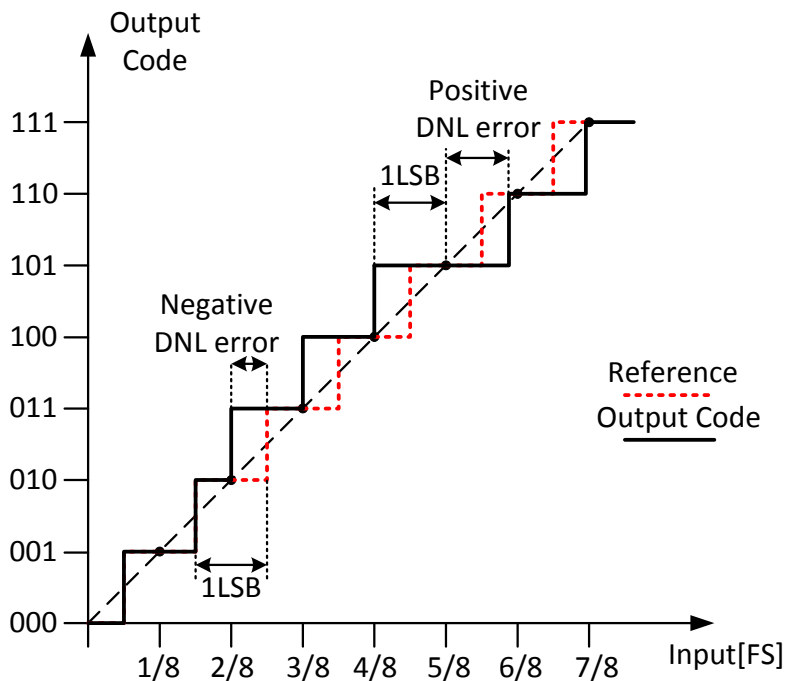
Figure 3.9: DNL error in A/D conversion
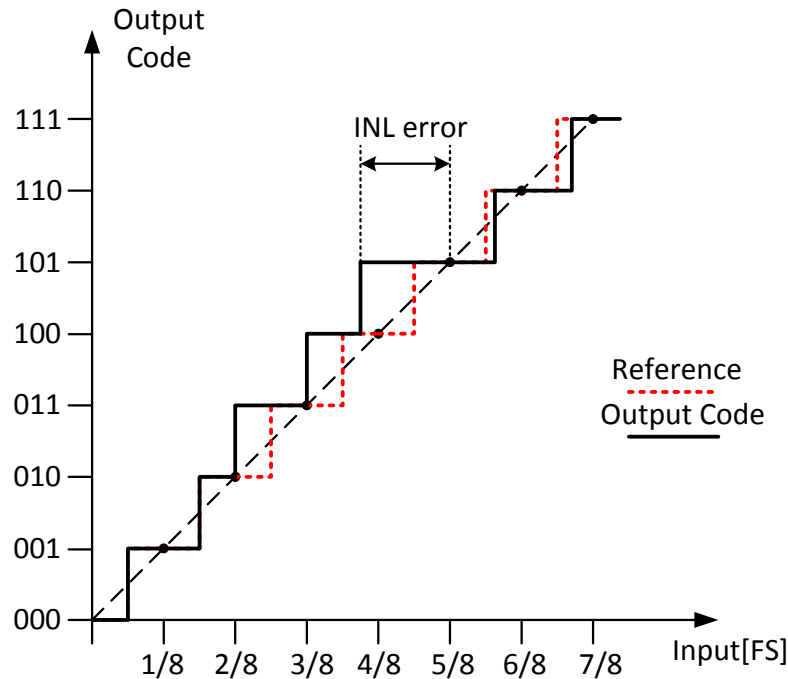
Figure 3.10: INL error in A/D conversion

The maximum of $|INL(k)|$ for all k is referred to INL. It can be expressed in Volt, Ampere, LSB, or percentage of the full scale. The name integral nonlinearity derives from the fact that the sum of the values of the DNL from step 0 to step k, determines the value of the INL for step k. The INL can be written, as:

$$INL(k) = \sum_{j=0}^{k} DNL(j). \tag{3.14}$$

- *Power Consumption* — The power consumption is the power consumed by the ADC during normal operation.
- *Temperature Range* — The temperature range is the range of temperatures in which the ADC can operate, while maintaining a proper functionality.

ADC Dynamic Performance Metrics

Te main ADC dynamic parameters are:
- *Analog Input Bandwidth* — The analog input bandwidth specifies the frequency at which the output code is -3 dB with respect to its value at DC.
- *Signal to Noise Ratio (SNR)* — The SNR, defined in (2.1), is the ratio between the power of the signal (normally sinusoidal) and the power of the quantization noise and circuit noise.

- *Signal to Noise and Distortion Ratio (SNDR)* — The SNDR is almost equal to the SNR but in the noise power, harmonic distortion is included. This parameters is linked with the ENOB.
- *Dynamic range (DR)* — The DR is the ratio between the maximum input signal and the minimum input signal level, which is detectable at the output (noise level), within a specified band.
- *Effective Number of Bits (ENOB)* — The ENOB, defined in (3.12) for the quantization noise, expresses the effective resolution of the ADC, considering the all the noise and distortion contributions. For a sinusoidal input signal the ENOB is defined as:

$$ENOB = \frac{SNDR_{dB} - 1.76}{6.02}. \tag{3.15}$$

- *Figure of Merit (FoM)* — The FoM is a parameter which includes many aspects of an ADC, in order to allow the comparison between different topologies. It is defined as:

$$FoM = \frac{Power}{2^{ENOB} \cdot 2BW}, \tag{3.16}$$

where *BW* is the input signal bandwidth and *Power* the power consumption. The FoM is expressed in Joule per conversion step and basically quantifies the amount of energy required for each quantization step.

3.2 Successive Approximation Register ADCs

Among the different ADC topology, SAR ADCs are by far the most energy efficient, thus allowing to achieve very low power consumption. Moreover, this architecture is very simple and it does not require any operational amplifier.

3.2.1 General Purpose Architecture

Successive approximation register ADCs are based on a binary search algorithm. Figure 3.11 illustrates the basic SAR ADC architecture, which consists of a front-end Sample-and-Hold (SH) circuit, a comparator, a DAC and the SAR logic. The SAR logic is basically a shift register combined with a decision logic and a decision register.

During the binary search, the circuit make the difference between the sampled signal (V_{IN}) and the DAC output (V_{DAC}). The conversion starts by setting the MSB to "1" and the other bits to "0", so that the DAC produces midscale as analog output. The comparator is then strobed to determine the polarity of $V_{IN} - V_{DAC}$. If $V_{IN} > V_{DAC}$, the MSB is maintained at "1" or otherwise it is set to "0". In the next clock cycle the bit following the MSB is set to "1" and, therefore, the DAC output settles to the a value. The comparator is strobed once again, allowing the decision logic to maintain the bit at "1" or set it to "0". This sequence is repeated until a decision is taken for all the bits.

For a resolution of *N* bits, the SAR ADC requires *N* clock cycles, but it offers several advantages:
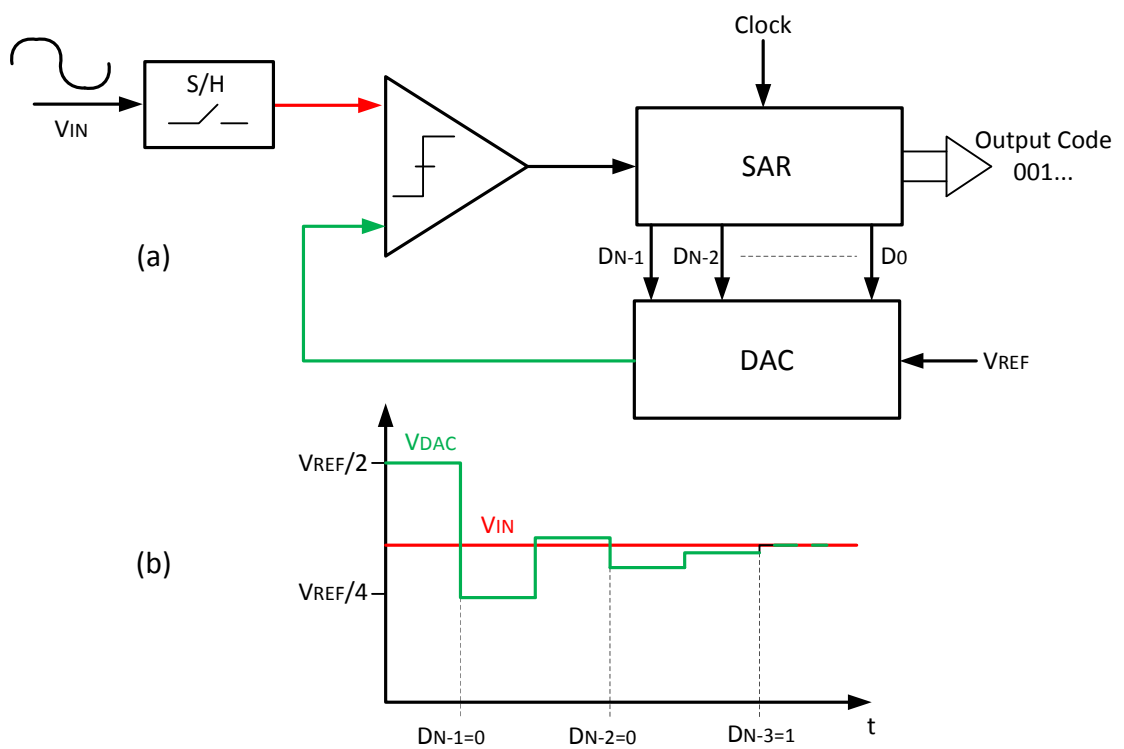
Figure 3.11: Block diagram of SAR ADC (a) and DAC output waveform (b)

- The comparator offset voltage does not affect the overall linearity of the ADC, but it produces just an offset in the overall transfer characteristic. Therefore, the comparator can be designed for high speed operation. Of course, the input noise of the comparator must be much less than 1 LSB [24].
- An explicit subtractor is not required.
- The circuit complexity and power dissipation are in general less than in other architectures.

If the SH circuit provides the required linearity and the input referred noise is small enough, then the ADC performances (in particular DNL and INL) depend primarily on the DAC. The maximum conversion rate is typically limited by the DAC output settling time. In the first conversion cycle, indeed, the DAC output must settle with the full ADC resolution, in order to allow the comparator to determine the MSB correctly. If the clock period is constant, the following conversion cycles will be as long as the first one, implying that the conversion rate is constrained by the speed of the DAC.

3.2.2 SAR Charge Redistribution Architecture

SAR ADCs based on capacitive DACs typically exploit the "charge redistribution" principle. In this scheme the comparison between the input signal V_{IN} and the reference voltage V_{REF} is made by loading the DAC with the input signal and then subtracting V_{REF} in the charge domain. A simplified diagram of this architecture is shown in Figure 3.12, where the DAC consists of binary-weighted capacitors $C_0 \div C_N$. In the initial sampling phase, the top plate of the capacitors is grounded, while all the bottom plates are connected to the input signal. The charge stored on the array is then:

$$Q_{TOT} = 2^N C V_{IN}. \tag{3.17}$$

During the first conversion cycle, S_P is turned off and the bottom plates of all the capacitors are grounded, causing the top plate voltage to be equal $-V_{IN}$. The conversion then proceeds by switching the bottom plate of the biggest capacitance (C_N) to V_{REF}, while the remaining part of the array is kept to ground. The voltage on the top plate, applied to the comparator, is then equal to:

$$V_{Comp} = \frac{V_{REF}}{2} - V_{IN}. \tag{3.18}$$

Since V_{Comp} is the difference between the MSB voltage and the input voltage, the comparator has just to determine its sign. The procedure is repeated for each bit.

This solution has some advantages, such as:
- the DAC operates as a SH circuit without requiring additional capacitors;
- the charge injection into the array by switch S_P is constant, since it always turns off with its source and drain terminals at ground;
- at the end of the conversion the top plate voltage is very close to zero, which means that the junction capacitance of S_P contributes very little to the overall non-linearity because its net voltage change is nearly zero [24].
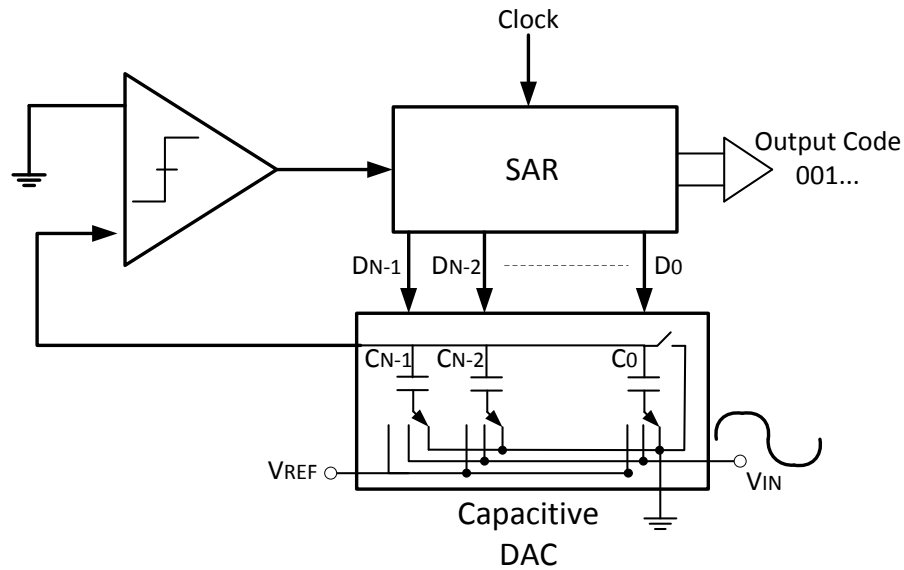
Figure 3.12: Charge redistribution SAR rchitecture

On the other hand, this architecture does not allow to sample different input signals as required in the SMPS.

3.3 Implemented Multifunction SAR ADC

As mentioned in Section 2.3, the SMPS regulator needs an ADC which can convert two different signals: the output voltage (V_{OUT}) and the battery voltage (V_{BAT}). Both signals require different precision and constraints. This involves the use of a customized structure able to sample, quantize and encode the two signals, by exploiting the same structure to avoid waste of power and area.

3.3.1 Requirements and Specifications

To perform the operations required by the SMPS controller it is necessary to design a SAR ADC that can accomplish several functions, thus leading to specific requirements and specifications.

Resolution Requirements

The ADC resolution when converting V_{OUT} is a main parameter of the SMPS, because it is directly affects the DC regulation performance, as well as the loop stability. A too small LSB would cause stability issues (due to DPWM resolution), and a too large LSB would degrade the regulation performance. However, the V_{OUT} A/D conversion does not need

to cover the whole V_{OUT} range. Once the set-point D_{REF} is fixed, a windowed conversion around D_{REF} with 4 bits of resolution is sufficient. In other words, given the 7-bit word D_{REF} (corresponding to a set-point voltage V_{REF}), the result of the V_{OUT} conversion has to be a 4-bit digital word (2's-complement coded), corresponding to ($V_{REF} - V_{OUT}$), as shown in Figure 3.13 and described in Section 2.3.1. The LSB required by the V_{OUT} conversion is 10 mV.

On the other hand, the resolution in the conversion of the V_{BAT} signal, used in the feedforward path, only affects the line transient performance. The resolution chosen to cover the whole voltage variation range of the battery is 7 bits (equal to the number of bits used to define the reference D_{REF}). The LSB value for the V_{BAT} conversion have to be bounded between 20 mV $< LSB <$ 80 mV.

Speed Requirements

The DPWM switching frequency F_S can be as large as 9.6 MHz with 5 bits of resolution. Therefore, the fastest available clock in the SMPS is at $9.6 \cdot 2^5 = 307.2$ MHz. However, the duty cycle of this clock is not controlled. The fastest available clock with "controlled" duty-cycle is at 307.2 MHz/2 = 153 MHz (equivalent to 6.51 ns period). In order to minimize the latency of the ADC, this clock is used to perform the successive approximation cycles during the conversion, leading to a sampling rate for V_{OUT} equal to 9.91 MS/s (100.9 ns sampling period).

Figure 3.14 shows the ADC control signals together with the master clock (153 MHz). The available control signals are:

- the selection signal *Mode*, to select which A/D conversion is currently done;
- the iteration signal SAR, to drive both SAR iterations;
- the sampling signal $Sample$, to sample the signals before the conversion.

Input Voltage Range

Another important parameter of the ADC is the input voltage range. The V_{OUT} signal can be vary between $V_{REF} - 45$ mV and $V_{REF} + 45$ mV, where V_{REF} can vary between 0.6 V and 1.35 V, as shown in Figure 3.13. Therefore the expected voltage range for the V_{OUT} conversion is only 900 mV (0.55 V $\div$ 1.45 V. This implies that, with a 10-mV LSB and 4 bits of resolution, only 11 of the 16 levels available are used.

On the other hand, the V_{BAT} voltage ranges between 2.3 V and 4.8 V and has to be converted with 7 bits of resolution. To manage both signal with same ADC the two input voltages have to be appropriately scaled to fit the ADC input range.

DC Accuracy

The gain error in the V_{OUT} conversion has a direct impact on the SMPS loop gain (as well as the DPWM gain error). A tolerance of 5% is acceptable on the total gain error, thus leading to an acceptable ADC gain error of 2.5%. The gain error in the V_{BAT} conversion can be relaxed to 5%. Also the offset has a direct impact on the SMPS DC accuracy.

VREF-VOUT [V]	DOUT (2-Comp)	DOUT (Decimal)	
>+75m			Bit not used
	1000	-8	
+75m			
	1001	-7	
+65m			
	1010	-6	
+55m			
	1011	-5	
+45m			
	1100	-4	
+35m			
	1101	-3	
+25m			
	1110	-2	
+15m			
	1111	-1	
+5m			Bit used
	0000	0	
-5m			
	0001	1	
-15m			
	0010	2	
-25m			
	0011	3	
-35m			
	0100	4	
-45m			
	0101	5	
-55m			
	0110	6	Bit not used
-65m			
	0111	7	
<-65m			

10mV LSB

Figure 3.13: Digital output requirements for V_{OUT} conversion
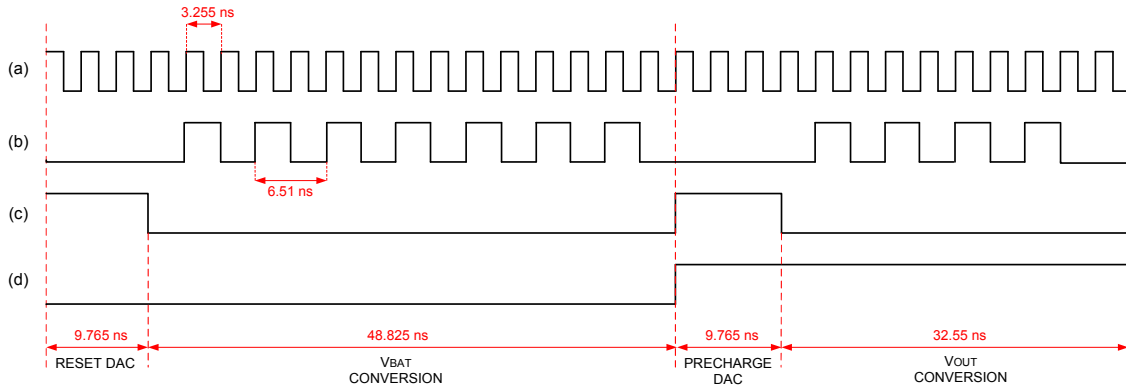
Figure 3.14: ADC control signals: master clock (a), *SAR* signal (b), *Sample* signal (c) and *Mode* signal (d)

Therefore, it has not be more than 10 mV. However, this offset error can be easily calibrated by adjusting D_{REF} which has a 10-mV LSB. The INL has no real importance in a windowed ADC context (for V_{OUT}) and, therefore, it is not an issue. For V_{BAT} conversion the INL has to be lower than 1 LSB. The DNL is the most critical DC parameter. Monotonicity must be guaranteed for proper operation of the digital PID controller and, therefore the DNL has to be lower than 0.5 LSB. Moreover, the LSB in the V_{OUT} conversion should not become too small to avoid stability issues (if LSB is too small, unwanted limit cycles can occur).

Technology, Area, and Power Consumption

The technology available is a CMOS 65-nm low-power process. For scalability, size, and speed issues the best choice for implementing the ADC core is to use the standard 1.2-V GO1 65-nm transistors. This constraint does not apply on input branch that will be realized whit a thick oxide device (GO2) to ensure proper operation while reading the battery voltage. The 1.2-V supply is generated from an on-chip LDO regulator, which provides a 1.2 V ± 30 mV voltage and the necessary current. Furthermore, a V_{CHARGE} reference voltage equal to 1 V is available. The LDO is powered by an external 1.8-V source.

Within the GO1 process, "Standard-VT" (SVT) and "High-VT" (HVT) transistors are available. However, in order to minimize the leakage current it is preferable to use HVT devices.

The target area for the ADC is 0.025 mm^2, while the current consumption is limited to 20 μA to ensure high efficiency in the SMPS.
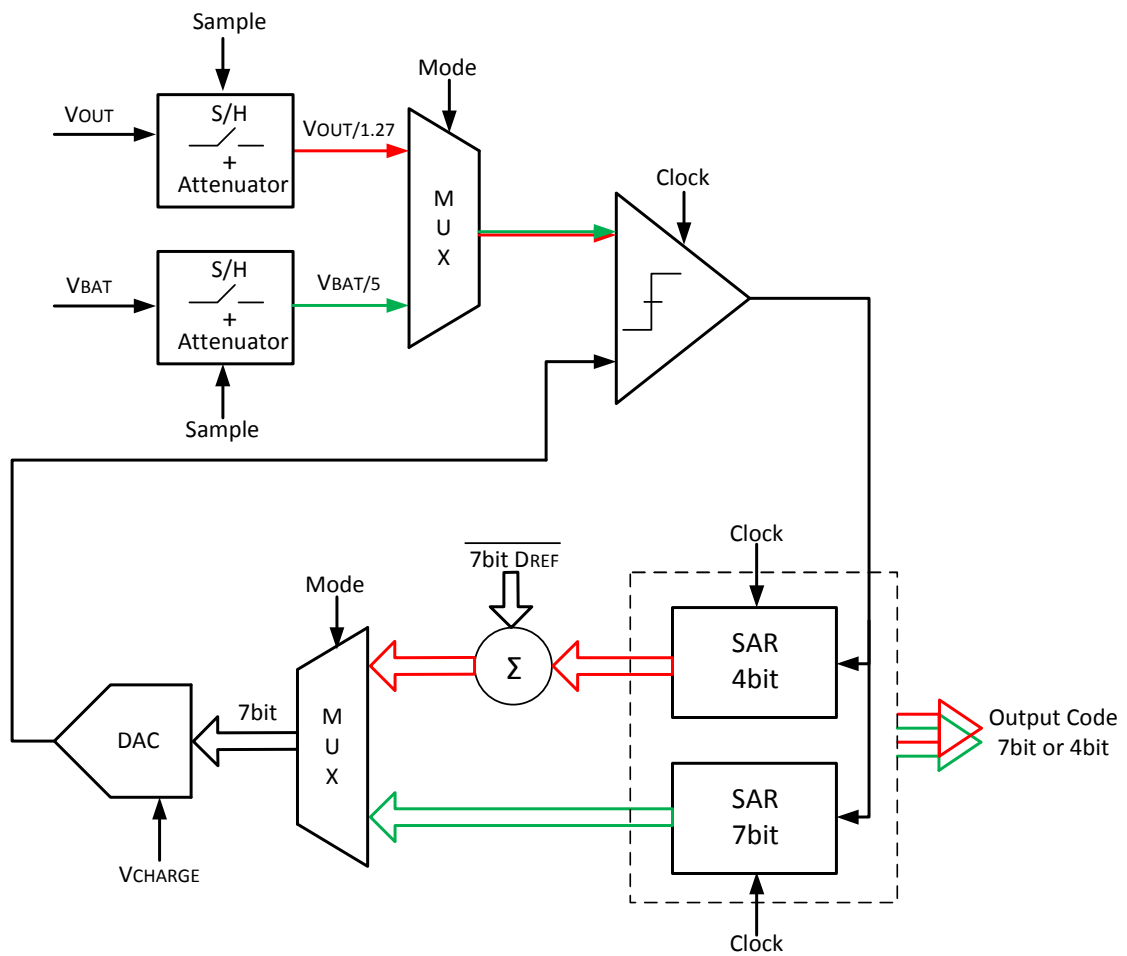
Figure 3.15: Architecture of the implemented SAR ADC

3.3.2 ADC Architecture

The SAR ADC has to perform three functions: it has to act as a DAC for D_{REF}, as 4-bit windowed ADC for V_{OUT} and as 7-bit full-range ADC for V_{BAT}. The implementation of these three functions in a single device allows a significant overall power consumption and area reduction. However, it requires different input conditioning circuits for V_{BAT} and V_{OUT}. The proposed architecture is shown in Figure 3.15. Two different Successive Approximation Registers (SARs), as well as two different voltage dividers, placed in front of the ADC core have been implemented. Moreover, it was chosen to implement the structure with a dedicated SH circuit in front of the ADC. Indeed, for sampling the input signal directly on the DAC, as typically done in SAR ADCs, a specific time slot would have been required, leading to a larger latency in the feedback control loop. The reference voltage (V_{CHARGE}), used to load the capacitors in the DAC, is 1 V. The input signals V_{OUT} and V_{BAT}, scaled by the corresponding voltage dividers, are sampled (actually V_{OUT} is sampled by the capacitive divider itself) and applied to the comparator input. The DAC, controlled by the SARs, is connected to the other comparator input. This choice allows sampling V_{BAT} while the ADC is converting V_{OUT} and vice-versa, thus increasing the time slot available for sampling, without degrading the conversion speed of the ADC.

V_{BAT} Scaling

To match the V_{BAT} voltage range (2.3 V ÷ 4.8 V) to the voltage reference used to charge the DAC (1 V) we chose to scale it by a factor 5 using a resistive divider placed in front of the SH circuit. In this way the V_{BAT} voltage range is reduced to:

$$V_{BAT,Scaled} = \frac{V_{BAT}}{5} = 0.46 \div 0.96 \text{ V}. \tag{3.19}$$

The reference voltage available $V_{CHARGE} = 1$ V implies an LSB equal to:

$$LSB = \frac{1 \text{ V}}{1.27} = 7.87 \text{ mV}, \tag{3.20}$$

which referred to V_{BAT} before scaling it is equal to:

$$LSB_{Effective} = 7.87 \text{ mV} \cdot 5 = 39 \text{ mV}, \tag{3.21}$$

as required (20 mV $< LSB_{Effective} <$ 80 mV).

V_{OUT} Scaling

The LSB required for V_{OUT} conversion is 10 mV. Using a reference voltage $V_{CHARGE} = 1$ V, the LSB is equal to 1 V/127 = 7.87 mV. Therefore, to achieve the correct LSB value it is necessary to scale $V_{OUT} = 0.55$ V ÷ 1.45 V by a factor:

$$Scaling = \frac{10 \text{ mV}}{7.87 \text{ mV}} = 1.27, \tag{3.22}$$
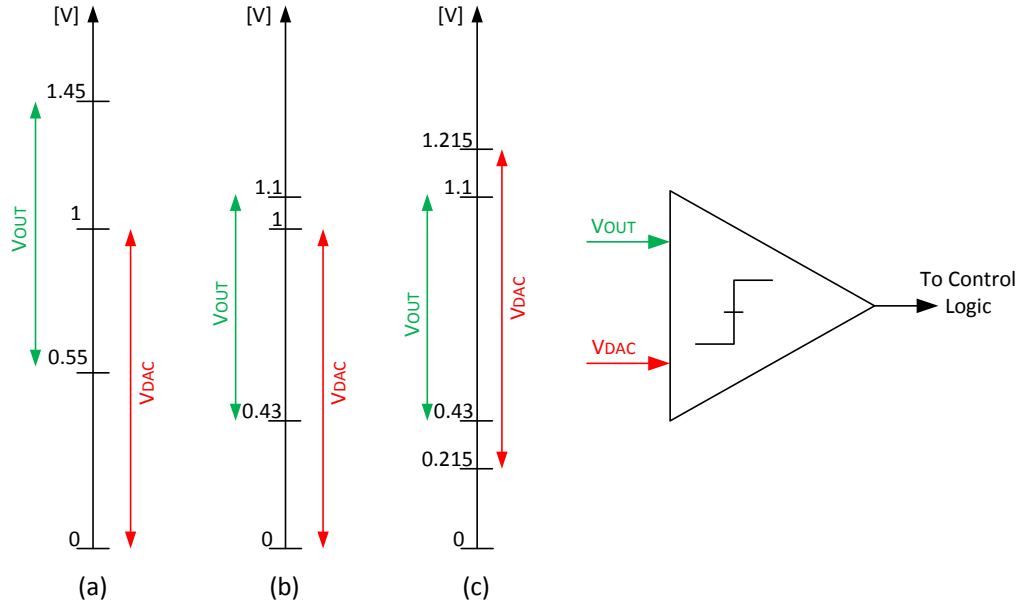
Figure 3.16: V_{OUT} voltage range before scaling (a), after scaling (b), and after offset subtraction (c)

obtaining a voltage range equal to:

$$V_{OUT,Scaled} = \frac{V_{OUT}}{1.27} = 0.43 \text{ V} \div 1.1 \text{ V}. \tag{3.23}$$

However, V_{CHARGE} is equal to 1 V and, hence, to cover the V_{OUT} range we have to add an offset equal to 430 mV/2 = 215 mV to accommodate the DAC voltage range, as shown in Figure 3.16. This offset, equivalent to 28 LSB, will be taken into account by the control logic, which will subtract it from the reference word D_{REF}, before charging the DAC to obtain V_{REF}. This phase of the conversion will be described in Section 3.3.6.

3.3.3 Sample-and-Hold Circuit

The function of a SH circuit is to buffer the input signal accurately during sampling, and to maintain a constant output level during hold. In this case the SH circuit must sample two different signals at different time and has also provide the V_{OUT} scaling. The schematic of the used SH circuit is shown in Figure 3.17. Voltage V_{BAT} is sampled on capacitor $C_2 = 585$ fF, while V_{OUT} scaling and sampling are realized with the capacitive divider C_0-C_1, according to:

$$\frac{1}{Scaling} = \frac{C_0}{C_0 + C_1} = \frac{470 \text{ fF}}{470 \text{ fF} + 125 \text{ fF}} = \frac{1}{1.27}. \tag{3.24}$$
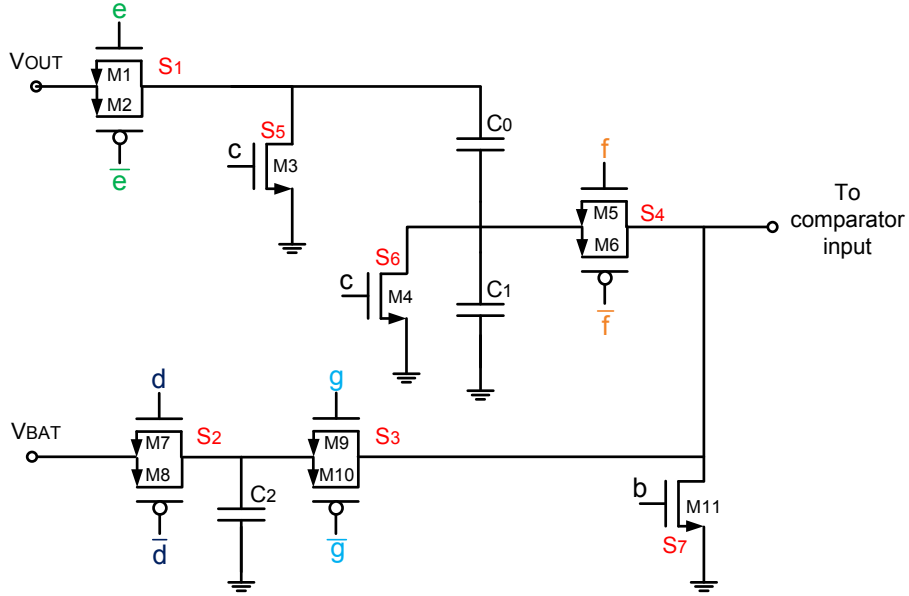
Figure 3.17: Schematic of the SH circuit

The switches S_1, S_2, S_3, and S_4 are realized with two complementary transistors [19]. The on-resistance of each transistor is given by:

$$R_{ON} = \frac{1}{\mu_{n,p} C_{ox} \frac{W}{L} \left(V_{gs} - V_{th} \right)}. \tag{3.25}$$

For a fixed sampling capacitor, the acquisition time can be decreased only by lowering the on-resistance. In a given CMOS process the mobility and oxide capacitance are normally constant and the gate-source voltage cannot exceed the supply voltage, leaving only the aspect ratio of the device as variable. In addition to finite channel resistance, the MOS switches exhibit channel charge injection. When the MOS is on, a certain amount of charge is stored in the channel which, under strong inversion conditions, can be expressed as:

$$Q_{ch} = WLC_{ox}(V_{gs} - V_{th}). \tag{3.26}$$

When the device turns off, this charge leaves the channel through the source and drain terminals, introducing an error voltage on the sampling capacitor. This error appears as an offset error because Q_{ch} is proportional to the control signal, which is constant. Therefore, the transistors used in the switches have been sized as a trade-off between on-resistance and charge injection.

Figure 3.18 shows the command phases of the switches obtained from the available control signals (shown in Figure 3.14). Each capacitor has a charging phase, a hold phase, and a reset phase. To avoid residual charge storage, the summing node at the comparator input is reset before sampling. The available phases are:
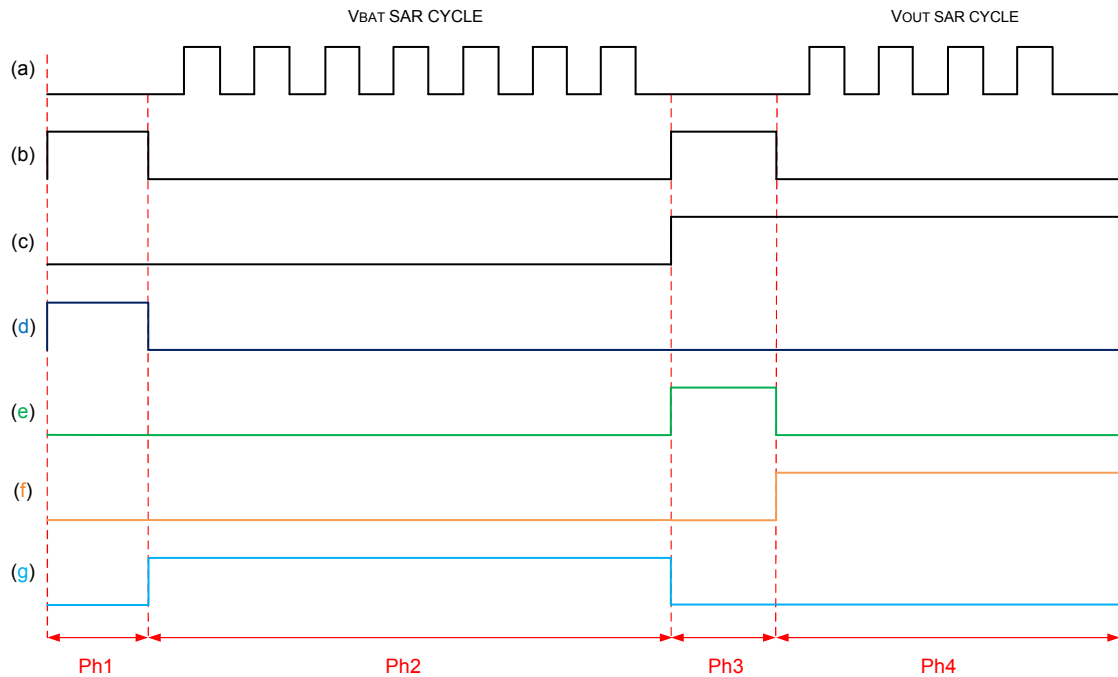
Figure 3.18: SH circuit control phases

- *Ph1* — In this phase S_1, S_4, and S_3 are open; C_0 and C_1 are shorted to ground by S_5 and S_6; C_2 stores the V_{BAT} voltage through S_2; S_7 is closed and the summing node is shorted to ground.
- *Ph2* — This is the V_{BAT} hold phase, during which V_{BAT} SAR cycle takes place; S_2 is open and the voltage sampled by C_2 is applied at the comparator input through S_3; all the other switches are open except S_5 and S_6 which short C_0 and C_1 to ground.
- *Ph3* — At the end of the V_{BAT} SAR cycle, the comparator input node is shorted to ground again by S_7; V_{OUT} is sampled and scaled by C_0 and C_1 through S_1 and the other switches are open.
- *Ph4* — During this phase the V_{OUT} SAR cycle is performed; V_{OUT} suitably scaled it is applied to the comparator input by S_4; all the other switches are open; at the end of this phase, a new cycle starts.

Transistors $M1$, $M2$ and $M3$ are GO2 devices driven by 2.5-V clock phases, since these devices must withstand a maximum voltage of 1.45 V, which is too large for GO1 transistors. To discharge the sampling capacitors, by S_5 and S_6, and to reset the summing node, by S_7, we used just a NMOS switch since the source voltage is close to ground.

3.3.4 Comparator

The comparator is the block which mostly affects the total analog power consumption of the SAR ADC. Speed, accuracy, power consumption, and input common mode range
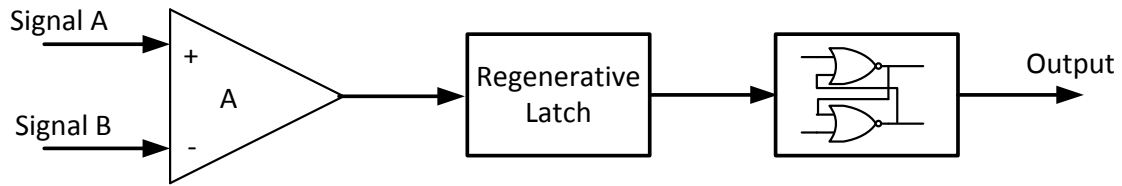
Figure 3.19: Block diagram of the latched comparator
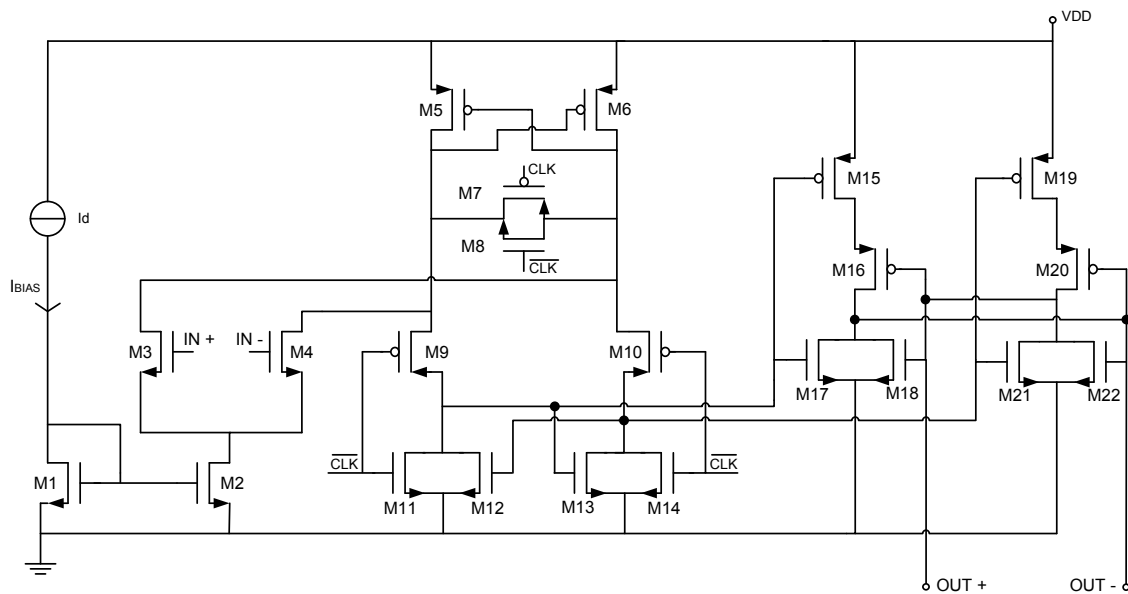
Figure 3.20: Schematic of the latched comparator

are the most important aspect considered in the comparator design. In a SAR ADC the comparator should be able to detect $1/2$ LSB (in this case $LSB = 3.93$ mV). The static offset, which originates from mismatches among transistors, affects the accuracy of the comparator decreasing the resolution of the ADC. To reduce this effect is necessary to properly design the comparator input stage and optimize the layout [19].

For the SAR ADC we used a latched comparator, based on the block diagram shown in Figure 3.19. The circuit consists of an input stage, a regenerative latch, and set-reset flip-flop. The detailed schematic of the comparator is shown in Figure 3.20. Transistors $M3$ and $M4$ are used to amplify the difference between the input voltages. When the clock signal (CLK) is low $M9$ and $M10$ are open, while $M11$ and $M14$ are closed. Moreover $M8$ and $M7$ are closed, thus resetting the comparator. This static situation persists until CLK becomes high. In this case $M7$, $M8$, $M9$, $M10$, $M11$, and $M14$ are open, while $M5$, $M6$, $M12$ and $M13$ become active and start the regenerative operation. This causes an imbalance in the comparator which depends on the input voltage, leading the output nodes to saturate. The set-reset flip-flop, realized with a pair of cross-coupled NOR gates

($M15 \div M22$), provides a stable output during the whole clock period.

A problem which can occur in a latched comparator is the metastability error. Considering the two operation phases, reset phase and regeneration phase, the latch has to produce a valid logic level within half of the clock period. When the input voltages are very close to each other, the latch takes more time to produce a logic level, which might result in a metastable state. In other words, a metastable situation occurs when the latch is not able to switch to a valid logic level, zero or one, in the regeneration time slot and reaches an intermediate value. The metastability error can adversely affect the accuracy of the comparator and of the ADC. The probability of metastability is inversely proportional to the comparator gain. To avoid this problem a reasonable gain and hence a 7 μA quiescent current are exploited to reduce the regeneration time and increase the speed.

Simulations showed a constant input offset in the comparator. Therefore, in order to avoid additionally power consumption to realize a compensation circuit, we decided to increase the DAC pre-charge voltage from 215 mV (28 LSB) to 230 mV (30LSB) restoring the proper voltage range.

3.3.5 Digital-to-Analog Converter

In a SAR ADC the DAC determines the overall linearity. The basic purpose of the DAC is to generate an analog voltage proportional to the digital code produced by the SAR. The DAC can be implemented with many different well-known techniques, e. g., capacitor-based DAC [25], switched-current DAC [26], or *R*-2*R* ladder DAC [27]. However, the most widely used DAC topology in SAR ADCs is the capacitive DAC, since capacitive arrays do not dissipate static power (zero quiescent current).

Binary-Weighted Capacitor Array

The simplest capacitive DAC is based on the binary-weighted capacitive (BWC) array shown in Figure 3.21. For *N* bits of resolution, it consists of *N* capacitors which sizes ranging from 2^0C to $2^{N-1}C$, with an additional unit capacitor at the rightmost side of the array, used to restore the correct proportions between the voltage contribution. The total capacitance of the array is equal to:

$$C_{TOT} = C + \sum_{n=0}^{N-1} 2^n C. \qquad (3.27)$$

This simple solution has the disadvantage of requiring very large capacitors which increases exponentially with the resolution required, thus increasing both the area and the time constant associated with the DAC itself and, hence, the DAC settling time.

When such a DAC is used in a SAR ADC, initially, all the capacitors are reset to ground. The top plates are reset trough S_R, and the bottom plate trough each command switch S_0, S_1...S_{N-1}. After reset, S_R is open and the bottom plate of the largest capacitor
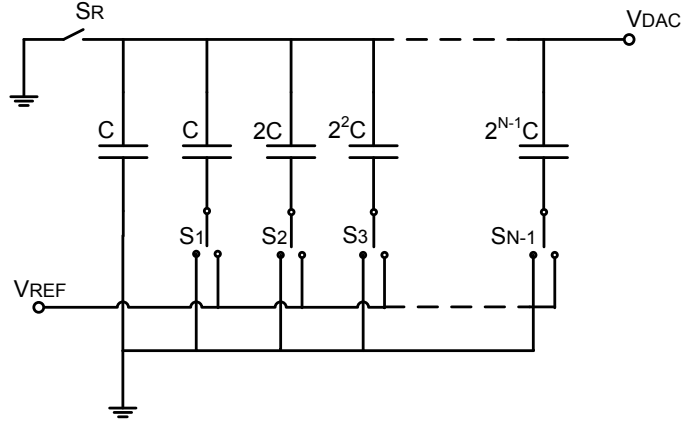
Figure 3.21: Binary-weighted capacitor array DAC

(MSB) is connected to V_{REF} and the DAC output voltage settles to $V_{REF}/2$:

$$V_{DAC} = \frac{C \cdot 2^{N-1}}{C \cdot 2^N} \cdot V_{REF} = \frac{1}{2} V_{REF}. \tag{3.28}$$

This voltage is compared with the sampled value of V_{IN} and, according to the result, the SAR logic maintains the MASB capacitor connected to V_{REF} (if $V_{REF}/2 < V_{IN}$) or connects it to ground (if $V_{REF}/2 > V_{IN}$). This procedure determines the value of the MSB. This operation is repeated for each of the remaining $N-1$ bits. When all the bits are fixed set and the output word is ready, the capacitive array can be reset to ground and a new conversion can start.

Two-Stage Binary-Weighted Capacitor Array

To reduce the capacitor size in the DAC it is possible two adopt a two-stage solution. With this approach the BWC array is divided by a coupling capacitor in a lower array, which realizes the L least significant bits, and an upper array, which realizes the $M = N - L$ most significant bits, as shown in Figure 3.22. The fundamental advantage of this architecture is the silicon area reduction: the capacitor value is obviously lower than in the BWC for the same number of bits. Indeed, the overall capacitor size is $(2^L + 2^{N-L})C < 2^N C$.

In order to guarantee proper DAC operation and linearity the series connection of the attenuation capacitor (C_{DIV}) and the lower array must be equal to the unit capacitor C:

$$C = \frac{\left(\sum_{n=0}^{L-1} 2^n C\right) \cdot C_{DIV}}{\left(\sum_{n=0}^{L-1} 2^n C\right) + C_{DIV}}. \tag{3.29}$$

Therefore, the value of C_{DIV} is:

$$C_{DIV} = \frac{2^L}{2^L - 1} \cdot C. \tag{3.30}$$
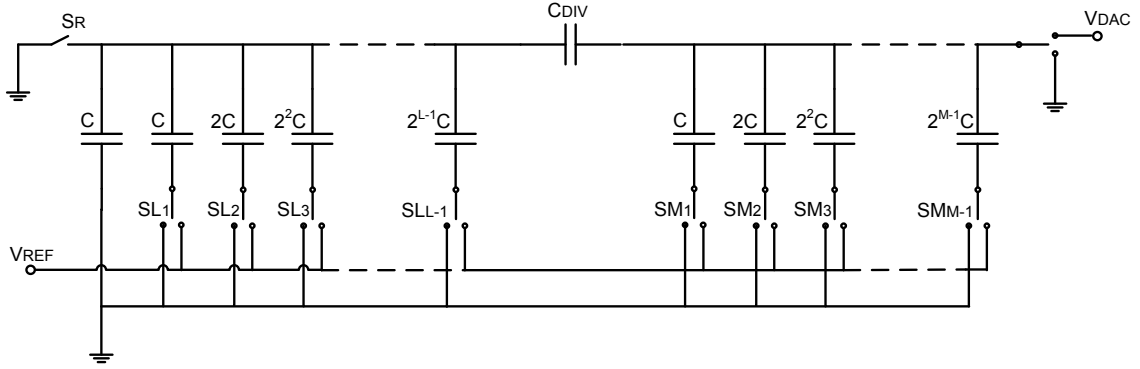
Figure 3.22: Two-stage binary-weighted capacitor array

The total capacitance of the array then is equal to:

$$C_{TOT} = C + \sum_{n=0}^{L-1} 2^n C + \sum_{i=0}^{M-1} 2^i C + C_{DIV}. \tag{3.31}$$

To reset the entire array, in this case, it is necessary to add a reset switch to force to ground the top plates of both arrays.

Implemented DAC

The implemented DAC is shown in Figure 3.23. We adopted a two-stage architecture to ensure small area. The lower array consists of 4 capacitors ($L = 4$), and is used both for V_{OUT} and V_{BAT} conversions. By contrast, the upper array is realized with 3 capacitors ($M = 3$), which are actually used for V_{BAT} conversion.

Unlike the conventional scheme, the switches adopted to reset the top plates of the arrays can be connected either to V_{CHARGE} (1 V) or to ground. Indeed, before the V_{OUT} conversion the output node V_{DAC} must be recharged to 215 mV to introduce the artificial offset required to achieve the proper voltage range, as shown in Figure 3.16. To charge the output node V_{DAC} to 215 mV, S_L and S_M are connected to V_{CHARGE}, while S_{Li} and S_{Mi} are connected to ground or V_{CHARGE} depending on the word to be loaded in the DAC. More precisely, 215 mV corresponds to $28 \cdot LSB = 00111000$ (the last zero is for switch S). The word to be applied is then 11000111. During the SAR cycle S_L and S_M are not used any longer.

To size suitably the unity capacitor C, some considerations about power consumption and linearity performance are needed. The energy required to charge the DAC array is one of the main sources of loss. The capacitor switching power consumption is directly proportional to the unit capacitor size [28]. Also, as mentioned before, the capacitor size determines the charging time constant, which must be less than half of the clock period available, as well as the kT/C noise. In practice, the unit capacitor size is determined
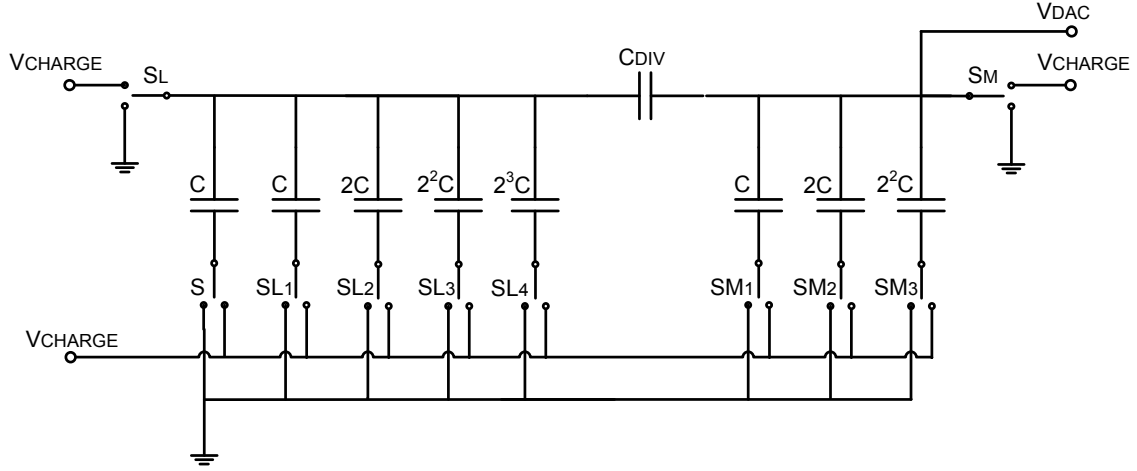
Figure 3.23: Schematic of the implemented DAC

as a trade-off between these parameters, the capacitor matching requirements, and the parasitic capacitances, which also affect the INL and the DNL.

In order to obtain an optimum value of C, an accurate analysis was made in [29]. To analyze the statistical behavior of the linearity metrics (INL and DNL), the capacitors C_i are modeled as sum of the nominal capacitance value and an error term, leading to:

$$C_i = 2^{N-i}C + \delta_i, \ \sigma_i^2 = E[\delta_i^2] = 2^{N-i}\sigma_0^2, \tag{3.32}$$

where C is the unit capacitance, δ_i is a random variable with zero mean and variance σ_i^2, while σ_0 is the standard deviation of the unit capacitance. For a SAR ADC with two-stage capacitive DAC, the variance of the INL and DNL can be calculated as:

$$\sigma_{INL}^2 = 2^{\frac{3N}{2}}\left(\frac{\sigma_0}{C_0}\right)^2\left(\frac{V_{IN}}{V_{CHARGE}}\right)LSB^2, \tag{3.33}$$

$$\sigma_{DNL}^2 = 2^{\frac{3N}{2}}\left(\frac{\sigma_0}{C_0}\right)^2 LSB^2. \tag{3.34}$$

The minimum unit capacitor can be obtained by imposing the maximum tolerable variance of the INL and DNL. Thanks to the 65-nm technology, where capacitors feature a very low mismatch $\frac{\Delta C}{C} = 0.04\%$, the elementary capacitor has been sized to $C = 25.5$ fF. The attenuation capacitor has been sized to $C_{DIV} = 27.8$ fF from (3.30), obtaining a total capacitance of $C_{TOT} = 614$ fF.

Another aspect to consider is the parasitic capacitor influence. The parasitic capacitors connected to the bottom plate of the arrays do not affect the linearity of the ADC, since they bare not involved in the charge distribution process. On the other hand, as demonstrated in [29] the parasitic capacitors connected to the top plate of the arrays degrade the linearity performance and, therefore, it has to be minimized in the layout.

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3.3.6   Successive Approximation Register and Control Logic

The SAR and control logic determines the output word depending on the successive approximation result. This function is sequentially performed to encode both V_{BAT} and V_{OUT}. Moreover, this logic block generates the clock phases required by the SH circuit, as shown in Figure 3.18. This circuit has been implemented as a Verilog code (Listing 3.1), which is then synthesized.

Listing 3.1: SAR and control logic Verilog code

```verilog
1  // Verilog HDL for "SAR", "sar_adc" "functional"
2
3  module sar_adc(di7, di6, di5, di4, di3, di2, di1, res, res_n, pre, pre_n, comp7, comp7_n
        , comp4, comp4_n, mode, mode_n, sample, comp, clock, clock_n, ro, ron, ris4, ris7,
        rst_n);
4
5
6  input mode, sample, clock, comp, di7, di6, di5, di4, di3, di2, di1 ,rst_n ;
7  output [7:0] ro;
8  output [7:0] ron;
9  output [6:0] ris7;
10 output [3:0] ris4;
11 output pre, pre_n, res, res_n, comp7, comp7_n, comp4, comp4_n, mode_n, clock_n;
12 wire pre;
13 wire pre_n;
14 wire res_n;
15 wire resn;
16 wire comp7;
17 wire comp7_n;
18 wire comp4;
19 wire comp4_n;
20 wire mode_n;
21 wire clock_n;
22 reg [7:0] va;
23 reg [3:0] ris4;
24 reg [6:0] ris7;
25 reg [7:0] dref;
26 reg [4:0] dac5;
27 reg [7:0] dac8;
28 wire [7:0] ron;
29 wire [7:0] ro;
30 reg [2:0] i;
31 reg [1:0] p;
32 wire [7:0] roint;
33 wire [7:0] prec;
34 wire reset_vout ;
35 wire reset_vbat ;
36
37
38 always @(posedge sample or negedge rst_n)begin
39   if(rst_n==1'b0)
40   begin
41      va = 8'b00000000;
42      dref = 8'b00000000;
43      end
44    else
45    begin
46    va[7] = di7;
47    va[6] = di6;
48    va[5] = di5;
49    va[4] = di4;
50    va[3] = di3;
51    va[2] = di2;
```

```
52        va[1] = di1;
53        va[0] = 0;
54        dref = va + 8'b11110000;
55      end
56  end
57
58  always @(negedge clock or negedge reset_vout)begin
59  if(reset_vout==1'b0)
60      begin
61          p = 2'b00;
62          dac5 = 5'b10000;
63          if(rst_n==1'b0)
64              begin
65                  ris4 = 4'b0000;
66              end
67      end
68  else
69  begin
70  if(mode==1'b1)
71          begin
72                  case (p)
73                  2'b00: begin
74                          dac5[4] = ~comp;
75                          dac5[3] = 1'b1;
76                          p = 2'b01;
77                          end
78                  2'b01: begin
79                          dac5[3] = ~comp;
80                          dac5[2] = 1'b1;
81                          p = 2'b11;
82                          end
83                  2'b11: begin
84                          dac5[2] = ~comp;
85                          dac5[1] = 1'b1;
86                          p = 2'b10;
87                          end
88                  2'b10: begin
89                          dac5[1] = ~comp;
90                          dac5[0] = dac5[1];
91                          p = 2'b00;
92                          ris4[3] = dac5[4];
93                          ris4[2] = dac5[3];
94                          ris4[1] = dac5[2];
95                          ris4[0] = dac5[1];
96                          ris4 = ris4 + 4'b1000;
97                          ris4 = ~ris4 + 4'b0001;
98                          end
99                  endcase
100         end
101 end
102 end
103
104 always @(negedge clock or negedge reset_vbat)begin
105 if(reset_vbat==1'b0)
106         begin
107         dac8 = 8'b10000000;
108         i = 3'b100;
109         if(rst_n==1'b0)
110           begin
111               ris7 = 7'b0000000;
112           end
113         end
114 else
115  begin
116    if(mode==1'b0)
```

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```
117            begin
118               case ( i )
119               3'b100 : begin
120                   dac8 [7] = ~comp;
121                   dac8 [6] = 1'b1;
122                   i = 3'b101;
123                   end
124               3'b101 : begin
125                   dac8 [6] = ~comp;
126                   dac8 [5] = 1'b1;
127                   i = 3'b111;
128                   end
129               3'b111 : begin
130                   dac8 [5] = ~comp;
131                   dac8 [4] = 1'b1;
132                   i = 3'b110;
133                   end
134               3'b110 : begin
135                   dac8 [4] = ~comp;
136                   dac8 [3] = 1'b1;
137                   i = 3'b010;
138                   end
139               3'b010 : begin
140                   dac8 [3] = ~comp;
141                   dac8 [2] = 1'b1;
142                   i = 3'b011;
143                   end
144               3'b011 : begin
145                   dac8 [2] = ~comp;
146                   dac8 [1] = 1'b1;
147                   i = 3'b001;
148                   end
149               3'b001 : begin
150                   dac8 [1] = ~comp;
151                   dac8 [0] = dac8 [1];
152                   i = 3'b100;
153                   ris7 [6] = dac8 [7];
154                   ris7 [5] = dac8 [6];
155                   ris7 [4] = dac8 [5];
156                   ris7 [3] = dac8 [4];
157                   ris7 [2] = dac8 [3];
158                   ris7 [1] = dac8 [2];
159                   ris7 [0] = dac8 [1];
160                   end
161            default : begin
162                   ris7 = ris7;
163                   dac8 = dac8;
164                   i = 3'b100;
165                   end
166
167               endcase
168 end
169 end
170 end
171 assign reset_vout = rst_n & mode ;
172 assign reset_vbat = rst_n & ~mode ;
173 assign roint = ((mode)==1) ? (dac5+dref) : dac8;
174 assign prec = ((sample & mode)==1) ? 8'b11000111 : 8'b00000000;
175 assign ro = ((sample)==0) ? roint : prec;
176 assign ron = ((sample)==0) ? ~roint : ~prec;
177 assign pre = ((sample & mode)==0) ? 1'b0 : 1'b1;
178 assign pre_n = ((sample & mode)==0) ? 1'b1 : 1'b0;
179 assign res = ((sample & ~mode)==0) ? 1'b0 : 1'b1;
180 assign res_n = ((sample & ~mode)==0) ? 1'b1 : 1'b0;
181 assign comp4 = (mode & ~sample );
```

```
182   assign comp4_n = ~comp4;
183   assign comp7 = (~mode & ~sample);
184   assign comp7_n = ~comp7;
185   assign mode_n = ~mode;
186   assign clock_n = ~clock;
187
188   endmodule
```

The code can be explained with the help of the conversion example shown in Figure 3.24.

- *Line (1 ÷ 35)* — Before the actual code, input and output pins, as well as variables are declared.
- *Line (38 ÷ 56)* — At the positive edge of the *Sample* signal, the D_{REF} word is read and adjusted with the pre-charge word. Note that the charge injection induced by S_L and S_M while loading the capacitive array is not compensated, resulting in a voltage offset on the DAC. To compensate it the word which is substrated from D_{REF} has been increased to 34LSB (*Ph*1 and *Ph*3).
- *Line (58 ÷ 102)* — At the negative edge of the clock signal (*SAR*) if *Mode* is "1" starts the V_{OUT} approximation cycle (*Ph*4). The 4-bit DAC command register is set according to the comparator output. If the reset signal is high the register is set to zero (*Ph*3).
- *Line (104 ÷ 167)* — At the negative edge of the clock signal (*SAR*) if *Mode* is "0" starts the V_{BAT} approximation cycle (*Ph*2). The 7-bit DAC command register is set according to the comparator output. If the reset signal is high the register is set to zero (*Ph*1).
- *Line (171 ÷ 186)* — At the SAR cycle end the output registers are written depending on the values of *Mode* and *Sample*

Referring to Figure 3.24, the operation of the circuit is the following:

- *Ph*1 — The 7-bit DAC register *ro* is forced to zero to reset the capacitor array to zero.
- *Ph*2 — The SAR 7-bit cycle is performed and the *ro* register is set according to the comparison results. At the end, the *ris*7 output register is written with the 7-bit result.
- *Ph*3 — The 7-bit DAC register *ro* is reset to the pre-charge word, in order to obtain the desired 230 mV on the capacitor array.
- *Ph*4 — The SAR 4-bit cycle is performed and the *ro* register is set according to the comparison results. At the end the output register *ris*4 is written with the 4-bit result.

3.3.7 Layout

In a SAR ADC the layout is very important for the performance. The DAC cell symmetry is the most important aspects which affects the mismatch. To reduce the mismatch effect it is useful to implement one unitary cell, consisting of a unit capacitance C and its control switch, and then connect in parallel a number of cell according to the desired capacitor value (e. g. $2^3 \cdot C$ will be realized with 8 parallel unitary cell). It is also important to ensure the same boundary conditions to all the cells. We used plate capacitors, which
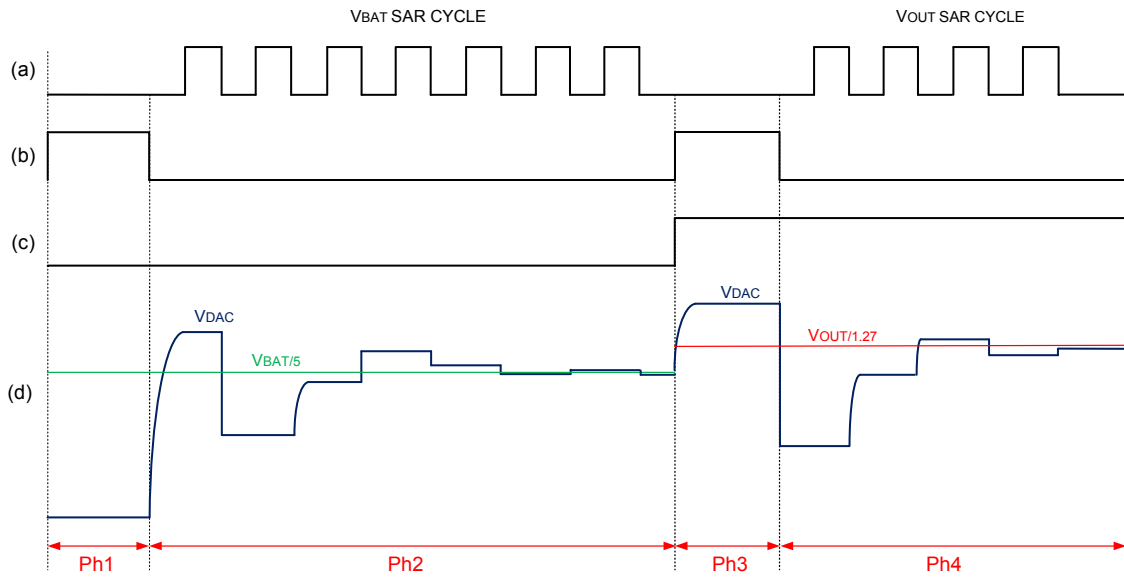
Figure 3.24: Circuit operation example: *SAR* (a), *Sample* (b), *Mode* (c), DAC voltage, V_{BAT} and V_{OUT} (d)

guarantee a better matching than fringing capacitors, in spite of a larger area. The unitary cell is shown in Figure 3.25. To optimize the size the command switch is placed under the capacitor, which employs the metals 2 to 5 of the 7 available in this technology.

The complete capacitive array is shown in Figure 3.26. On the edges dummies capacitors have been added to maintain the same boundary conditions. The yellow line are the switch command phases, while the power rail are gray.

The complete ADC layout is shown in Figure 3.27. The area is 150 μm × 140 μm = 0.021 mm^2. The capacitive sampling circuit for V_{OUT} has been placed on a side, while the digital logic is placed at the bottom to separate it from the analog part.

3.3.8 Experimental Results

The measurement results of the complete digital SMPS are reported in Section 2.3.2. However, we also verified the performance of the SAR ADC stand-alone. To measure the performance in the V_{BAT} conversion we just applied the input signal to the ADC, while for the V_{OUT} conversion we also applied different values of D_{REF}.

Figure 3.28 shows the digital output of the ADC as a function of V_{BAT} (0.27 V ÷ 0.98 V). The resulting INL and DNL are shown in Figure 3.29. The worst INL and DNL values are equal to 0.6 LSB.

The linearity gets worse with signals near the full scale due to the increased comparator common-mode voltage. The results improve by increasing the comparator bias current, which helps the regenerative operation.

Table 3.1 summarizes the main performance obtained in the V_{BAT} and V_{OUT} conver-
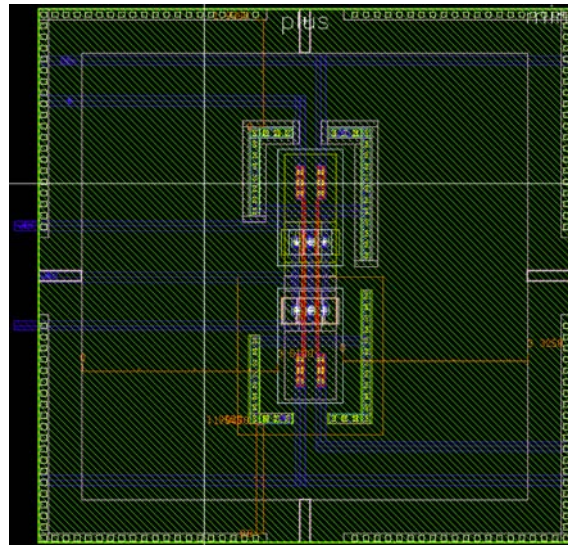
Figure 3.25: Unitary capacitor and switch cell layout

sions. Moreover, the output spectrum of the ADC with a sinusoidal input signal, altho not important for the SMPS application, is shown in Figure 3.30 for completeness. The achieved SNR is 34 dB.
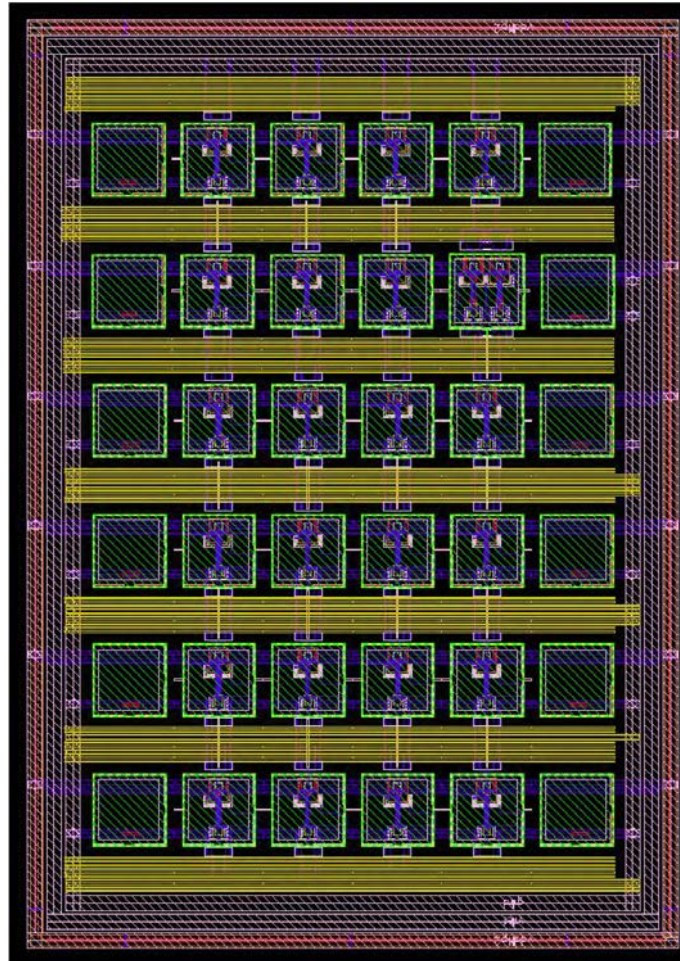
Figure 3.26: DAC capacitive array layout

Figure 3.27: Complete ADC layout
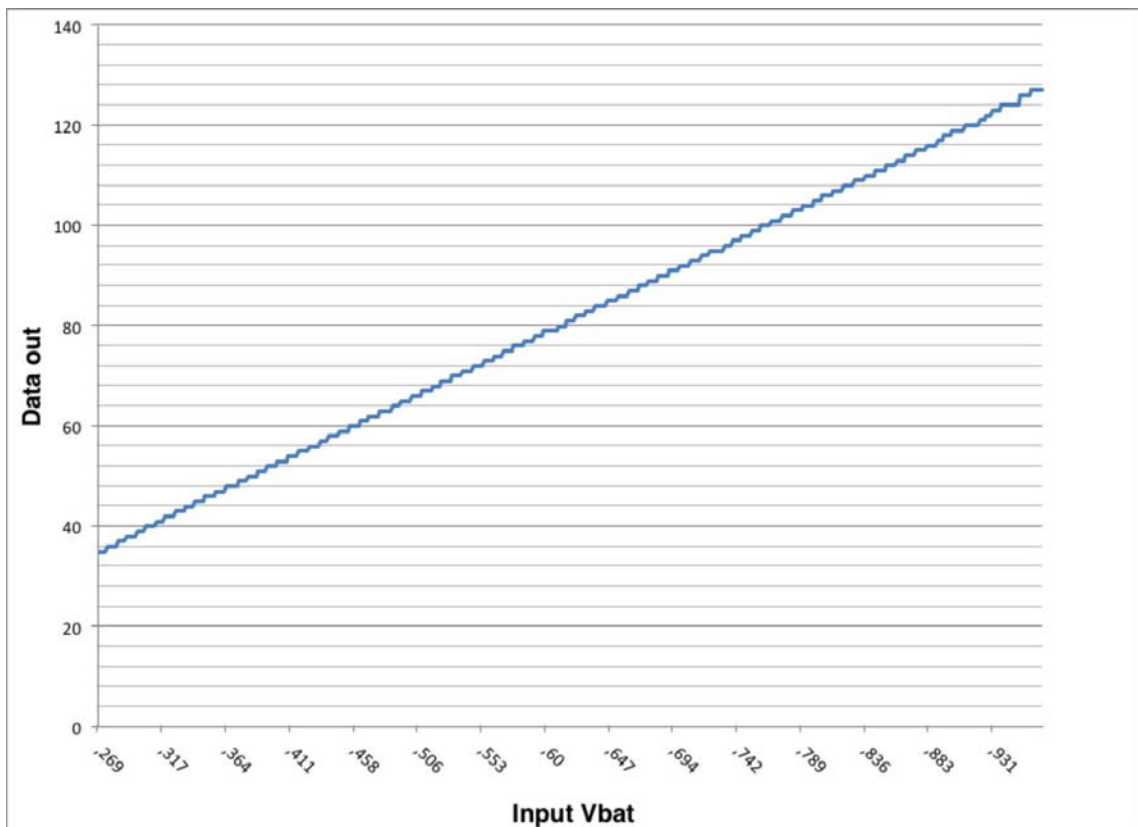
Figure 3.28: Measured ADC output code as a function of V_{BAT}
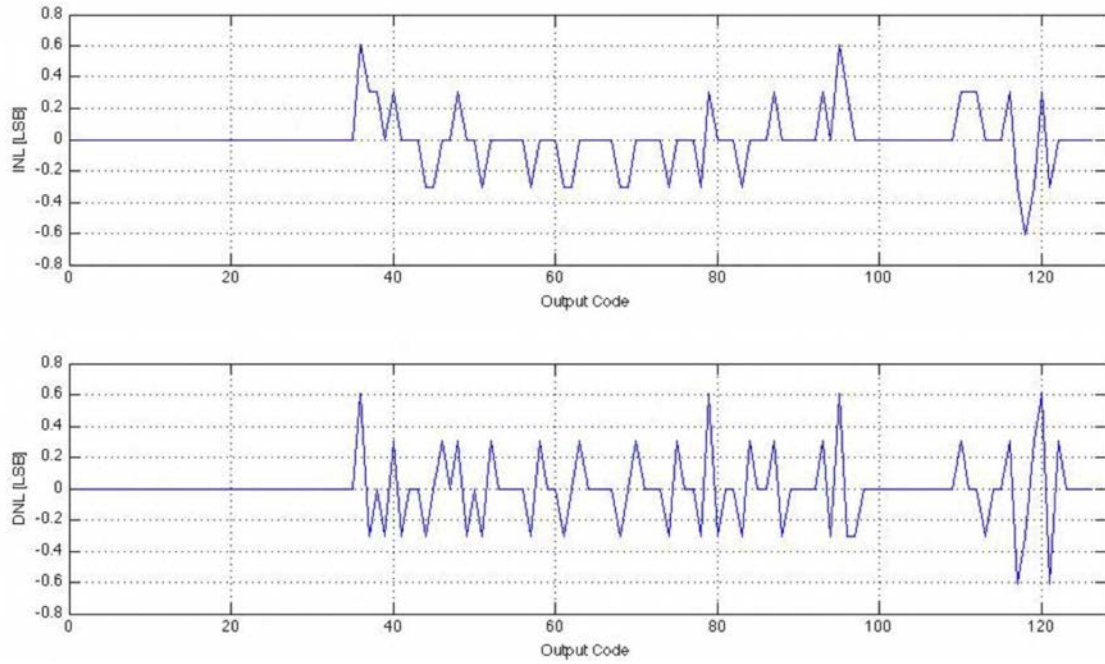
Figure 3.29: Measured INL and DNL of the ADC
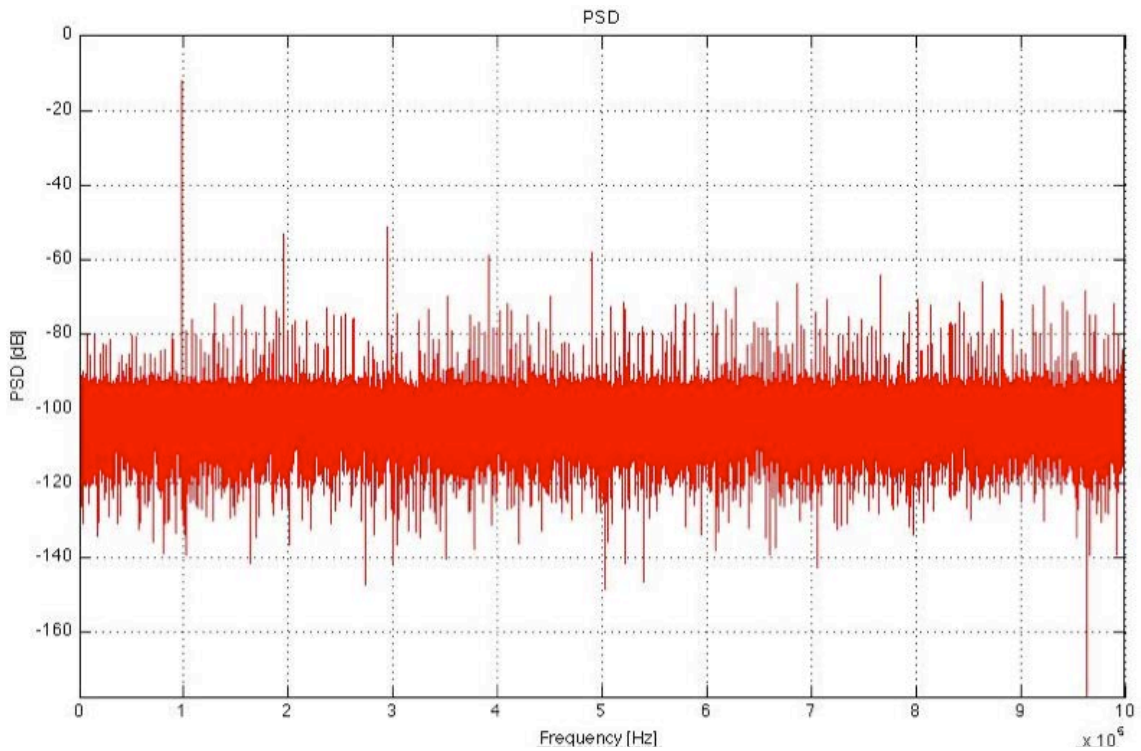
Figure 3.30: ADC output spectrum with a sinusoidal input signal at 1 kHz

Table 3.1: SAR ADC performance summary

Parameter	Value
Process	CMOS 65 nm
Power supply voltage	1.2 V
Bias current	1 μA
V_{BAT} input signal	Input range 2.3 V ÷ 4.8 V Scale factor = 5 LSB = 39 mV Resolution = 7 bits
V_{OUT} input signal	Input range 0.55 V ÷ 1.45 V Scale factor = 1.27 LSB = 10 mV Resolution ($V_{REF} - V_{OUT}$) = 4 bits
Analog power consumption	19 μW
Digital power consumption	33 μW
Analog power consumption (sleep mode)	0.8 μW
Digital power consumption (sleep mode)	0.5 μW
Sampling rate	9.9 MS/s
Clock frequency	153 MHz
V_{BAT} conversion linearity	INL = 0.6 LSB DNL = 0.6 LSB
V_{OUT} conversion linearity	INL = 0.6 LSB DNL = 0.6 LSB
Unit capacitor C	25.5 fF
Active area	0.021 mm^2

Chapter 4

ΣΔ ADC for Digital Class-D Amplifier

In this chapter we will describe the A/D converter designed to realize the feedback branch in the digital class-D audio amplifier described in the Section 2.6.

In the Chapter 2 some ADC topologies have been evaluated, each characterized by one or more features (e. g. low power consumption, high resolution and high sampling frequency), which make them suitable for specific applications. For example the SAR ADC, used for the digital SMPS, features very low power consumption, but it reaches low sampling frequency and medium resolution.

In the audio field high resolution and high linearity are required over a relatively small bandwidth, thus making oversampled ADCs the perfect candidates. Indeed, sigma delta (ΣΔ) modulators are quite popular in audio applications, since they achieve high resolution through noise shaping and oversampling techniques.

4.1 Basic ΣΔ Modulator Theory

The principle of operation of a ΣΔ modulator is illustrated in Figure 4.1. The circuit consists of a loop filter, which in its simplest form is an accumulator or integrator, followed by an A/D converter which introduces a quantization error E. The digital output signal is subtracted from the analog input via a D/A converter in the feedback path. The error E due to the quantization process is the difference between the analog quantizer input signal and the quantized digital output signal. Suppression of the quantization error in a ΣΔ modulator is provided by two mechanisms: oversampling and noise shaping. Since the reduction of the quantization error is quite effective, a high-resolution digital output is obtained, using a low-resolution quantizer. In many cases, a one-bit quantizer with two output levels is sufficient.

4.1.1 Oversampling

A one-bit quantizer generates a bitstream with output levels $\pm\frac{q}{2}$, where q is the quantization step size. The bitstream spectrum contains information about the input signal as well
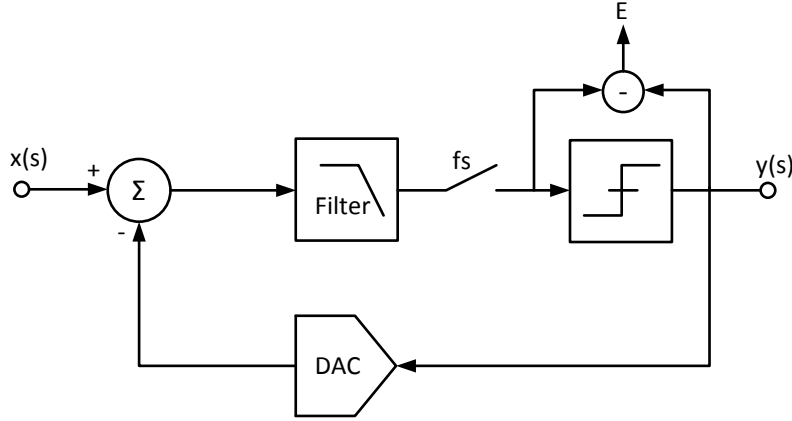
Figure 4.1: General ΣΔ modulator block diagram

as the quantization error, which is introduced by the quantizer. Assuming the quantization error to have a white noise spectrum [30] and to be uniformly distributed in the range $\pm\frac{q}{2}$ [31], we obtain the quantization noise power as:

$$e_{rms}^2 = \frac{1}{q} \int_{-\frac{q}{2}}^{\frac{q}{2}} e^2 de = \frac{q^2}{12}. \tag{4.1}$$

The power spectral density of the quantization error signal is then:

$$E(f) = \frac{q^2}{6f_s}; \;\; 0 \leq f < \frac{f_s}{2}, \tag{4.2}$$

where f_s is the sampling frequency. From (4.2) it is evident that the higher is the sampling frequency, the lower is the noise power spectral density.

Figure 4.2 shows the power spectral density, $E(f)$, of the quantization noise for Nyquist rate sampling with rate f_{s1} and oversampling rate f_{s2}. For Nyquist rate sampling, the signal band is $f_b = f_{s1}/2$ and all the quantization noise power, represented by the shaded area, has to be considered. In the oversampled case, the same noise power, represented by the area of the unshaded rectangle, has been spread over a bandwidth equal to $f_{s2}/2$, which is much larger than f_b. Only a relatively small fraction of the noise power falls in the band $[-f_b, f_b]$, while the noise power outside the signal band can be filtered out.

The total in-band quantization noise power is equal to:

$$N_q = \int_0^{f_b} E(f)df = \frac{e_{rms}^2}{OSR}, \tag{4.3}$$

where f_b is the signal bandwidth, and OSR the oversampling ratio, given by:

$$OSR = \frac{f_s}{2f_b}. \tag{4.4}$$
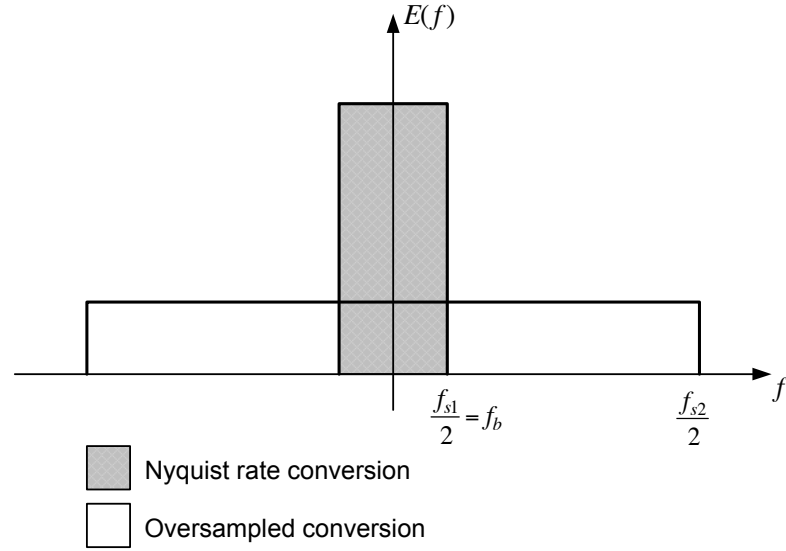
Figure 4.2: Oversampling principle

By doubling the sampling frequency the quantization noise power is reduced by 3 dB and the resolution is increased by half a bit. The *ENOB*, defined in (3.12), can be written as a function of the *OSR* as:

$$ENOB = n + 0.5 \cdot \log_2(OSR), \tag{4.5}$$

where n is the number of bits of the quantizer. By combining (3.12) and (4.5) it turns out that an increase of the *OSR* by a factor four improves the ADC resolution by 1 bit, as expected. This is valid for any ADC which is operated at a sampling frequency larger than twice the signal bandwidth.

4.1.2 Noise Shaping

For low frequency signals, the DAC in the feedback path has a gain of approximately 1. Figure 4.3 shows a highly simplified linear model of a ΣΔ modulator. Using this model, the output $Y(s)$ of the modulator is given by:

$$Y(s) = \frac{H(s)}{1 + H(s)} \cdot X(s) + \frac{1}{1 + H(s)} \cdot E(s), \tag{4.6}$$

where $X(s)$ is the analog input signal and $H(s)$ is the loop-filter transfer function. The first term of the right-hand side of (4.4) is the Signal Transfer Function (STF) and the second term is the Noise Transfer Function (NTF). If $H(s)$ has a lowpass filter characteristic with high DC gain, then for low-frequencies the STF is close to 1, while the quantization error tends toward zero (NTF is 0). For frequencies close to half the sampling frequency, the input signal is filtered and the quantization error becomes large. This shows that
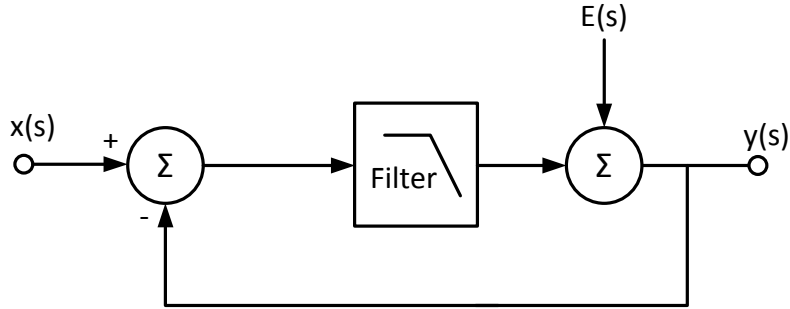
Figure 4.3: Simplified linear model of a ΣΔ modulator

the quantization noise spectral density is not constant over frequency, but has a shaped frequency spectrum. This is the principle of noise-shaping.

A more effective quantization noise shaping can be achieved by increasing the order of the loop filter or adding resonators to the loop. As shown in [32] the in-band quantization noise power of a 2$^{\text{nd}}$-order modulator is:

$$N_q \approx \frac{\pi^{2n}}{2n+1} \cdot \frac{e_{rms}^2}{OSR^{(2n+1)}}.$$

(4.7)

Figure 4.4 shows the quantization noise attenuation as a function of the *OSR* for different loop filter orders. The curve with slope equal to −10 dB per decade with $n = 0$ characterizes the case where the noise shaping is absent (just oversampling); the quantization noise attenuation then increases of 20 dB per decade whenever the filter order is increased by 1. Therefore, increasing the filter order is more effective than increasing the *OSR*. This is a significant improvement compared to (4.3) and it enables the use of a low resolution internal quantizer. However, increasing the filter order could lead to instability and appropriate compensation techniques must be adopted.

4.2   ΣΔ Modulator Circuit Topologies

The general ΣΔ modulator architecture illustrated in Figure 4.1 and Figure 4.3 can actually be implemented with Discrete-Time (DT) or Continuous-Time (CT) circuits.

4.2.1   Continuous-Time vs. Discrete-Time ΣΔ Modulators

Figure 4.5 shows the general block diagram of a ΣΔ modulator implemented either with CT or DT techniques. In a DT ΣΔ modulator a S/H stage is required at the input to convert the CT analog signal in a discrete-time signal. This block can limit the linearity and noise floor of the whole ΣΔ modulator and, furthermore, an anti-alias filter is needed in front of the sampler. In a CT ΣΔ modulator the sampling occurs only in the ADC and eventual
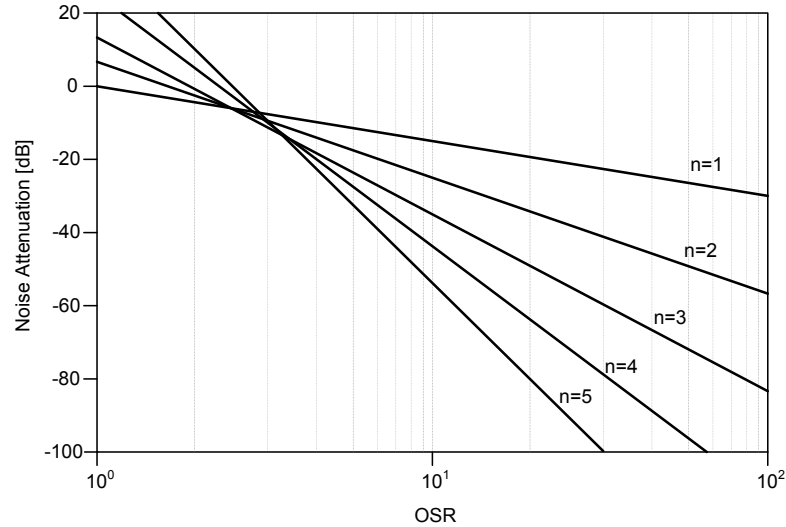
Figure 4.4: Theoretical in-band quantization noise attenuation as a function of the *OSR* for ΣΔ modulators of different order *n*

sampling errors are attenuated by the loop gain. The loop filter also operates as an anti-aliasing filter and, therefore, no filter is required at the input. This aspect will be quite important in the choice of circuit to use for the digital class-D amplifier. Indeed, since the anti-aliasing filtering is fundamental in the operation of the digital class-D amplifier, a DT solution would require an additional circuit in the feedback loop, which would increase the delay.

The power consumption in CT ΣΔ modulators is usually lower than in their DT counterparts, thus making them suitable for high-speed and low-power applications. However, the linearity requirements are harder to achieve with CT than with DT circuits. For example CT circuits implemented with the active-*RC* or g_mC techniques, feature worse linearity performance than DT circuits implemented with the switched capacitor (SC) technique. Furthermore, the main drawback of CT circuits is the clock jitter sensitivity in the feedback DAC where the DT feedback signal is added to the CT analog input signal [33]. Time uncertainty in the feedback DAC raises the noise floor at the notch frequency, thus degrading the performance. The jitter effect can be reduced by using a return-to-zero (RZ) DAC [19] or by increasing the number of bits in the quantizer. A time-variant feedback waveform DAC, called an SCR-DAC, can also be used in order to reduce the effect of clock jitter, at the expenses of tougher requirements for the operational amplifiers and, hence, higher power consumption.

4.2.2 Feedforward vs. Feedback Compensation

Increasing the order of the loop filter of a ΣΔ modulator provides more aggressive quantization noise shaping and effectively improves the signal-to-quantization noise ratio. The

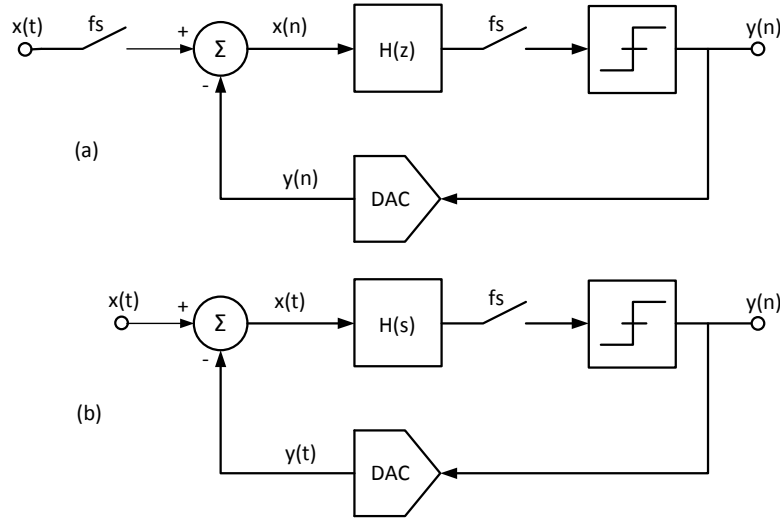Figure 4.5: Block diagram of DT and CT ΣΔ modulators

general transfer function of a CT n^{th}-order loop filter consisting of n integrators is given by:

$$H(s) = \left(\frac{\omega_u}{s}\right)^n, \tag{4.8}$$

where ω_u is the unity-gain frequency of the integrators. However, a ΣΔ modulator with the filter transfer given by (4.8 is not stable for $n > 1$. An uncompensated second-order loop-filter has $-180°$ phase shift at high frequencies. Feedforward and feedback compensation techniques are typically used for compensating the loop. Both compensation techniques can provide the same noise transfer function, but have different signal transfer function characteristics.

Feedforward Compensation

To ensure stability in a second-order ΣΔ modulator, a zero should be introduced in the loop-filter transfer function to reduce the high frequency phase shift. This can be done by adding a feedforward path in the loop filter, as shown in Figure 4.6. The choice for the ratio between c_1 and c_2 is determined by considerations concerning stability, maximum input level, signal-to-noise ratio and spread due to non-ideal processing. By increasing the coefficient ratio c_1/c_2 the zero in the loop filter transfer function is shifted toward lower frequencies. An optimum can be found, which provides both small phase shift at high frequencies and second-order noise shaping at low frequencies.

In general, filters of any order can be designed using this compensation technique. However, when increasing the filter order the zero locations move toward lower frequencies to achieve stability. Therefore, increasing the filter order decreases the effective bandwidth where quantization noise is shaped. This severely limits the maximum obtainable
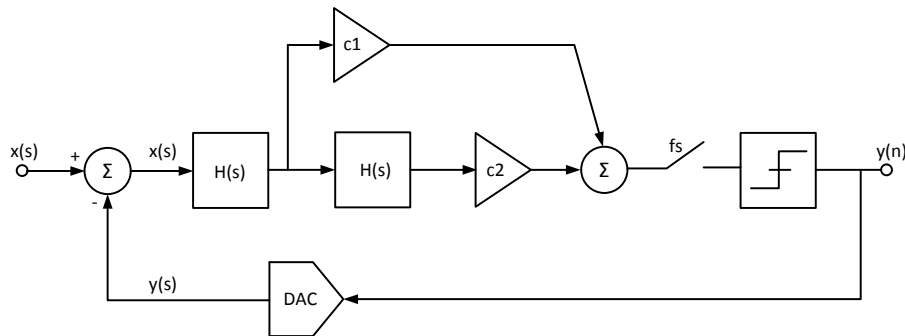
Figure 4.6: Second-order ΣΔ modulator with feedforward compensation
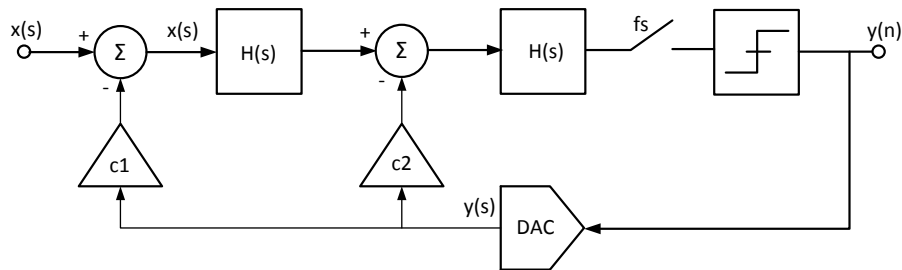
Figure 4.7: Second-order ΣΔ modulator with feedback compensation

bandwidth. An effective way to maintain sufficient noise shaping while guaranteeing stability is to introduce local feedback paths in the loop-filter, thus creating resonator stages. The resonator stages can provide some extra notches at the edge of the signal band, which suppress the quantization noise.

Feedback Compensation

An alternative way to stabilize the loop is to use feedback paths, as shown in Figure 4.7 for a second-order ΣΔ modulator. In this case, a fraction of the output is fed back to the input of each integrator stage of the loop-filter. Generally, the STF of an nth-order feedforward compensated filter has n poles and $n - 1$ zeros, while in a feedback compensated filter, the STF has n poles only. Therefore, in the feedforward case, the STF is a first-order low-pass filter (first-order anti-aliasing filter), while in the feedback case, the STF is an nth-order low-pass filter (n^{th}-order anti-aliasing filter). Clearly, the STF in a feedback compensated ΣΔ modulator provides much stronger filtering for high frequency signals than in the feedforward case. This is shown graphically in Figure 4.8 for a high-order modulator.

A further difference between the two compensation techniques is that, due to the zeros in the transfer function, in the feedforward case the STF is not flat at low frequencies, but

Figure 4.8: STF of a high-order ΣΔ modulator with feedforward compensation (a) and feedback compensation (b)

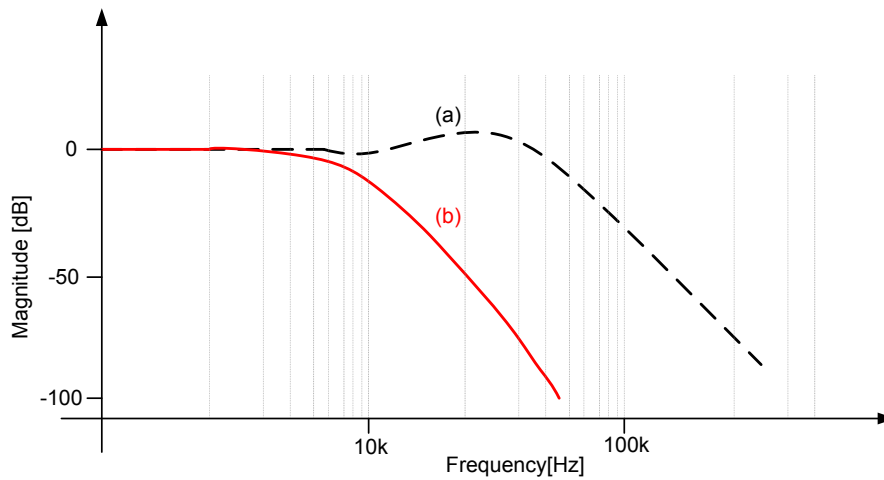shows some peaking at a certain frequency. This implies that at the peaking frequency the maximum stable input level is reduced by the gain of the peaking. This is not the case with the feedback technique, since the STF has no zeros, and, hence, no peaking occurs.

A major drawback of the feedback filter architecture is that the outputs of the integrators contain, besides the quantization noise, a substantial part of the input signal [31]. This implies that a larger output swing and a better linearity is required in the operational amplifiers, thus leading in general to a higher power consumption.

Often, feedforward and feedback compensation techniques are implemented together in order to obtain an optimal filter design.

4.2.3   Multi-Bit vs. Single-Bit Quantizer

The main motivation for adding more bits in the quantizer is the direct reduction of the quantization noise and of the jitter sensitivity. Furthermore with more bits in the quantizer, the stability constraints are easier to achieve than with single-bit structures and the internal signal swing is lower, thus alleviating the operational amplifier requirements in terms of output swing and slew rate. On the other hand, a larger number of bits in the quantizer increases the capacitive load of the amplifiers, which is a problem especially in high-frequency applications [34]. Moreover, more analog circuit components are needed to implement the internal ADC and DACs. The possibility of using higher gain in the integrators with multi-bit quantizer than in a single-bit loop, can improve the SNR by even more than 6 dB per additional bit. Moreover, in multi-bit ΣΔ modulators the out-of-band quantization noise is also reduced, which relieves the digital filtering required in the decimator. Despite the advantages of multi-bit structures, single-bit ΣΔ modulators are the most frequently used. The reason is the linearity requirement in multi-bit feedback DACs,
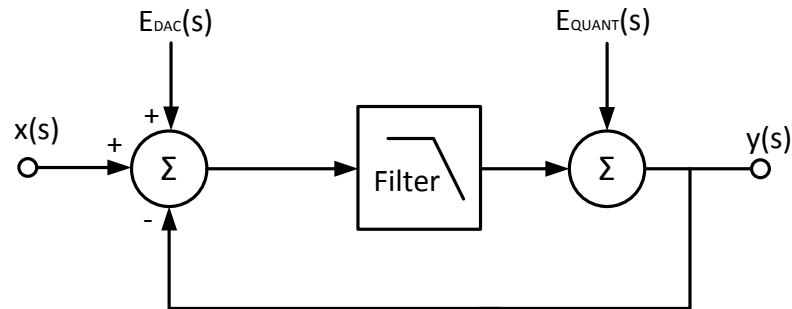
Figure 4.9: ΣΔ modulator whit non-linear DAC error (ϵ_{DAC})

which sets the upper limit for the ΣΔ modulator performance. The distortion introduced in the first-stage DAC, indeed, is not shaped, but it is directly added to the input, as shown in Figure 4.9.

Therefore, the linearity of the whole ΣΔ modulator cannot be better than the linearity of the DAC. The DAC linearity can be improved by element trimming, but this is expensive and it is not suitable for mass-produced products. Calibration techniques may also be utilized, but extra hardware and calibration time are needed [35]. Nowadays, different Dynamic Element Matching (DEM) techniques, which randomize and/or shape the distortion contribution of the DAC to improve the linearity over the signal band [36], are widely used.

4.3 Implemented ΣΔ ADC

As mentioned in Section 2.6, the closed-loop digital class-D amplifier requires an ADC to close the feedback loop, featuring large dynamic range, good linearity, and intrinsic anti-aliasing filtering, thus making a CT ΣΔ modulator one of the best candidates.

4.3.1 Requirements and Specifications

Particular features are required for a ΣΔ modulator suitable to realize the feedback branch in a digital class-D audio amplifier. High linearity and SNR are required, but a low latency is mandatory to ensure the system stability. Moreover, in order to be competitive with analog solution it has to ensure a low power consumption. Finally, intrinsic anti-aliasing filtering is required, to avoid an additional filter which would increase the latency. The main requirements are summarized in Table 4.1.

Considering the system requirements, the best circuit topology for implementing the ADC can be identified through the following considerations.

- *Anti-aliasing filtering* — To ensure an intrinsic anti-aliasing filtering a CT ΣΔ modulator must be adopted. To increase the filtering effect a nth-order modulator with feedback compensation must be used.

Table 4.1: ΣΔ ADC requirements

Parameter	Value
Process	CMOS 40 nm
Power supply voltage	1.1 V
Bias current	1 μA
Max power consumption	1.5 mW
Resolution	5 bits
Sampling frequency (f_s)	3.072 MHz
Bandwidth (f_b)	20 kHz
Oversampling ratio (OSR)	64
Signal-to-noise ratio (SNR)	$\geq$ 100 dB
Dynamic range (DR)	$\geq$ 100 dB
Maximum latency	$\approx$ 1 μs
Active area	0.9 mm^2

- *Power consumption* — A DT switched-capacitor circuit needs very fast operational amplifier with a bandwidth (f_o) much larger than the sampling frequency (f_s), while in a CT solution f_o may be comparable to f_s, thus reducing the power required.
- *High SNR* — An nth-order modulator, with M-bit quantizer and oversampling ratio equal to *OSR*, theoretically, achieves a SNR given by:

$$SNR = \frac{2^{2M}3(2n+1)OSR^{2n+1}}{2\pi^{2n}}. \tag{4.9}$$

With M = 5 bits and OSR = 64, the required SNR (100 dB), can be obtained with n = 3, thus guaranteeing inherently third-order anti-aliasing filtering. Another aspect to be considered for maximizing the achievable SNR is the topology used. Indeed, in a DT solution the thermal noise is determined by sampling capacitors (kT/C noise). To reduce the kT/C noise in a DT loop, an input capacitor of the order of several hundred picofarads is required. This large capacitor occupies a large area and could cause non-linear settling of the analog input signal. Therefore, a CT solution in which the thermal noise is determined by resistances, which have to be small, is preferable.

For these considerations, the best solution to meet the requirements is a 3$^{\text{rd}}$-order, feedback compensated, CT ΣΔ modulator topology. The jitter sensitivity is an issue and must be evaluated to find a solution which allows us to achieve the desired SNR.

4.3.2   ADC Architecture

The first step in the design of a ΣΔ modulator is the implementation of an ideal model in Matlab. Thanks to the *DelSig* toolbox, publicly available, it is possible to obtain automat-

Table 4.2: Coefficients of the ΣΔ modulator

Coefficient	Value from *DelSig*	Actual Value
a_1	0.044	0.044
a_2	0.287	0.287
a_3	0.8	0.8
b_1	0.044	0.044
b_2	0.287	0
b_3	0.8	0
c_1	1	1
c_2	1	1
c_3	1	1
g_1	0.001	0

ically the filter coefficient values required to guarantee system stability. This toolbox is designed for DT modulators. Therefore, to analyze the performance of a CT circuit (SNR and stability), we have first to derive the equivalent *s*-domain transfer function of the filter from the DT counterpart. The transfer function of a DT integrator, $H(z) = 1/(z-1)$, can be replaced by the transfer function of the corresponding CT integrator, $H(s) = f_s/s$, using the Euler transformation. The achieved noise-shaping of the resulting CT ΣΔ modulator will then be identical to its DT counterpart.

The *DelSig* toolbox allows selecting the topology of the filter between Cascade of Integrators with FeedBack (CIFB), with feedback compensation, shown in Figure 4.10(a), and Cascade of Integrators with FeedForward (CIFF), with feedforward compensation shown in Figure 4.10(b). As described above we decided to implement the feedback structure to ensures a better anti-aliasing filtering. However, in the CIFB scheme available in the *DelSig* toolbox, in addition to the feedback branches, also feedforward branches are included. With the feedforward paths only the quantization noise flows through the integrators, thus allowing more relaxed operational amplifier specifications. However, the feedforward paths also degrade the anti-aliasing filtering effectiveness, and, therefore, we decided not to include these paths (b_2 and b_3). Moreover, we also removed the local resonator g_1, in order to minimize the component spread required to implement the coefficients. The circuit implemented is shown in Figure 4.10(c). Figure 4.11 and Figure 4.12 show the STF achieved with the conventional CIFB and the modified CIFB topologies, respectively. Table 4.2 summarizes the used coefficient values.

4.3.3 Quantizer

The quantizer in a ΣΔ modulator is not a very critical circuit block in terms of noise and distortion, because of the large gain of the preceding blocks. Therefore, a flash ADC is the natural choice, since it allows the A/D conversion to be performed in just one clock

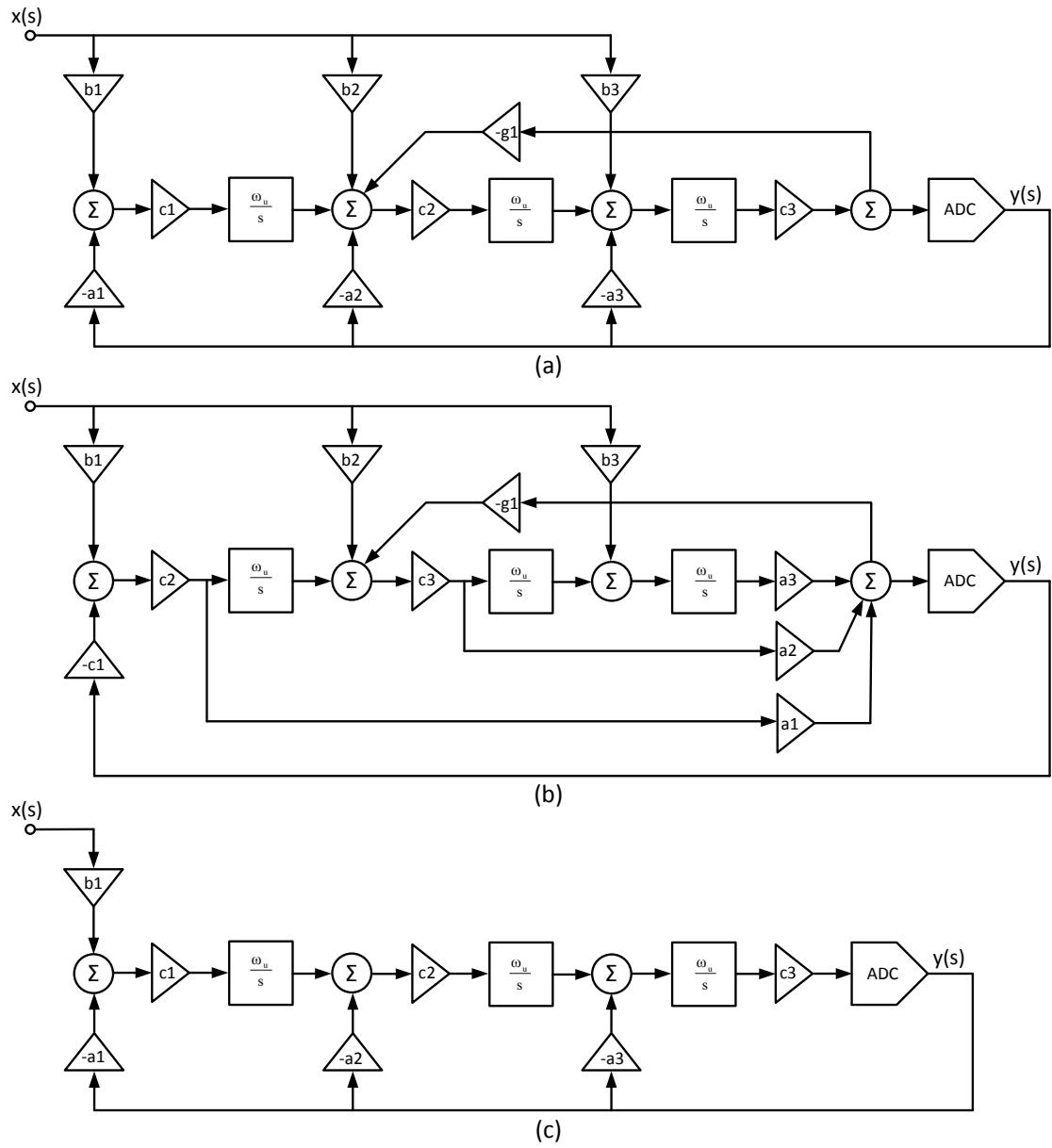Figure 4.10: Third-order ΣΔ modulator: CIFB structure (a), CIFF structure (b) and implemented modified CIFB structure (c)
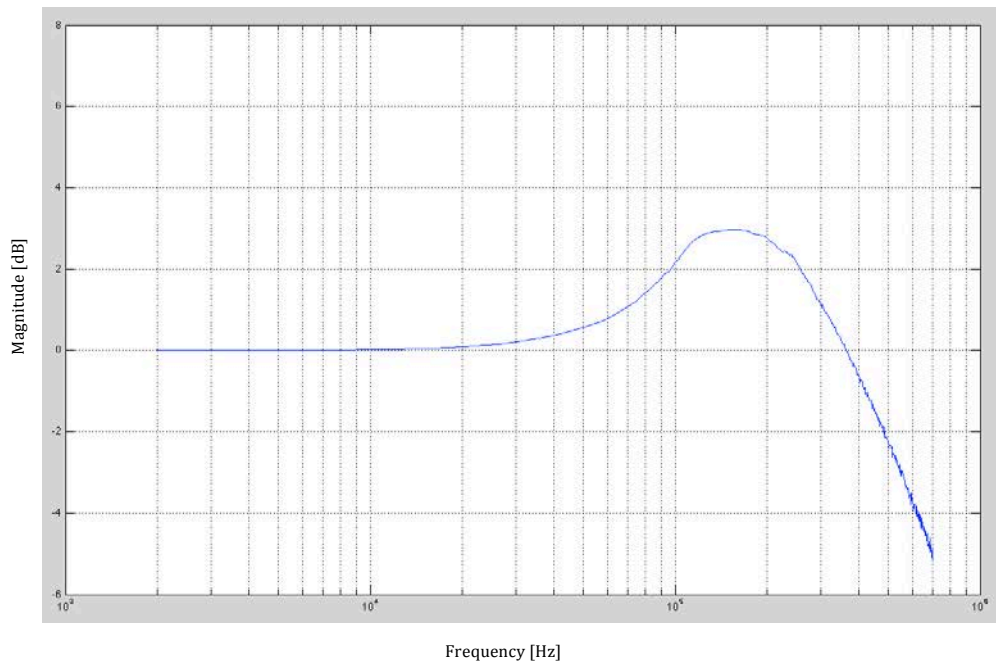
Figure 4.11: STF of the 3rd-order conventional CIFB structure
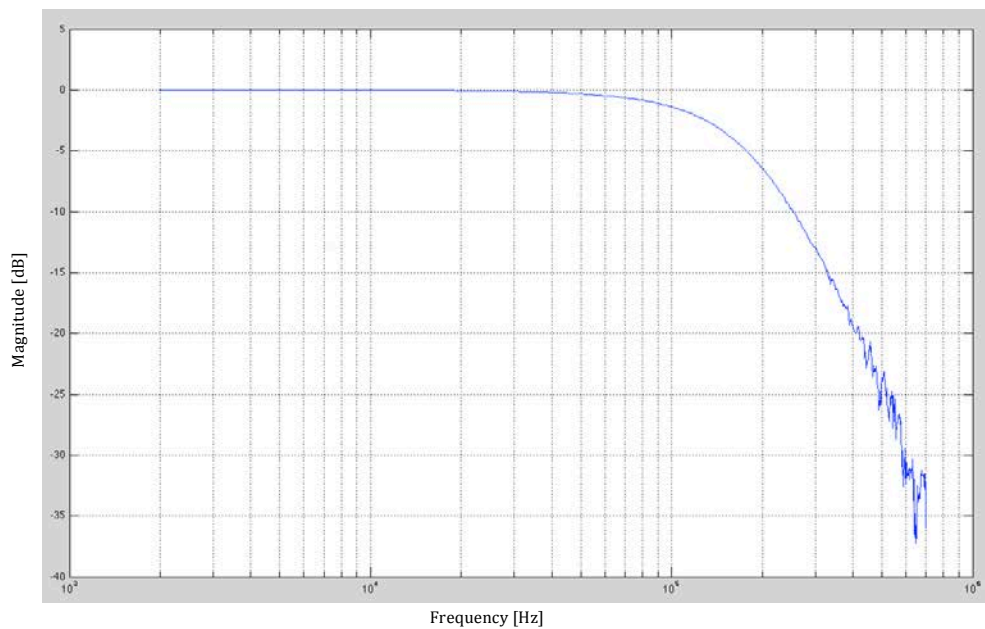

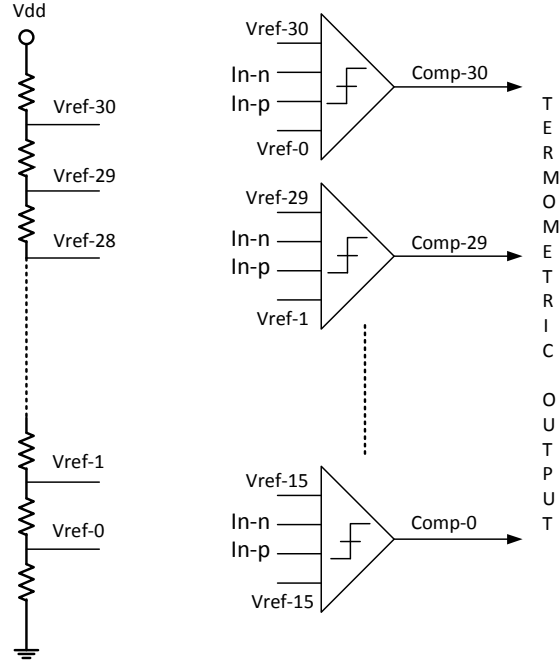Figure 4.12: STF of the 3rd-order modified CIFB structure

Figure 4.13: Block diagram of the quantizer

period. The implemented flash ADC, shown in Figure 4.13, features 32-levels, realized with 31 comparators that compare the input signal with a reference voltage ladder.

The reference voltages are realized through a resistive divider connected to a dedicate power supply. The 31 voltage levels are centered around the common mode voltage ($V_{DD}/2$ = 550 mV) and cover the required signal swing with 31 20-mV steps. The unit resistance has been fixed to 1 kΩ to reduce the quiescent current consumption (24 μA). The mismatch guaranteed by the technology is lower than $\Delta R/R = 1.8\%$.

The schematic of the comparator is shown in Figure 4.14. The circuit consists of two stages. The first stage, a continuous-time fully differential pre-amplifier, performs the difference between the input signals and compares it with the difference between the threshold voltages, according to:

$$V_{on} = A \cdot \left[\left(V_{ref+} - V_{In+}\right) - \left(V_{ref-} - V_{In-}\right)\right]$$
$$V_{op} = A \cdot \left[\left(V_{ref-} - V_{In-}\right) - \left(V_{ref+} - V_{In+}\right)\right],$$

(4.10)

where A is the DC-gain and V_{on} and V_{op} are the differential output signals of the pre-amplification stage. The output common-mode voltage of the pre-amplifier is controlled by the red MOS transistors, working in the triode region. The amplified difference between the input signals and the threshold voltages ($V_{op} - V_{on}$) is then passed to the latch, which, on the positive edge of the clock, determines the digital output signals, depending on its input. The continuous-time pre-amplifier reduces the comparator kick-back on the previous integrator output and guarantees a constant input capacitance, thus allowing the
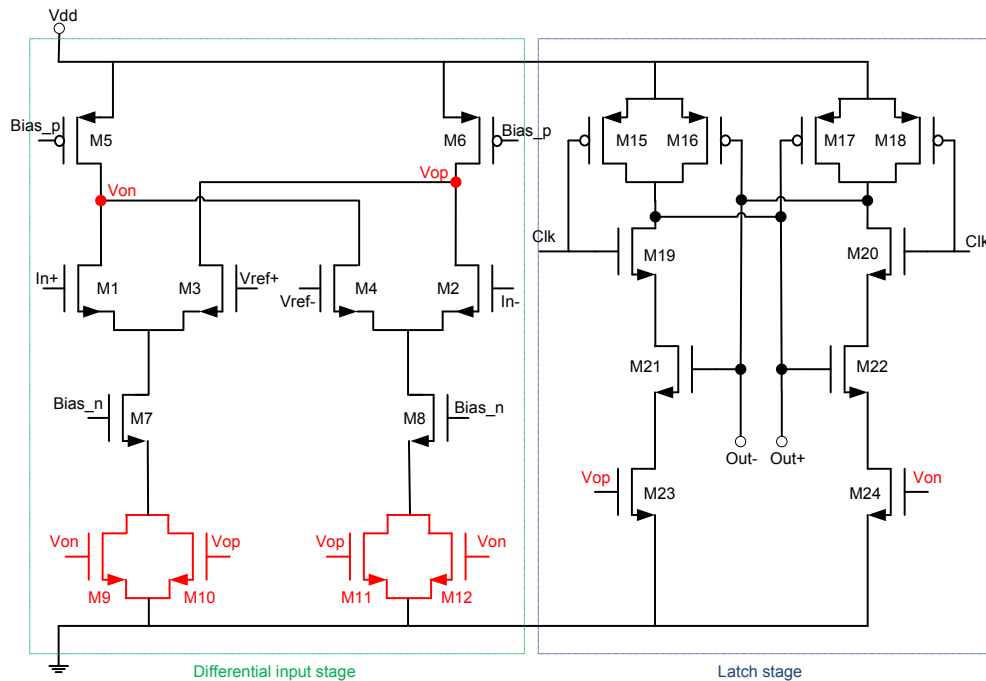
Figure 4.14: Schematic of the fully-differential comparator

optimization of the previous stage bandwidth and power consumption. The total current consumption is equal to $10\,\mu$A.

4.3.4 Digital-to-Analog Converter

The feedback DAC is most critical block in a CT ΣΔ modulator. As already mentioned, its linearity affects the linearity of the entire circuit and any noise components injected by the DAC cannot be distinguished from the input signal, thus degrading the SNR. A typical problem in CT modulators is the jitter sensitivity. Generally the feedback DAC pulses remain constant over the whole clock period, and, therefore, their integral varies linearly with the integration time, which is modulated by the clock jitter. This leads to an error which affects both the SNR and the linearity. The effect of the clock jitter strongly depends on the DAC implementation, thus requiring a careful choice of the best topology to use.

Current Steering and Resistive DACs

The current steering DAC, shown in Figure 4.15, is most common solution adopted in CT ΣΔ modulators. In this circuit a set of current mirrors are connected to the switches controlled by the quantizer output, thus adding or subtracting a given amount of current from the integrator summing node [37]. This solution is quite simple, since it does not
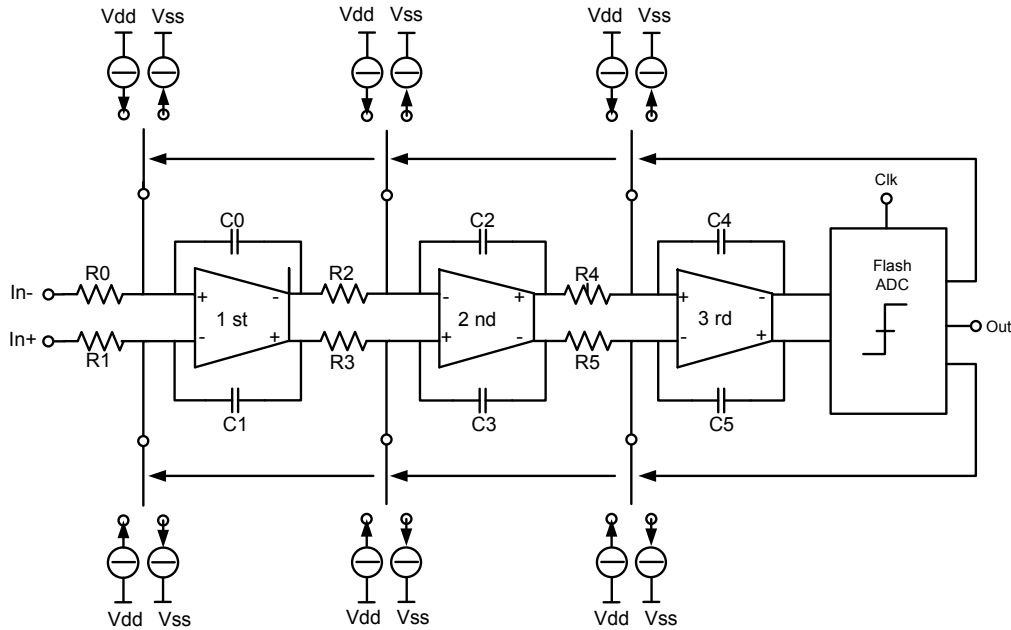
Figure 4.15: Current steering DAC

require any reference voltage, but is very sensitive to the clock jitter. This problem can be partially alleviated using the return-to-zero (RZ) code (i. e. the current goes back to zero at the end of each sampling period), which makes the error due to clock jitter independent of the input signal.

The major drawback of this solution is the switch charge injection, illustrated in Figure 4.16. The circuit can behave as shown in Figure 4.16(b) or Figure 4.16(c), depending on the size of the switches ($M3$, $M4$, $M5$, and $M6$), leading in any case to distortion.

Another solution to implement the DAC is to use resistive feedback branches [38], as shown in Figure 4.17. This solution is expensive in terms of power consumption, since the resistors should have small size to reduce the thermal noise ($4kTR$) the parasitic capacitance, which causes excess delay in the loop.

Switched-Capacitor-Resistor DAC

Considering the drawback of current steering and resistive DAC the solution adopted in the implemented ΣΔ modulator is the Switched-Capacitor-Resistive (SCR) topology, shown in Figure 4.18. During each clock cycle, the capacitors C_r store a precise amount of charge ($Q = C_r \cdot V$). The capacitors are then discharged into the integrator summing node through an additional resistor R_r, which defines an exponentially decaying current pulse, with time constant $\tau = R_r \cdot C_r$, according to:

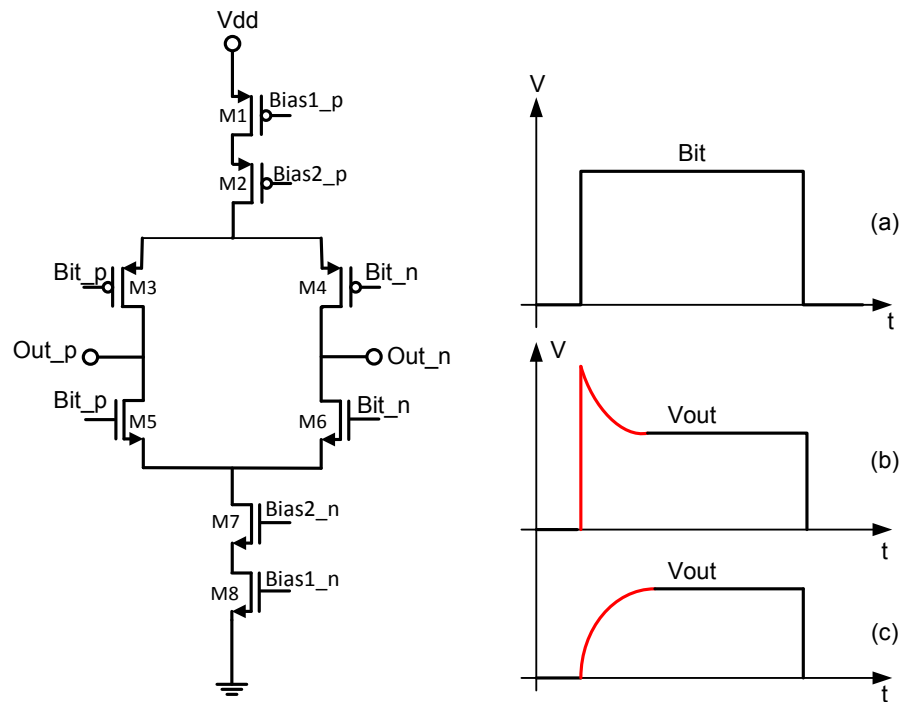$$I_c = \frac{V}{R_r} e^{-t/\tau}. \tag{4.11}$$

Figure 4.16: Unitary current mirror of a current steering DAC: command bit (a), error due to large switches (b) and error due to small switches (c)
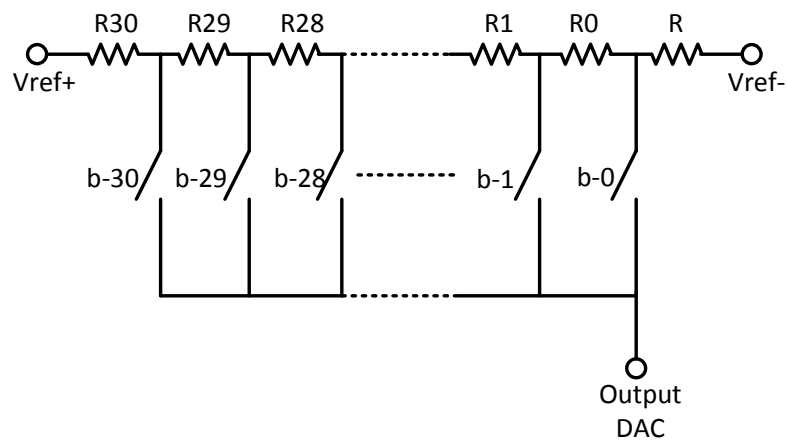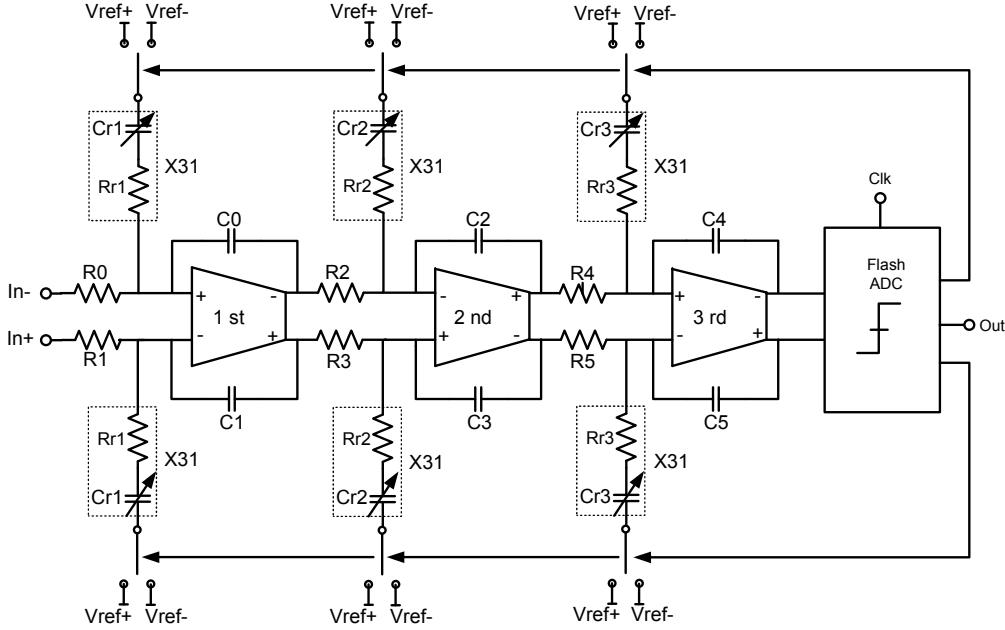
Figure 4.17: Resistive DAC

Figure 4.18: Switched-capacitor-resistor DAC

The main advantage of this structure is the insensitivity to clock jitter. Indeed, if the time constant τ is sufficiently smaller than the sampling period (T_s), the current injected in the integrator summing node goes inherently to zero before the end of each cycle, and therefore, the amount of charge transferred is well controlled and constant (given by Q), as shown in Figure 4.19. Obviously, the on-resistance R_{on} of the switches $M7$ and $M8$ must be such that $R_{on} \ll R_r$, so that τ is well controlled.

Referring to the detailed schematic of the implemented SCR DAC, shown in Figure 4.18, during half of the clock period, the capacitors are reset to the common-mode voltage V_{CM} (through $M3$, $M4$, $M5$, and $M6$). On the falling edge of the clock, one plate of the capacitor is connected to the integrator summing node (through $M7$ and $M8$), while the other is connected to V_{ref+} ($M1$) or V_{ref-} ($M2$), depending on the corresponding quantizer output. To limit the charge injection, dummy switches ($M9$ and $M10$) have been added. Being the quantizer resolution 5 bits, 31 DAC levels are required, which are obtained with 31 identical SCR branches. To ensure a constant capacitive load, independent of the input signal level, 31 capacitors are always connected to both V_{ref+} and V_{ref-} in the fully-differential structure. This is achieved by connecting the capacitors in complementary mode.

The first feedback branch is the dominant jitter error source, and hence τ should be sized accurately. On the other hand, the other feedback branches can be sized less aggressively, because the jitter error is shaped. Consequently the time constants have been chosen as:

$$\tau_1 = 7.5\% T_s, \ \tau_2 = 1.5\% T_s, \ \tau_3 = 3\% T_s. \tag{4.12}$$
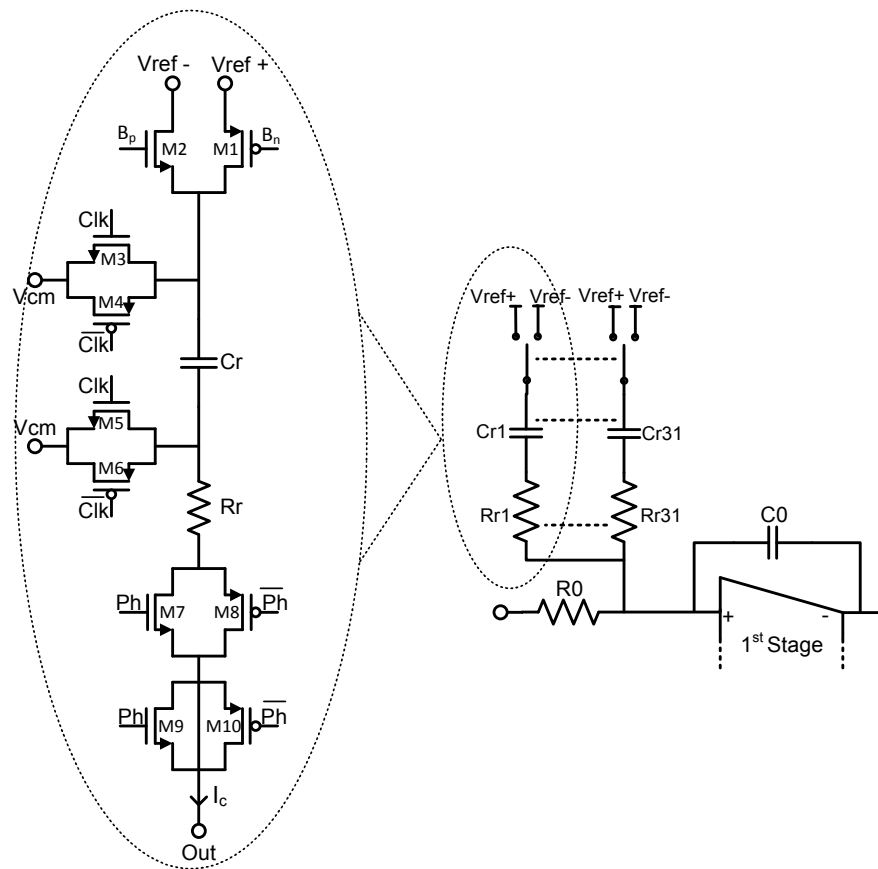
Figure 4.19: Detailed schematic of the implemented SCR DAC

An analytical calculation of the resulting jitter sensitivity [39] leads to:

$$N_j = \frac{(\frac{\Delta}{2})^2 (\frac{\sigma_t}{T_s})^2}{OSR} \cdot \left(\frac{T_s}{s\tau}\right)^2 e^{\frac{-T_s}{\tau}}, \qquad (4.13)$$

where T_s is the sampling period ($T_s = 1/F_s = 160$ nS), σ^2 is the variance of the clock period and Δ the quantizer step width. Furthermore, the capacitor size cannot be arbitrary, but depends on the noise contribution tolerated at the input to meet the SNR requirement. This aspect is important only in the first stage, where the noise contribution is:

$$V_{n,c}^2 = \left(\frac{2kT}{CA^2}\right), \qquad (4.14)$$

where A is the integrator gain, k the Boltzmann constant, T the absolute temperature and C the capacitor size. To ensure low input noise contribution and low jitter sensitivity, the first stage DAC is sized as: $R_{r,1} = 20$ kΩ and $C_{r,1} = 600$ fF ($\tau_1 = 12$ ns). Instead. the second and third stages, which do not affect the input noise, have been sized as: $R_{r,2} = 20$ kΩ, $C_{r,2} = 100$ fF, $R_{r,3} = 40$ kΩ, and $C_{r,3} = 100$ fF ($\tau_2 = 2$ ns and $\tau_3 = 4$ ns).

4.3.5 Integrators

The first integrator resistors and capacitors have been sized to satisfy the thermal noise requirements, taking into account the signal attenuation by a factor of 12 required to accommodate the 5-V power bridge output swing within the 400-mV ΣΔ modulator input range. Referring to Figure 4.18, the first stage has been sized with $R_1 = 163$ kΩ and $C_1 = 81$ pF. The resistors and capacitors of the second and third integrators have been scaled to optimize area, power consumption, and output swing: $R_2 = 160$ kΩ, $C_2 = 13$pF, $R_3 = 25$ kΩ and $C_3 = 6.5$ pF.

A SCR solution requires a more powerful integrator then a classical CT implementation with resistive or current steering DAC. To follow correctly the feedback pulse, the integrator bandwidth and slew-rate have to be larger than usual. However, they can still be smaller then in a DT solution, since the rising and falling times of the DAC pulses are limited by R_r (τ). Moreover, the first integrator determines the overall noise and linearity of the modulator, and, hence, low flicker noise and high linearity are required too. To comply also with the low power consumption required, a two stage unfolded class-AB operational amplifier, shown in Figure 4.20, was used in first stage. This architecture allows a better efficiency with respect to folded cascode or two-stage class-A topologies, reducing the quiescent current for the same performance [40].

Two important parameters of the push-pull, rail-to-rail output stage of this operational amplifier, formed by $M9$ and $M12$ ($M10$ and $M11$), are the output voltage range and the maximum output current that can be supplied to the load. Indeed, the output swing required in the absence of feedforward branches is pretty high. Therefore, in order to allow proper operation, the maximum differential input voltage has been fixed to 400 mV (-8 dB$_{FS}$). The ratio W/L of the output transistors has been chosen as large as possible
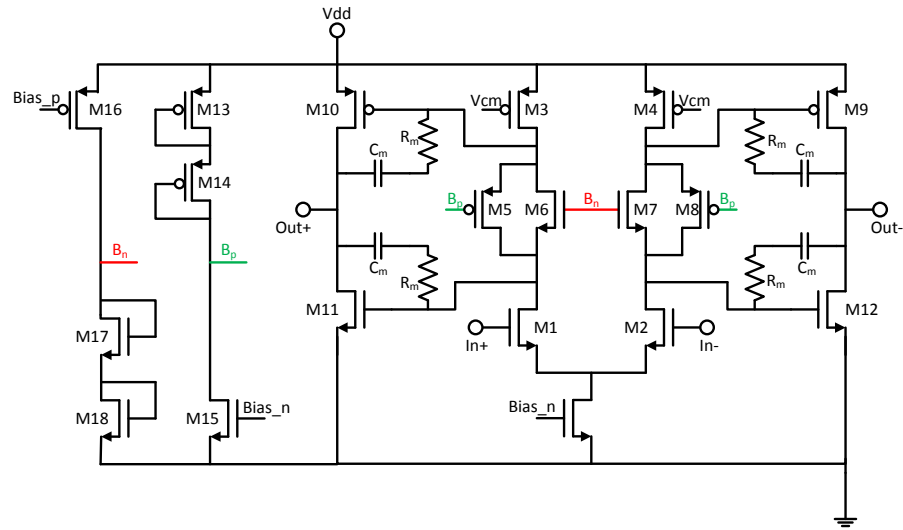
Figure 4.20: Operational amplifier used in the first integrator

to achieve rail-to-rail output swing. The virtual battery inserted between $M9$ and $M12$ ensures the proper biasing (quiescent current), while the available output current is determined by the aspect ratio of $M9$ and $M5$ ($M8$).

In the used class-AB topology each gain stage requires a separate common-mode feedback (CMFB) circuit, which is realized with a conventional CT structure. Miller-compensation (R_m and C_m) is used to guarantee stability. The bode diagram of the amplifier is reported in Figure 4.21.

The performance required for the operational amplifiers used in the second and third integrators are more relaxed and can be easily obtained with a conventional two-stage operational amplifier. Moreover, the noise introduced by these amplifiers is attenuated by first integrator gain. The performances obtained for each operational amplifier are summarized in Table 4.3.

Table 4.3: operational amplifier performance summary

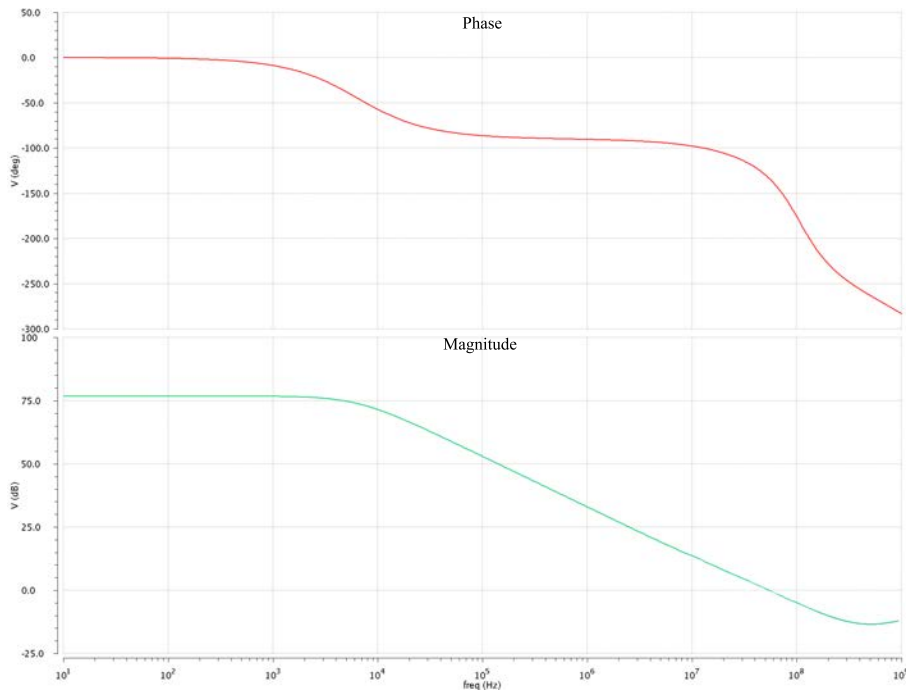| Stage	GBW [MHz]	DC Gain [dB]	Phase Margin [°]	Current [μA]
1st	50	66	50	800
2nd	80	50	58	170
3rd	80	50	58	170

Figure 4.21: Bode diagram of the operational amplifier used in the first integrator

4.3.6   Dynamic Element Matching Logic

To improve matching of the feedback capacitors, Dynamic Element Matching (DEM) is implemented. Dynamic element matching is based on periodic exchanging of reference elements which may have a mismatch. As a result, the mismatch is modulated with the exchange rate to another (out-of-band) frequency.

The main problem to implement the DEM randomization code is the excess-loop-delay which may produce instability in the system. For this reason, we implemented a simple Data Weighted Averaging (DWA) algorithm that only requires one logical step to obtain the randomization. Basically, the thermometric code produced by the quantizer is transformed into a binary code D and, in the DAC, D elements are connected to V_{ref+}. A pointer stores the position of the last used DAC element (D_0), so that the D required elements are selected starting from D_0. The value of D_0 is then updated to $D_0 + D$. An example is shown in Figure 4.22 for $D = 5$.

This solution ensures that the DEM introduces a small fixed time delay. Indeed, thanks to the 40-nm technology a very fast logic is obtained. The total time required to generate the DAC control bits from the comparator output is just over half clock period, which ensures the stability of the ΣΔ modulator.
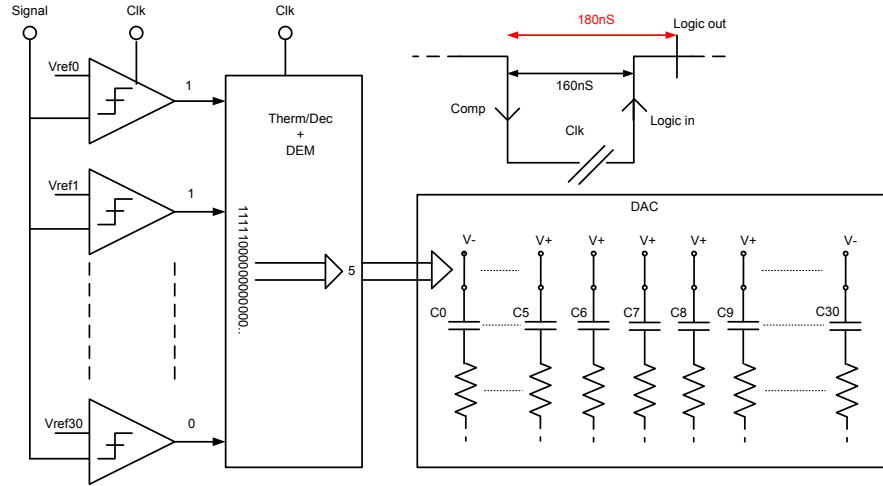
Figure 4.22: Dynamic element matching implementation and timing

4.3.7 Noise Analysis and Simulation Results

To ensure 100 dB of SNR, we simulated the noise contribution of each block as a function of the maximum input signal, thus obtaining:

$$SNR = 20 \log \frac{V_{SIGN}}{V_{NOISE}}. \tag{4.15}$$

Considering a maximum input signal equal to 0.4 V, the maximum input referred noise value is 2.82 μV. The noise contributions are the following:

- *Input resistance* — The input resistance ($R = 160$ kΩ) generates thermal noise with root mean square value equal to $V_{n,r}^2 = 4kTR$. However, the output signal amplitude of the class-D amplifier power bridge (i. e. the actual input signal of the ΣΔ modulator) is 5 V and, hence, the noise contribution is scaled by a factor of 12 when referred to the actual input, leading to $V_{n,r}^2 = 4kTR/144$.
- *Input stage* — In the operation amplifier of the first integrator, the input transistors generate Flicker noise given by $V_{n,f}^2 = k_F/(C_{ox}WLf)$.
- *RC feedback* — In the feedback branch the dominant noise contribution is due to capacitors (kT/C), scaled by the ΣΔ modulator gain (A): $V_{n,c}^2 = 2kT/(CA^2)$.

The total noise obtained in simulation is equal to 2.7 μV which ensures a $SNR = 101$ dB.

To analyze the anti aliasing filter proprieties of the ΣΔ modulator, we performed simulations with a PWM input signal. Figure 4.23 shows the obtained input and output spectra of the circuit, together with the ΣΔ modulator signal transfer function, thus highlighting the AAF effect.

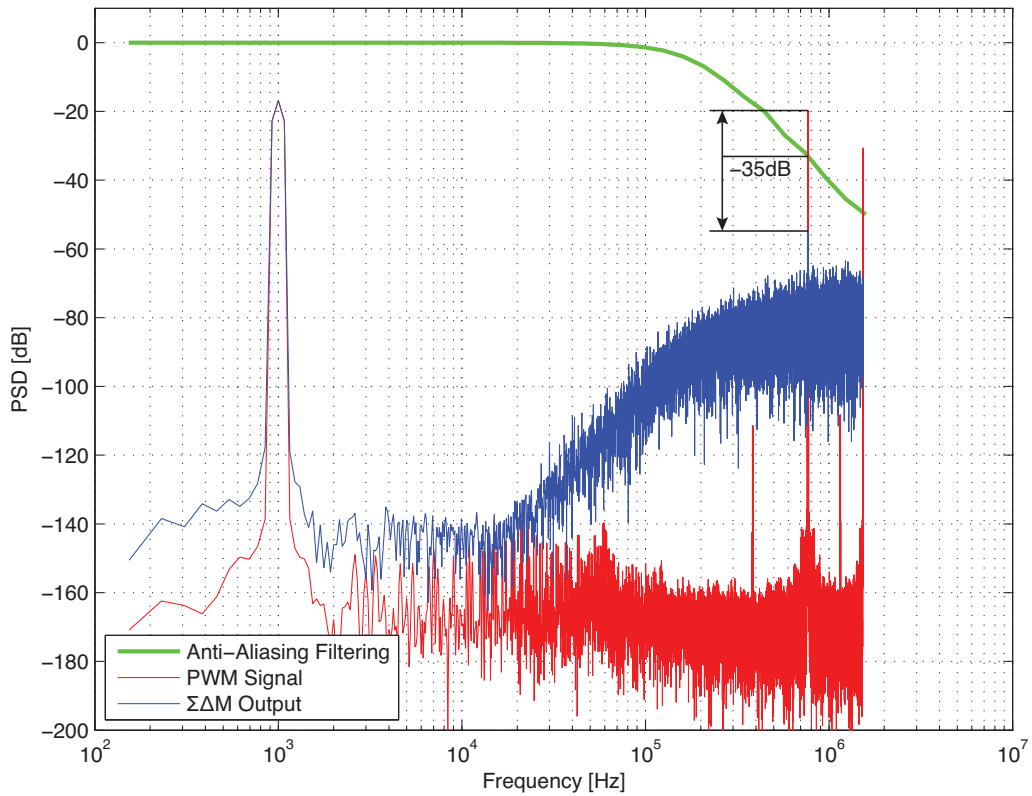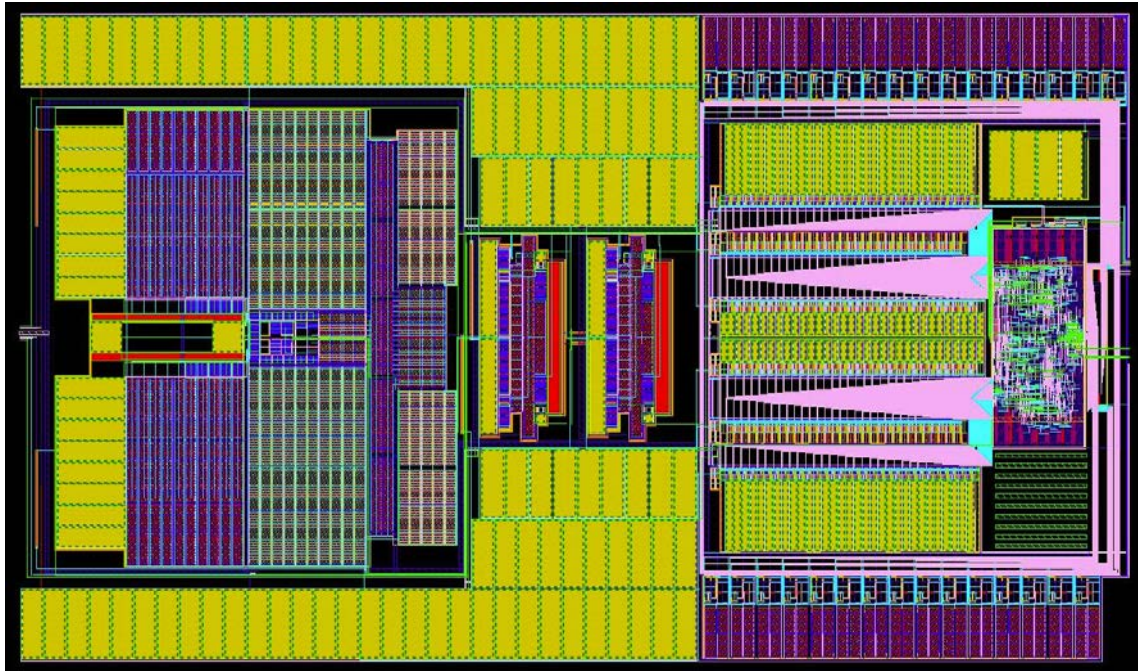Figure 4.23: Simulated input and output spectra of the ΣΔ modulator for a PWM input signal and ΣΔ modulator signal transfer function (AAF)

Figure 4.24: CT ΣΔ modulator layout

4.3.8 Layout

The realized third order CT ΣΔ modulator has been integrated using a 40-nm, 7-metal, CMOS technology. The active chip area is 1.1 mm × 0.6 mm = 0.66 mm^2.T he layout of the realized chip is shown in Figure 4.24, while Figure 4.25 shows the chip photo. The layout is as symmetric as possible to minimize interferences. The clock tree is placed at the bottom of the chip and all the generated clock phases and the digital control signals are as far away as possible from the analog core. The analog core includes the three operational amplifiers, the resistances, the SCR network, and the reference voltage generators. The quantizer is positioned near the DACs, while the digital logic is placed at the right side of the chip.

4.3.9 Experimental Results

The realized ΣΔ ADC is presently being tested. The first results show a problem in the reference voltage generator (V_{ref+} and V_{ref-}), which limits the performance of the circuit for large input signals. However, for small input signals the circuit operates as expected. Basically, this is due to cross-coupling between the digital output and the DAC reference voltages. Figure 4.26 shows the measured SNDR of the modulator as a function of the input signal amplitude. The noise floor, indeed, increases for large signals, leading to a SNDR degradation for input signals above −40 dB$_{FS}$, while above –20 dB$_{FS}$ distortion becomes dominant, as shown in the spectra reported in Figure 4.27. However, this noise
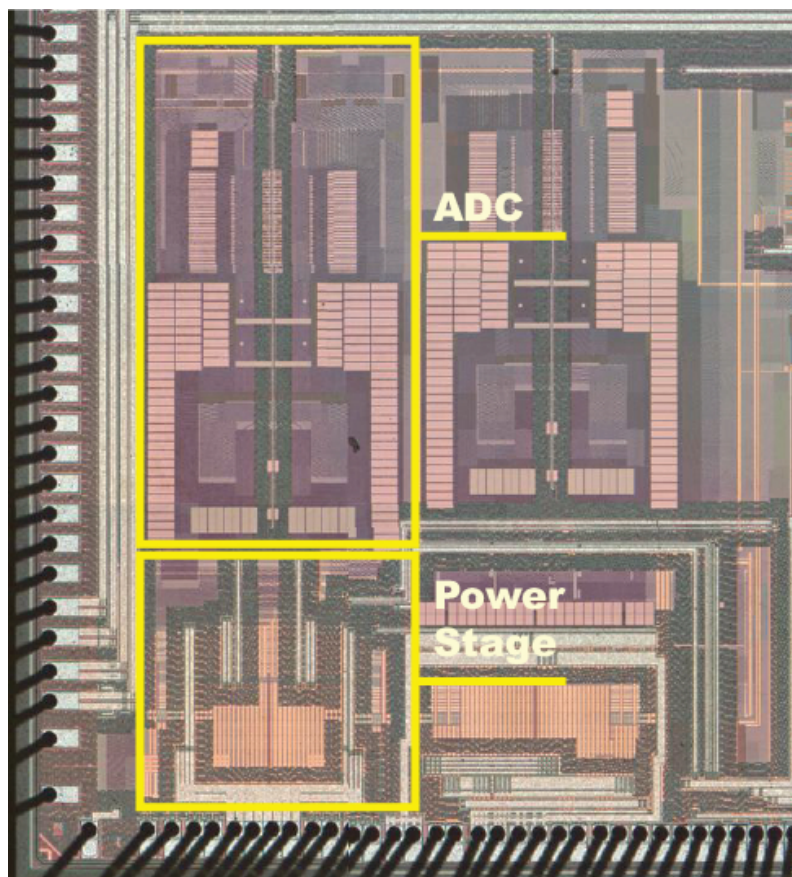
Figure 4.25: Chip micrograph of the CT ΣΔ modulator, including the class-D amplifier power stage)

Table 4.4: CT ΣΔ ADC features

Parameter	Value
Technology	CMOS 40 nm
Area	0.6 6mm^2
Supply voltage	1.1 V
Power consumption	1.7 mW
Full-scale signal	0.4 V
Bandwidth	24 kHz
Dynamic range	101 dB
Peak SNR	101 dB
Peak SNDR	72 dB
ENOB	11.5 bit
AAF	Third order
AAF cutoff frequency	150 kHz

floor increase has little effect on the Class-D amplifier performance, considering the requirements illustrated in Figure 4.26 (for large signals more noise is tolerated since it is not perceived on the loudspeakers).

The main features of the implemented third-order modulator are summarized in Table 4.4.

Figure 4.26: SNDR of the ΣΔ modulator as a function of the input signal amplitude at 1 kHz and SNDR requirements

Figure 4.27: Spectra of the ADC output signal with –42 dB$_{FS}$ and –22 dB$_{FS}$, 1 kHz input signals

Chapter 5

Conclusions

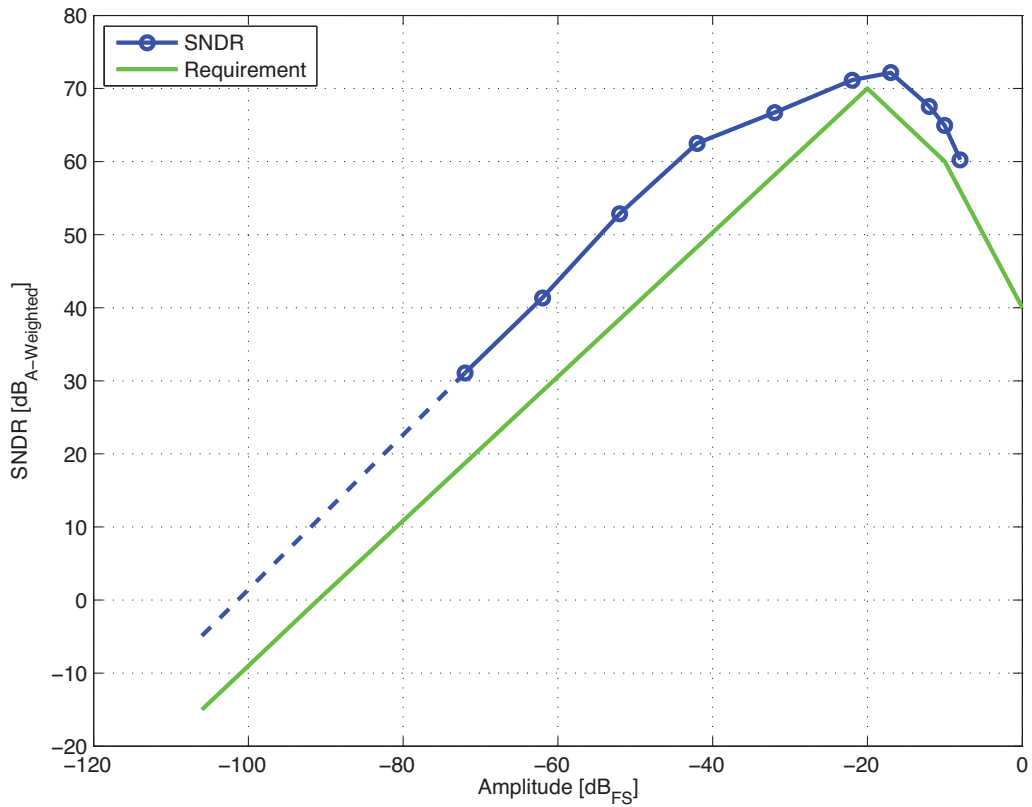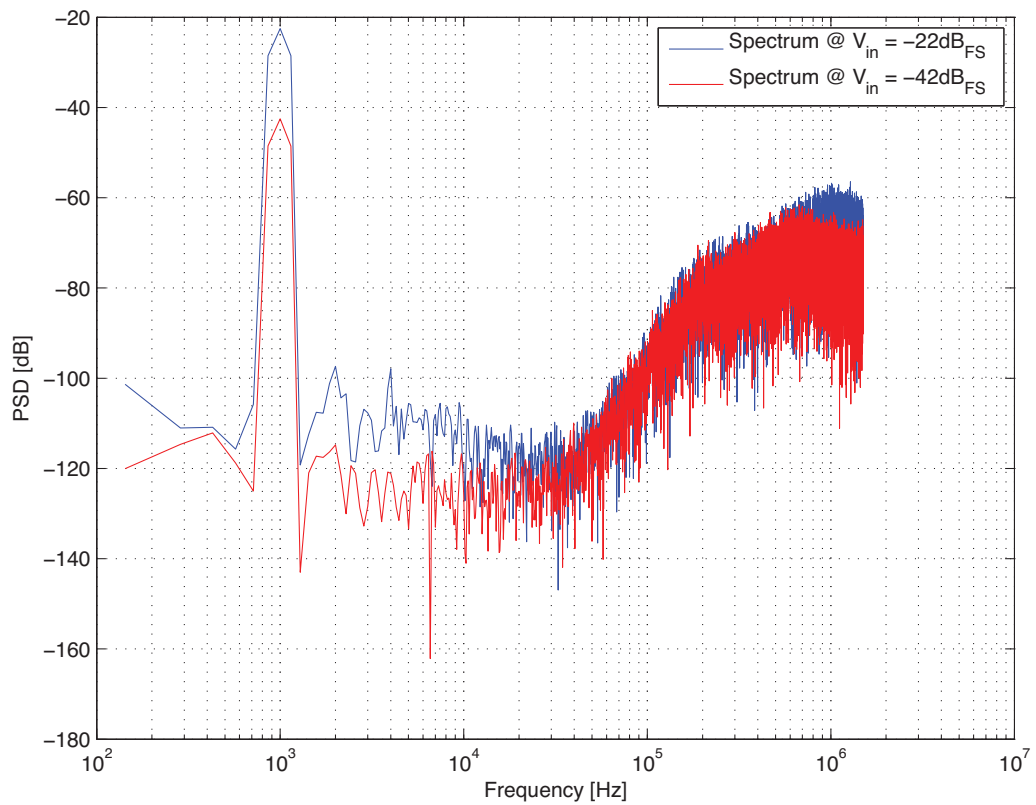This thesis work has been focused on the design of two different low-voltage, low-power A/D converters for two different switching-mode systems The goal of this research was to explore efficient digital control techniques to improve the performance of switching-mode systems, such as DC-DC converters and class-D audio amplifiers, which so far are implemented with analog control circuits. Ideally the digital control is the most efficient solution to regulate and monitor the operation of these systems. Moreover, the rapid scaling of CMOS technology shall give even more significance to digital solutions which integrate more features than their analog counterparts.

However, the A/D converters are the bottleneck that limit the diffusion of digitally controlled switching-mode systems. Basically, the ADC performance is often limiting the performance of the entire system and, hence, the ADC requirements in switching-mode systems are extremely tough. In addition, the technology scaling does not bring that much benefit to analog circuit performance and introduces a hard challenges for achieving an acceptable dynamic range, due to the reduction of the supply voltage. At the same time, the threshold voltage is not scaling linearly with the supply voltage, thus leading to a further strong degradation of the useful dynamic range, making difficult to drive CMOS switches and use cascode configurations circuits.

Despite these limitations, in these thesis we designed two A/D converters, in 65-nm and 40-nm CMOS technologies, with suitable performance for a digital SMPS and a digital class-D amplifier, respectively. The achieved results demonstrate that using digital control in switching-mode systems is indeed possible.

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