Università degli Studi di Pavia

Facoltà di Ingegneria
Dipartimento di Ingegneria Industriale e dell'Informazione

Doctoral Thesis in Microelectronics
XXVIII Cycle

Continuous-Time ΣΔ Modulator for MEMS Microphones

Advisor:
Chiar.mo Prof. Piero Macovati
Co-Advisor:
Chiar.mo Prof. Andrea Baschirotto
Coordinator:
Chiar.mo Prof. Franco Maloberti

Author:
Claudio De Berti

November 2015

UNIVERSITÀ DEGLI STUDI DI PAVIA

Abstract

Facoltà di Ingegneria
Dipartimento di Ingegneria Industriale e dell'Informazione

Doctor of Philosophy

Continuous-Time ΣΔ Modulator for MEMS Microphones

by Claudio De Berti

A 3rd-order continuous-time ΣΔ modulator for MEMS microphones in 0.16-μm CMOS technology is presented. The ΣΔ modulator, based on a feedforward architecture, uses only two operational amplifiers for achieving the 3rd-order loop-filter transfer function, a 15-level quantizer, and a feedback DAC with three-level current-steering elements, which minimizes the noise contribution at small input signal, in order to achieve high *DR*. The proposed modulator achieves 106.7-dB *DR* and 93.2-dB peak *SNDR*, consuming 390 μW from a 1.6-V power supply and occupying an area of 0.21 mm^2. This work has the largest reported Schreier *FoM* (184 dB).

Contents

List of Figures

List of Tables

Introduction

Several low-power devices under development require the audio input module (i. e. the microphone) to be continuously active to offer the possibility of voice control. Therefore, digital microphone interface circuits, required for digitizing the microphone capacitance variation, have to feature extremely low power consumption, i.e. lower than 1 mW. Moreover, micro-electro-mechanical-systems (MEMS) are becoming very popular to realize microphones with dynamic range (DR) higher than 90 dB, for this reason high-quality audio performance are required more and more in the microphone interface path.

The typical microphone interface circuit is shown in Fig. 1. The first stage is a programmable gain amplifier (PGA), needed to amplify the signal generated by the microphone, thus allowing to drive the analog/digital converter (ADC). The noise and distortions introduced by the ADC stage should not be dominant in the interface chain, in order to not limit the performance of the PGA. Moreover, an ADC with high DR can increase the possibility of back-end signal processing: for instance, the signal gain can be set in digital domain, therefore avoiding unwanted signal clipping in the PGA. This possibility is very important in a far field voice control scenario, where environment sounds can be louder than the human voice.

For this reasons, the ADC in digital microphone interface circuits is typically a $\Sigma\Delta$ modulator, because it offers high performance at lower power consumption in comparison to other topologies. Furthermore, with a $\Sigma\Delta$ modulator it is possible to achieve HiFi audio performance ($DR > 100$ dB, $THD < 0.1\%$), required for advanced audio signal processing.

Traditionally, the audio $\Sigma\Delta$ modulators are realized with Switched-Capacitor (SC) techniques, to guarantee the required Total Harmonic Distortion (THD) and DR. However, SC-$\Sigma\Delta$ modulators intrinsically require an operational amplifier (opamp)

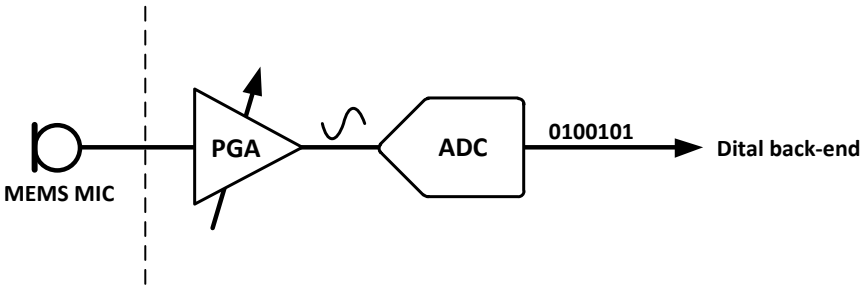

Figure 1: Digital microphone interface block diagram

unity-gain bandwidth (UGB) correlated to the sampling frequency (f_S), i. e. much larger than the signal bandwidth, leading to large power consumption [2].

As an alternative, audio Continuous-Time (CT) $\Sigma\Delta$ modulators are becoming popular, since they exploit a CT loop filter, which requires opamps with smaller UGB and, hence, lower power consumption than SC-$\Sigma\Delta$ modulators. Moreover, CT-$\Sigma\Delta$ modulators exhibit inherent antialiasing properties. However, audio CT-$\Sigma\Delta$ modulator DR is limited by some implementation aspects (like opamp slew-rate, jitter, spikes, etc.), which can be reduced at the cost of power consumption increase [3], preventing their use in portable devices.

This work focuses on facing this challenge and proposes a device able to achieve $DR > 100$ dB with power consumption lower than 500 μW. This is achieved with the adoption of several low-power techniques (some of them innovative), such as single-opamp resonator, feedforward CT-$\Sigma\Delta$ modulator architecture, multi-bit quantizer, and DAC with three-level current-steering elements.

Chapter 1 covers in a general and with just an introductory purpose the $\Sigma\Delta$ modulator theory, highlighting the advantages of CT implementations over DT topologies. In the second section, the assisted design of $\Sigma\Delta$ transfer function is presented. In the third section, an analysis of noise due clock jitter is proposed, focusing the attention on audio modulators.

Chapter 2 presents a novel loop filter architecture that can be used to reduce the power consumption. This architecture can be implemented with only two opamps, instead of four needed in a traditional solution. In the second section the compensation needed for the excess loop delay is introduced, and in the third

section is proposed a noise transfer function that remains stable over ±30% of process variations.

Chapter 3 deals with the circuit design of the proposed CT-ΣΔ modulator where low-power and low-noise techniques were adopted. The first section covers the implementation of the loop-filter based on two opamps, highlighting its noise performance. In the second section the excess loop delay compensation is implemented with a low-power and low-area solution, while the third section describes the quantizer circuit. The fourth section is dedicated to the main feedback DAC realized with three-level current-steering elements in order to minimizing the noise at low input signals, and therefore increasing the DR. Moreover, in this section the dynamic element matching necessary to linearize the feedback DAC is presented. The final part of this chapter is dedicated to simulation results and physical layout.

Chapter 4 presents the experimental results, as well a comparison with the state-of-the-art.

Chapter 1

Background Theory

In this chapter a brief introduction to the field of $\Sigma\Delta$ modulators will be held. The first section is about the basic theory behind the $\Sigma\Delta$ modulators, showing the principle of operation and the possible main topologies. In particular, it will be highlighted the advantages of choosing a continuous time (CT) topology over a discrete time (DT) one. The second section is concerning the automated design of the noise transfer function, starting from required specifications. It will be illustrated the steps needed to obtain the loop filter coefficients with the use of the dedicated Matlab toolbox. The last section is about the problems relate to clock jitter in CT topologies and how much they can influence the overall performances, focusing the attention on $\Sigma\Delta$ modulators for audio applications. It will be demonstrated that, under reasonable assumption, the clock jitter can not be an issue.

1.1 $\Sigma\Delta$ modulator basic theory

Fig. 1.1 shows a simple block diagram of a generic $\Sigma\Delta$ modulator architecture. The input signal X comes into the modulator via a summing junction. It then passes through the loop-filter, which in its simplest form is an accumulator or integrator, which feeds an A/D converter (ADC). The ADC introduces a quantization error E in the signal. The ADC output is fed back to the input summing junction via a D/A converter (DAC). The error E due to the quantization process is the difference between the analog quantizer input signal and the quantized digital output signal. Suppression of the quantization error in a $\Sigma\Delta$ modulator is provided by two

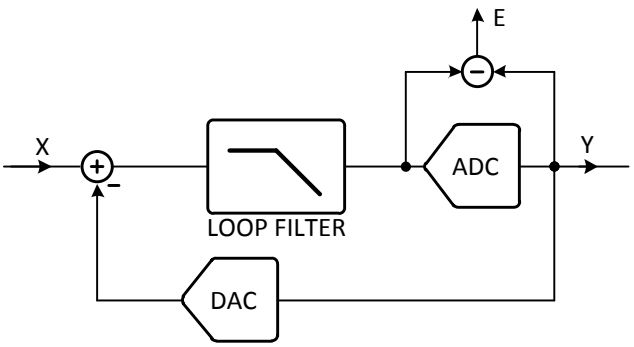

Figure 1.1: $\Sigma\Delta$ modulator basic architecture

mechanisms: oversampling and noise shaping. Since the reduction of quantization error is quite effective, even with a low-resolution quantizer a high-resolution digital output can be achieved.

1.1.1 Oversampling

The first technique of quantization error suppression is the oversampling. For simplicity reasons, the oversampling benefits are presented assuming the use of a single-bit quantizer. Such quantizer generates a bitstream with output levels $\pm\frac{q}{2}$, where q is the quantization step size. The bitstream spectrum contains information about the input signal as well as the quantization error, which is introduced during the quantization process. The noise spectrum of the quantization noise can be assumed to be white and to be uniformly distributed over the range $\pm\frac{q}{2}$ [4]. Therefore, it is possible to derive the quantization noise power as

$$e^2{}_{RMS} = \frac{1}{q}\int_{-\frac{q}{2}}^{+\frac{q}{2}} e^2 \,\mathrm{d}e = \frac{q^2}{12} \tag{1.1}$$

from the above equation, the power spectral density of a signal sampled with frequency f_s is

$$E(f) = \frac{q^2}{6f_s} \qquad for \qquad 0 \leq f < \frac{f_s}{2} \tag{1.2}$$

Therefore, for higher f_s corresponds lower noise power spectral density.

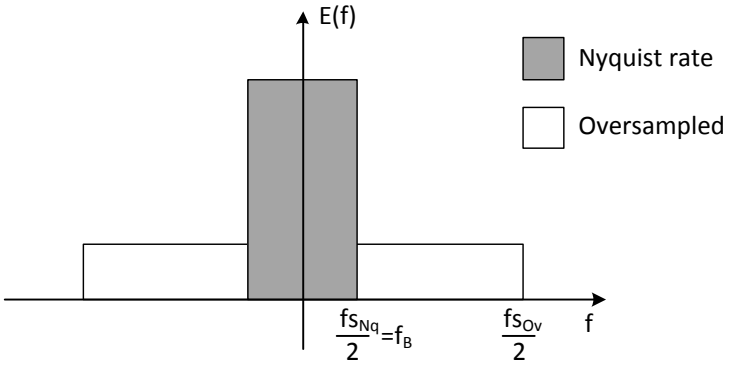

Figure 1.2: Oversampled rate conversion

In a traditional Nyquist rate converter, the sampling frequency $f_{s_{Nq}}$ is equal to two times the signal band f_B, while in an oversampled converter, the sampling frequency $f_{s_{Ov}}$ is higher than f_B. Fig. 1.2 shows the power spectral density $E(f)$ of the quantization noise in case of Nyquist rate sampling and in case oversampling rate. For Nyquist rate sampling, all the quantization noise power in the range $\pm\frac{f_{s_{Nq}}}{2}$ represented by the grey area (i.e. the signal bandwidth), has to be considered. In the oversampled case, the same noise power, represented by the area of the white rectangle, has been spread over a bandwidth equal to $\pm\frac{f_{s_{Ov}}}{2}$, which is much larger than f_B. Only a relatively small fraction of the noise power falls in the signal bandwidth, while the noise power outside the signal band can be filtered out. Therefore, by doubling the sampling frequency the quantization noise power is reduced by 3 dB. Referring to the effective number of bits (ENOB) expression (i.e. the measure of the dynamic performance of an ADC)

$$ENOB = \frac{SQNR - 1.76}{6.01} \tag{1.3}$$

where SQNR is the signal to quantization noise ratio, by doubling the sampling frequency the SQNR is increased by 3 dB and the resolution is increased by half a bit.

1.1.2 Quantization Noise Shaping

The second technique of quantization error suppression is the Noise Shaping. To better understand this behavior, a simplified linear model of a $\Sigma\Delta$ modulator can

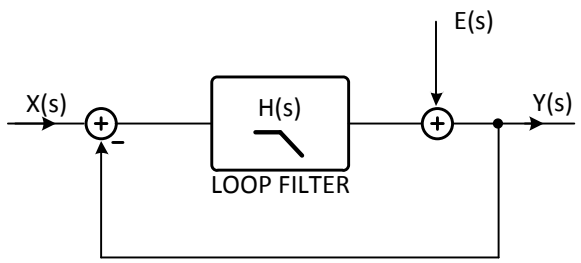

Figure 1.3: Simplified linear model for a generic ΣΔ modulator

be used, where the loop filter has a transfer function $H(s)$ and the feedback path has unitary gain, as shown in Fig. 1.3. Using this model, the output $Y(s)$ of the modulator is given by:

$$Y(s) = \frac{H(s)}{1 + H(s)} \cdot X(s) + \frac{1}{1 + H(s)} \cdot E(s) \tag{1.4}$$

where $X(s)$ is the analog input signal and $E(s)$ is the linearized quantization error. Therefore, from (1.3), in $Y(s)$ two contributions can be found. The first one is given by the Signal Transfer Function (STF)

$$STF = \frac{H(s)}{1 + H(s)} \tag{1.5}$$

and the second one is given by the Noise Transfer Function (NTF)

$$NTF = \frac{1}{1 + H(s)} \tag{1.6}$$

If $H(s)$ has a low-pass filter characteristic with high DC gain, then for frequencies before the low-pass cut-off of $H(s)$ the STF is close to 1, while the quantization error tends toward zero (NTF gain is close to 0). For frequencies close to half the sampling frequency, the input signal is filtered and the quantization error becomes large. This shows that the quantization noise spectral density is not constant over frequency, but has a shaped frequency spectrum. This is the principle of noise-shaping. A more effective quantization noise shaping can be achieved by increasing the order of the loop filter or adding resonators to the loop. However,

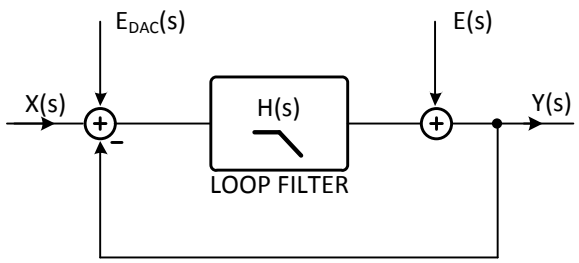

Figure 1.4: DAC error in the linear model for a generic ΣΔ modulator

increasing the filter order could lead to instability and appropriate compensation techniques must be adopted.

1.1.3 Multi-Bit Vs. Single-Bit Quantizer

If the reduction of quantization noise obtained with oversampling and noise shaping is not sufficient, a solution is the reduction of the quantization noise at the source, i.e. increasing the number of bits in the ADC. Furthermore with more bits in the quantizer, the stability constraints are easier to achieve than with single-bit structures and the internal signal swing is lower, thus alleviating the operational amplifier requirements in terms of output swing and slew rate. On the other hand, a larger number of bits in the quantizer increases the capacitive load of the amplifiers, which is a problem especially in high-frequency applications [5]. Moreover, more analog circuit components are needed to implement the internal ADC and DACs. The possibility of using higher gain in the integrators with multi-bit quantizer than in a single-bit loop, can improve the SNR by even more than 6 dB per additional bit. Moreover, in multi-bit ΣΔ modulators the out-of-band quantization noise is also reduced, which relieves the digital filtering required in the decimator. Despite the advantages of multi-bit structures, single-bit ΣΔ modulators are the most frequently used. The reason is the linearity requirement in multi-bit feedback DACs, which sets the upper limit for the ΣΔ modulator performance. All the non-idealities (i.e. E_{DAC}) of the main feedback DAC, indeed, are not shaped, but they are directly added at the input, as shown in Fig. 1.4. Therefore, the linearity of the whole ΣΔ modulator cannot be better than the linearity of the DAC. The

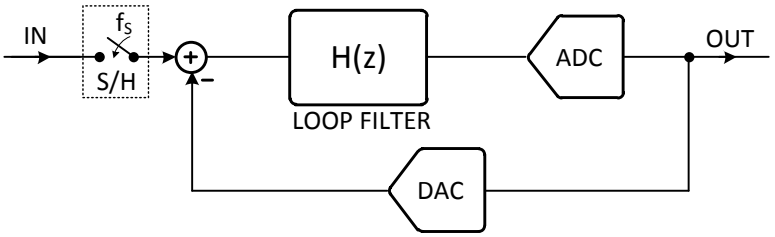

Figure 1.5: Generic Discrete-Time ΣΔ modulator

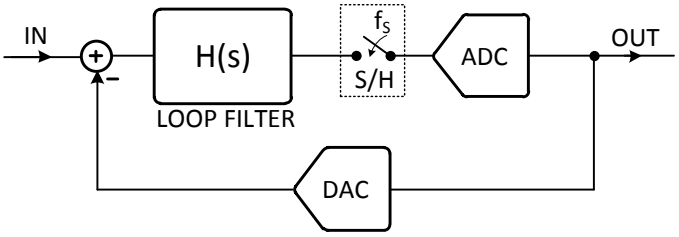

Figure 1.6: Generic Continuous-Time ΣΔ modulator

DAC linearity can be improved by element trimming, but this is expensive and it is not suitable for mass-produced products. Calibration techniques may also be utilized, but extra hardware and calibration time are needed [6]. Nowadays, different Dynamic Element Matching (DEM) techniques, which randomize and/or shape the distortion contribution of the DAC to improve the linearity over the signal band [7], are widely used.

1.1.4 Continuous-Time Vs. Discrete-Time

The generic ΣΔ modulator architecture illustrated in Fig. 1.1 can be implemented either with a Discrete-Time (DT) topology or with a Continuous-Time (CT) topology. The block diagram for the DT implementation is shown in Fig. 1.5, while the block diagram for the CT implementation is shown in Fig. 1.6. The main different among the two topology is that in a DT ΣΔ modulator the S/H stage, used to convert the CT analog input signal in a discrete-time signal, is at the input of the ΣΔ, while in a CT ΣΔ modulator the S/H stage after the loop filter, just before the ADC. Therefore, in a DT ΣΔ modulator the S/H can limit the linearity

and noise floor of the whole modulator, while in a CT ΣΔ modulator all the non idealities introduced by the S/H are attenuated by the loop gain, i.e. they have the same transfer function of the quantization noise. Moreover, the power consumption in CT ΣΔ modulators is usually lower than in their DT counterparts, thus making them suitable for high-speed and low-power applications. In fact, DT topologies based on switched-capacitors integrators demands gain-bandwidth products from eight to ten times higher than the sampling frequency for the proper settling of signals. On the other hand, CT integrators need GBW as low as one to two times, consuming drastically less power.

Another important advantage of the CT implementation are the intrinsic anti-aliasing properties of the ΣΔ modulator. Since the sampling is realized inside the loop, the high-frequency alias signals folded into the signal band are injected right at the quantizer input (i.e. the component A in Fig. 1.7(a)), thus being also noise shaped by the NTF, as shown in Fig. 1.7(e-f). Moreover, the high-frequency signals around f_s are attenuated by the loop filter transfer function $H(s)$, as shown in Fig. 1.7(c-d).

However, the linearity requirements are harder to achieve with CT than with DT circuits. For example CT circuits implemented with the active-RC or gmC techniques, feature worse linearity performance than DT circuits implemented with the switched capacitor (SC) technique. The main drawback of CT circuits is the clock jitter sensitivity in the feedback DAC where the DT feedback signal is added to the CT analog input signal. Time uncertainty in the feedback DAC raises the noise floor at the notch frequency, thus degrading the performance. A more detailed analysis of the noise due to jitter error will be shown in the dedicated section of this chapter, focusing the attention on audio CT ΣΔ modulator.

1.2 NTF design for CT ΣΔ

In the field of ΣΔ modulators, during the last two decades several tools were developed to simplify the work in NTF design [8] [9]. The Matlab tool called ΣΔ toolbox, created by R. Schreier [10], will be extensively employed because it offers design aid also in CT topologies.

The design of a NTF for CT-ΣΔ modulators consists in two steps.

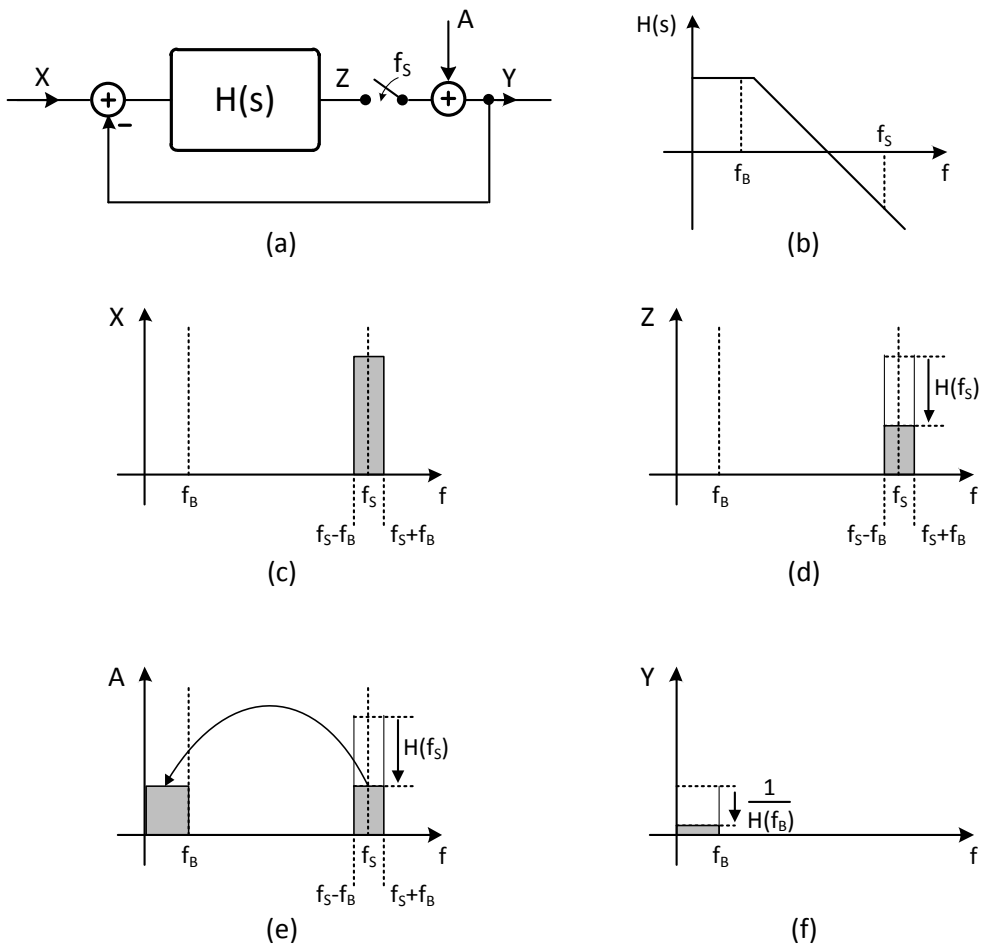

Figure 1.7: Intrinsic anti-aliasing properties in Continuous-Time ΣΔ modulators: (a) CT-ΣΔ model with alias source (b) Loop-filter transfer function $H(s)$ with high gain at f_B and attenuation at f_s (c) Input signals with frequencies around f_s (d) Signals around f_s attenuated by $H(s)$ (e) Alias folded in signal bandwidth (f) Loop gain attenuation of the in-band alias

- Design of the DT-NTF.
- Conversion of the DT-NTF into the CT-NTF using the impulse invariance method.

The first published works about CT-ΣΔ have used some previously well-known DT-ΣΔ modulators as starting points. Then, after the work published in [11], the impulse invariance method has been widely applied, like in [12] and [13]. The complete methodology for the impulse invariance has been proposed by R. Schreier in [14], where the linear blocks of the ΣΔ modulator are described using the state space representation.

The design of the DT-NTF can be done with the function $synthesizeNTF$ from toolboxt [10]. By using an optimization algorithm, this function conducts an iterative loop that searches a set of poles resulting at the specified out-of-band gain (for Butterworth type filter). Furthermore, if the optimum zeroes placement is requested, the function analytically deduces the conjugate zeroes frequencies based on the oversampling ratio. This function assumes in its general form:

$$ntf = synthesizeNTF(order, OSR, opt, H_{inf}, f0) \tag{1.7}$$

where ntf is the DT-NTF in Matlab Zero-Pole-Gain form (i.e. zpk object), with f_s=1, $order$ is the loop filer order, OSR is the oversampling ratio of the modulator, opt is the flag for zero placing optimization, H_{inf} is the out-of-band gain of the NTF and f_0 is the center frequency of the modulator ($f_0 \neq 0$ for bandpass modulator). Note that the NTF can be built using merely the 3 degrees of freedom

To translate the DT-NTF function into a tangible continuous-time filter, a second function from the toolbox can be used:

$$[ABCD] = realizeNTF\_ct(ntf, form, t_{DAC}) \tag{1.8}$$

where ABCD is the state-space description of the CT loop filter, $form$ specifying the filter topology (see Chapter 2) and t_{DAC} is the timing of the feedback DAC (e.g. $t_{DAC} = [01]$ means a zero-delay non-return-to-zero DAC). This routine estimates the space-state continuous-time matrix according to a certain discrete time system. With the aim of the impulse invariant transformation it creates a generic space-state structure based on the specified orientation and matches its impulse response to that of the DT-NTF.

A last function is needed to convert the space-state system into a real filter topology:

$$[a, g, b, c] = mapABCD(ABCD, form) \tag{1.9}$$

where a, g, b, c are the coefficients of the desired loop filter.

1.3 Jitter Noise in Audio CT-ΣΔ Modulators

In the field of ADCs for audio applications, CT-ΣΔ modulators are very promising solutions, since they potentially consume less power compared to their Switched-Capacitor (SC) DT counterparts for the same performance. Moreover, CT-ΣΔ modulators feature inherent antialiasing filtering, avoiding the need for dedicated filters in the input path. For these reasons, CT-ΣΔMs are becoming popular, not only in state-of-the-art research, but also in many commercial products. The main drawback of CT-ΣΔMs is the dynamic range (DR) degradation in the presence of clock jitter, which occurs also in SC architectures, but with a much lower DR loss for the same clock jitter. In fact, in CT-ΣΔMs the jitter on the clock used in the feedback DAC produces an equivalent noise component, which is directly added to the input signal, as shown in Fig. 1.8, while this is not the case in SC structures, in which the clock jitter only affects the input signal sampling.

1.3.1 Clock Jitter Model

In a clock signal, the period jitter J_{per} is defined as the time difference between an actual cycle period T_{per} and the ideal cycle period T_s. As a first approximation, the J_{per} can be modeled with a random variable. Since the clock frequency is constant, the mean value of J_{per} is zero ($\langle J_{per} \rangle = 0$). On the other hand its Root Mean Square (RMS) value is given by

$$J_{RMS} = \sqrt{\langle J_{per}^2 \rangle}, \tag{1.10}$$

where $\langle \cdot \rangle$ is the expected value operation.

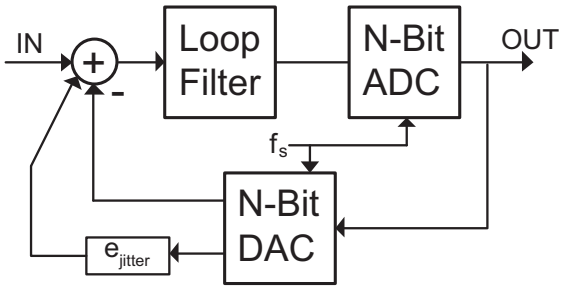

Figure 1.8: Noise contribution (e_{jitter}) of the clock jitter in the feedback DAC of a CT-ΣΔM

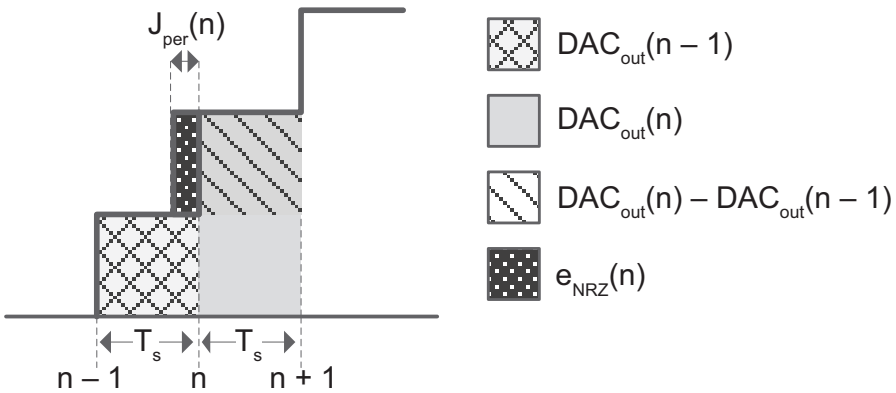

Figure 1.9: NRZ DAC amplitude error due to clock jitter

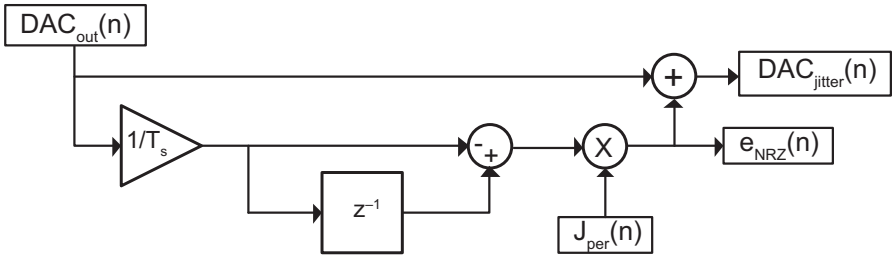

Figure 1.10: Simulink model of the jitter noise in a NRZ DAC

Different techniques have been proposed to reduce clock jitter effects in CT-ΣΔMs. As explained in [15], CT-ΣΔMs with Non-Return-to-Zero (NRZ) feedback DAC pulses are less sensitive to clock jitter than CT-ΣΔMs with Return-to-Zero (RZ) or half-delayed RZ DAC pulses. For all these structures, multi-bit DAC reduces the jitter error effects, due to the smaller steps at the DAC output. In a multi-bit NRZ DAC, clock jitter leads to an amplitude error in the output, as illustrated in Fig. 1.9, which shows the transient evolution of the feedback DAC output signal. The resulting error sequence can be expressed as

$$e_{NRZ}(n) = [DAC_{out}(n) - DAC_{out}(n-1)]\,\frac{J_{per}(n)}{T_s}. \tag{1.11}$$

In order to achieve fast and, at the same time, efficient CT-ΣΔM behavioral simulation in the time domain, the feedback NRZ DAC Simulink model shown in Fig. 1.10 directly implements (1.11) [8, 9]. In this model $J_{per}(n)$ is a time-domain random sequence featuring the desired clock jitter noise spectrum.

As test bench for validating the proposed jitter model, a 3rd-order CT-ΣΔM with 4-bit quantizer ($N = 4$), signal bandwidth $BW = 20$ kHz, oversampling ratio

$OSR = 75$, and sampling frequency $f_s = 3$ MHz is used. These are typical design parameters for audio ΣΔM, resulting in a signal-to-quantization-noise ratio ($SQNR$) larger than 120 dB. A 3rd-order loop filter can be implemented with a cascade-of-integrators either in feedback form (CIFB) or feedforward form (CIFF). To save power and area in CT-ΣΔM, the CIFF structure is more common in literature, since it requires fewer DACs and thus has been chosen as test bench. However, the choice of the topology of the loop filter does not affect the study of the jitter effects on the feedback DAC. In fact, in a CIFB loop filter, the inner feedback DACs are affected by jitter error, but their non-idealities are attenuated by the transfer function of the preceding integrators and, hence, they are irrelevant. The simulink model of the modulator based on a CIFF loop filter is shown in Fig. 1.11, where the block called *Jitter model* has been previously described in Fig. 1.10. The coefficients $a1$, $a2$, $a3$ and $g1$ of the loop filter are obtained from [**?**] and lead to a $SQNR$ of 122 dB for a 1-kHz, full-scale (FS) input signal. Moreover, an input referred thermal noise value that leads to a Signal-to-Noise Ratio (SNR) of 105 dB is considered, which fixes the target CT-ΣΔM DR. Finally, a PLL-based clock generator with an output signal (f_s) of 3 MHz and $J_{RMS} = 200$ pS is used. The effects of different clock jitter spectra featuring the same value of J_{RMS} are now studied.

1.3.2 White Jitter Noise

For modeling a white clock jitter, $J_{per}(n)$ in Fig. 1.10 is a random sequence with gaussian distribution, zero mean, and standard deviation J_{RMS}. From [16], for a multibit CT-ΣΔM, the expected value of the Signal-to-Jitter-Noise Ratio ($SJNR$) in this case is given by

$$SJNR = 10 \cdot \log_{10} \left[\frac{\left(2^N - 1\right)^2}{16 OSR \cdot J_{RMS}^2 \cdot BW^2} \right] \text{ [dB]}, \tag{1.12}$$

According to (1.12), a straightforward solution for reducing the performance degradation due to jitter is to increase the number of bits of the quantizer (N). However, this would results in a more complex structure, larger power consumption, and larger silicon area.

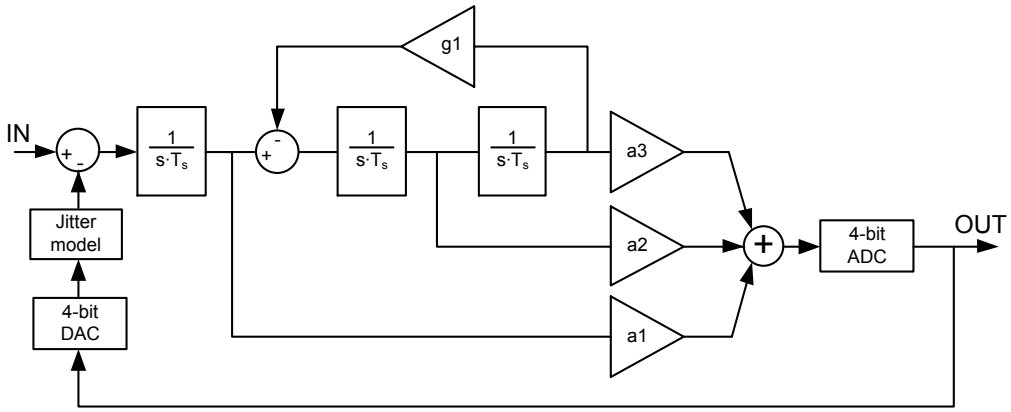

Figure 1.11: Simulink test bench for 3rd-order CT-ΣΔM

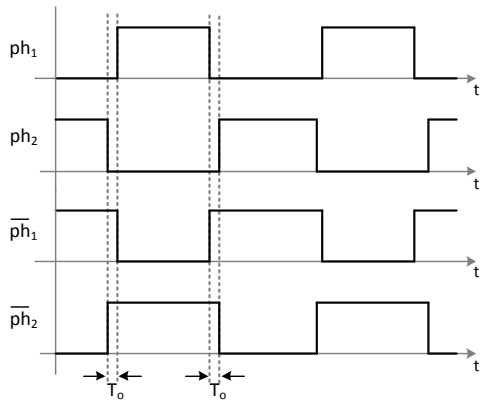

Figure 1.12: Typical *PN* spectrum of the clock signal generated by a PLL

Behavioral simulations of the considered test bench, performed using the model shown in Fig. 1.10 with white jitter featuring $J_{RMS} = 200$ ps, a *SJNR* of 101 dB is achieved (i. e. 21-dB *SNR* degradation with respect to the ideal *SQNR*), as correctly predicted by (1.12). This means that jitter noise turns out to be dominant, also with respect to thermal noise (that would lead to $SNR = 105$ dB). Therefore, in order to achieve the target *SNR* performance, extremely severe clock signal generator specifications are required ($J_{RMS} < 50$ pS).

Table 1.1: Coefficients of the piece-wise linear PN spectra

	Phase-Noise Function [dB$_c$/Hz]			
Δf from Carrier [Hz]	PN_a	PN_b	PN_c	**White Jitter**
10^1	-75	-59	-45	-112
10^2	-84	-77	-79	-112
10^3	-93	-95	-112	-112
10^4	-102	-112	-126	-112
10^5	-112	-118	-130	-112
10^6	-118	-120	-134	-112

1.3.3 Colored Jitter Noise

Due to the loop filter transfer function, the clock signal generated by a PLL does not actually feature white jitter. Therefore, the jitter of a clock signal produced by a PLL cannot be described only with J_{RMS}, but it necessary to consider the whole phase-noise (PN) spectrum, which is defined as

$$PN\left(f - f_s\right) = 10 \cdot \log_{10}\left[\frac{S_d\left(f\right)}{S_d\left(f_s\right)}\right] \quad [\mathrm{dB_c}]\,, \tag{1.13}$$

where $S_d\left(f\right)$ is the power spectral density of the clock signal and f_s is the clock frequency (the carrier). Fig. 1.12 illustrates the definition of $PN\left(f\right)$. This spectrum strictly depends on the PLL design (like, for instance, on the loop filter transfer function). Therefore, different PLLs feature different PN spectra, which have to be properly modeled in the CT-ΣΔM behavioral simulation. The proposed model, as a trade-off between accuracy and complexity, approximates the actual PN spectrum with a piece-wise linear function, e. g. described with six points at 10 Hz, 100 Hz, 1 kHz, 10kHz, 100 kHz, and 1 MHz offset from the carrier, respectively. A non-gaussian sequence of $J_{per}\left(n\right)$ samples (colored jitter) corresponding to a piece-wise linear PN spectrum can be generated with inverse Fast Fourier Transform (iFFT), as shown for example in [17], and used in the model shown in Fig. 1.10. Tab. 4.1 shows three different PN spectra that generate three different colored distributions of $J_{per}\left(n\right)$, all of them characterized by the same total RMS jitter ($J_{RMS} = 200$ ps). Fig. 1.13 graphically compares the different PN spectra, including the white jitter case.

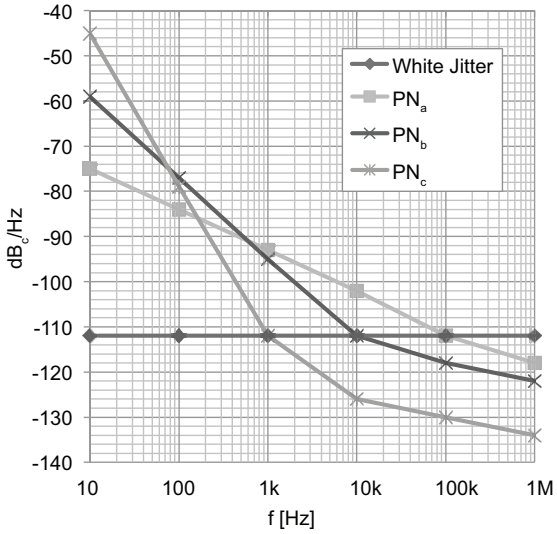

Figure 1.13: Piece-wise linear *PN* spectra

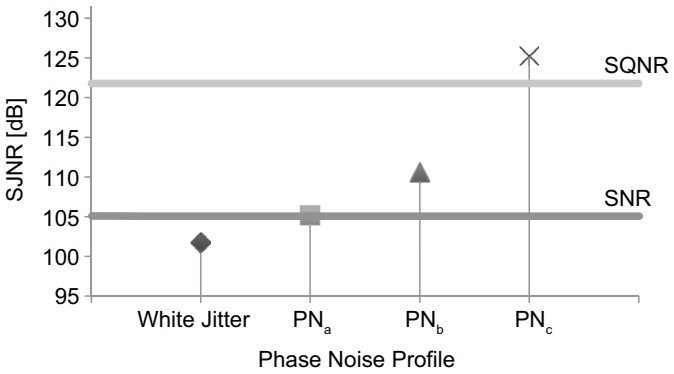

Figure 1.14: *SJNR* for different *PN* spectra compared to *SNR* and *SQNR* with a 1-kHz, FS input signal

1.3.4 Simulation Results

Behavioral simulations of the considered test bench with a 1-kHz, FS input signal show that, with spectrum PN_a, the jitter noise component is still dominant over the thermal noise, while with spectrum PN_b it becomes smaller. Finally, with spectrum PN_c the jitter noise component is even lower than the quantization noise, as shown in Fig. 1.14, and for this reason PN_c will be taken as example case in the next analyses. Basically, according to (1.11), the in-band noise due to jitter is dominated by the intermodulation products between the high-frequency tones of the shaped quantization noise and the clock signal *PN* spectrum. To better understand this concept, Fig. 1.15 shows a simplified case of three out-of-band tones representing the shaped quantization noise. In the case of white jitter (Fig.

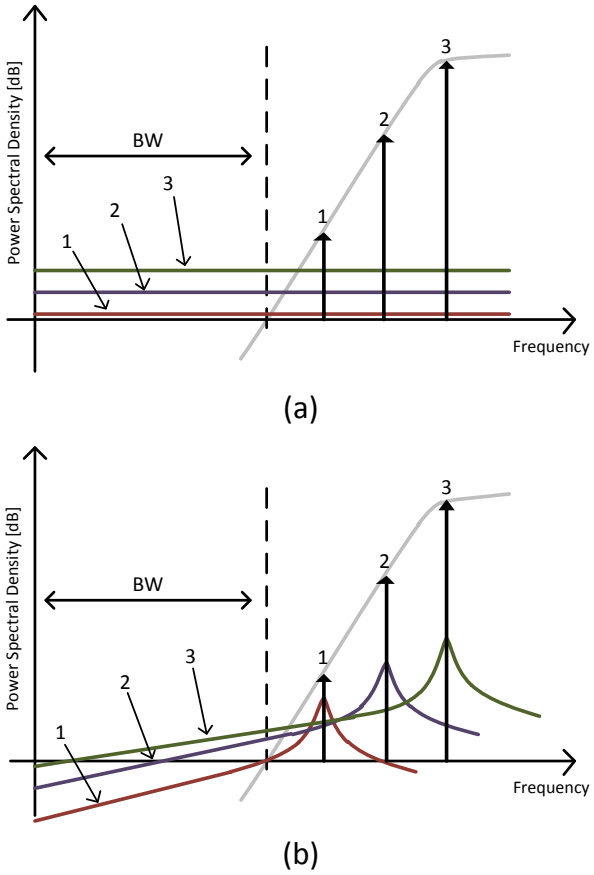

Figure 1.15: In-band noise due to jitter for three quantization noise tones: white jitter (a), colored jitter (b)

1.15a), the in-band jitter noise is the sum of the intermodulation of the tones with the white spectrum of the jitter, and, thus, is not frequency dependent. Instead, in the case of colored jitter (Fig. 1.15b), the in-band jitter noise is the sum of the tails of the intermodulation products between the tones and the PN spectrum of the jitter. Therefore, the lower are the clock signal PN spectral components with large offset from the carrier (e. g. 100 kHz and 1 MHz in Fig. 1.13), the lower are the resulting in-band noise components and, hence, the better is the $\Sigma\Delta$M performance. Fig. 1.16 shows the comparison between the simulated output spectra obtained with white jitter and with jitter with spectrum PN_c and the quantization noise. All the spectra are obtained with a 1-kHz, FS input signal. As illustrated in Fig. 1.15, the in-band jitter noise is lower in the case of colored jitter.

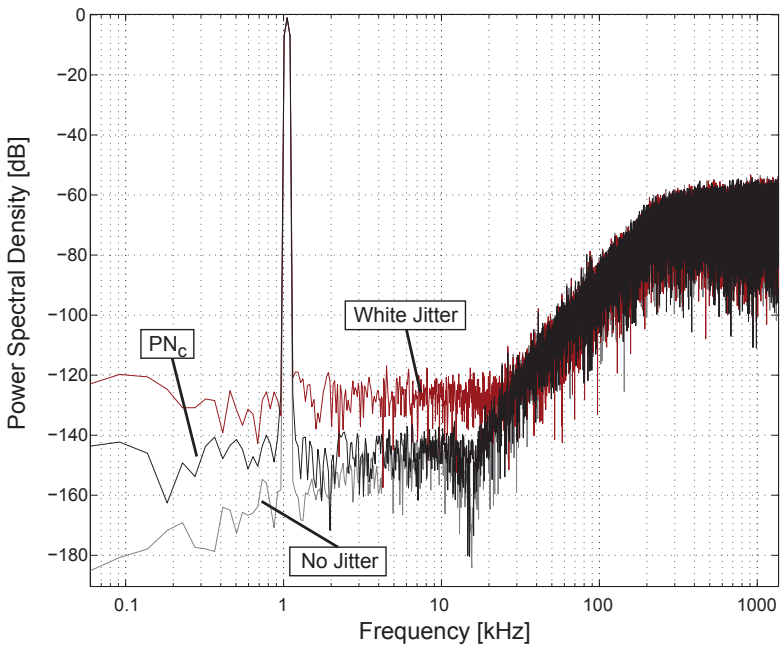

Figure 1.16: Simulated output spectra without jitter, with white jitter, and with jitter spectrum PN_c

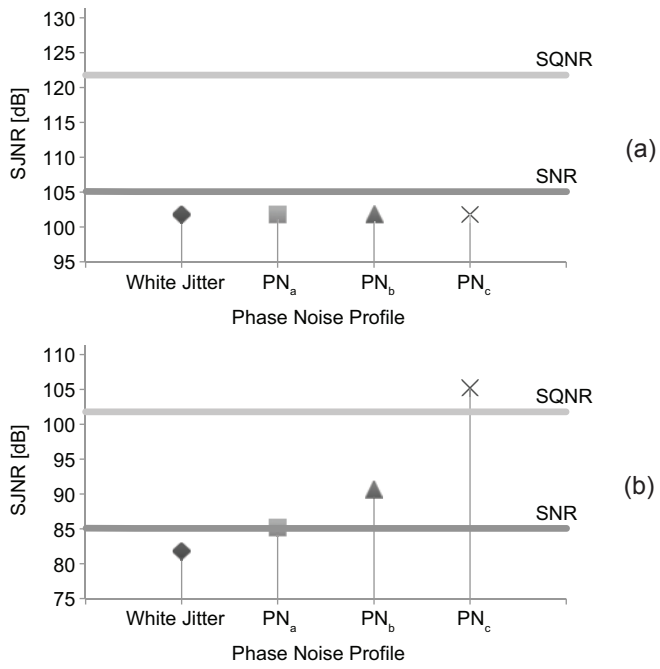

Figure 1.17: *SJNR* for different *PN* spectra compared to *SNR* and *SQNR* with a 15-kHz input signal at FS (a) and at -20 $\mathrm{dB_{FS}}$ (b)

The intermodulation products between the input signal and the PN spectrum, according to (1.11), are always negligible for input signal amplitudes lower than -20 $\mathrm{dB_{FS}}$ and become significant only for input signals close to FS at the edge of the audio band (e. g. with frequency larger than 10 kHz), as shown in Fig. 1.17. In fact, in those cases, the discrete derivative of the DAC output in (1.11) increases with the input signal amplitude and frequency, and thus its intermodulation with the PN spectrum become relevant. Fig. 1.18b shows how the integrated noise is increased due to the intermodulation product in the case of a 15-kHz, FS input signal and jitter with spectrum PN_c. The integrated noise return to low value, or rather at the value obtained in the case of a 1-kHz FS input signal, when the input signal amplitude is -20$\mathrm{dB_{FS}}$, as shown in Fig. 1.18c. Anyway, at large amplitude and at frequency close to the edge of the audio band the ΣΔM performance is typically dominated by other non-idealities, such as harmonic distortion.

In conclusion, for accurate design of audio CT-ΣΔM it is crucial to know and properly model the PN spectrum of the clock signal, while the RMS value of the jitter (J_{RMS}) alone is not sufficient. Indeed, as demonstrated in this paper, different clock signals with same value of J_{RMS} can lead to completely different ΣΔM performance. Only by properly modeling the colored jitter, it is possible to avoid over-design of the CT-ΣΔM, e. g. by increasing the number of bits in the quantizer, thus saving power and area. Moreover, a suitable clock generator (PLL) has to be used to maximize the CT-ΣΔM performance.

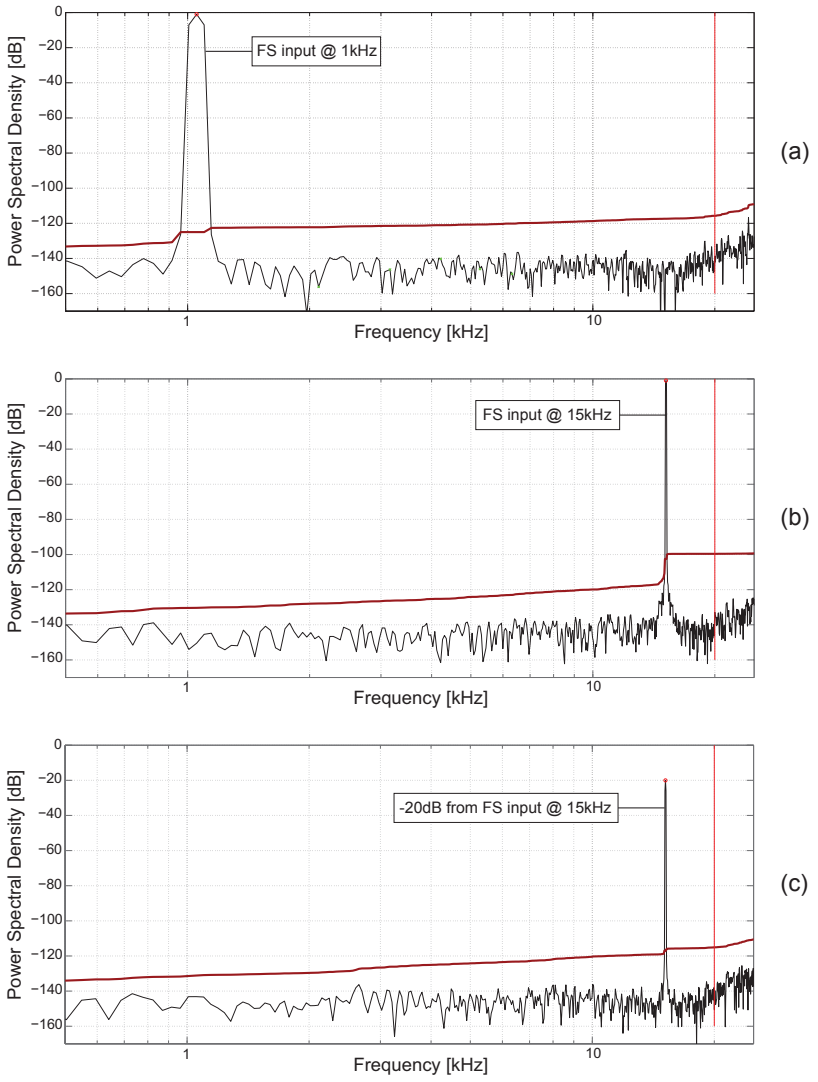

Figure 1.18: Simulated in-band output spectra and integrated noise profiles (solid line) in the case of jitter spectrum PN_c with: (a) 1 kHz, FS input signal; (b) 15 kHz, FS input signal; (c) 15 kHz, -20 $\mathrm{dB_{FS}}$ input signal

Chapter 2

Architecture

This chapter is about the study of a new architecture for CT-ΣΔ modulators for audio signals with bandwidth of 20kHz. The architecture is base on a 3rd order loop filter and a 4bit quantizer. From these specifications and considering an OSR of 75, this architecture guarantees to achieve the assigned targets for this project of 100+ dB of DR and 90+ dB of SNDR. In the first section will be introduced the developed architecture for the loop filter. In the second section will be study a solution to compensate an excess delay in the loop filter, while in the third section will be analyzed the suitable NTF for the CT-ΣΔ modulator obtained from the first two sections.

2.1 Loop Filter Architecture

In this section will be investigated the optimal implementation of a 3rd loop filter for CT-ΣΔ modulators. Will be also underlined all the steps followed to optimize the loop filter, which have led to an innovative architecture proposed for the first time in [18].

2.1.1 Feedback Form Vs. Feedforward Form

Looking at the theory of ΣΔ modulator, there are two ways to implement a 3rd loop filter: it can be realized with a cascade-of-integrators in multiple feedback form (CIFB), as shown in Fig. 2.1, or with a cascade-of-integrators with feedforward

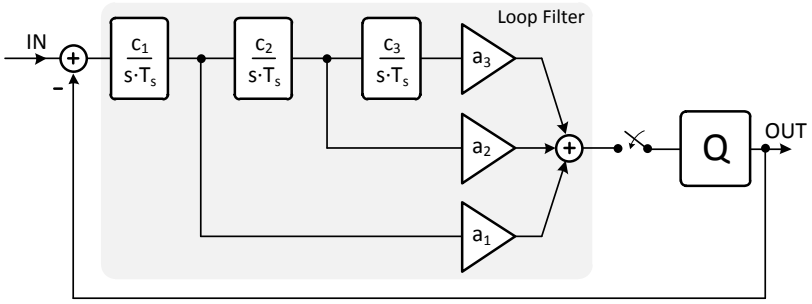

Figure 2.1: 3rd ΣΔ modulator realized with a cascade-of-integrators in multiple feedback form

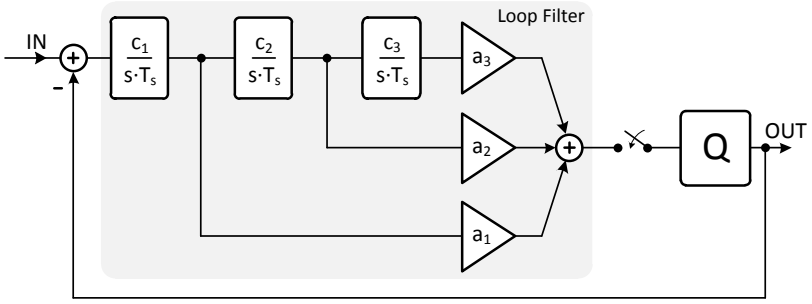

Figure 2.2: 3rd ΣΔ modulator realized with a cascade-of-integrators with feedforward form

form (CIFF), as shown in Fig. 2.2 . In both cases, considering a CT active-RC realization, three opamps are needed.

Concerning the realization of CT-ΣΔ modulators, the most followed way in literature [19] is the CIFF structure. Such a structure has the following advantages when compared with the more common CIFB approach. The first advantage is that the CIFF loop filter requires a lower number of DACs, ideally only one. On the other hand, a CIFB loop filter would need three DACs, thus increasing the chip area and the complexity of the circuit. The second advantage is the integrator capacitor sizes. To understand this aspect, notice that the value of the integrating resistor in the first integrator in both designs is governed by thermal noise considerations. The second and third integrators can, in principle, be implemented with much larger resistors and the sizes of the corresponding capacitors can be reduced. In

a CIFF design the first integrator is the fastest, while the first integrator is the slowest in the CIFB design. Thus, the integrating capacitor of the first integrator in a feedforward loop filter will be much smaller than that in a CIFB modulator. The final advantage is regarding the optimization of the power consumption. Noise and distortion considerations necessitate the use of large bias currents in the first opamp. In the first integrator, therefore, poles resulting from the finite bandwidth of the opamp can be expected to be at high frequencies. This can be used to advantage in the CIFF design, since the first integrator has the highest unity gain frequency and needs to have the least delay. While in a CIFB design, steps must be taken to ensure that the extra poles in the last integrator are not so low that loop stability is impacted, therefore increasing the bias current without improving the noise performance. It is thus seen that the large bias currents in the first opamp, which are needed anyway for noise reasons, are more efficiently used in a CIFF loop filter.

For all the advantages previously described, a CIFF loop filter has been chosen. Moreover, the coefficients c_1, c_2 and c_3 are set to be 1. In this way it is possible to reduce the complexity of the transfer function, thus allowing an easier manipulation of the structure, as described in the fallowing section. The CIFF loop filter has the transfer function

$$H_{loop}(s) = \frac{a_1 s^2 T_s^2 + a_2 s T_s + a_1 g_1 + a_3}{s^3 T_s^3} \tag{2.1}$$

2.1.2 Loop Filter Manipulations

The transfer function of the CIFF loop filter described in previous paragraph has all the poles (i.e. the NTF zeros) at band-center. High-performance CT-$\Sigma\Delta$ modulators usually are designed with NTF with optimized zeros, or rather it contains conjugate complex zeros. In this way it it possible to lower the quantization noise close to the upper edge of the band, i.e. extending the usable bandwidth. Traditionally, these zeros are implemented with a resonance generated by a local feedback around two integrators of the loop filter, as shown in Fig. 2.3. The loop filter has the transfer function

$$H_{loop}(s) = \frac{a_1 s^2 T_s^2 + a_2 s T_s + a_1 g_1 + a_3}{s T_s \left(s^2 T_s^2 + g_1\right)} \tag{2.2}$$

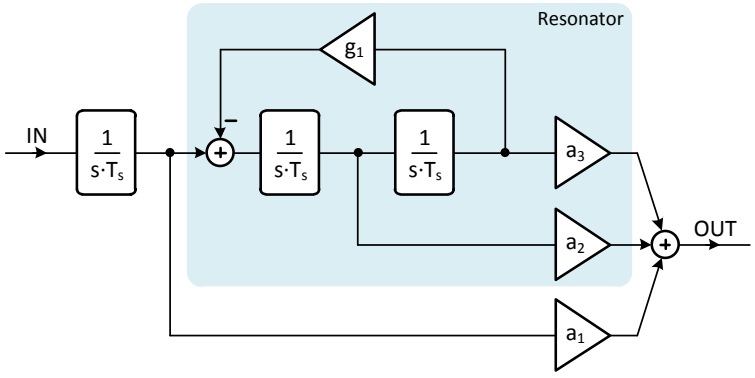

Figure 2.3: CIFF loop filter with local feedback to optimize NTF zeros

An equivalent NTF with complex zeros can be obtained with the proposed loop filter structure depicted in Fig. 2.4. In this solution, the local feedback has been moved around the first two integrators of the loop filter, allowing to obtain a resonator that presents a single output. This is a crucial aspect because it allows to use a resonator implemented with a single-opamp structure, and thus to reduce area and power consumption [20], [21]. The resonator has the transfer function

$$H_{res}(s) = \frac{a_1 s T_s + a_2}{s^2 T_s^2 + g_1} \tag{2.3}$$

so it has complex conjugate poles at the frequency w_0, a zero at the frequency w_Z and a DC_{gain} given by

$$w_0 = \frac{\sqrt{g_1}}{T_s} \qquad w_Z = \frac{a_2}{a_1 T_s} \qquad DC_{gain} = \frac{a_2}{g_1} \tag{2.4}$$

The transfer function from the output of the resonator to the output of the loop filter is

$$H_b(s) = \frac{sT_s + a_3/a_2}{sT_s} \tag{2.5}$$

and thus the resulting transfer function of the proposed loop filter is

$$H'_{loop}(s) = H_{res}(s) \cdot H_b(s) \approx H_{loop}(s) \tag{2.6}$$

Finally, an ulterior manipulation that leave the overall transfer function unchanged is shown in Fig. 2.5: the final adder is moved before the last integrator allowing to sum passively the feedforward path, after it has been derived, at the input of the

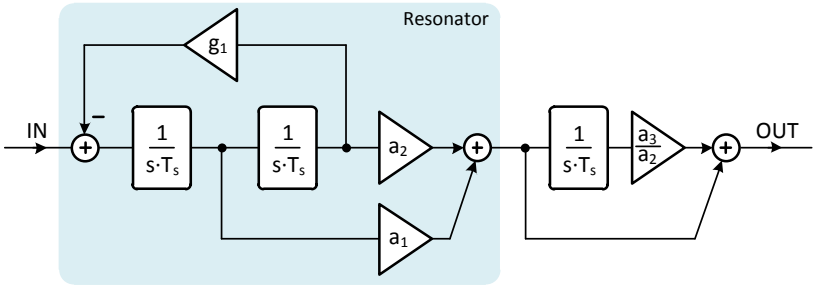

Figure 2.4: proposed loop lilter with single output resonator

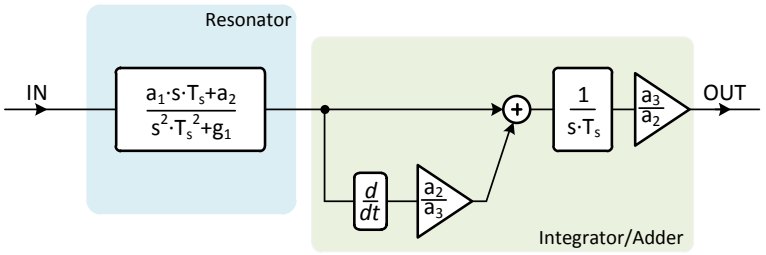

Figure 2.5: proposed loop lilter with single output resonator and with final adder moved before last integrator

integrator and avoiding the use of an active (power hungry) or passive (inaccurate) adder as output stage of the loop filter. In conclusion, the three poles of the CT loop filter are realized using the cascade of a single-opamp resonator and of a conventional CT integrator. The adopted feedforward architecture leads to a reduced resonator opamp output voltage swing, thus allowing us to save power.

2.2 Excess Loop Delay Compensation

The comparators in the ADC of a CT-ΣΔ modulator require some time to take a decision. Therefore, the feedback DAC must be clocked at a time τ delayed with respect the sampling instant of the ADC, as shown in Fig. 2.6. This amount of time τ is called Excess-Loop-Delay (ELD).

The ELD is a problem in CT-ΣΔ because it degrades the performance of the loop and even a low amount of delay can result in an unstable structure. In literature several techniques for compensating the loop filter transfer function in case of

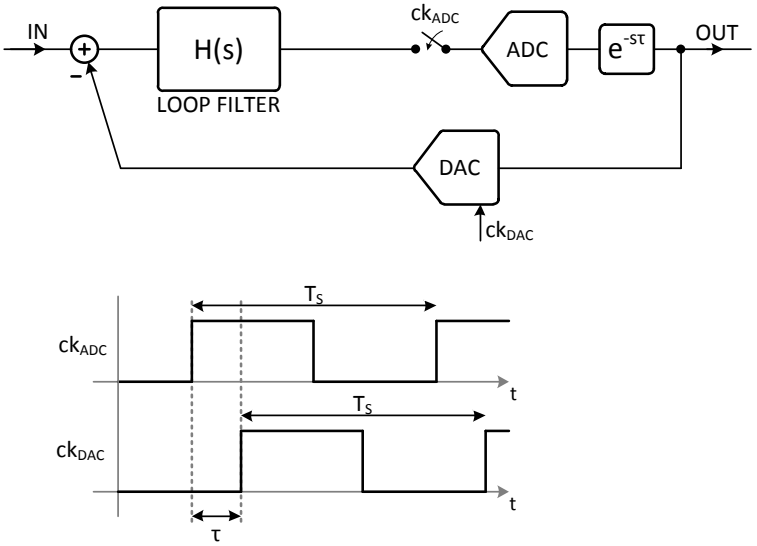

Figure 2.6: Excess loop delay problem

ELD have been proposed. Conventional methods of finding the appropriate filter coefficients to account for loop delay work in the z-domain, leading to cumbersome algebra. In [22] the authors show that the same objective can be accomplished entirely in the continuous-time domain, resulting in a procedure that lends itself to hand calculations, even for high order modulators. The technique to compensate ELD has been studied for CIFF loop filter CT-ΣΔ modulator, employing an Not-Return to Zero (NRZ) DAC. The NRZ DAC is chosen for Jitter noise reason, that will be explained in the dedicated section of this work. A generic N-order CIFF loop filter has the transfer function

$$H\left(s\right) = \frac{a_1}{s} + \frac{a_2}{s^2} + ... + \frac{a_N}{s^N} \tag{2.7}$$

where the sampling rate is assumed to be 1Hz, thus simplifying the fallowing equations. The coefficients a_1, a_2, ... , a_N are whose calculated for the desired NTF without ELD. The desired loop filter (compensated for excess delay) is written as

$$\hat{H}(s) = H(s) \cdot e^{\tau} \tag{2.8}$$

Conceptually, one could compensate for excess delay by cascading $H(s)$ with a block whose transfer function is e^{τ}. Unfortunately, such an impulse response is non-causal and not realizable in practice. The solution is the transfer function of the loop filter compensated for an excess delay τ given by

$$\begin{aligned}\hat{H}(s) = \frac{a_N}{s^N}\left(1 + s\tau + \frac{s^2\tau^2}{2!} + ... + \frac{s^N\tau^N}{N!}\right) \\ + ... + \frac{a_i}{s^i}\left(1 + s\tau + \frac{s^2\tau^2}{2!} + ... + \frac{s^i\tau^i}{i!}\right) \\ + ... + \frac{a_1}{s^1}(1 + s\tau)\end{aligned} \tag{2.9}$$

and it is valid under the condition $0<\tau<T_s$.

The transfer function described by (2.9) introduces a feedforward path across the loop filter, as direct consequence of ELD compensation. The gain of the feedforward path is given by the equation

$$a_{0c} = a_1 \cdot \tau + a_2 \cdot \frac{\tau^2}{2!} + ... + a_N \cdot \frac{\tau^N}{N!} \tag{2.10}$$

According to (2.9), the modified coefficients $a_{1c} - a_{3c}$ and the gain a_{0c} of the direct feedforward path across the loop filter needed to restore the NTF of a 3rd CT-ΣΔ are

$$\begin{aligned}a_{0c} &= a_1 \cdot \tau_d + a_2 \cdot \frac{\tau_d^2}{2} + a_2 \cdot \frac{\tau_d^3}{6} \\ a_{1c} &= a_1 + a_2 \cdot \tau_d + a_2 \cdot \frac{\tau_d^2}{2} \\ a_{2c} &= a_2 + a_3 \cdot \tau_d \\ a_{3c} &= a_3\end{aligned} \tag{2.11}$$

In practice, it is convenient to force the ELD τ to be 1/2 or 1 period of the clock (T_s), operation usually obtained by placing a D-flip-flop before the feedback DAC, in order to make sure that the ELD is well known and constant, independently of process and voltage variations as well as temperature.

The feedforward path across the loop filter, as shown in Fig. 2.7(a), cannot be directly implemented in the proposed circuit because the subtraction between the

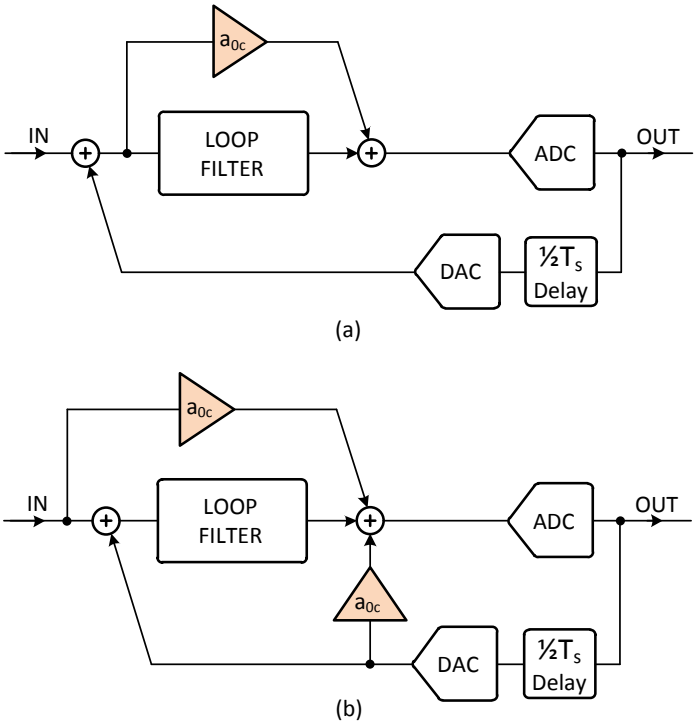

Figure 2.7: (a) ELD compensation with feedforward across the loop (b) Equivalent solution scheme

ΣΔ modulator input and the feedback DAC output is done by the resonator itself. Anyway, the same result can be accomplished with a feedforward path from the ΣΔ modulator input and a local feedback, both in the final adder, as shown in Fig. 2.7(b).

In the proposed implementation, both the ELD compensation feedforward and feedback paths are derived and summed passively at the input of the last integrator, as it has been done for the feedforward path of the loop filter. The resulting architecture for the CT-ΣΔ modulator is shown in Fig. 2.8.

2.3 NTF design

In a CT-ΣΔ modulator, the NTF influences several aspects in term of performance. In particular these aspects are correlated to the out-of-band gain of the NTF. Multibit operation enables NTFs with large out-of-band gains, which result in

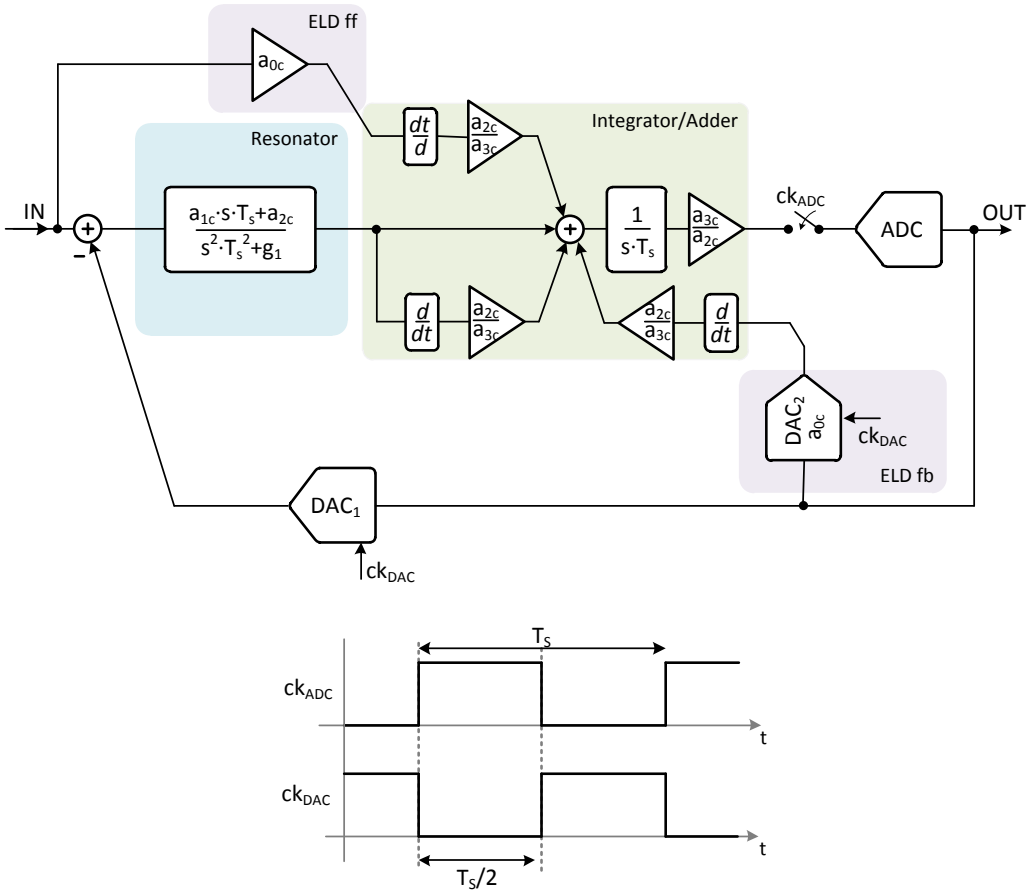

Figure 2.8: Block diagram of the proposed CT-ΣΔM

reduced in-band quantization noise. However, a large out-of-band gain results in increased noise due to clock jitter, and this aspect will be highlighted in the dedicated section of this chapter.

Another aspect related to the out-of-band gain of the NTF is the performance in case of RC time constants variation. The RC time constants in the loop filter vary due to process shifts and changes in ambient temperature. A decrease in time constants from the nominal value causes the in-band quantization noise to reduce, while simultaneously increasing the out-of-band gain. This results in a poor rejection of the in-band quantization noise. Vice versa, a increase in time constants causes the in-band quantization noise to increase, while simultaneously decreasing the out-of-band gain. This behavior impacts the stability of the modulator. To combat the increased quantization noise when the time constants become larger, the NTF can be chosen so that the in-band noise satisfies the specification under this worst case condition. On the other hand, a modulator with a large out-of-band

Table 2.1: Coefficients for the desired NTF

Coefficient	Value
a_{0c}	0.4180
a_{1c}	0.9194
a_{2c}	0.3442
a_{3c}	0.0642
g_1	0.0014

gain is more sensitive to the RC component variations and excess loop delay. Thus, to combat possible stability issues when the time constants become larger, the NTF can be chosen so that the stability of the modulator is guarantee also under this worst case condition.

The target of the CT-ΣΔ modulator is 100+ dB of Dynamic Range (DR), for this reason the NTF must guarantee a signal-to-quantization noise (SQNR) greater than 103 dB to have reasonable headroom for the thermal noise. To achieve this performances, and taking into account an OSR of 75, a 4bit/15-level quantizer was chosen as a reasonable compromise between the benefits offered by multibit operation and the exponential complexity of implementation.

On the above considerations, an out-of-band gain of 1.65 was chosen. Moreover, with the aid of Simulink simulations, some additional trims of the coefficients have been done, such increasing even further the performances in case of component variations. Such a strategy obviates the need for an RC time-constant tuning loop. The resulting coefficients are reported in Tab. 2.1.

2.3.1 Simulink model results

As already mentioned, the evaluation of the NTF has been done with the aid of Simulink. The model that has been developed has exactly the same architecture shown in Fig. 2.8. The CT-ΣΔ modulator model output spectra obtained with -60-dB$_{\mathrm{FS}}$ and -1-dB$_{\mathrm{FS}}$, 1-kHz input signals are shown, respectively, in Fig. 2.10 and Fig. 2.9.

Resistor and capacitor variations have also been incorporated into the analysis. The modulator remains stable over ±30% of RC component variations. The results of a 500-cycles simulation are shown in Fig. 2.12 for the DR calculated with

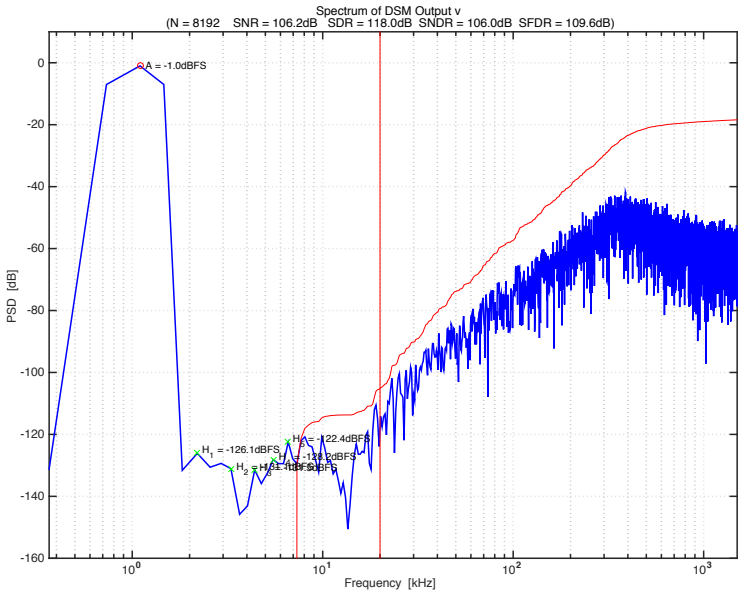

Figure 2.9: Output spectra of the proposed CT-ΣΔ modulator Simulink model with -1-dB$_{\mathrm{FS}}$, 1-kHz input signals

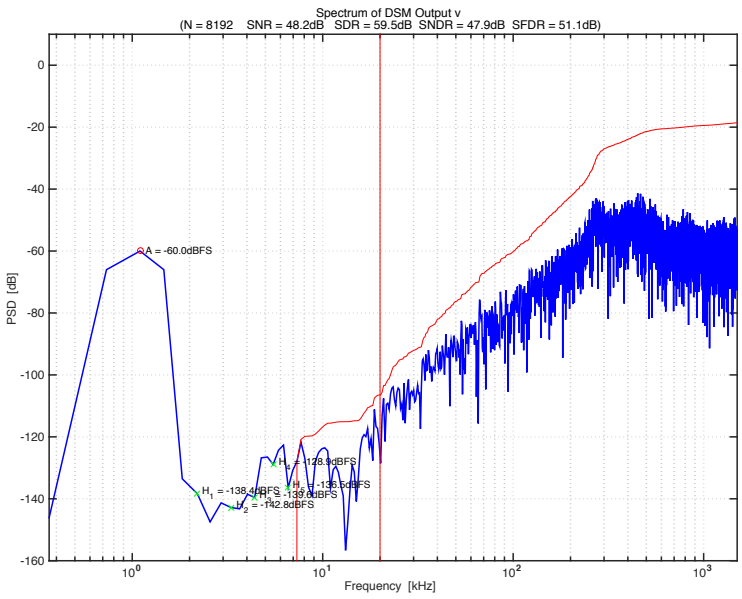

Figure 2.10: Output spectra of the proposed CT-ΣΔ modulator Simulink model with -60-dB$_{\mathrm{FS}}$, 1-kHz input signals

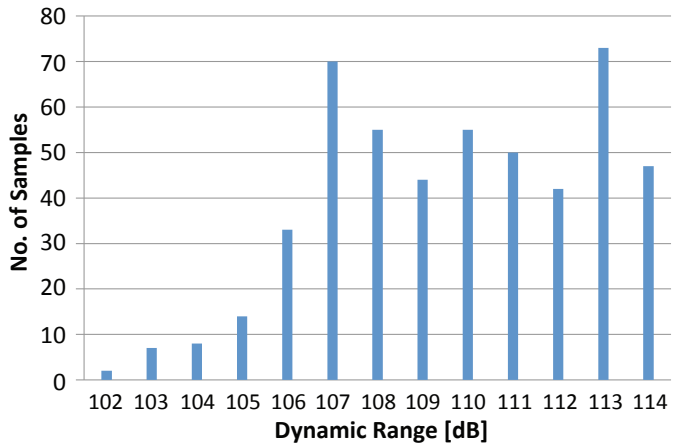

Figure 2.11: Distribution of the simulated DR with ±30% RC component variations

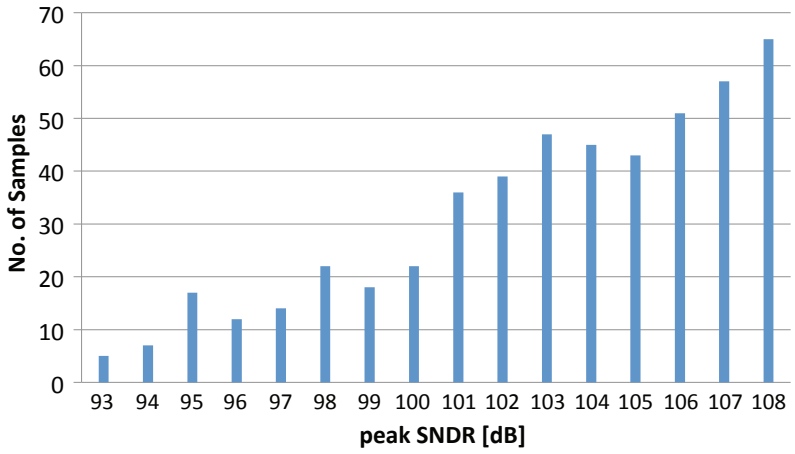

Figure 2.12: Distribution of the simulated DR with ±30% RC component variations

-60-dB$_{\mathrm{FS}}$, 1-kHz input and in Fig. 2.12 for the peak SNDR calculated with -0.5-dB$_{\mathrm{FS}}$. It thus seen that the DR is less sensitive to component variations: more than 96% of the 500-cycles have a DR greater than 103-dB and more than 43% of them exhibits a DR greater than the nominal value of 110dB. In fact, the DR is increased when the time constants are decreased from the nominal value because the in-band quantization noise is reduced and the out-of-band gain is increased. On the other hand, this statement is not valid for the peak SNDR. In fact, for large input signals, the optimal SNDR is achieved in nominal condition. If the time constants are decreased, the more aggressive NTF brigs to more in-band distortions, thus reducing the SNDR. For both DR and peak SNDR, if the time constant are increased from the nominal value, the in-band quantization noise is

increased and thus the overall performances are deteriorated. Anyway, the target SNDR is satisfied in all cases. Moreover, the 0.16 μm CMOS technology with Metal-Insulator-Metal (MIM) capacitors used for fabricate the proposed CT-ΣΔM have ±26% of RC component variations, ideally improving the results achieved in the model analysis.

Chapter 3

Circuit Design

This chapter describes the implementation of the architecture proposed in Chapter 2 for an audio CT-ΣΔ modulator. The first section is about the implementation of the loop filter, including also the circuit design of the two opamp used to achieve a third order NTF. The second section is about the implementation of the ELD, that requires a small amount of area an power, while the third section is concerning the realization of the quantizer. The fourth section is dedicated to the realization of the feedback DAC, that consist in many challenges to achieve low noise, low power and good linearity. The fifth section describes the digital circuit for the conversion of the output thermometer code in binary code, that is necessary to interface the modulator during measurements. The sixth section is dedicated to the noise transient simulations, necessary to evaluate the performances that will be expected during measurements. Finally, in section seventh the physical layout of the entire CT-ΣΔ modulator will be described.

3.1 Loop Filter

This section is dedicated at the realization of the proposed 3rd order loop filter that can be implemented with only two opamps: the first opamp is needed to implement the resonator, while the second one is needed to implement the integrator/adder.

3.1.1 Single-opamp resonator

As introduced in Chapter 2, the proposed loop filter has the peculiarity to have a resonator that can be implemented with a single-opamp topology. To reduce the number of opamps, single-opamp resonators have been proposed in several woks: in [23] and [24] the Twin-T resonator was modified to obtain an arbitrary second order polynomial in the numerator of its transfer function. However, there are some issues with the Twin-T based resonators:

- Increased power consumption in preceding stage due to loading: load for preceding stage is partly capacitive and input signal is not injected at virtual ground in Fig. 3.1 which results in significant coupling between opamp output and preceding stage.
- Sensitivity to parasitic coupling between opamp input and output: Parasitic capacitance between these nodes represents a path parallel to the Twin-T notch filter in the feedback of the opamp in Fig. 3.1 and consequently limits the quality factor of the resonator.
- Modification of Twin-T degrades matching: Quality factor of resonator is sensitive to component mismatch within Twin-T network. Modification of Twin-T in Fig. 3.1 results in large non-integer ratios of component values and consequently reduces their matching.

Moreover, the transfer function of the resonator inside the proposed loop-filter has a first order polynomial in the numerator. For this reason and to overcome the issues of the Twin-T based resonators, it is suitable the single op-amp resonator proposed [21]. This cross-coupled resonator is derived from complex two-stage polyphase notch filters. Mapping such a network from complex to real with opposite phase rotation in each stage after some simplifications yields the notch filter network comprising resistors R_1-R_3 and capacitors C_1-C_3 in Fig. 3.2. If this notch filter is placed in the feedback loop of an ideal opamp, a perfect resonance at the frequency

$$\omega_0 = \sqrt{\frac{\frac{1}{R_1R_2} + \frac{1}{R_1R_3} + \frac{1}{R_2R_3}}{C_1C_2 + C_1C_3 + C_2C_3}} \tag{3.1}$$

is obtained under the condition:

$$\frac{C_1}{R_2} + \frac{C_1}{R_3} + \frac{C_2}{R_1} + \frac{C_2}{R_3} + \frac{C_3}{R_1} + \frac{C_3}{R_2} = 0 \tag{3.2}$$

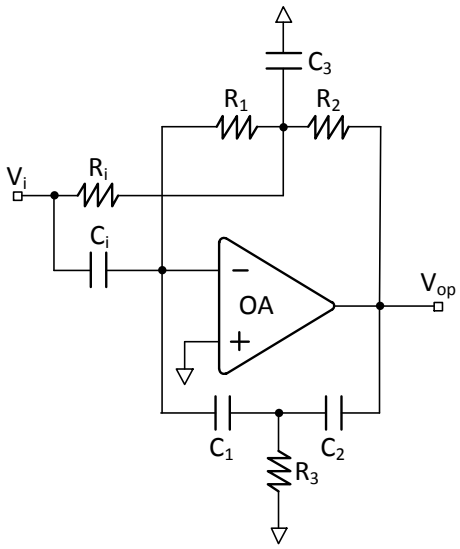

Figure 3.1: Twin-T sigle-opamp resonator

With the DC resistance of the feedback network

$$R_0 = R_1 \parallel (R_2 + R_3) \tag{3.3}$$

the transfer function becomes

$$H_X(s) = \frac{R_1}{R_i} \frac{s/\omega_z + 1}{s^2/{\omega_0}^2 + 1} \tag{3.4}$$

with a real zero at:

$$\omega_z = \frac{1}{(C_2 + C_3)(R_2 \parallel R_3)} \tag{3.5}$$

Since (3.2) leaves degrees of freedom in choosing the component values for a given transfer function, the network can be optimized for low number of components, reasonable component values, low load on the preceding stage and low load on the opamp by the differential impedance of the feedback network itself, which is at the resonance frequency:

$$Z_{\omega_0} = \frac{C_2 + C_3 + \frac{1}{j\omega_0}\left(\frac{1}{R_2} + \frac{1}{R_3}\right)}{\frac{C_3}{R_2} + \frac{C_2 + 2C_3}{R_3}} \tag{3.6}$$

In case of a real opamp, the peak gain at ω_0 is determined by the open loop gain of the opamp at this frequency, because there is no feedback at ω_0. Hence minimum

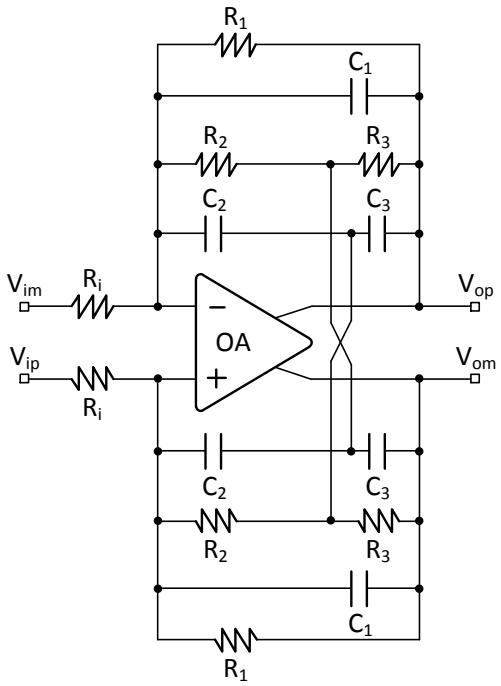

Figure 3.2: Cross-coupled sigle-opamp resonator

requirements for GBW and DC gain of the opamp are determined by the required peak gain at ω_0. In this respect the cross-coupled resonator behaves in the same way as the Twin-T resonator.

The cross-coupled network has been optimize for the proposed CT-$\Sigma\Delta$ modulator loop-filter. A cross-coupled feedback in RC cross configuration is suitable to achieve the required $H_{res}(s)$. The schematic is shown in Fig. 3.3: the notch filter is now made only with capacitors C_1-C_2 and resistors R_1-R_3. With an ideal opamp, the condition (3.2) becomes

$$\frac{C_1}{R_3} + \frac{C_2}{R_3} + \frac{C_3}{R_1} = 0 \tag{3.7}$$

therefore, the fallowing equations are obtained

$$\omega_0 = \frac{1}{\sqrt{R_1 R_3 C_1 C_2}} \qquad \omega_z = \frac{1}{R_3 C_2} \qquad DC_{gain} = \frac{R_1}{R_i} \tag{3.8}$$

From (2.5) and (3.8) the relation between the coefficients of the loop filter and the component of resonator circuit can be derived. Given the value of R_i, that is bounded by thermal noise constraints (as will be analyzed in the dedicated section

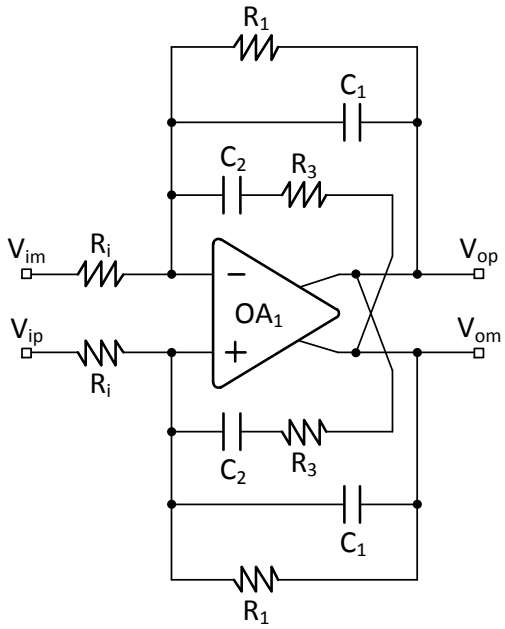

Figure 3.3: RC cross-coupled sigle-opamp resonator

of this chapter), the resulting values of the components are

$$
\begin{aligned}
R_1 &= DC_{gain} \cdot R_i = \frac{a_{2c}}{g_1} \cdot R_i \\
R_3 &= \frac{R_1}{\left(\frac{\omega_z}{\omega_0}\right)^2 + 1} = \frac{R_1}{\frac{a^2{}_{2c}}{a^2{}_{1c} \cdot g_1} + 1} \\
C_2 &= \frac{1}{\omega_z \cdot R_3} = \frac{T_s a_{1c}}{a_{2c} R_3} \\
C_1 &= C_2 \cdot \frac{(R_1 - R_3)}{R_1}
\end{aligned}
\tag{3.9}
$$

3.1.1.1 RC Cross-Coupled Resonator Noise Analysis

The RC cross-coupled resonator is placed as input stage of the loop filter, therefore its input referred noise limits the performance of the entire CT-ΣΔ modulator. Thus it is very important to analyze its noise contributions and the ways they affect the performances in the audio bandwidth. The noise sources in the circuits are the resistors and the opamp, as shown in Fig. 3.4.

One of the main contribution of noise is given by the input resistors R_i, whose noise is entirely added to the input. Considering the fully differential implementation,

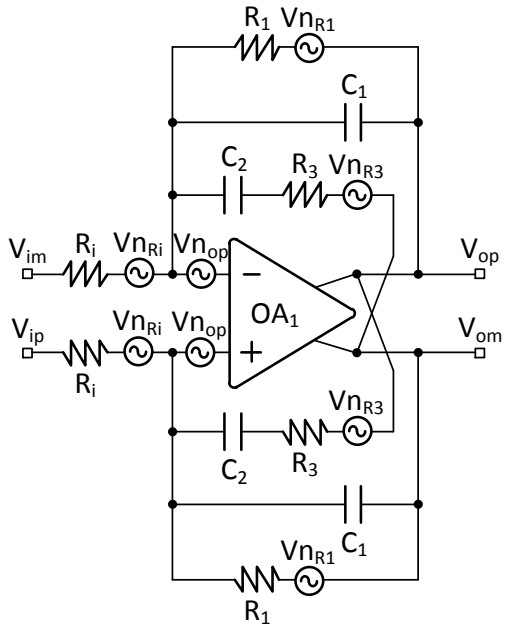

Figure 3.4: Noise sources in RC cross-coupled sigle-opamp resonator

the total input referred noise from the input resistors is

$$n_{i\_R_i} = \sqrt{2} \cdot n_{R_i} = \sqrt{2 \cdot 4KT \cdot R_i} \tag{3.10}$$

Another relevant contribution of noise in given by the opamp. The transfer function for the input referred noise of the opamp can be obtained from the transfer function of V_{n_op} to V_o as

$$H_{ni_{op}}(s) = \frac{V_{ni\_op}}{V_{n_{op}}} = \frac{V_o}{V_{n_{op}}} \cdot \frac{1}{H_X(s)} \tag{3.11}$$

where $H_X(s)$ is the transfer function of the RC cross-coupled resonator obtained from (3.4) and (3.8), while V_{n_op} is the equivalent noise source of the differential input (i.e. virtual grounds) referred noise of the opamp. Considering only the frequencies where the noise is integrated, (3.11) can be simplified and the input referred noise results to be

$$n_{i\_op} = n_{op} \cdot H_{ni_{op}}(s) = n_{op} \cdot \left(1 + \frac{R_i}{R_1}\right) \simeq n_{op} \tag{3.12}$$

because the value of R_1 is greater than R_i. In fact the DC_{gain} (i.e. R_1/R_i) must be $\gg 1$. Therefore, in the bandwidth of interest, all the noise generated by the

opamp is referred at the input.

Looking at the input referred noise of R_1, the equation can be derived as it has been done in the previous case. The transfer function of $V_{n\_R_1}$ to V_i is

$$H_{ni_{R1}}(s) = \frac{V_o}{V_{n_{R_1}}} \cdot \frac{1}{H_X(s)} = \frac{R_i}{R_1} \tag{3.13}$$

the input referred noise for both resistors R_1 is

$$n_{i_{R1}} = \sqrt{2} \cdot n_{R_1} \cdot \frac{R_i}{R_1} = \sqrt{2 \cdot 4KT \cdot R_1 \cdot \left(\frac{R_i}{R_1}\right)^2} = \frac{n_{R_i}}{\sqrt{DC_{gain}}} \tag{3.14}$$

therefore the noise contribution of R_1 are strongly attenuated by design, and thus are irrelevant compared to the noise generated by R_i.

Finally, the transfer function for the input referred noise of R_3 is

$$H_{ni_{R3}}(s) = \frac{V_o}{V_{n_{R_3}}} \cdot \frac{1}{H_X(s)} = \frac{s \cdot R_i C_2}{1 + s \cdot R_3 C_2} \tag{3.15}$$

the input referred noise for both resistors R_3 is

$$n_{i_{R3}} = \sqrt{2} \cdot n_{R_3} \cdot \frac{s \cdot R_i C_2}{1 + s \cdot R_3 C_2} \tag{3.16}$$

thus, the noise of R_3 is high-pass filtered and if the frequency of the pole in (3.15) is higher than the bandwidth of interest, its input referred noise is negligible.

In conclusion, the input referred noise for the RC cross-couple resonator can be expressed in good approximation as

$$n_{i_{Res}} = \sqrt{(n_{i_{Ri}})^2 + (n_{i_{op}})^2} \tag{3.17}$$

3.1.2 Final Integrator/Adder

An active-RC circuit based on differential opamp provides the final integration operation, with a frequency ω_i at 0-dB gain equal to

$$\omega_i = \frac{a_{3c}}{a_{2c} T_s} = \frac{1}{R_4 C_4} \tag{3.18}$$

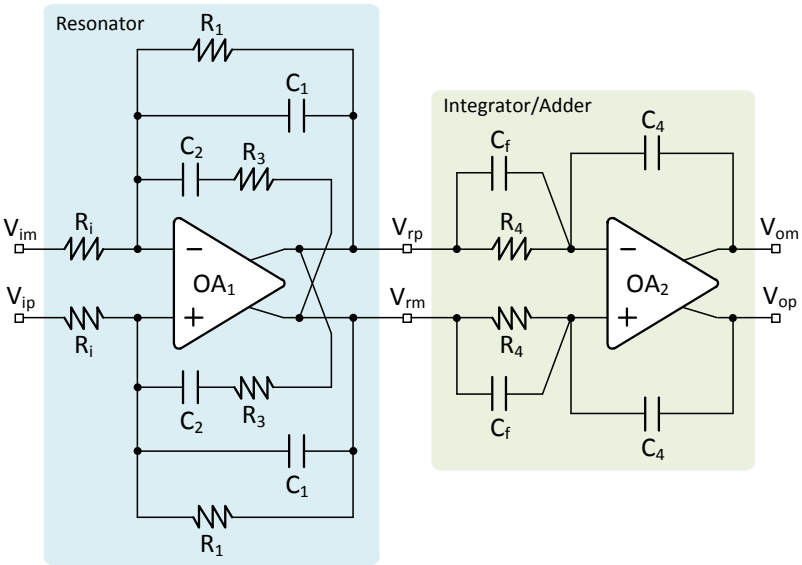

Figure 3.5: Loop filter implementation

The need of an additional summing amplifier can be avoided with the use of capacitive feedforward structures directly at the summing junction of the final integrator opamp [25]. The feedforward path is implemented with capacitive branches C_f, directly coupled to the virtual ground of opamp OA_2, thus realizing a simple gain coefficient and actually bypassing the integrator. The feedforward gain is given by the ratio C_f/C_4. The transfer function for the integrator/adder is

$$H_b(s) = \frac{C_f}{C_4} \cdot \frac{1}{sR_4C_4} \tag{3.19}$$

The entire schematic of the proposed loop filter is thus obtained cascading the single-opamp resonator and the final integrator/adder, as shown in Fig. 3.5, and the resulting transfer function for the loop filter is

$$H_{loop}(s) = H_X(s) \cdot H_b(s) \tag{3.20}$$

The input referred noise generated from R_4 is negligible because it is strongly attenuated in the audio bandwidth by $H_X(s)$. It is thus possible choosing the value of R_4 in function of area optimization.

Table 3.1: Components Values

Resistor	**Value [Ω]**	**Capacitor**	**Value [F]**
R_i	47k	C_1	9.2p
R_1	11M	C_2	9.2p
R_3	114k	C_f	2p
R_4	1M	C_4	2p
Approx. Area	0.076 mm^2	**Approx. Area**	0.025 mm^2

3.1.3 Componet Values

The component values are obtained from the coefficient values in Tab. 2.1 and the equations (3.9). For thermal noise requirements, the input resistors R_i are designed as low as 47 kΩ. The corresponding values are reported in Tab. 3.1. In the table are reported also the approximation values for the required areas, both for capacitors and resistors. These values are obtained from the 0.16 μm CMOS technology with MIM capacitors used for fabricate the proposed CT-ΣΔM. In this technology the MIM capacitors have a density of 2 pF/μm^2, while the poly resistors have a resistance of 0.33 kΩ/μm if a width of 1 μm is assumed. Notice that the MIM capacitors are realized with the top layers of metal (i.e. metal 5 and metal 4), while the resistors are realized in poly silicon and metal 1. In the physical layout, it is therefore possible placing the capacitors above the resistors to save area. For this reason, would be better have the same area for resistors and for capacitors, thus optimizing the overall area. To achieve that, the coefficients must be scaled in order to reduce the total resistance and increase the total capacitance.

From (3.20), the coefficients scaling can be done dividing by a factor K the transfer function of the resonator and restore the overall transfer function multiplying by the same factor the transfer function of the integrator/adder:

$$H_{loop}(s) = \left[\frac{1}{K} \cdot H_X(s)\right] \cdot [K \cdot H_b(s)] \tag{3.21}$$

For increasing the total capacitance and decreasing the total resistance, the factor K must be greater than 1.

There are also other benefits by choosing a factor $K>1$. As already mentioned, for the cross-coupled resonator, in case of a real opamp, the peak gain at ω_0 is determined by the open loop gain of the opamp at this frequency, because there is

Table 3.2: Components Values from scaled coefficients with K=2

Resistor	**Value [Ω]**	**Capacitor**	**Value [F]**
R_i	47k	C_1	18p
R_1	5.7M	C_2	18p
R_3	57k	C_f	2p
R_4	1M	C_4	1p
Approx. Area	0.041 mm^2	**Approx. Area**	0.041 mm^2

no feedback at ω_0. Therefore, the resonator Q factor is bounded by the open loop gain of the opamp and by the resonator DC_{gain} (Fig. 3.6a). There are two ways to increase the resonator Q factor:

- increasing the open loop gain of the opamp at ω_0, i.e. increasing the bandwidth of the opamp. This solution has the drawback to require more power consumption.
- decreasing the resonator DC_{gain}, as shown in Fig. 3.6b.

The loop filter requires a Q greater than 1.5 for exhibiting the benefits of conjugate complex zeros in the NTF. Therefore, scaling the coefficients with K>1 (i.e. decreasing the resonator DC_{gain}) improves also the NTF.

Another benefit brought by a factor K>1 is the reduction of the resonator output swing. The transient responses of the loop filter inside the proposed CT-ΣΔ modulator are analyzed in Fig. 3.7. The 1 V_{rms} full-scale differential input signal is shown in Fig. 3.7a, while the corresponding full scale loop filter output (i.e. the quantizer input) is shown in Fig. 3.7b. The differential resonator output is shown in Fig. 3.7c in case of original coefficient values, while in Fig. 3.7d it is shown in case of scaled coefficient values. Notice that the resulting swing is attenuate by the factor K, thus choosing K>1 permits to relax the requirements for the output stage of the resonator opamp.

A good trade-off between optimized area, Q factor and resonator output swing is obtained for K=2. The scaled coefficient values are shown in Tab. 3.2.

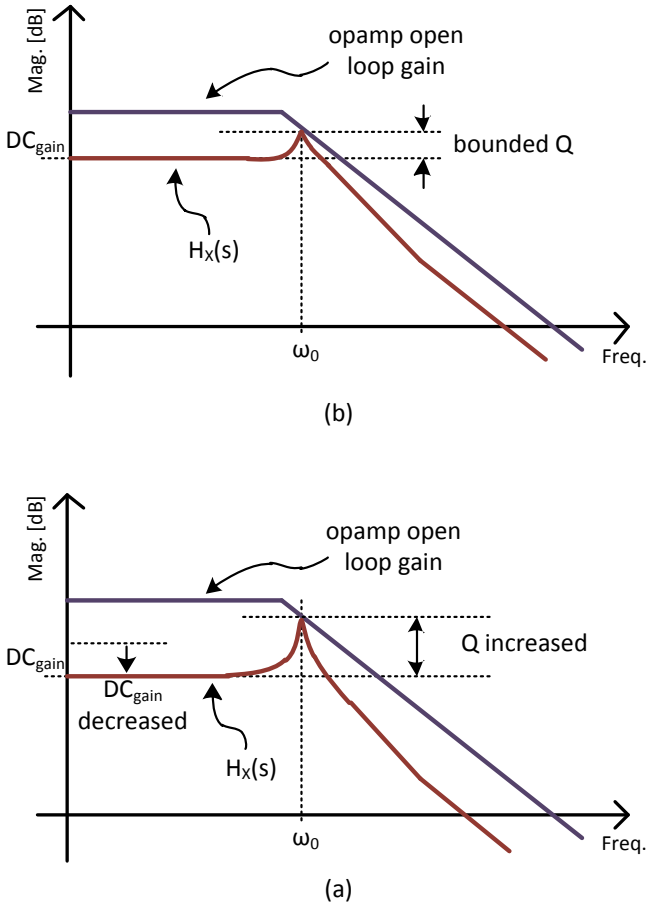

Figure 3.6: Resonator Q factor limits with real opamp: (a) Q factor proportional to distance from opamp open loop gain at ω_0 and resonator DC_{gain} (b) Q factor increasing due the decreasing of resonator DC_{gain}

3.1.4 Operational Amplifiers

The opamp used in the resonator (OA_1) is realized using a Miller two-stage topology, which features low output impedance, as required for achieving the desired resonator transfer function. In fact, the RC cross-coupled feedback network can works properly only assuming a low output impedance, thus other opamp topology (e.g. folded cascode) with higher output impedance are not suitable. Remember, from the previous section, that the Q-factor of the resonator depends on the opamp open-loop gain at the frequency of resonance. Although this gain needs to be larger compared to a conventional implementation (i. e. simple integrator at

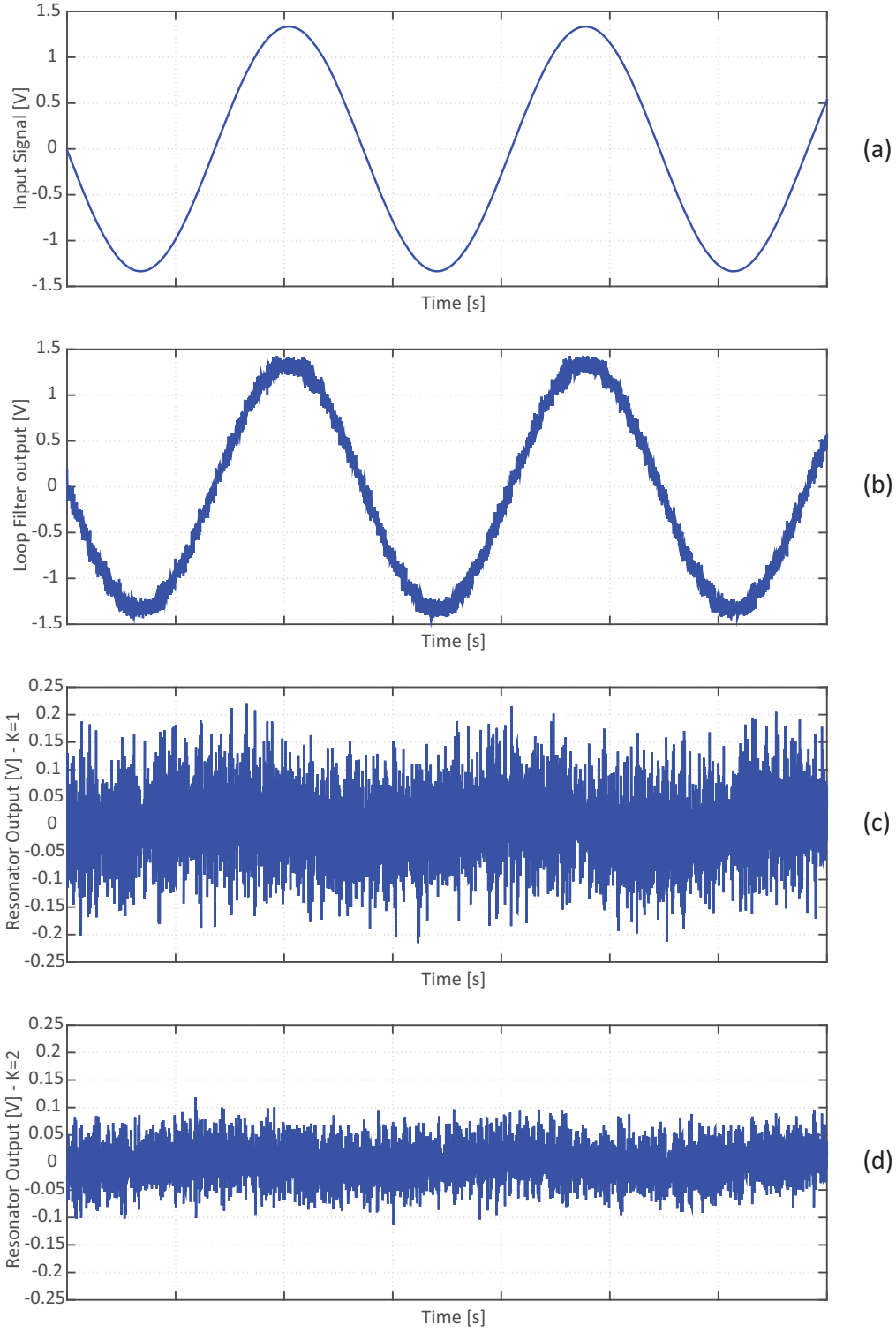

Figure 3.7: Transient response in the CT-ΣΔ modulator loop filter: (a) 1 V_{rms} full-scale differential input signal (b) 1 V_{rms} full-scale differential output signal (c) original resonator differential output signal (d) resonator differential output signal scaled with factor K=2

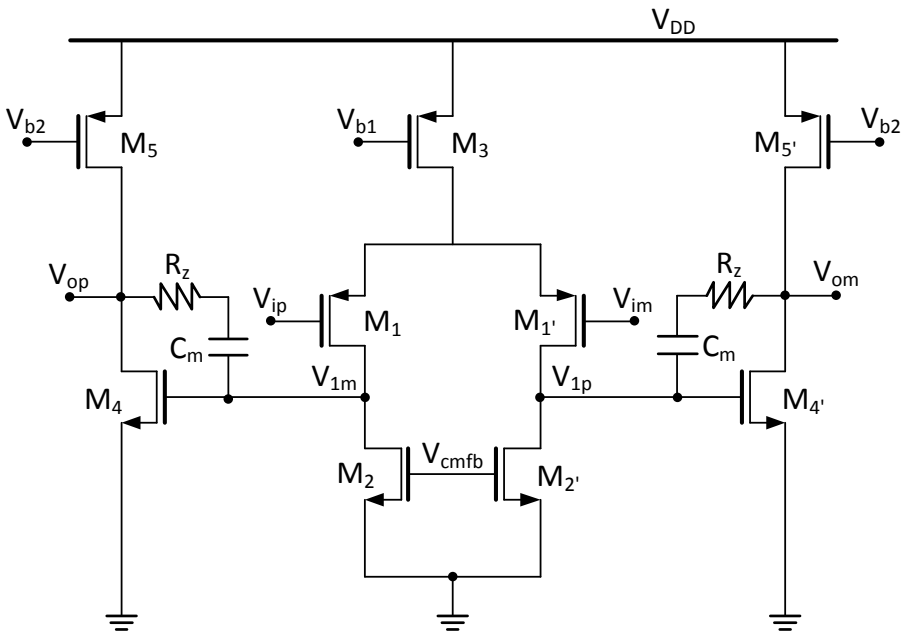

Figure 3.8: Circuit schematic of the opamp OA_1 used in the resonator

the input), in order to guarantee a Q-factor large enough, the extra amount of gain is provided at no cost by the increased value of transconductance of the input pair, required to fulfill thermal noise constraints. These concepts, in conjunction with the low output voltage swing guaranteed by the feedforward architecture, further halved by scaling factor K=2, allows the opamp to be designed focusing on the optimization of the frequency-response and not of the output swing or the current driving capability, thus saving power.

The circuit schematic of the opamp is shown in Fig. 3.8. The input pair (M_1-M_1') is made with pMOS transistors with long channels to lower the $1/f$ input-referred noise. The transistor M_3 sets the quiescent current of the input pair to be 20 μA, thus allowing to obtain a value of transconductance of the input pair that fulfills the thermal noise constraints. The class-A second stage (M_4-M_4') ensures a constant low output impedance. The opamp is Miller-compensated using R_z and C_m. The value of C_m is chosen to be 2 pF, while R_z is chosen to be 30 kΩ.

The common-mode feedback (CMFB) circuit that stabilizes the output level of OA_1 is shown in Fig. 3.9. The quiescent output voltage at nodes V_{1p} and V_{1m} (which is also the gate-source voltage of M_4-M_4') sets the quiescent currents in the second stage. To set the output quiescent currents accurately, the CMFB controls the

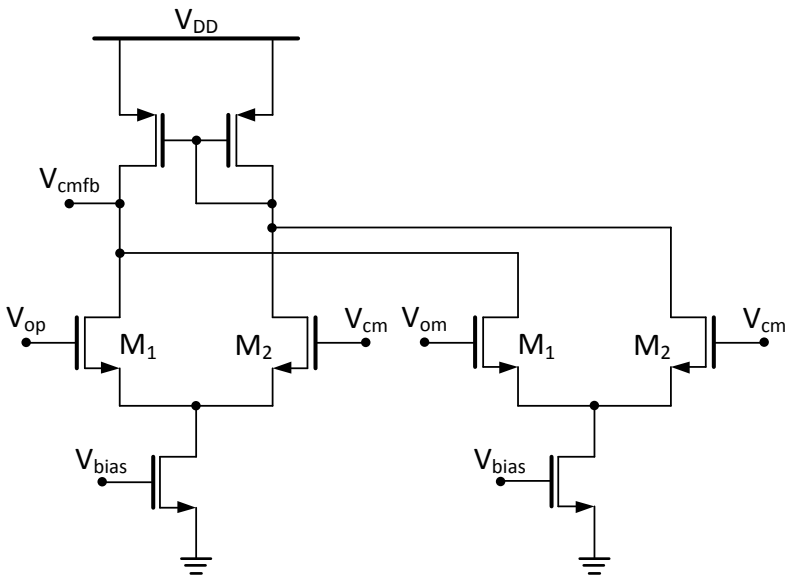

Figure 3.9: Circuit schematic of the CMFB used in opamp OA_1

V_{cmfb} bias voltage. The common-mode reference V_{cm} is the desired common-mode voltage of the output stage, equal to $V_{DD}/2$. Since the signal swings at V_{om} and V_{op} are modest, the linearity of the common-mode detector is not critical. Quiescent current through each output branch (M_4 and M_4') is 14 µA. The total bias current of OA_1, including the CMFB circuit, is 50 µA

The integrator/adder opamp (OA_2) is also based on a two-stage topology, since it has to sustain the full-scale signal voltage swing (1.4 V) at the input of the multibit quantizer. The circuit schematic of the opamp is shown in Fig. 3.10. The topology is a replica of OA_1, but with a much smaller input pair because noise contributions from M_1 and M_1' are negligible if referred at the input of the loop-filter. For the same reason, the quiescent current of the input pair can be as low as 4 µA to have enough bandwidth. The value of C_m is chosen to be 1 pF, while R_z is chosen to be 20 kΩ.

Since the output swings of OA_2 are large, linear operation of the CMFB mechanism is ensured by using resistive averaging to detect the output common mode, as shown in Fig. 3.11a. The C_c=250 fF capacitors provide a fast high-frequency path, bypassing the resistive common-mode detector and the error amplifier [19], thus increasing the stability. The quiescent currents in the transistors M_4 and M_4' are made 1.5 times larger than quiescent currents in the upper transistors M_6 and

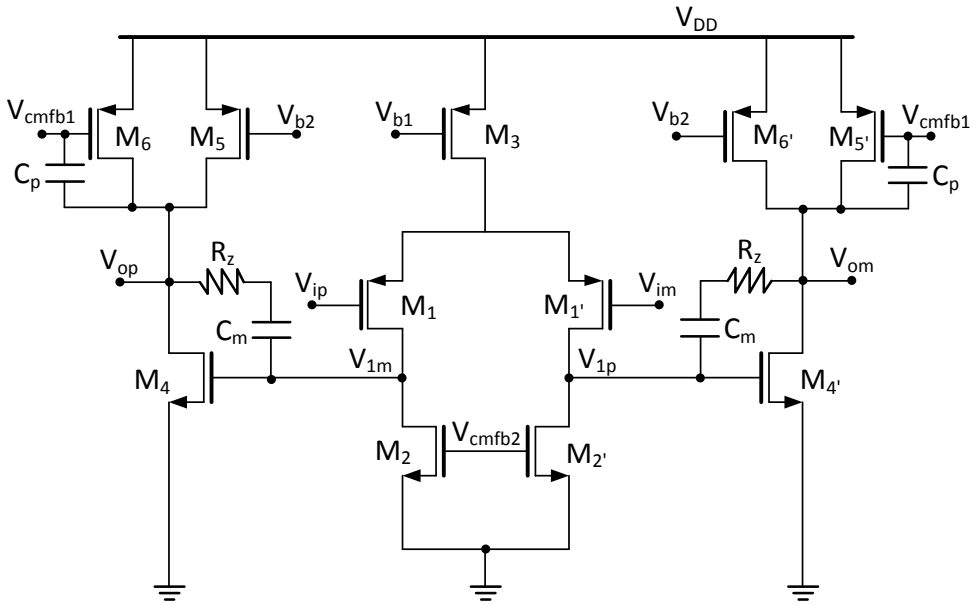

Figure 3.10: Circuit schematic of the opamp OA_2 used in the integrator/adder

M_6'. The remain of the quiescent current is provided by the CMFB circuitry. This technique ensures stability and reliable operation of the CMFB loop. Quiescent current through each output branch (M_4 and M_4') is 12 μA. A second CMFB is necessary to set the common mode value at nodes V_{1p} and V_{1m} (Fig. 3.11b). A resistive averaging is used to detects the common mode, then an error amplifier generates the voltage V_{cmfb2} to ensure a common mode equal to V_{ref}. To set the active-load (M_2 and M_2') quiescent currents accurately, the common-mode reference V_{ref} is derived from a diode-connected transistor biased with a fixed current. The total bias current of OA_1, including both CMFB circuits, is 30 μA

3.1.5 Loop Filter Input Referred Noise

The input referred noise of the loop filter is limiting the performance of the entire CT-ΣΔ modulator, therefore it is fundamental a detailed analysis. In the previous section, an analytical analysis of the input referred noise in the single opamp resonator was presented, while in this section the related simulation results are reported, this time considering the entire loop filter. The input referred noise values have been integrated in the range from 20Hz to 20kHz, i.e. the audio bandwidth.

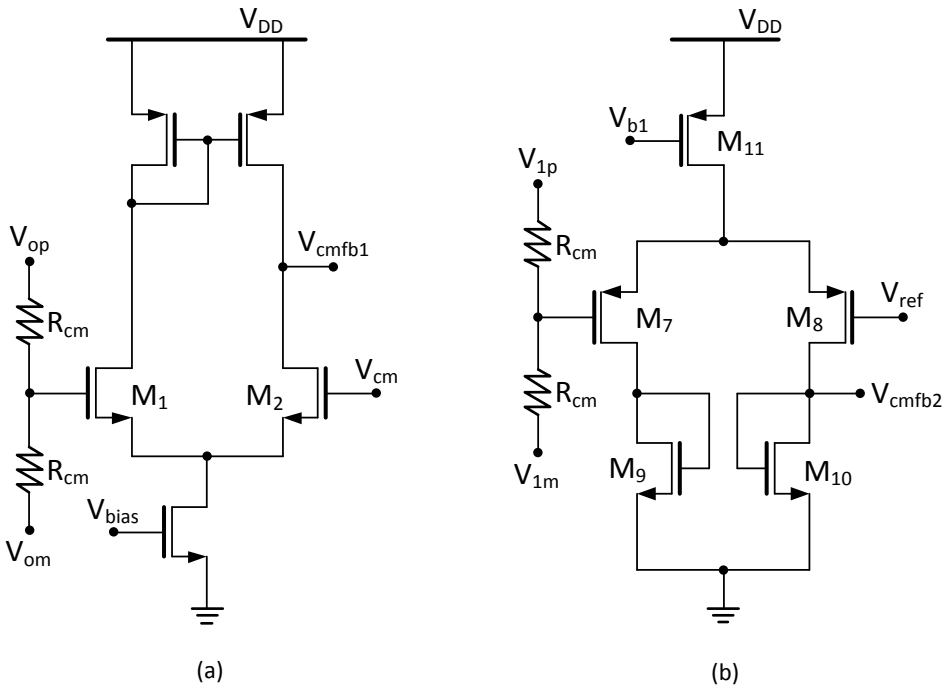

Figure 3.11: Circuit schematic of the CMFBs used in opamp OA_2. (a) CMFB for common mode of V_{om} and V_{op} (b) CMFB for common mode of V_{1p} and V_{1m}

Table 3.3: Input referred noise of loop filter resistors integrated from 20Hz to 20kHz

Component	**Noise Contribution [μV]**
R_i	5.57
R_3	0.38
R_1	0.49
R_4	0.15
Total	**5.61**

Regarding the resistors of the loop filter, their input referred noise values are reported in Tab. 3.3. These values are related to the differential implementation (e.g. R_i=$R_{i+} + R_{i-}$). The main contribution of noise is given by the input resistors R_i, while, as expected form (3.13)-(3.16), the contributions of noise of the other resistors are not dominant.

In Tab. 3.4 the input referred noise values of the transistors inside OA_1 are reported, always considering the differential implementation. The main contribution of noise is the thermal noise of the input pair M_1 and M_1' (referring to Fig. 3.9), while its flicker noise is much lower since these pMOS transistors are made with long

Table 3.4: Input referred noise of the transistors of OA_1 integrated from 20Hz to 20kHz

Component	Type	Noise Contribution [μV]
M_1	Thermal	1.84
M_1	Flicker	0.99
M_2	Thermal	0.46
M_2	Flicker	0.32
M_4	Flicker	0.29
	Total	**2.18**

channel. The other contributions of noise in the OA_1 are the transistors of the active load M_2 and M_2' and the transistors of the second stage, M_4 and M_4'. The input referred noise from the remaining transistors is completely irrelevant, as well the input referred noise of OA_2.

The total differential input referred noise is 6.02 μV, or rather -104.4-dBV$_{\text{RMS}}$, while the differential full scale input signal is 2.8 V_{pp}, i.e. 1 V_{RMS}. Therefore, the SNR of the loop filter is 104.4-dB.

3.2 Excess Loop Delay Compensation implementation

The ELD compensation, that has been studied in Chapter 2, requires a feedforward path from the ΣΔ modulator input and a local feedback, both derived and summed passively at the input of the last integrator.

The feedforward path is implemented is the same way of the feedforward path inside the loop filter: a capacitive branch C_d is directly coupled to the virtual ground of opamp OA_2, thus realizing a simple gain coefficient and bypassing the integrator. The feedforward gain is given by the ratio C_d/C_4. The differential implementation is shown in Fig. 3.12.

The local feedback is implemented with a 15-levels pseudo SC-DAC shown in Fig. 3.13 that is directly coupled to the virtual ground of opamp OA_2 too. The ΣΔ modulator thermometric output delayed bits control the switches at the bottom plate of each unit capacitor as fallows:

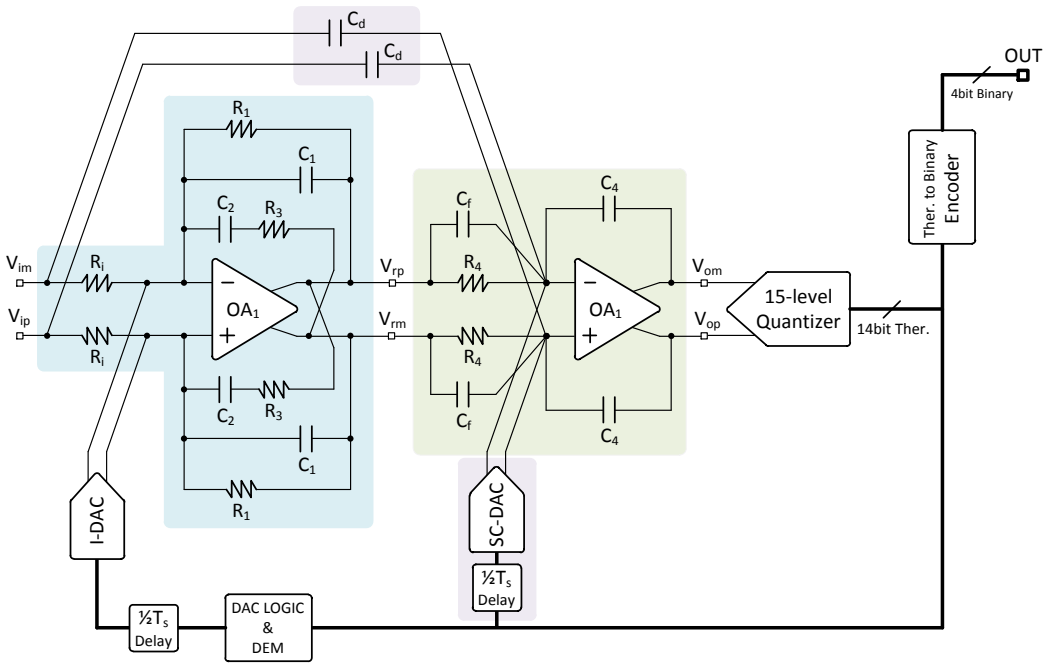

Figure 3.12: Schematic of the proposed CT-ΣΔM. Highlighted in blu: RC cross-coupled single opamp resonator. Highlighted in green: integrator/adder. Highlighted in purple: ELD compensation (feedforward and local feedback)

- n **thermometric bit=1** The bottom plate of the n unit capacitor connected to the negative virtual ground is connected at power ground ($avss$), while the bottom plate of the n unit capacitor connected to the positive virtual ground is connected at power supply ($avdd$)

- n **thermometric bit=0** The bottom plate of the n unit capacitor connected to the negative virtual ground is connected at $avdd$, while the bottom plate of the n unit capacitor connected to the positive virtual ground is connected at $avss$

Therefore the total charge stored at the virtual grounds is proportional to the thermometric code, as reported in Tab. 3.5. The feedback gain is given by the ratio C_{tot}/C_4, where $C_{tot} = 14 \cdot C_{dac}$.

Notice that dedicated voltage references are not necessary, in fact all the possible non-idealities derived from the power supplies $avdd$ and $avss$ (i.e. noise, spikes..) are shaped by the NTF. For the same reason, also an additional dynamic elements matching (DEM) will be unnecessary: non-linearities introduced by unit capacitors mismatch does not affect the performance of the ΣΔ modulator. Thus, the local

Table 3.5: Local feedback DAC charge Q levels

Thermeter Code	Minus Ground Q	Plus Ground Q
00000000000000	$avss \cdot 14 \cdot C_{dac}$	$avdd \cdot 14 \cdot C_{dac}$
00000000000001	$avss \cdot 12 \cdot C_{dac}$	$avdd \cdot 12 \cdot C_{dac}$
00000000000011	$avss \cdot 10 \cdot C_{dac}$	$avdd \cdot 10 \cdot C_{dac}$
00000000000111	$avss \cdot 8 \cdot C_{dac}$	$avdd \cdot 8 \cdot C_{dac}$
00000000001111	$avss \cdot 6 \cdot C_{dac}$	$avdd \cdot 6 \cdot C_{dac}$
00000000011111	$avss \cdot 4 \cdot C_{dac}$	$avdd \cdot 4 \cdot C_{dac}$
00000000111111	$avss \cdot 2 \cdot C_{dac}$	$avdd \cdot 2 \cdot C_{dac}$
00000001111111	$0 \cdot C_{dac}$	$0 \cdot C_{dac}$
00000011111111	$avdd \cdot 2 \cdot C_{dac}$	$avss \cdot 2 \cdot C_{dac}$
00000111111111	$avdd \cdot 4 \cdot C_{dac}$	$avss \cdot 4 \cdot C_{dac}$
00001111111111	$avdd \cdot 6 \cdot C_{dac}$	$avss \cdot 6 \cdot C_{dac}$
00011111111111	$avdd \cdot 8 \cdot C_{dac}$	$avss \cdot 8 \cdot C_{dac}$
00111111111111	$avdd \cdot 10 \cdot C_{dac}$	$avss \cdot 10 \cdot C_{dac}$
01111111111111	$avdd \cdot 12 \cdot C_{dac}$	$avss \cdot 12 \cdot C_{dac}$
11111111111111	$avdd \cdot 14 \cdot C_{dac}$	$avss \cdot 14 \cdot C_{dac}$

feedback DAC requires a negligible amount of power and area compared to the main feedback DAC.

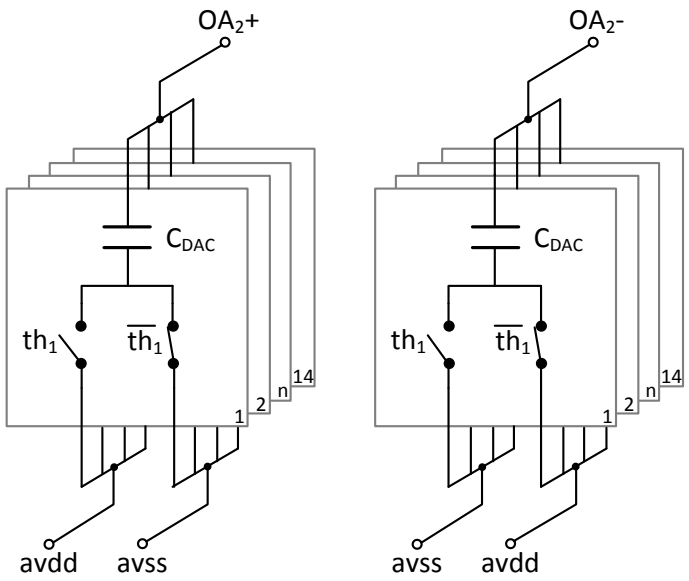

Figure 3.13: Local feedback DAC scheme

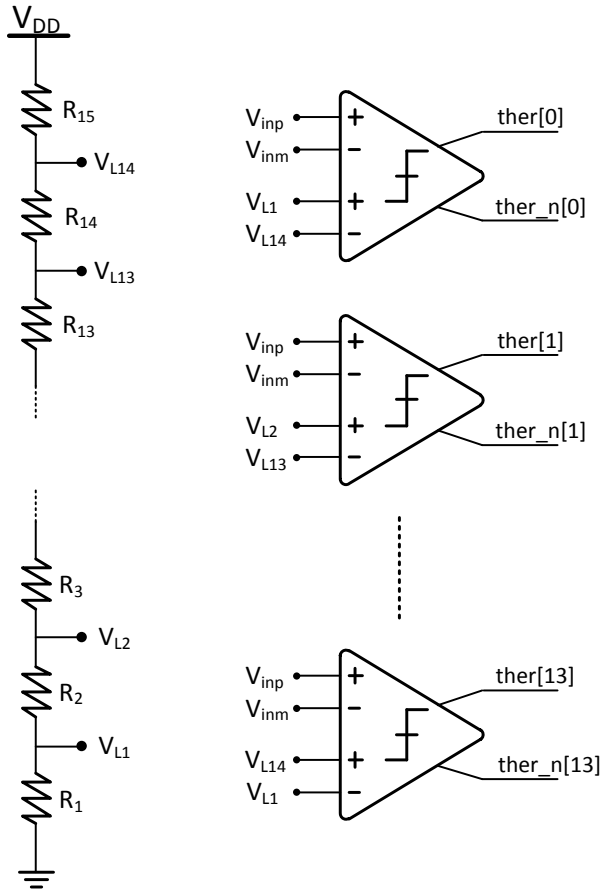

Figure 3.14: Structure of the flash ADC with 14 identical differential comparators and threshold voltages generated from analog power supply with a resistive divider

3.3 Quantizer

The 15-level quantizer used in the proposed CT-ΣΔM is illustrated in Fig. 3.14. It is a flash ADC realized with 14 identical differential comparators and a resistive divider from the analog power supply for generating the threshold voltages. The circuit diagram of the comparator and the corresponding clock waveforms are shown in Fig. 3.15 and Fig. 3.16, respectively. The input range of each converter is [0.1 V, 1.5 V], and thus the nominal step size is 93.3 mV, relaxing the offset requirements of the comparators. The operating principle of each comparator it described as fallow. During phase ph_1 the required threshold voltages are applied, respectively, to one plate of the capacitors C_{inp} and C_{inm}, while the common mode of the analog signal (equal to $V_{DD}/2$) is applied to the other plates, that are also

connected to the inputs of the differential pair (M_1 and M_2). During phase ph_2 the input signal (output of the loop filter) is sampled and stored in the input capacitors C_{inp} and C_{inm}, in order to obtain the subtraction between the threshold voltage and the input voltage to be compared. In Fig. 3.15 is shown the low power clocked comparator with a latch as active load of the differential input pair (latched comparator). The differential pair is biased with a constant current (M_7), avoiding large dynamic current consumption during the comparison time. The decision take place during ph_2, while during $\overline{ph_2}$ the output is forced by sw_2 and sw_3 to the hold-state and the input pair is reset by sw_1. The output of the comparator is hold during ph_1 and until the next comparison by an additional latch, that also guarantees the driving capabilities of the interconnected digital logics. It thus seen that the latched comparator and the additional latch are acting like a master-slave D flip-flop that is triggered on the rising edge of ph_2. A problem which can occur in a latched comparator is the metastability error. Considering the two operation phases, reset phase and regeneration phase, the latch has to produce a valid logic level within half of the clock period. When the input voltages are very close to each other, the latch takes more time to produce a logic level, which might result in a metastable state. In other words, a metastable situation occurs when the latch is not able to switch to a valid logic level, zero or one, in the regeneration time slot and reaches an intermediate value. The metastability error can adversely affect the accuracy of the comparator and of the ADC. The probability of metastability is inversely proportional to the comparator gain. To avoid this problem a reasonable gain and hence a 2.8 μA quiescent current are exploited to reduce the regeneration time and increase the speed. The static bias current of the whole quantizer is 40 μA.

3.3.1 Non-overlapping phases generator

In Fig. 3.17 the schematic of the phases generator is reported. The circuit has been designed to supply two in-counter-phase non-overlapping clocks ph_1 and ph_2, with their relative negated versions, named $\overline{ph_1}$ and $\overline{ph_2}$, as shown in Fig. 3.16. Using this non-overlapping phases to drive the comparator threshold capacitors, it is possible to strongly limit the charge injection and so improve the linearity. All the logic ports are the default ports included in the technology digital library, except for the highlighted inverters included in the delay paths, of which length dimensions are 1 μm. The non-overlapping time T_o is equal to 600 pS.

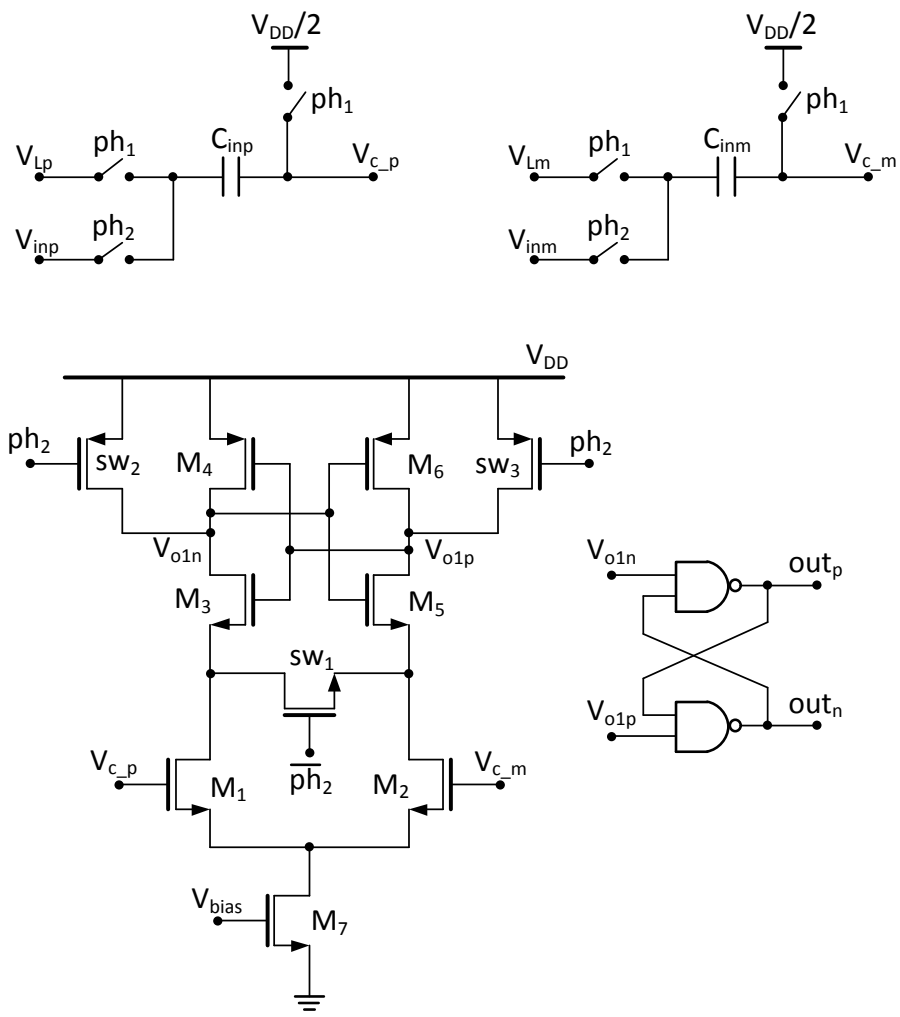

Figure 3.15: Circuit schematic of the low power clocked comparator

3.4 Feedback DAC

The main ΣΔ modulator feedback loop is realized with a 15-level current-steering DAC, directly coupled at the virtual grounds of OA_1, as seen in Fig. 3.12.

There are several ways to implement such kind of DAC. In [25] the authors use the architecture depicted in Fig. 3.18: in this topology of current-steering DAC, the output currents are given by the difference of the fixed currents I (provided by the generators on the top) and the selected current DAC elements, each with a current equal to $2I/n$, where n is the number of comparators inside the ADC (i.e. the number of DAC levels minus 1). The total number of DAC element is n. The current I must be equal to the current flowing through the loop-filter input resistor

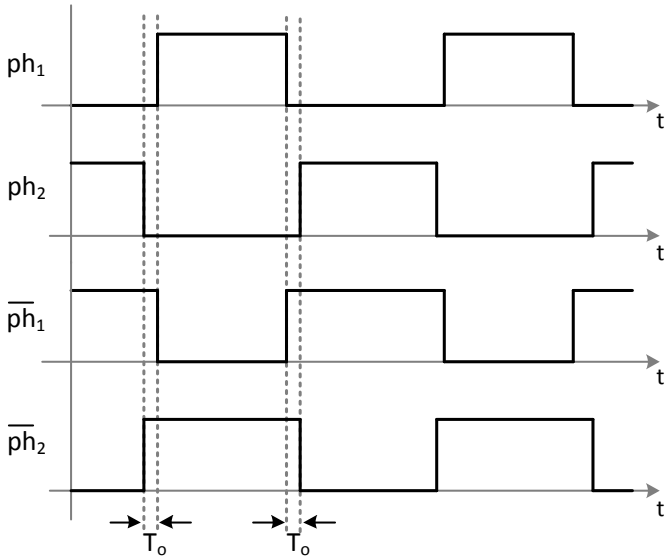

Figure 3.16: Non-overlapping phases behavior

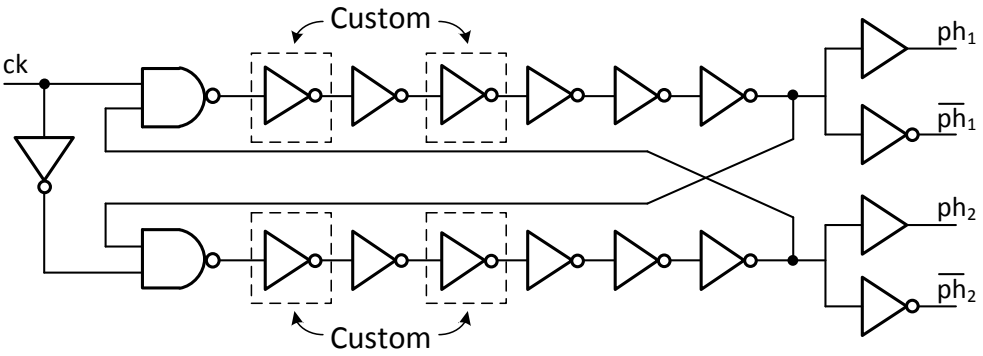

Figure 3.17: Non-overlapping phases generator schematic

when the input signal is at full scale (i.e. $I = V_{pp}/R_{in}$). In this topology, the switches inside the DAC elements are driven by the thermometer output code of the ADC, thus allowing an easy implementation. Moreover, the two-levels $(+1, -1)$ nature of each DAC element allows the use of traditional dynamic element matching (DEM), like in [19]. However, there are two main drawbacks. The first one in concerning the power consumption. In fact, in this topology, the total current required is $3 \cdot I$, while only a peak current $2 \cdot I$ is injected in the virtual grounds of the opamp. Therefore, there is always a loss of I current. The second drawback, even more important, in concerning the noise performance of the architecture.

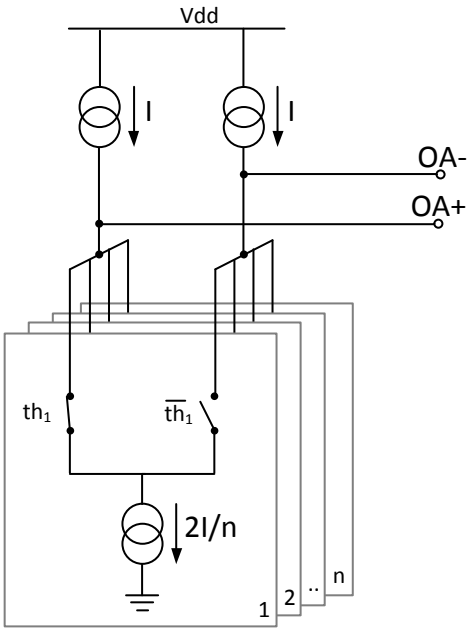

Figure 3.18: Current-steering DAC based on two-level elements

All the generators are constantly injecting noise (both thermal and flicker) in the virtual grounds, therefore the noise level is constant and independent from the input signal amplitude. This aspect can lead to limit the DR of the $\Sigma\Delta$ modulator. For instance, the results reported in [25] show a DR lower than 100 dB. For this reason this topology is not suitable to achieve the required performance in term of DR.

In order to increase the DR, a current-steering DAC based on three-level $(+1, 0, -1)$ elements can be used. This solution has been proposed in [26] and [27] for a single-bit implementation (i.e. only one three-level element is used). Then in [28] a multi-bit implementation and the theory to implement the DEM have been proposed. The architecture is shown in Fig. 3.19: in this topology the output currents are given by the sum of the currents $2I/n$ of the selected DAC elements. The principle of this topology is to not connect the inactive elements to the opamp virtual grounds during the 0 state (as shown in Fig. 3.20), leading to a significant reduction of the thermal noise contribution from the elements. Therefore, for low input signals, only one DAC three-level element is used and the DAC injects minimum noise current, improving the DR. For instance, this topology has been implemented in [29] and the reported DR is 102 dB. Moreover, in this topology the total current required is only $2 \cdot I$, therefore an amount of current I can be saved.

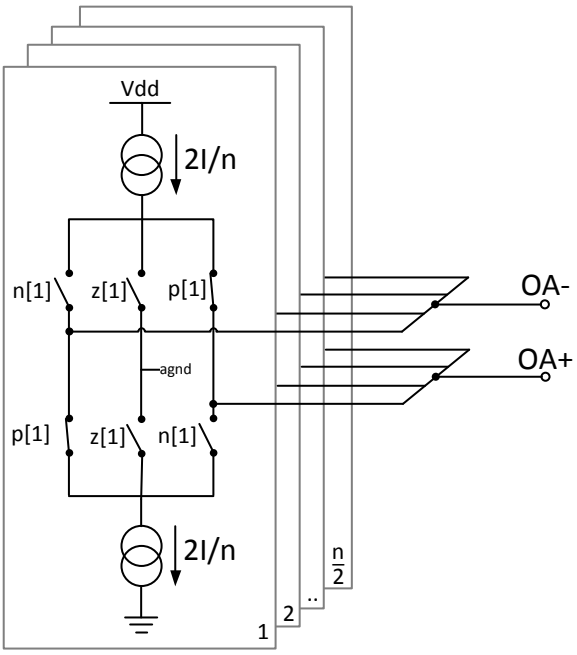

Figure 3.19: Current-steering DAC based on three-level elements

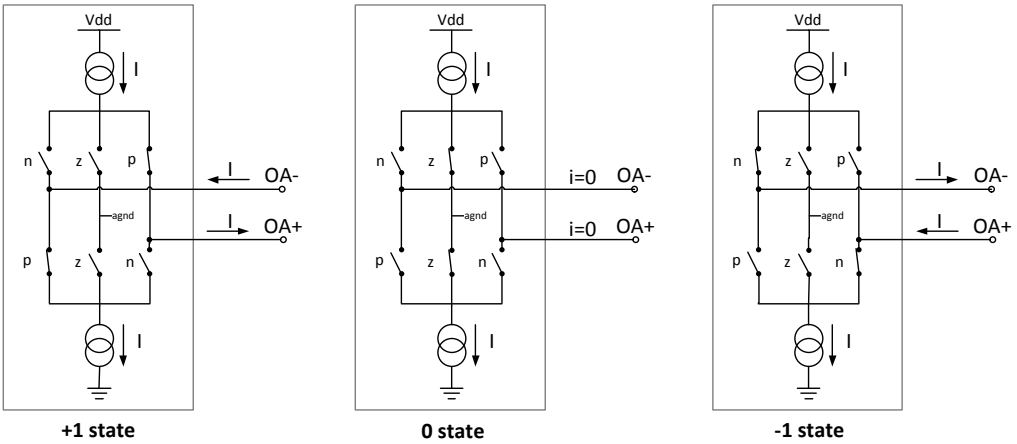

Figure 3.20: Different states in the current-steering three-level element

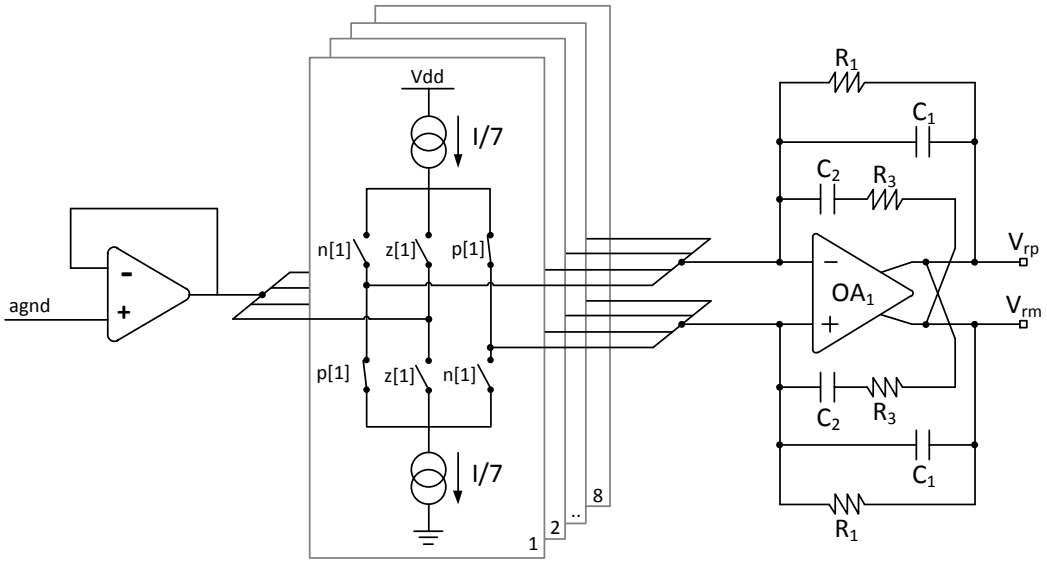

Figure 3.21: 15-level current-steering DAC to close the main feedback loop

The main 15-level current-steering DAC to realize the main feedback loop is based on 8 identical three-level current-steering elements, directly coupled at the virtual grounds of OA_1 (i.e. the resonator opamp), as shown in Fig. 3.21. Although 7 identical three-level elements are sufficient to achieve 15 levels, 8 elements are actually used because of the requirements of the Dynamic Element Matching (DEM) circuit, that will be introduced in the following section.

Each three-level current-steering element injects into the virtual grounds of OA_1 a current either equal to $+I/8$, 0, or $-I/8$, depending on the control bits $p[i]$, $n[i]$, and $z[i]$. When the injected current is equal to 0, the current generators are disconnected from the virtual grounds, therefore the current noise contribution at the input of the ΣΔM is null. With this solution, for low input signals (< -17 dB$_{\mathrm{FS}}$), only one DAC three-level element is used and the DAC injects minimum noise current, improving the *DR*. By contrast, for large input signals (> -17 dB$_{\mathrm{FS}}$), several DAC elements are used, increasing the DAC noise contribution, which becomes dominant, limiting the *SNR*.

3.4.1 Dynamic Element Matching

In order to improve the ΣΔ modulator linearity in the presence of mismatches in the DAC current-steering elements, a 1st-order DEM has been used. The 1st-order

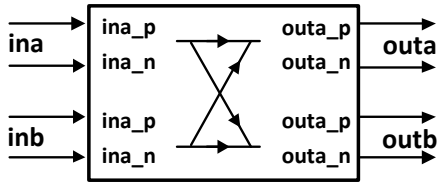

Figure 3.22: Single data shuffler cell

Table 3.6: Signed-thermometer encoding scheme

Value	Code p+n
$+1$	10
-1	01
0	00

DEM algorithm for three-level elements is realized with a structure of a data shuffler based on the butterfly-configuration presented in [28]. This structure shapes the mismatch error in a pair of three-level elements (data shuffler cell) while assumes a perfect matching between the $+1$ and the -1. The mismatch between these quantities will be analyzed later.

In the data shuffler cell, whose block diagram is shown in Fig. 3.22, the inputs and outputs are 2 signed-thermometer coded bits. The encoding values are reported in Tab. 3.6. The use of this encoding scheme allows an easier front-end digital implementation and a simple decoding circuit on the analog side, as will be dealt further. The outputs *outa* and *outb* of the shuffler cell drive a pair of analog elements whose output is from -2 to 2. This pair of analog elements has the transfer function shown in Fig. 3.23, where the input is the digital code and the output is the analog value, while e_a and e_b are the mismatch error associated with element a and b. According to [28], the error delivered by each output stream *outa* and *outb* is defined to be the difference between the ideal and the actual value of the outputs. Therefore the possible values of the error in the analog output are

$$0 \qquad or \qquad \frac{e_a - e_b}{2} \qquad or \qquad \frac{e_b - e_a}{2} \tag{3.22}$$

To keep track of the cumulative error of each cell, a 2-bit state machine can be

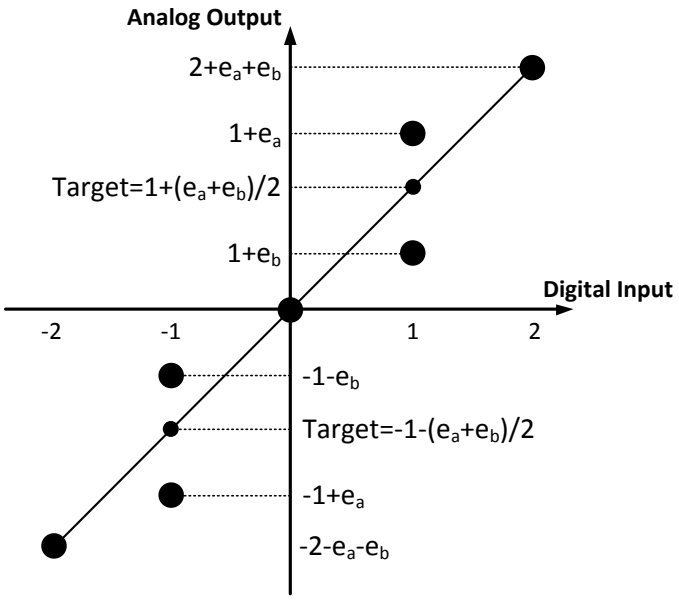

Figure 3.23: Transfer function of a pair of analog elements

used [28]. Therefore, the data shuffler cell is a state machine that monitors the input data and the cumulative error. This state machine then swap the inputs to the appropriate outputs in order to keep the cumulative error at zero. The state diagram of the state machine is shown in Fig. 3.24. The transfer function of the cumulative error has a 1st-order highpass characteristic which implies that any mismatch between the element a and b is 1st-order noise shaped.

The circuit diagram of the single data shuffler cell is shown in Fig. 3.25. All the digital ports are minimum size, thus saving area and power. The two D flip-flops keep track of the sequential process (i.e. the cumulative error), while the combinatory process controls the four multiplexers to swap the inputs to the appropriate outputs, thus keeping the cumulative error at zero. The change of state happens at the rising edge of ph_2, or rather after the commutation of the DAC analog outputs and before the generation of a new input code by the comparators inside the ADC.

The data shuffler cells are then connected in a butterfly network to form a 16-bit signed-thermometer input data shuffler, as shown in Fig. 3.26. The signed-thermometer input of the data shuffler is derived from the 14-bit unsigned-thermometer coded output word of the quantizer this the use . The outputs of the

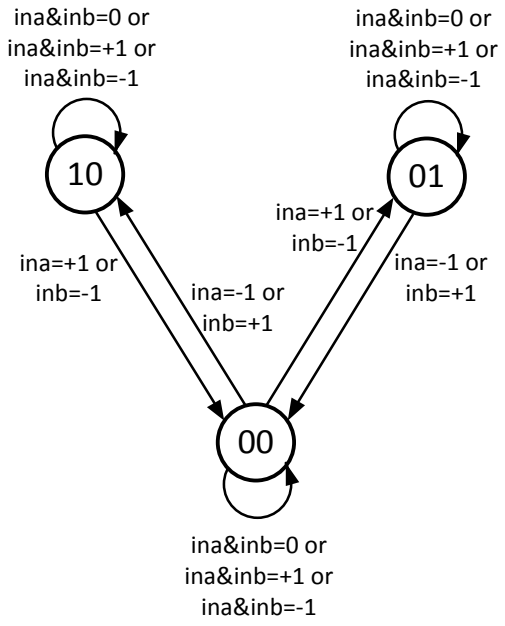

Figure 3.24: State diagram of the state machine inside the data shuffler cell

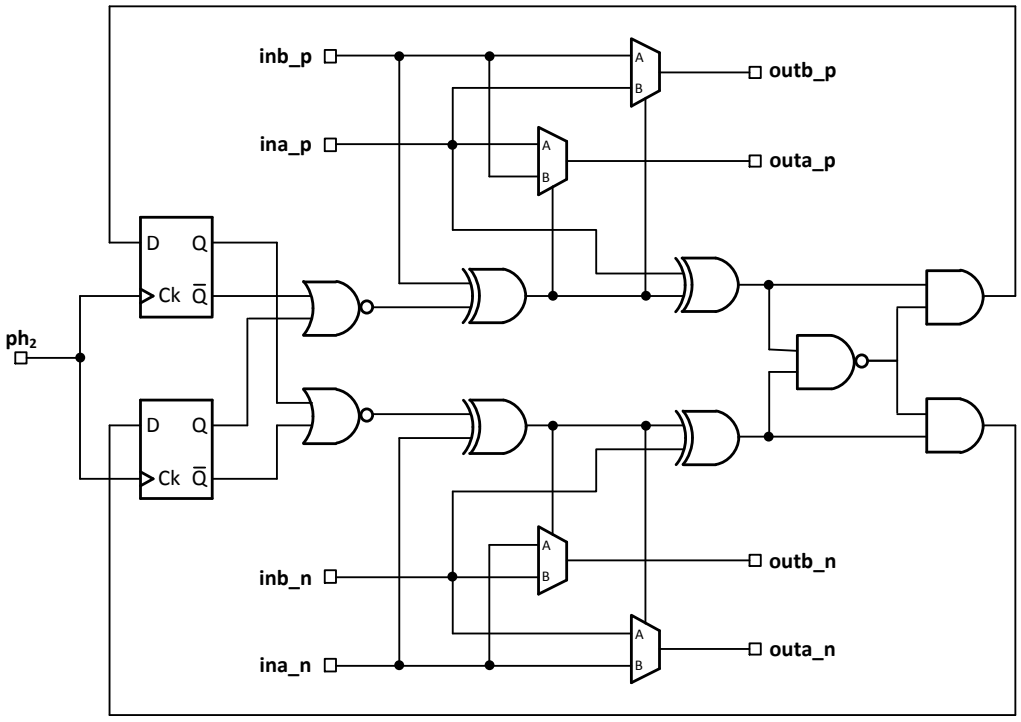

Figure 3.25: Circuit diagram of the state machine inside the data shuffler cell

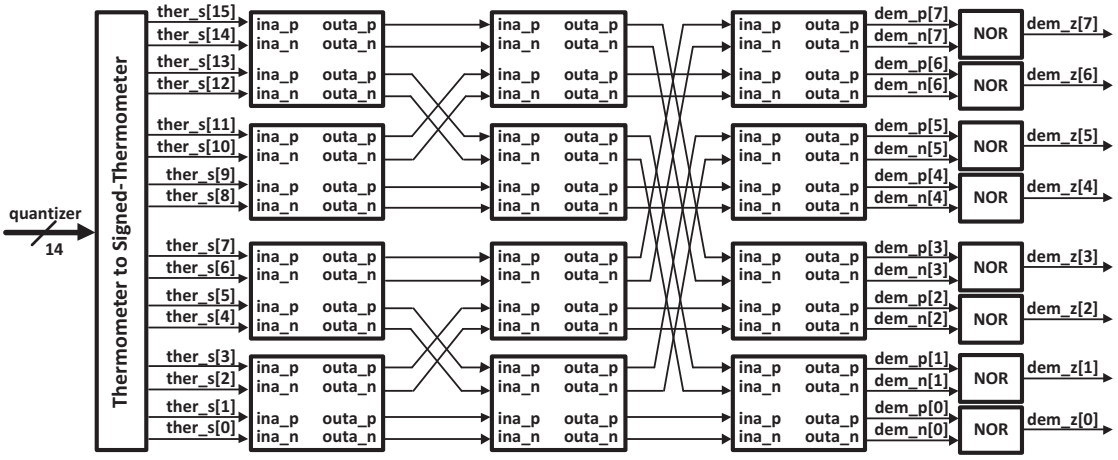

Figure 3.26: DEM schematic and generation of the DAC control bits

data shufflers are the control bits $dem\_p[i]$ and $dem\_n[i]$ for the DAC elements, while the remaining control bit $dem\_z[i]$ is generated from $dem\_p[i]$ and $dem\_n[i]$ with a simple NOR logic gate.

Moreover, in the three-level element DEM architecture the switching activity is directly proportional to the amplitude of the input signal. Hence, at low input level such as -17 dB_{FS} or below, the power consumption of the DEM mentioned above is lower compared to a two-level element architecture, thus saving power.

3.4.2 Circuit Design

The first challenge in the design of the current-steering DAC is to handle the offset referred at the input of OA_1, as shown in Fig. 3.27. The offset voltage changes the drain voltage of the pMOS and nMOS current generators depending on the signal, results in a nonlinear transfer function for the cell, i.e. a dynamic mismatch that can not be corrected by the DEM. Moreover, this nonlinearity affects both differential and single-ended outputs and cannot be fixed by the use of differential circuit. A solution is the use of cascode devices that keep constant the drain voltages. Furthermore, to maintain a reasonable headroom in the current sources, an high compliance cascade has been used.

The circuit diagram of the single three-level DAC element is shown Fig. 3.28. Both the pMOS (M_3) and nMOS (M_1) current generators have a length dimensions of 20 µm, while the width is 9.4 µm for the pMOS and 5.4 µm for the nMOS. Such value of length allows to keep low the flicker noise and to decrease the gm

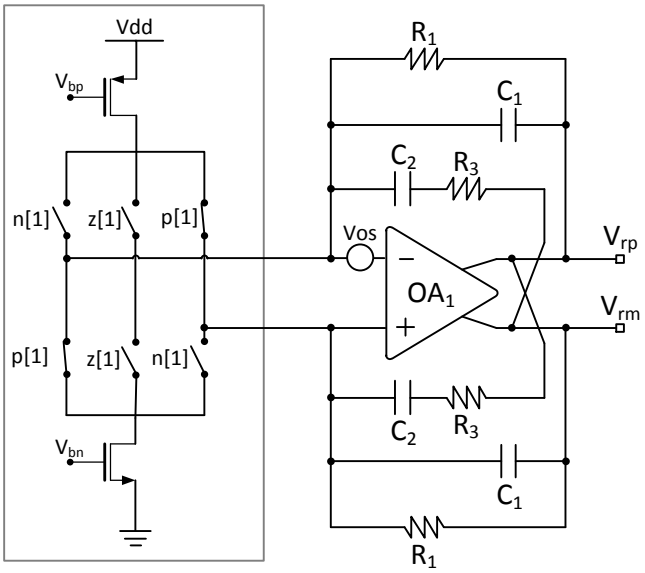

Figure 3.27: Opamp offset and 3-level DAC element

of the transistors, thus lowering the thermal noise too. The current generated by M_1 and M_3 is I_{unit}=2.1 µA. The noise performance will be analyzed later. The transistors M_2 and M_4 are the cascode devices. The switches sw_1-sw_6 are minimum size transistors to reduce the capacitive load for the control bits, thus allowing a fast transition from one state to another.

The circuit needed to generate all the bias voltages for each single DAC element is shown in Fig. 3.29. The reference current I_{ref_p} is obtained as the ratio between the main reference voltage V_{ref} and a resistor R_x matched with the loop-filter input resistor R_i, in order to guarantee a unity $\Sigma\Delta$ modulator gain even in the presence of PVT variations. The voltage V_x is set to be equal to V_{ref} by the single stage opamp OA_b. Basically, OA_b and M_1 are forming a two-stage opamp in buffer configuration, where the input is V_{ref} and the output is V_x. Moreover, the gate voltage of M_1 is the bias voltage V_{bp} for the pMOS current generators in the DAC elements. The current I_{ref_p} is 6 times the current I_{unit}, thus allowing a good trade-off between power-consumption ad noise generated by M_1. In fact the width of M_1 is 6 times the width of the pMos generator, thus further decreasing its flicker noise, that is propagated at the output of all the DAC elements. The current I_{ref_p} is then mirrored by M_3 and M_4 with a unitary ratio, therefore I_{ref_n}=I_{ref_p}, while M_4 is generating the bias voltage V_{bn} for the nMOS current generators in the DAC elements. The cascade references V_{cn} and V_{cp} are derived from diode-connected

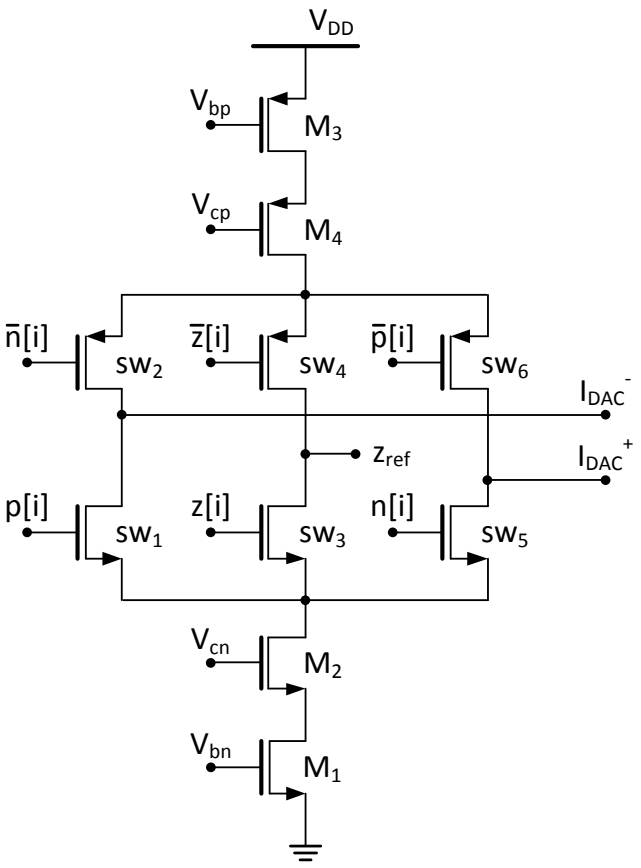

Figure 3.28: Circuit diagram of the single three-level DAC element

transistors biased with currents mirrored, respectively, from the nMOS branch and the pMOS branch, thus ensuring the start-up of the high compliance current mirror. The static current consumption of the complete DAC is 70 μA.

3.4.3 Feedback DAC Noise Analysis

The main ΣΔ modulator feedback DAC is directly coupled at the virtual grounds of OA_1, therefore the noise at the output of the DAC has the same transfer function of OA_1 noise (3.11). For this reason, all the noise generated by the feedback DAC is referred at the input. The DAC three-level elements are injecting noise only when are connected at the virtual grounds, therefore the current noise contribution at the input of the ΣΔ modulator is proportional to the input signal amplitude. In this section will be analyzed the input referred noise of a single DAC element in a static configuration, i.e assuming that is constantly injecting noise in the

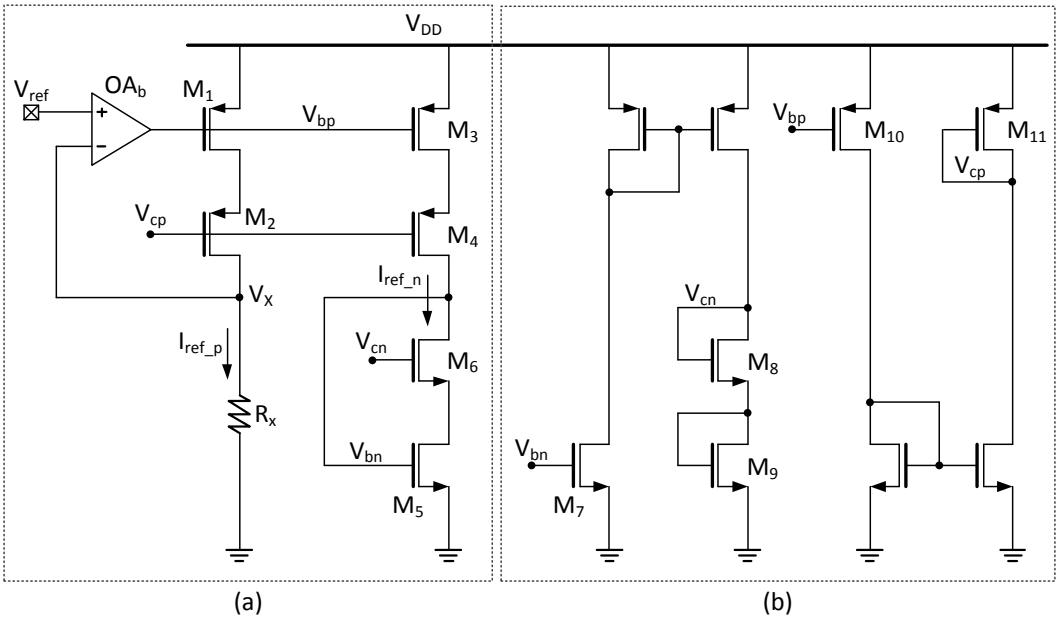

Figure 3.29: Circuit diagram for the bias generator for the current DAC: (a) Reference currents mirrored in DAC elements (b) Cascade voltage references generator

Table 3.7: Input referred noise of the DAC bias generator integrated from 20Hz to 20kHz

Component	Type	Noise Contribution [μV]
M_1	Thermal	1.72
M_5	Thermal	1.27
R_X	Thermal	1.12
M_5	Flicker	0.95
M_3	Thermal	0.85
M_1	Flicker	0.64
OA_b		0.45
	Total	**2.84**

virtual grounds. The differential input referred noise of the bias generator circuit, integrated in the range 20Hz-20kHz, is reported in Tab. 3.7, referring to Fig. 3.29. Notice that this noise is in common in all the DAC elements, thus when the input voltage is at full scale and 7 DAC elements are connected at the virtual grounds, the equivalent input referred noise is 7 times the total noise reported in Tab. 3.7.

The differential input referred noise of the single DAC element is reported in Tab. 3.8. The noise of each DAC element is independent and not correlated to the noise

Table 3.8: Input referred noise of the DAC element integrated from 20Hz to 20kHz

Component	Type	Noise Contribution [μV]
M_1	Thermal	2.62
M_3	Thermal	2.53
M_1	Flicker	1.94
M_3	Flicker	0.78
	Total	**4.2**

of other elements, therefore, when all the 7 DAC elements are connected at the virtual grounds, the input referred noise is $\sqrt{7}$ times the total noise reported in Tab. 3.8.

The total differential input referred noise when a single DAC element is connected is 5.07 μV, or rather -105.9-dBV$_{\mathrm{RMS}}$. Since the total differential input referred noise of the loop-filter is 6.02 μV, the differential input referred noise of the entire ΣΔ modulator should be 7.87 μV, i.e. -102.1-dBV. However, for low input level, such as -17 dB$_{\mathrm{FS}}$ or below, the single DAC element used is constantly switching from the +1/-1 state state to the 0 state (i.e. the state without noise injection), in function of both input signal and quantization noise. Therefore, to achieve a more realistic noise analysis, it is necessary to run transient noise simulation. Only in this way it is possible to evaluate the DR and the SNR of the entire ΣΔ modulator. The results are reported in the dedicated section.

3.4.4 Inter-Symbol Interference

In the actual implementation, if a DAC control bit interferes with subsequent bit can cause an unwanted injection of current in the virtual grounds of OA_1, and this leads to distortion at the output of the ΣΔ modulator. The technique proposed in [28] to remove the Inter-Symbol Interference (ISI) cannot be implemented in this case because the I-V conversion of the current steering DAC actually takes place in the CT single-opamp resonator. Therefore, to alleviate the problems related to ISI, a latch is placed in each control bit path, as shown in Fig. 3.30. The path becomes transparent during the time interval T following the falling edge of the sampling clock (f_S). In this way a fixed amount of delay is allocated in the feedback loop, as required for ELD compensation, introduced in the previous chapter. When the

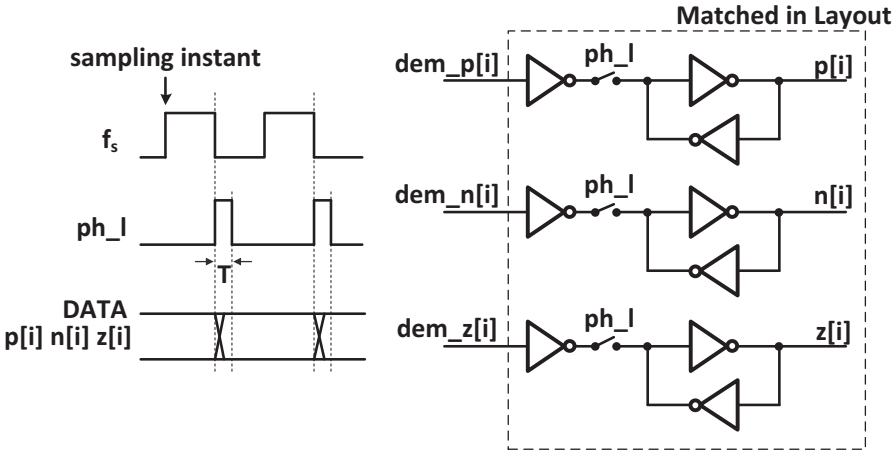

Figure 3.30: Propagation of the DAC control bits to minimize ISI effects

latches become transparent are driven by identical inverters to make the rising and the falling times of the control bits uniform. In the physical layout, the latches have been placed close to the corresponding DAC elements, carefully minimizing the mismatches among them and among the metal lines carrying the control bits to the switches of the DAC elements, therefore limiting the ISI impact. Moreover, the timing requirements of the combinational logic in front of the latches are relaxed, since almost half period of the sampling clock is available to set the output values, thus saving power.

3.5 Thermometer to Binary Decoder

The 14-digit thermometer code generated by the comparators (i.e. the $\Sigma\Delta$ modulator output) must be converted through a decoder in normal 4-bit binary code, that is necessary to interface the modulator during measurements; a large number of output ports would increase the complexity of the measurement setup, therefore it is preferable using the lower possible number of outputs. The multiplexer-based decoder consists entirely of multiplexers, as illustrated in Fig. 3.31 for a 4bit case [30]. It requires less hardware and has a shorter critical path than a ones-counter decoder [31], [32]. In addition it gives bubble error suppression, although the suppression is slightly lower than for a ones-counter decoder [32]. Another advantage of the multiplexer-based decoder is the more regular structure than, e.g., the ones-counter decoder. This is a major benefit in the layout of the circuit. The multiplexers used in this work are based on transmission gates. An inverter is used

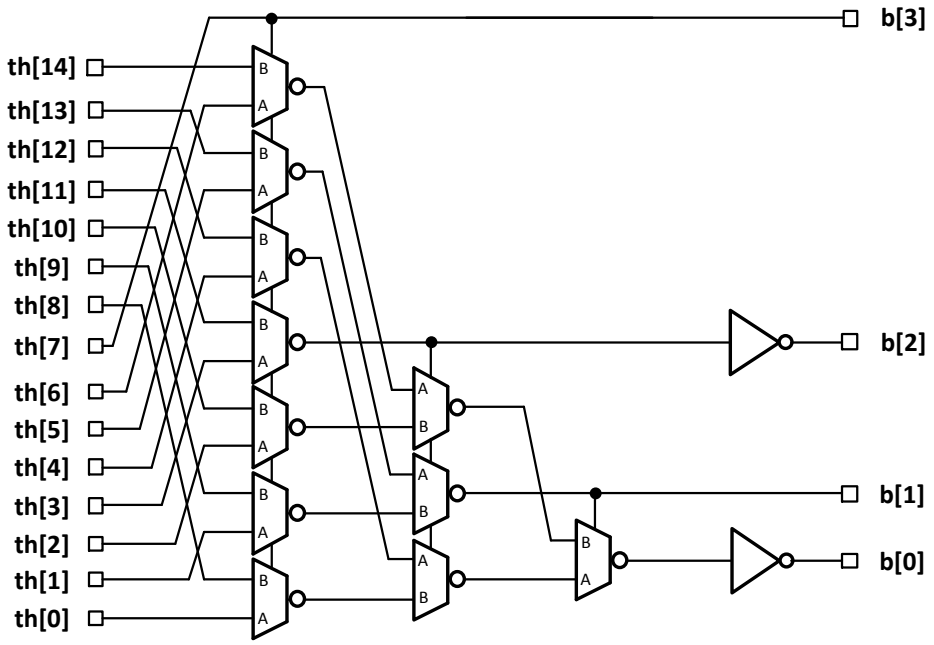

Figure 3.31: Multiplexer-based 4 bit decoder

as a buffer in each transmission gate multiplexer. Since the comparators are only 14, the bit $th[14]$ is connected to ground.

3.6 Transient noise simulation

As already mentioned, for the evaluation of the noise performance in the proposed CT-ΣΔ modulator it is necessary rely on transient noise simulations. Only in this way the expected performances of the modulator can be evaluated, since the current-steering DAC for small input signal does not have a constant noise contribution. The simulated output SNDR versus input amplitude is shown in Fig. 3.32. For input signal lower than -17 $\mathrm{dB_{FS}}$, the feedback DAC minimizes the noise contribution and the CT-ΣΔM *DR* is mainly limited by the opamp and resistor thermal noise, while for larger input signal more DAC elements are injecting noise, thus the peak SNDR is limited by the feedback DAC. The simulated DR is 102.9 dB, while the peak SNDR at -1 $\mathrm{dB_{FS}}$ is 94.8 dB.

In the field of audio converters, the values of DR and SNDR are generally reported A-weighted in order to match the behavior of human hearing [33]. Basically, the

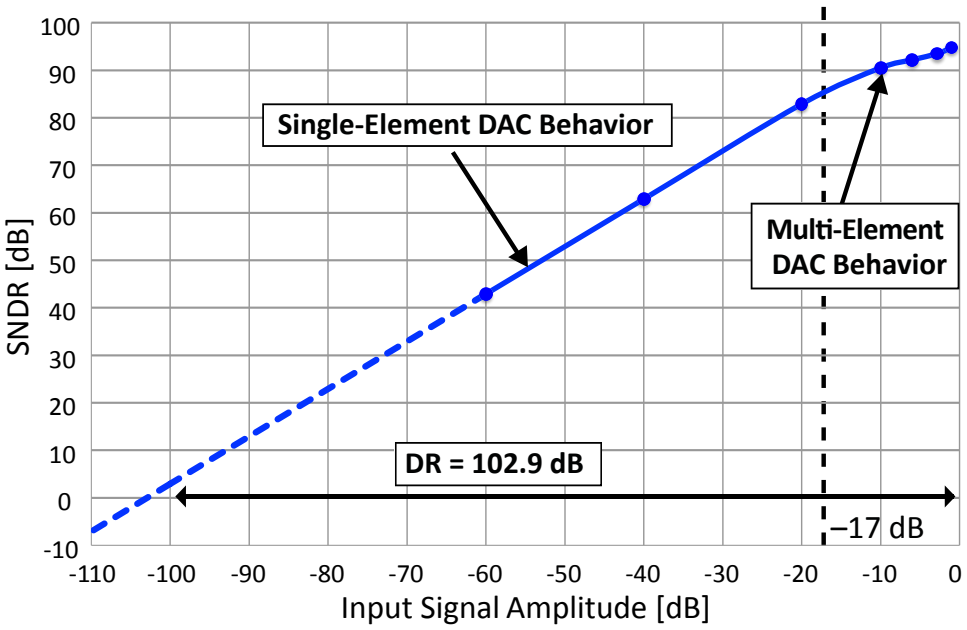

Figure 3.32: Measured *SNDR* as a function of the input signal amplitude

frequencies below 1 kHz and above 10 kHz are attenuated by the human hearing, therefore the perception of noise is lower in such frequencies, increasing the real SNDR for input signal frequencies in optimal audible range (i.e. from 1 kHz to 10 kHz). The SNDR A-weighted vs input amplitude is shown in Fig. 3.33. Since the the *DR* is 106.1 dB_A (A-weighted) and the SNDR at -1 dB_{FS} is 97.7 dB_A, the expected performances are well above the assigned targets.

3.7 Layout

The complete layout of the proposed CT-ΣΔ modulator, including all the digital parts, is shown in Fig. 3.34. It has been done using a 0.16 μm CMOS technology with MIM capacitors. The fully-digital cells (i.e. the phase generator, the digital delay for ELD compensation, the DEM and the thermometer-to-binary decoder) have dedicated deep-nwells and a dedicated power supply line, in order to avoid possible interferences coming from the switching activities of the digital ports. The rest of the ΣΔ modulator has a common deep-nwell and a dedicated analog power supply. The loop filter has been placed in the middle of the layout, with the second integrator opamp close to the ADC and the resonator opamp close to the RC cross-coupled feedback network. Notice that, in both resonator and integrator, the capacitors have been placed above the resistors to save area. The ADC is

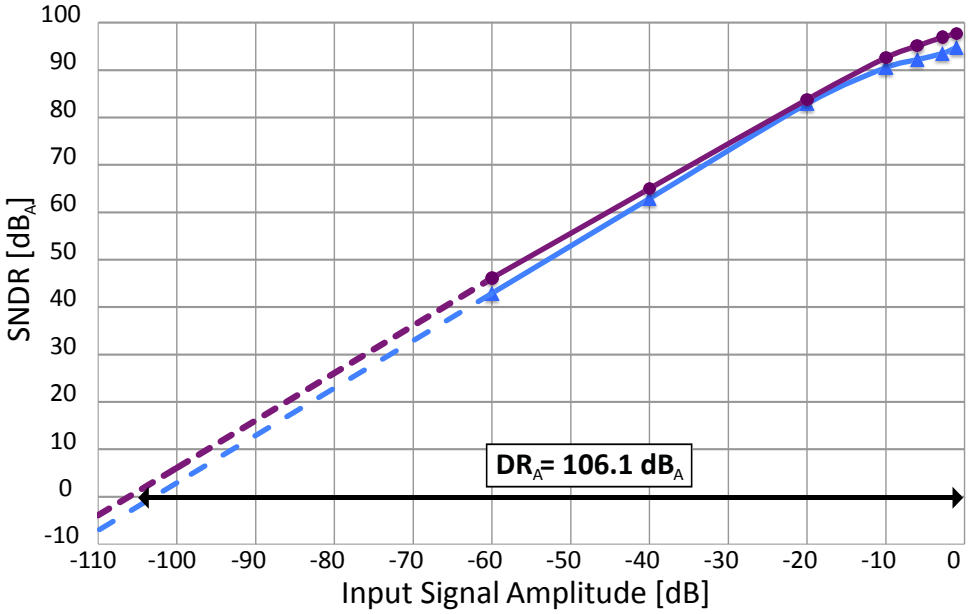

Figure 3.33: Measured *SNDR* A-weighted as a function of the input signal amplitude

formed by the replica of 14 identical comparator cells. In order to save area, the interconnections inside each comparators have been made with only 3 layers of metal, thus allowing top level interconnection lines in metal 4 above the comparator cells. The 14 thermometer output digits of the ADC are directly connected to the DEM cel and the thermometer-to-binary decoder that are allocaded at the top of Fig. 3.34. The ADC feeds also the digital delay for ELD compensation, that is directly connected to the adjacent SC-DAC. This local DAC is formed by 14 identical 2-level SC-DAC elements. The main feedback DAC has been placed between its DEM and the loop-filter.

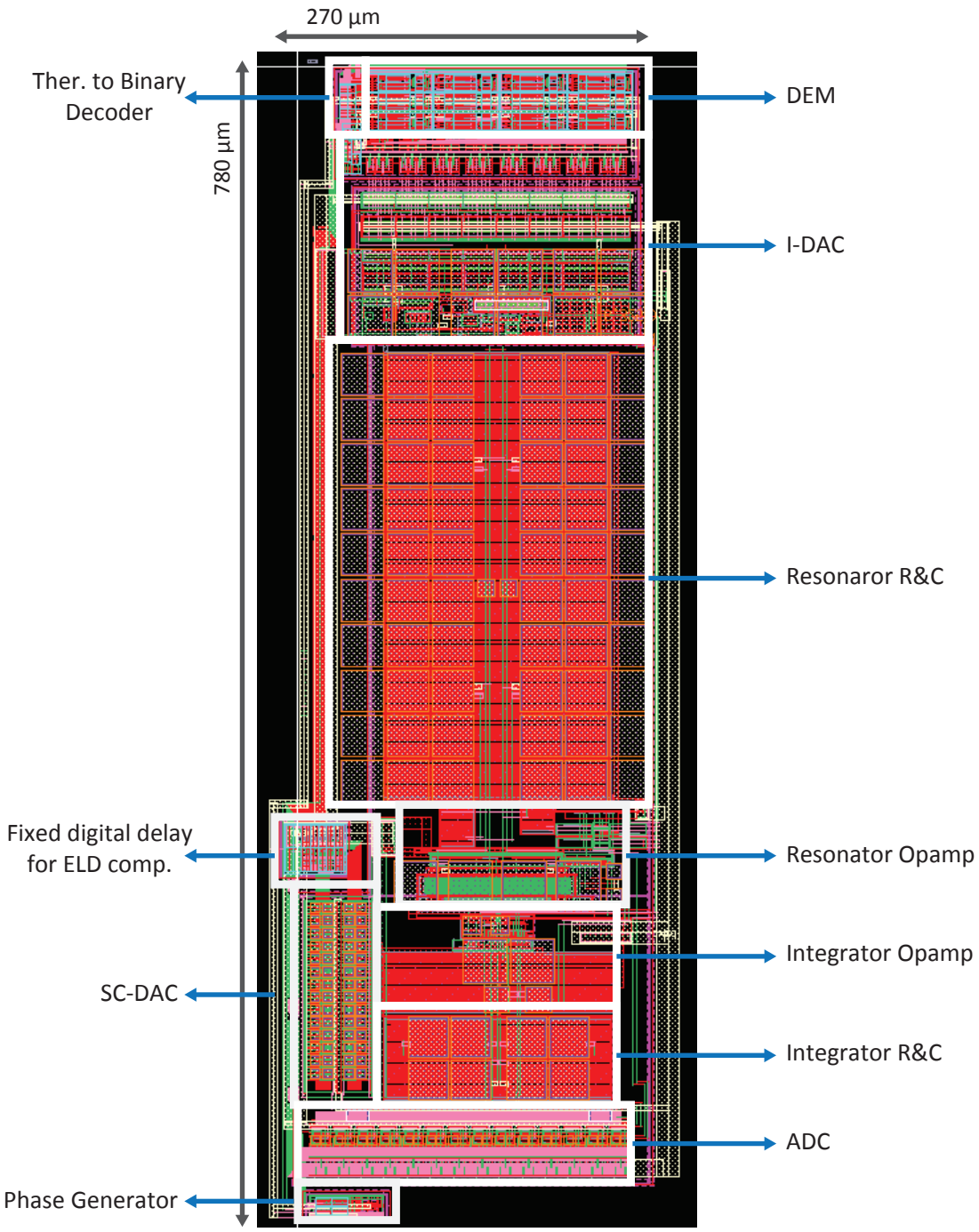

Figure 3.34: Complete CT-ΣΔ modulator layout

Chapter 4

Experimental Results

In this last chapter the experimental results achieved during the characterization of the proposed CT-ΣΔ modulator will be reported. The first section is about the fabrication of the test-chip, as well its measuring setup. The second section is reporting the measured results and the last section is about the comparison with the state-of-the-art.

4.1 Test-chip and Measuring Setup

The proposed CT-ΣΔ modulator has been fabricated using a 0.16 μ modulator CMOS technology with MIM capacitors. The micrograph of the 0.21-mm^2 chip is illustrated in Fig. 4.1.

The test chip has been characterized with the setup shown in Fig. 4.2. The differential input is provided by an Audio Precision signal source. The 3MHz clock

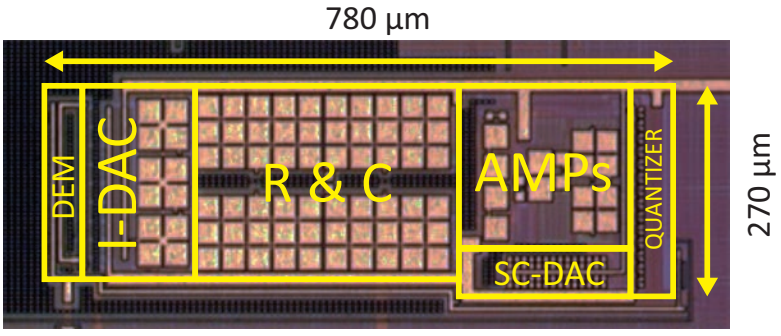

Figure 4.1: Chip micrograph

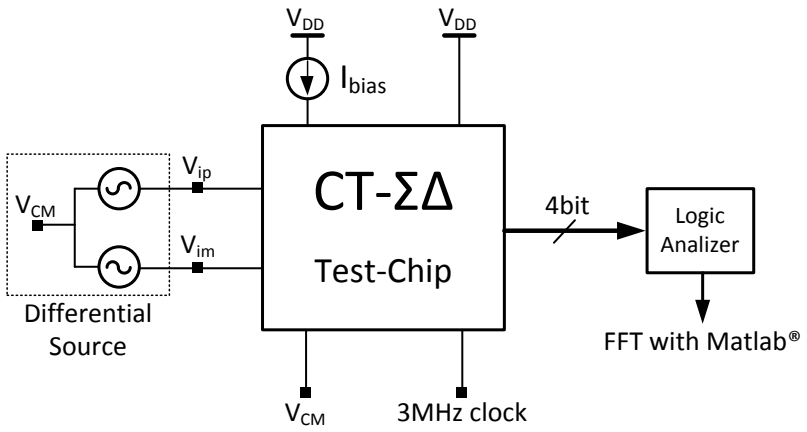

Figure 4.2: Measuring Setup

is obtained with a function generator. The samples from the modulator output were captured using a logic analyzer synchronized with the falling edge of the clock. The bias current is obtained with a simple resistor, with a dedicated large capacitor to filter its thermal noise. The common mode *agnd* of the test-chip can be adjust independently from V_{DD}, although a value of $V_{DD}/2$ is optimal. Additional control bits, not shown in Fig. 4.2, can be used to activate the internal DEM, as well to use an external DEM.

The evaluation board is shown in Fig. 4.3. This board has been designed in Conexant Systems with the purpose of testing all the IPs developed by the Analog and Mixed Signal group, such DACs, head-phone amplifiers, class-D amplifiers, pre-amplifiers, ADCs, and so on.

4.2 Measured Results

Fig. 4.4 shows the measured *SNDR* as a function of the input sinusoidal signal amplitude at 1 kHz. The full-scale input signal (0 dB_{FS}) corresponds to 2.8 V_{pp} differential. The achieved *DR* is 106.7 dB_A (A-weighted), corresponding to an *ENOB* $>$ 17 bits, whereas the peak *SNDR* is 93.2 dB_A. The change of slope in the SNDR curve for input signal amplitudes larger than -17 dB_{FS} is due to

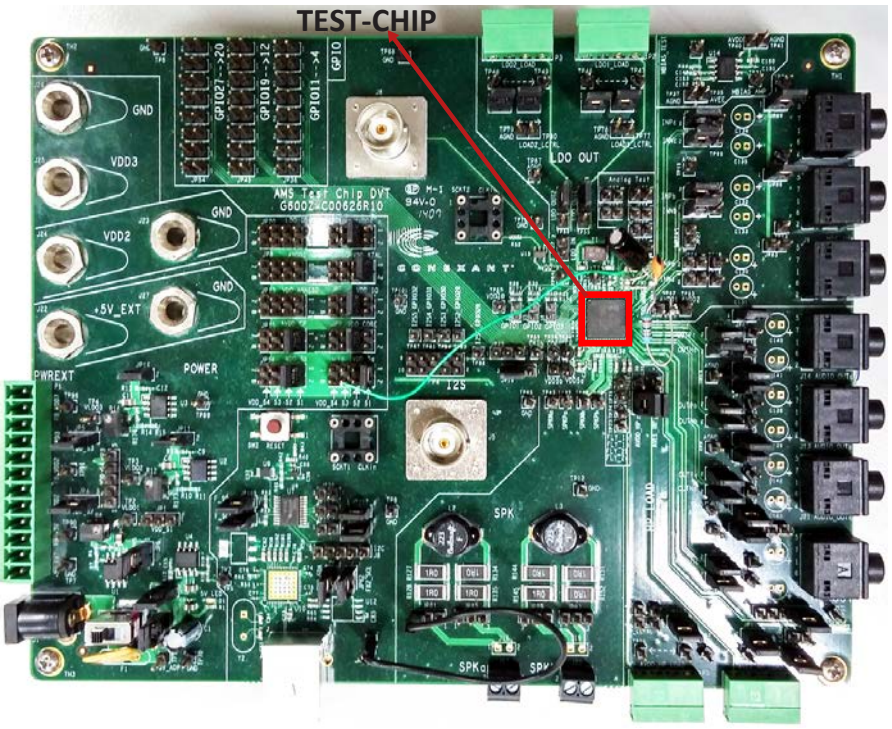

Figure 4.3: Test board for Conexant IPs

the increased current-steering DAC noise when more than one three-level current-steering element cell is used (acceptable for the microphone application, where linearity is limited by the microphone itself).

The CT-ΣΔ modulator output spectra obtained with -60-dB$_{\mathrm{FS}}$ and -1-dB$_{\mathrm{FS}}$, 1-kHz input signals are shown in Fig. 4.5. As expected, at -1 dB$_{\mathrm{FS}}$ the noise floor increases of about 13 dB with respect to -60 dB$_{\mathrm{FS}}$, due to the increased DAC noise.

Fig. 4.6 shows the measured inherent antialiasing properties of the CT-ΣΔ modulator. The spectral components around f_S are aliased back to the audio band attenuated more than 70 dB.

The analog section of the 3rd-order ΣΔ modulator consumes 350 μW, while the digital blocks (i. e. DEM, and thermometer-to-binary converter) consume 40 μW, both from a 1.6-V power supply and during conversion.

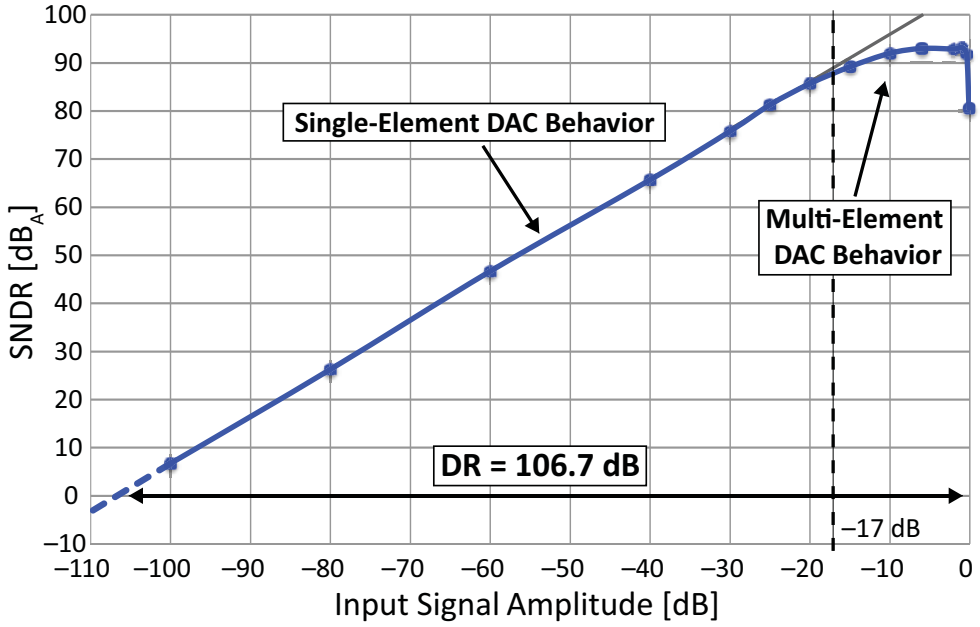

Figure 4.4: Measured *SNDR* as a function of the input signal amplitude

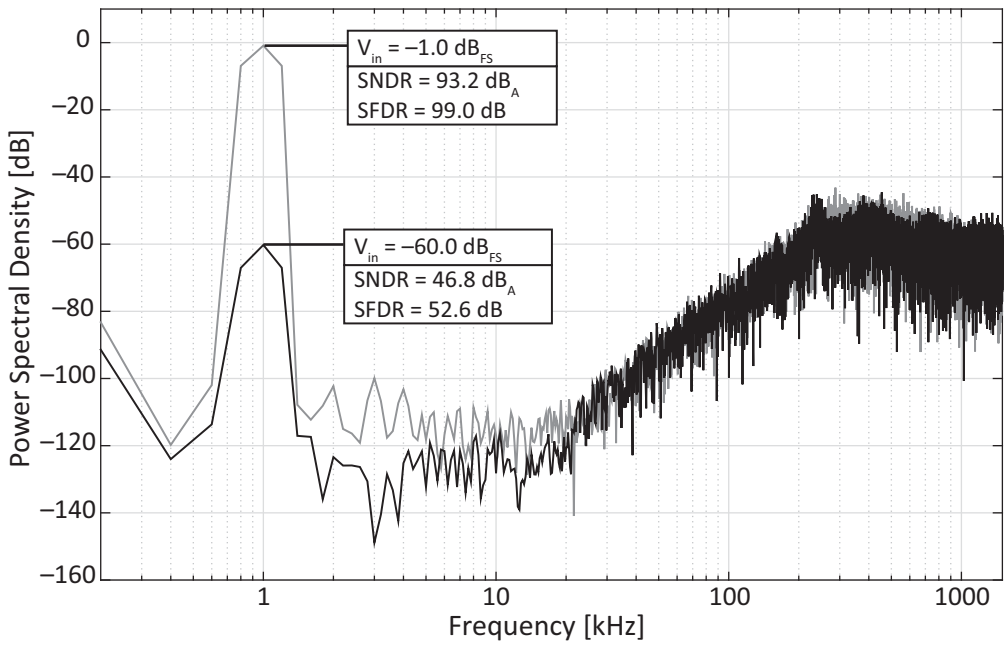

Figure 4.5: Measured output spectra of the proposed CT-ΣΔ modulator with -60-dB$_{\mathrm{FS}}$ and -1-dB$_{\mathrm{FS}}$, 1-kHz input signals

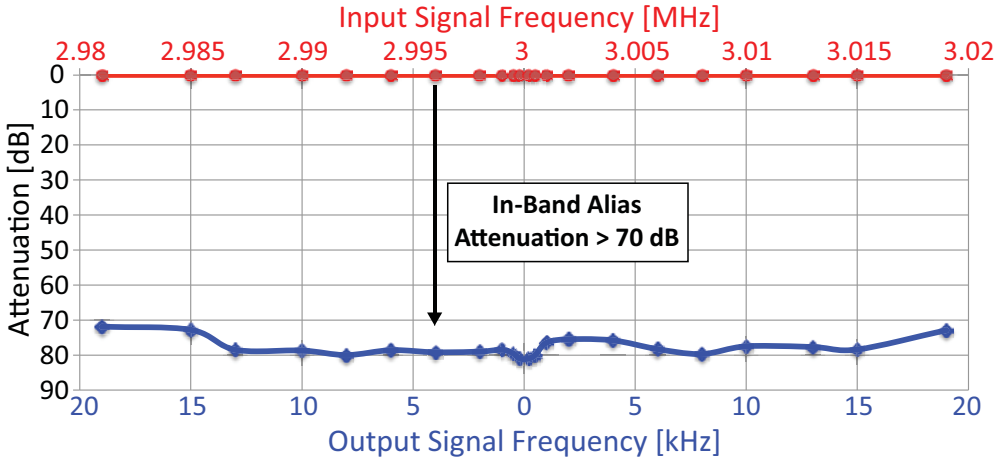

Figure 4.6: Measured antialiasing properties for 0-dB$_{\mathrm{FS}}$ input signals around f_S

4.3 Comparison With the State-Of-the-Art

The achieved Schreier Figure-of-Merit, defined as $FoM_S = DR + 10\log(B/P)$ (B being the bandwidth and P the power consumption), is 184 dB, the largest reported for audio $\Sigma\Delta$ modulator with $DR > 100$ dB. Tab. 4.1 shows the achieved performance summary, as well as a comparison among audio $\Sigma\Delta$ modulators with $DR > 100$ dB. They are designed in different technologies with varying supply voltages which makes a true comparison difficult, nonetheless the FOM can be used to evaluate power efficiency. Fig. 4.7 shows a comparison with the state-of-the-art from [1].

Table 4.1: Performance summary and comparison with the state-of-the-art of high-DR audio $\Sigma\Delta$ modulators

Parameter	**This Work**	**[34]**	**[29]**	**[35]**	**[36]**	**[37]**	**[38]**	**[3]**	**[39]**	**[40]**
Technology [nm]	160	180	40	180	180	350	130	350	65	180
Architecture	CT	CT	CT/SC	SC	SC	SC	SC	CT/SC	CT/SC	CT/SC
Supply Voltage [V]	1.6	1.8	2.5/1.2	0.7	5.0/1.8	5.0/1.8	3.3	3.3	3.3	3.3
Power Consumption (P) [**mW**]	0.39	0.28	0.50	0.87	1.10	68.00	9.90	18.00	15.00	37.00
Bandwidth (B) [**kHz**]	20	24	24	25	20	20	20	20	20	20
Oversampling Ratio (OSR)	75	128	135	100	64	153.6	128	128	256	128
Area [mm^2]	0.21	0.24	0.05	2.16	0.38	5.62	0.49	0.82	0.28	0.65
Dynamic Range (DR) [**dB**]	106.7	103	102	100	101.3	114	105	106	101	102
Peak $SNDR$ [**dB**]	93.2	98.2	90	95	99.3	105	97.5	99	85	95
FoM_S [**dB**]	184	182	179	175	174	169	168	166	162	159

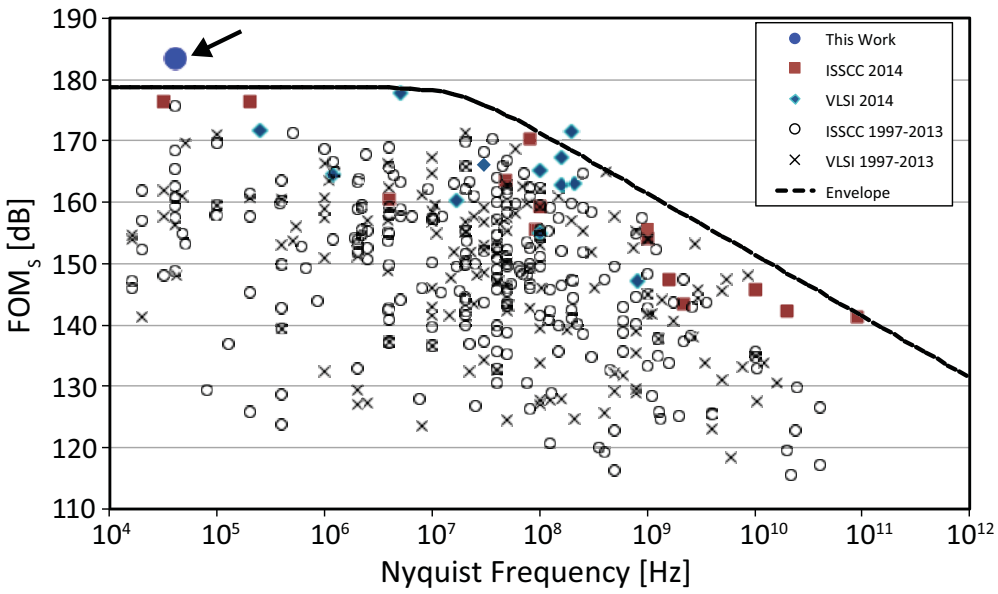

Figure 4.7: Comparison with the state-of-the-art based on FoM_S from [1]

Chapter 5

Conclusions

In this thesis, an audio CT-ΣΔM for MEMS microphones has been presented. The CT-ΣΔM 3rd-order loop filter is realized with the use of only two opamps. This solution is an alternative to a traditional loop filter that requires four opamp to be implemented. The proposed loop filter optimizes the power consumption, allocating part of the power obtained by the removal of the unnecessary opamps to the first opamp, thus lowering its thermal noise and increasing the DR. Moreover, the feedback DAC, realized with three-level current-steering elements, minimizes the noise at low input signals, thus reducing its impact on DR. The proposed CT-ΣΔM achieves a $DR = 106.7$ dB$_{\text{A}}$ with a power consumption as low as 390 μW, leading to the highest reported $FoM_S = 184$ dB. The inherent antialiasing properties and the relatively high input impedance of the CT-ΣΔM (47 kΩ) allow the simplification of the microphone front-end circuit, saving power and area in the overall system.

Bibliography

[1] B. Murmann, "ADC performance survey 1997-2014." [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html

[2] Y. Yang, A. Chokhawala, M. Alexander, J. Melanson, and D. Hester, "A 114-dB 68-mW chopper-stabilized stereo multibit audio ADC in 5.62 mm^2," vol. 38, no. 12, pp. 2061–2068, Dec. 2003.

[3] K. Nguyen, B. Adams, K. Sweetland, H. Chen, and K. McLaughlin, "A 106-dB SNR hybrid oversampling ADC for digital audio," Feb. 2005, pp. 176–591.

[4] S. Norsworthy, R. Schreier, and G. Temes, *Delta-Sigma data converters: theory, design, and simulation.* IEEE Press, 1997.

[5] S. Lindfors, M. Lansirinne, T. Lindeman, and K. Halonen, "On the design of 2nd order multi-bit delta-sigma modulators," in *Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on*, vol. 2, Jul 1999, pp. 13–16 vol.2.

[6] M. Sarhang-Nejad and G. Temes, "A high-resolution multibit sigma-delta adc with digital correction and relaxed amplifier requirements," *Solid-State Circuits, IEEE Journal of*, vol. 28, no. 6, pp. 648–660, Jun 1993.

[7] B. Leung and S. Sutarja, "Multibit sigma-delta a/d converter incorporating a novel class of dynamic element matching techniques," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 39, no. 1, pp. 35–51, Jan 1992.

[8] P. Malcovati, S. Brigati, F. Francesconi, F. Maloberti, P. Cusinato, and A. Baschirotto, "Behavioral modeling of switched-capacitor sigma-delta modulators," vol. 50, no. 3, pp. 352–364, Mar. 2003.

[9] P. Malcovati. SDToolbox 2. [Online]. Available: http://www.mathworks.it/matlabcentral/fileexchange/25811-sdtoolbox-2

[10] R. Schreier. Toolbox documentation. [Online]. Available: http://www.mathworks.com/matlabcentral/fileexchange/19

[11] J. Candy, "A use of double integration in sigma delta modulation," *Communications, IEEE Transactions on*, vol. 33, no. 3, pp. 249–258, Mar 1985.

[12] A. Thurston, T. Pearce, and M. Hawksford, "Bandpass implementation of the sigma-delta a-d conversion technique," in *Analogue to Digital and Digital to Analogue Conversion, 1991., International Conference on*, Sep 1991, pp. 81–86.

[13] O. Shoaei and W. Snelgrove, "Optimal (bandpass) continuous-time sigma-delta modulator," in *Circuits and Systems, 1994. ISCAS '94., 1994 IEEE International Symposium on*, vol. 5, May 1994, pp. 489–492 vol.5.

[14] R. Schreier and B. Zhang, "Delta-sigma modulators employing continuous-time circuitry," *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on*, vol. 43, no. 4, pp. 324–332, Apr 1996.

[15] J. A. Cherry, "Clock jitter and quantizer metastability in continuous-time delta-sigma modulators," vol. 46, no. 6, pp. 661–676, Jun. 1999.

[16] R. H. M. van Veldhoven and A. H. M. van Roermund, *Robust sigma-delta converters*. Springer, 2011.

[17] A. Bar-Guy. Phase noise. [Online]. Available: http://www.mathworks.it/matlabcentral/fileexchange/8844-phase-noise

[18] C. De Berti, P. Malcovati, L. Crespi, and A. Baschirotto, "A low-power, continuous-time sigma-delta modulator for MEMS microphones," Jun. 2013, pp. 53–56.

[19] S. Pavan, N. Krishnapura, R. Pandarinathan, and P. Sankar, "A power optimized continuous-time $\Delta\Sigma$ ADC for audio applications," vol. 43, no. 2, pp. 351–360, Feb. 2008.

[20] H. Chae, J. Jeong, G. Manganaro, and M. Flynn, "A 12mw low-power continuous-time bandpass $\Delta\Sigma$ modulator with 58db sndr and 24mhz bandwidth at 200mhz if," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*, Feb 2012, pp. 148–150.

[21] S. Zeller, C. Muenker, and R. Weigel, "A X-coupled differential single-opamp resonator for low power continuous time ΣΔ-ADCs," Jul. 2011, pp. 233–236.

[22] S. Pavan, "Excess loop delay compensation in continuous-time delta-sigma modulators," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 55, no. 11, pp. 1119–1123, Nov 2008.

[23] K. Matsukawa, Y. Mitani, M. Takayama, K. Obata, S. Dosho, and A. Matsuzawa, "A fifth-order continuous-time delta-sigma modulator with single-opamp resonator," *Solid-State Circuits, IEEE Journal of*, vol. 45, no. 4, pp. 697–706, April 2010.

[24] K. Matsukawa, Y. Mitani, M. Takayama, K. Obata, Y. Tokunaga, S. Sakiyama, and S. Dosho, "A 69.8 db sndr 3rd-order continuous time delta-sigma modulator with an ultimate low power tuning system for a worldwide digital tv-receiver," in *Custom Integrated Circuits Conference (CICC), 2010 IEEE*, Sept 2010, pp. 1–4.

[25] X. Jiang, J. Song, J. Chen, V. Chandrasekar, S. Galal, F. Y. L. Cheung, D. Cheung, and T. L. Brooks, "A low-power, high-fidelity stereo audio codec in 0.13-μm CMOS," vol. 47, no. 5, pp. 1221–1231, May 2012.

[26] J. Paulos, "Improved signal-to-noise ratio using tri-level delta-sigma modulation," in *IEEE ISCAS Digest of Technical Papers.*, Feb 1987, pp. 463–466.

[27] C. Thompson and S. Bernadas, "A digitally-corrected 20b delta-sigma modulator," in *Solid-State Circuits Conference, 1994. Digest of Technical Papers. 41st ISSCC., 1994 IEEE International*, Feb 1994, pp. 194–195.

[28] K. Nguyen, A. Bandyopadhyay, B. Adams, K. Sweetland, and P. Baginski, "A 108-dB SNR, 1.1-mW oversampling audio DAC with a three-level DEM technique," vol. 43, no. 12, pp. 2592–2600, Dec. 2008.

[29] T.-Y. Lo, "A 102-dB dynamic range audio sigma-delta modulator in 40-nm CMOS," Nov. 2011, pp. 257–260.

[30] E. Sail and M. Vesterbacka, "Thermometer-to-binary decoders for flash analog-to-digital converters," in *Circuit Theory and Design, 2007. ECCTD 2007. 18th European Conference on*, Aug 2007, pp. 240–243.

[31] F. Kaess, R. Kanan, B. Hochet, and M. Declercq, "New encoding scheme for high-speed flash adc's," in *Circuits and Systems, 1997. ISCAS '97., Proceedings of 1997 IEEE International Symposium on*, vol. 1, Jun 1997, pp. 5–8 vol.1.

[32] E. Sail and M. Vesterbacka, "A multiplexer based decoder for flash analog-to-digital converters," in *TENCON 2004. 2004 IEEE Region 10 Conference*, vol. D, Nov 2004, pp. 250–253 Vol. 4.

[33] D. Self, *Audio Power Amplifier Design Handbook*. Focal Press/Elsevier, 2009.

[34] A. Sukumaran and S. Pavan, "A 280-μW audio continuous-time ΔΣ modulator with 103-dB DR and 102-dB A-weighted SNR," Nov. 2013, pp. 385–388.

[35] H. Park, K. Y. Nam, D. K. Su, K. Vleugels, and B. A. Wooley, "A 0.7-V 870-μW digital-audio CMOS sigma-delta modulator," vol. 44, no. 4, pp. 1078–1088, Apr. 2009.

[36] T. Wang, W. Li, H. Yoshizawa, M. Aslan, and G. C. Temes, "A 101-dB DR 1.1-mW audio delta-sigma modulator with direct-charge-transfer adder and noise shaping enhancement," Nov. 2012, pp. 249–252.

[37] Y. Q. Yang, A. Chokhawala, M. Alexander, J. Melanson, and D. Hester, "A 114-dB 68-mW chopper-stabilized stereo multibit audio ADC in 5.62 mm^2," vol. 38, no. 12, pp. 2061–2068, Dec. 2003.

[38] Y.-G. Kim, M.-H. Cho, K.-D. Kim, J.-K. Kwon, and J.-D. Kim, "A 105.5-dB, 0.49-mm^2 audio ΣΔ modulator using chopper stabilization and fully randomized DWA," Sep. 2008, pp. 503–506.

[39] M.-Y. Choi, S.-N. Lee, S.-B. You, W.-S. Yeum, H.-J. Park, J.-W. Kim, and H.-S. Lee, "A 101-dB SNR hybrid ΔΣ audio ADC using post-integration time control," Sep. 2008, pp. 89–92.

[40] P. Morrow, M. Chamarro, C. Lyden, P. Ventura, A. Abo, A. Matamura, M. Keane, R. O'Brien, P. Minogue, J. Mansson, N. McGuinness, M. McGranaghan, and I. Ryan, "A 0.18-μm 102-dB-SNR mixed CT SC audio-band ΔΣ ADC," Feb. 2005, pp. 178–179.