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DOTTORATO DI RICERCA IN MICROELETTRONICA
XXVIII CICLO

HIGH DENSITY MICROELECTRONIC SYSTEMS FOR AN INTELLIGENT READOUT OF SEMICONDUCTOR PIXEL SENSORS

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Introduction

The demanding requirements set by the consumer electronics industry are leveraging the relentless advances in microelectronic technologies. Such improvements are also inspiring the photon science community, currently committed to the development of high performance systems for next generation X-ray Free Electron Lasers. X-ray Free Electron Lasers are considered among the most powerful probing tools for investigating the complex structure of organic and inorganic materials and the natural phenomena taking place at the nanometer scale. The unprecedented features of these facilities, capable of producing photon pulses with outstanding brightness and ultra-short duration, promise to revolutionize a number of research fields, including structural biology, chemistry, material science and nuclear and molecular physics. The experiments taking place at such facilities set very severe requirements on each building block of the overall system, including the detector and the readout electronics. The detector must feature a small pixel pitch, of the orders of tens of μm, and a quite large sensing area. The electronic instrumentation must be able to cope with an input dynamic range of up to 120 dB. At the same time, single photon resolution for small input signals is needed. This results in a challenging requirement in terms of Signal-to-Noise ratio, compelling the designers to embed in a single pixel a very large amount of intelligence and signal processing blocks. The readout of the full detector must occur at very high speed, approaching the 5 Mfps. Finally, both the detector and the readout electronics must be able to withstand extreme radiation environments, with a total ionizing dose ranging from 10 MGy up to 1 GGy. To fulfil such requirements, the photon science and the High Energy Physics (HEP) communities have started to explore the 65 nm technology node and are adopting cutting-edge microelectronic fabrication technologies. Active edge pixel sensors represent an interesting solution to minimize the dead area of the detector. The 3D approach of layering tiers of active circuitry, besides increasing the overall circuit density, reduces the overall length of the device interconnections, increases the speed and reduces the power consumption.

This thesis work discusses the design and the characterization of microelectronic systems potentially advancing the state-of-the-art in electronic instrumentation for X-ray Free Electron Lasers applications. The first chapter begins with a brief description about the main requirements set by the experiments conducted at such facilities, and then will go through an overview about the state-of-the-art in electronic instrumentation developed by the main research collaborations active in the photon science community. The second chapter will be devoted to the design and the characterization of in-pixel circuitry to be used for the calibration of detector front-end electronics. The activity has been carried out in the framework of an international collaboration developing a new detector system for a facility under construction in Hamburg, Germany. After a brief overview about the detector system under development, the characterization activity carried out on a prototype chip of the Application Specific Integrated Circuit reading out the sensor will be described. Then, the optimization of an injection circuit for pixel-level calibration, conducted on the basis of the measurement results, will be presented. The third chapter will describe the design and the characterization of an analog front-end for X-ray pixel imagers, devised in the framework of a national collaboration aiming to substantially advance the state-of-the-art in the field of 2D X-ray imaging by exploring cutting-edge solutions in fabrication technologies and detector readout architectures. After introducing a novel signal compression principle enabling to fit a wide input dynamic range of a readout channel into a reasonable output swing, the design of the building blocks of the analog front-end will be debated. Then, the preliminary results, achieved from the first prototype chips of the readout channel, will be presented.

Chapter 1

X-ray Free Electron Lasers

1.1 Main features of FELs

Investigating the extremely small, the extraordinarily fast phenomena taking place at the nanometer scale and the complex structure of organic and inorganic materials is one of the main trends of modern scientific and technological research. Nanotechnologies are based on the ability to perform measurements and manipulate objects at a molecular scale. At such dimensions, the time scale of the dynamic processes is defined by the femtosecond vibration of an atom in a chemical bond. Understanding of the states of matter and its organization is of crucial importance for the development of advanced materials with innovative functionalities. Free Electron Lasers (FEL) are bound to become the predominant tool for investigating natural phenomena in this research framework. Figure 1.1 depicts the principle of free electron lasers. A beam of relativistic electrons is made to wiggle through an undulator (a periodic magnet array) eventually producing a coherent and collimated X-ray beam. Self-amplified spontaneous emission (SASE) is used to start the light amplification process. The minimum wavelength, of the order of one Angstrom, and the intensity of the laser beam made available in FEL systems, make it possible to see objects with nanometer feature size. Laser flash duration, from some tens to some hundreds of femtoseconds, is short enough that the influence of the laser pulse itself on the time evolution of the investigated phenomena can be considered negligible. A number of research centers, in Europe, United States and Japan, have started studying, designing and building free electron laser facilities. A broad set of research programs is being outlined. Some of these facilities, like the SLAC Linear Coherent Light Source (LCLS), in Stanford, or the SPring-8 Compact SASE Source (SCSS), in Japan, are already

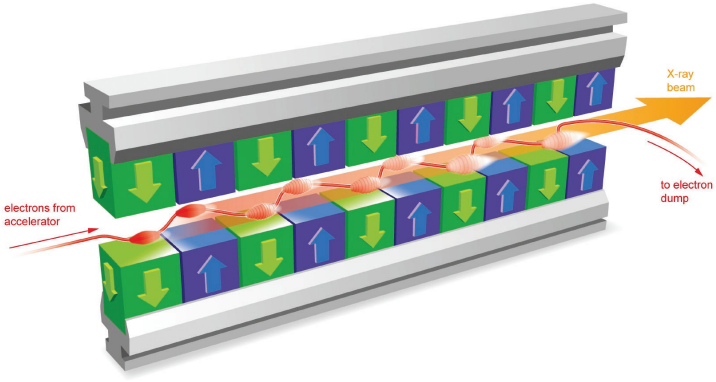

Figure 1.1: the principle of a free-electron laser. Electrons are first brought to high energies in a superconducting accelerator. They then fly on a slalom course through a special arrangement of magnets (the "undulator"), in which they emit laserlike flashes of radiation.

operational. Other facilities, for example the European XFEL, are currently under construction or, like in the case of the SwissFEL, the upgrade program of LCLS (LCLS2) , or Iride, are finalizing their proposed design.

The science base accessible at FELs is quite broad. A non exhausting list of research fields includes:

- **structural biology**: aims at studying and solving the structures of large macromolecular biological systems;
- **chemistry**: one of the goals here is to understand the mechanisms of catalytic processes responsible for efficient conversion of light into electrical/chemical energy;
- **material science**: experiments at FELs in this field are expected to shed light on the mechanisms of transport and storage of information on increasingly smaller lengths and at faster time scales;
- **atomic and molecular science**: is concerned with the study of fundamental interactions among electrons, between electrons and nuclei and between light and matter.

Most of the measurements performed at FEL experiments are based on the scattering of coherent X-rays and the detection of the coherent diffraction

pattern. More details about the experiments and measurement techniques deployed at FELs can be found in conceptual and technical design reports and publications [1–3]. In general, FEL facilities have several beam lines differing in photon energy range. Also, the different beam lines make it possible to address different types of experiments. FEL operation may change significantly from one facility to the other. As an example, Figure 1.2 shows the stucture of the X-ray pulses foreseen at the European XFEL, generated with a repetition rate of 4.5 MHz and with a time interval of about 100 ms between two subsequent bursts, each one composed of a train of 3000 X-ray pulses with a temporal distance of 200 ns. While the European XFEL is operated in a burst mode, the LCLS facility in Stanford, on the other hand, is operated at a constant pulse rate of 120 Hz. The main features of a few FEL facilities already built or under construction are summarized in Table 1.1.

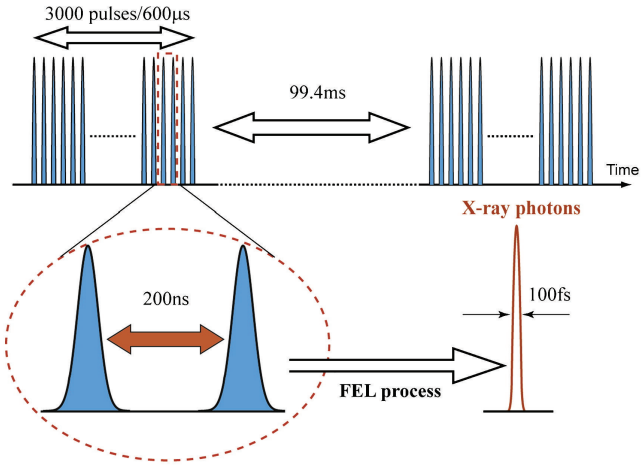

Figure 1.2: X-ray bunch structure at the European XFEL [4].

1.2 Specifications for FEL imagers

Electronic instrumentation to be used for coherent diffration pattern imaging at FEL facilities mainly consists of two-dimensional pixelated X-ray imagers, as depicted in the conceptual sketch of an X-ray FEL camera in Figure 1.3. Since conventional X-ray cameras are designed to obtain images from a continuous beam of X-rays and cannot operate with such intense microburst and beam pulses as the ones occurring at FEL facilities, specific electronic imagers able to cope with the X-ray beam properties (which may vary from one

Project	Start of operation	Beam energy [GeV]	Min. photon wavelength [Å]	Max. photon energy [keV]	Burst rate [Hz]	Number of X-ray pulses
LCLS	2009	13.6	1.5	8.3	120	1
SCSS	2010	8	1	12	60	1
Fermi	2010	2.4	40	0.32	10	1
Eu-XFEL	2014	17.5	1	12	10	2700@220 ns
SwissFEL	2016	5.8	1	12	100	2@50 ns
NGLS	>2020	2.4	10	1.2	10^6	1

Table 1.1: main features of some existing and future FEL facilities.

facility to the other, or from one beam line to the other within the same facility) and the experiment specifications need to be developed. All the FEL characteristics and operation modes listed in Table 1.1 have an impact on the instrumentation design choices, and lead to a specific design for each particular beam line at each particular FEL facility. Among the specifications setting the bounds for X-ray FEL instrumentation, the most challenging ones prescribe a detector able to image scattered X-rays on a per-shot basis with sufficiently

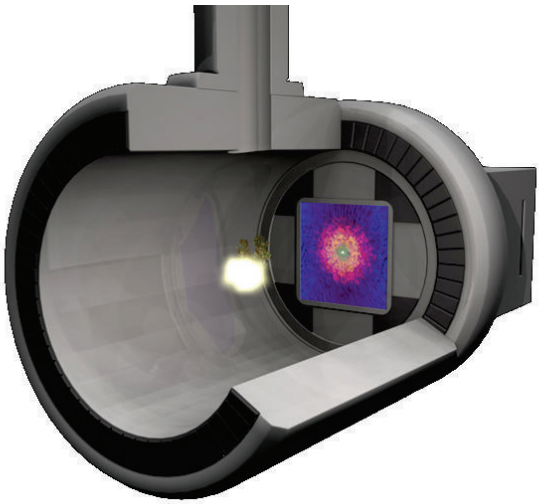

Figure 1.3: conceptual view of a camera system for X-ray FEL applications.

high efficiency, with an excellent spatial resolution over a large solid angle and providing both single photon resolution and a large input dynamic range.

In this section, the main specifications leading to the design and the development of a specific detector to be used at next generation FEL facilities are summarized.

1.2.1 Photon energy and input dynamic range

The photon energy and the input dynamic range are among the most challenging specifications for the design of an X-ray imager for FEL. Indeed, according to the characteristics of FEL facilities already built or under construction worlwide [1–3, 5], the input signal can range from 1 photon with an energy of 250 eV to 10000 photons with an energy of 90 keV (more than 130 dB of input dynamic range), meaning that a single detector or detector technology are not suitable for all applications. Hence, different systems need to be developed, each one optimized for a limited energy range, by taking into account the following considerations [5]:

- **Resolution and input dynamic range:** the single photon resolution is a desirable feature for X-ray imagers. If direct detection by means of a silicon sensing unit is used, one photon at 250 eV will generate 70 electron-hole pairs only. Hence, a noise performance below 25 electrons is needed to provide single photon detection. At the same time, it is desired to be able to measure up to 10^3 or even 10^4 photons per pulse per pixel. If the same system is used at 12 keV, for example, 3315 electron-hole pairs would be generated per absorbed photon, thus reducing the dynamic range by a factor of 50 and making the single photon detection at 250 eV and a large dynamic range at 12 keV incompatible. These considerations must be taken into account not only for the sensing element, but for the design of the signal processing electronics as well.

- **Vacuum operation and entrance surface:** typically, soft X-ray detectors have to be in the same vacuum as the experiments (windowless beamline), and thus have to be vacuum compatible. If the sensing element is based on silicon, even the entrance surface on the detector has to be specially fabricated to reduce the photon absorption by the insensitive layers. On the other hand, hard X-ray detectors have less critical points, since they can be used outside the sample chamber using X-ray transparent, but optically opaque windows.

1.2.2 Single shot imaging

In some experiments carried out at FEL facilities, the sample under study is static and not, or only negligibly, damaged by the beam. There are other cases, in so called single shot experiments, where the focussed beam have such a high photon density that the sample under study does not survive a single shot, meaning that every single shot have to be trated as a separate experiment and the complete X-ray scattering image has to be recorded in a single pulse [5]. For the image to be of statistical relevance, many pixels have to record more than one photon, thus leading to X-ray detectors based on integration techniques to be used instead of photon counting solutions. At the same time, many of these experiments require single photon resolution. This means that the characteristic of the experiment itself will drive the design of the detector.

1.2.3 FEL beam structure

The structure also depends, among other factors, on whether the FEL is operated in the "burst" or "continuous" mode. This specification, which may vary from one facility to the other, sets the bounds for the readout technique employed in the detector:

- **Burst mode:** in burst mode operation, a large sequence of short pulses is delivered with a low duty cycle. For example, as depicted in Figure 1.2, at the European XFEL up to 3000 pulses, separated by 200 ns, will be delivered in ten pulse trains per second. Hence, for single shot imaging, a complete image has to be recorded every 200 ns (5 MHz) during the 600 μs train duration. Since, with the current technology, it is impossible to transmit a full megapixel image in 200 ns, the frame has to be stored inside the front-end of the detector, and read out during the inter-train period of 99.4 ms. This leads to either an analog or a digital pipeline to be employed in the pixel, along with a storage capacity of 3000 events. Since such a great storage capability would increase the area of the single pixel, a tradeoff between the number of images to be stored and the pixel size must be found, along with proper vetoing mechanism to discriminate whether a successfull hit has occured or not, on the basis of the considered experiment.

- **Continuous mode:** in continuous mode operation, each pulse of X-ray is delivered with a relatively low frequency, in the order of 100 Hz. Even though in this case the readout speed does not represent an issue, a tradeoff must be carried out again according to the experiment

specifications. The spatial resolution can be increased by reducing the pixel pitch and the in-pixel functionalities, leading to complex blocks performing readout, signal processing and digitization either in the chip periphery or off-chip. On the other hand, the pixel dimensions can be increased, providing space for embedding the signal processing chain and even the ADC, thus reducing the functionalities outside the pixel.

1.2.4 Central hole

Since the focussed primary X-ray beam has enough energy to damage most materials, small primary beam stops cannot be used in front of the detector. Therefore, the X-ray imager need to have a central hole in the forward scattering direction to let the beam pass through. In order to minimize the loss of small-angle data, which is of paramount importance especially for image reconstruction, the central hole has to be as small as possible, while still being large enough to avoid hits due to occasional small fluctuations in the direct beam position.

1.2.5 Radiation tolerance

Another key point to be taken into account in the design of X-ray imagers for FEL applications is the radiation hardness of the device, especially when devised for hard X-ray environments. In [5] an example about the total dose absorbed by the detector is given, with reference to the case of the European XFEL. Starting from the assumption of 1250 hours per year of detector usage, a number of photons equal to 10^{16} can be reckoned over a period of three years of facility operation for the hottest pixels. Such a value leads to a worst case scenario of 1 GGy of total absorbed dose with a photon energy of 12 keV and a square pixel with a pitch of 200 μm. In the design of the microelectronic building blocks, special radiation hard structures need to be used for hard X-ray applications, leading to an increase of the area occupancy thus reducing the functionality per unit area.

1.2.6 Angular coverage

The angular coverage of the detector to be used in the experiments is mainly given by the scientific application and the wavelength of the radiation being used. The reason leading to an X-ray FEL facility operating with up to 12 keV (0.1 nm) X-rays relies upon the capability to investigate structures down to the atomic level (feature size of 0.1 nm) [5].

- **Atomic level structures:** in order to distinguish features of 0.1 nm with 12 keV X-rays, Braggs's law shows that a scattering angle of 60 degrees is required. Since, in almost all cases, both positive and negative scattering angles need to be measured, the total angular coverage should extend to 120 degrees. Such a high angular range cannot be covered with a single flat detector. Hence, either multiple segmented detectors or higher photon energies have to be used.

- **X-ray Photon Correlation Spectroscopy:** in the case of X-ray Photon Correlation Spectroscopy (XPCS), studying phenomena at length scales down to 10 nm with 0.1 nm radiation wavelength, Braggs's law shows that a scattering angle of 0.6 degrees, and therefore a detector span of 1.2 degrees, is required. In case no monochromator is used, this range is reduced due to the limited longitudinal coherence length and path length differences (PLD) in rays hitting one pixel. Figure 1.4 shows the geometrical layout of a small angle scattering experiment for a sample with thickness W and a beam size D. It can be shown that the PLD between ray 1 and ray 2 is given by:

$$PLD \; = \; 2W \sin^2(\theta) + D \sin(2\theta) \tag{1.1}$$

  In order for the various rays hitting a pixel to be coherent, the PLD has to be smaller than the longitudianl coherent length, given by the following equation:

$$\xi_1 \; = \frac{\lambda^2}{\Delta\lambda} \tag{1.2}$$

  where λ is the wavelength and $\Delta\lambda$ the bandwidth or monochromaticity. Since the natural bandwidth of an experiment radiation of 0.1 nm is 0.1%, the longitudinal coherence length is 100 nm. Assuming a sample thickness, W, of 1 mm, a typical beamsize, D, of 25 μm and a maximum allowed PLD equal to the longitudinal coherence length of 100 nm, the maximum allowed scattering angle is approximately 0.1 degrees, leading to a total detector coverage of 0.2 degrees.

1.2.7 Angular resolution

Another key parameter set by the scientific application is the angular resolution, which impacts on the size of the pixel and/or the sample-to-detector distance. In almost all cases, the angular resolution is the real experimental requirement, resulting in a detector specification about the pixel size [5].

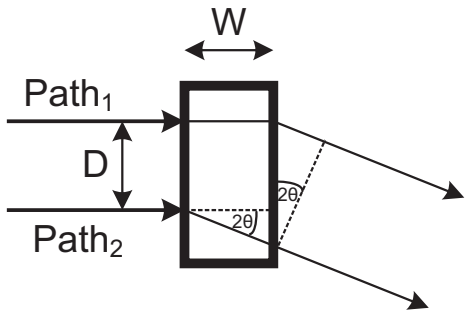

Figure 1.4: geometrical layout of a small angle scattering experiment.

- **Atomic level structure experiments:** since studies on atomic level structures are necessarily limited to changes in a few atomic distances only, a total number of 250 sampling points is largerly sufficient [5], resulting in 500 pixels to cover both positive and negative scattering angles. The total angular coverage of 120 degrees derived in Subsection 1.2.6 gives an angular resolution of 120 / 500 = 0.24 degrees. Even for sample-to-detector distances as small as 10 cm, this would correspond to a comfortably large pixel size of 420 μm.

- **XPCS:** in XPCS, in order to get the highest quality time-correlated data, no more than one speckle per pixel should occur. This means that the pixel size should be equal or smaller than the speckle size. The angular speckle size is given by the following equation:

$$\theta_s = \frac{\lambda}{D} \tag{1.3}$$

  where λ is the wavelength and D is the size of the incident beam. Hence, the angular speckle size can be tuned by adjusting the width D of the incident beam using focussing elements. Again, a trade-off must be carried out between using a large beam, which would lead to negligible sample heating and radiation damage but an impractically small pixel size, and using a focussed beam, which would give comfortably large speckle sizes but a too much concentrated beam. It has to be noticed that, with a beam size of 25 μm, a wavelength of 0.1 nm, the angular speckle is 4 μrad, leading to a pixel not larger than 160 μm with a reasonable detector distance of 40 m [5].

1.2.8 Photon transfer noise sources

The interaction between photons and the detector produces a variation in the signal, or noise, from pixel-to-pixel. In this section, two noise sources related to photon interaction, which have to be taken into account in order to achieve the proper Signal-to-Noise ratio (SNR) in the design of the detector, will be described [6].

Photon shot noise or Poisson noise

The photon shot noise is a spatially and temporally random phenomena described by Bose-Einstein statistics, given by the following equation:

$$\sigma_{SHOT}\left(P_I\right)^2 = P_I \frac{e^{hc/\lambda kT}}{e^{hc/\lambda kT} - 1} \tag{1.4}$$

where P_I is the average number of photon-pixel interaction, $\sigma_{SHOT}\left(P_I\right)^2$ is the interacting photon shot noise variance, h is Planck's constant, λ is the photon wavelength, k is Boltzmann's constant, c is the speed of light in vacuum and T is the absolute temperature.

The trend of $\sigma_{SHOT}\left(P_I\right)^2$ is shown in Figure 1.5 as a function of the wavelength, λ, and the temperature, T. For wavelengths greater than 10 μm, photons couple with phonons increasing shot noise. As the operating temperature is reduced, the semiconductor produces less coupling action and therefore a lower variance. Assuming that $hc/\lambda \gg kT$, $\sigma_{SHOT}\left(P_I\right)^2$ reduces to the familiar shot noise relation characteristic of visible imagers:

$$\sigma_{SHOT}\left(P_I\right)^2 = \sqrt{P_I} \tag{1.5}$$

Since the standard deviation of shot noise corresponds to the square root of the average number of photon-pixel interactions, the signal-to-noise ratio is given by the following equation:

$$SNR = \frac{P_I}{\sqrt{P_I}} = \sqrt{P_I} \tag{1.6}$$

This is a key parameter to be taken into account in the design of an X-ray imager for FEL applications. In order to achieve a sound measurement of the diffraction pattern, the noise introduced by the overall detector chain must be lower than the shot noise contribution in the whole considered input dynamic range.

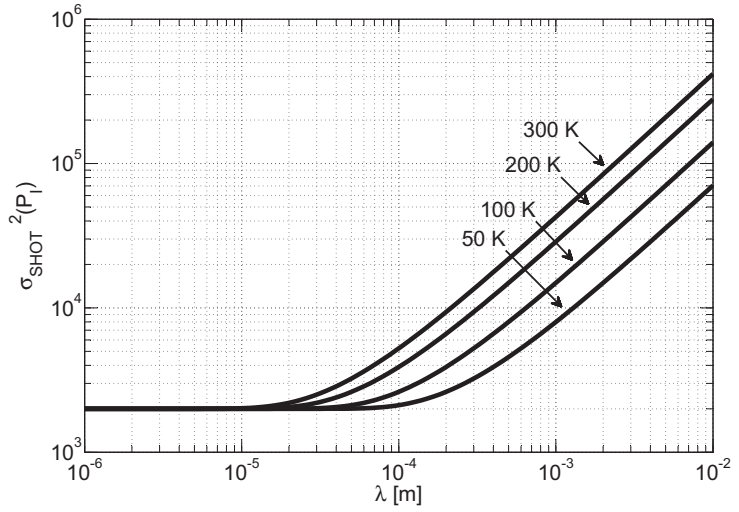

Figure 1.5: trend of the photon shot noise variance as a function of the wavelength and the temperature.

Photon shot noise, also known as Poisson noise, is described by the classical Poisson density function:

$$p_i = \frac{P_I^i}{i!} e^{-P_I} \tag{1.7}$$

where p_i is the probability that there are i interactions per pixel. Figure 1.6 shows the fitting of Poisson distributed photon-pixel interactions for three different values of P_I by using a Gaussian distribution:

$$p_i = \frac{1}{\sqrt{2\pi}\sigma_{PI}} e^{-(i-P_i)^2/2\sigma_{PI}^2} \tag{1.8}$$

As it can be noticed, the Poisson distribution approximates to a Gaussian distribution when the number of interacting photons per pixel is large.

Fano noise

Another noise contribution, smaller than the Poisson one, is the so called Fano noise, defined by the following equation:

$$\sigma_{FN} = \sqrt{\left(F_F \frac{h\nu}{E_{e-h}}\right)} \tag{1.9}$$

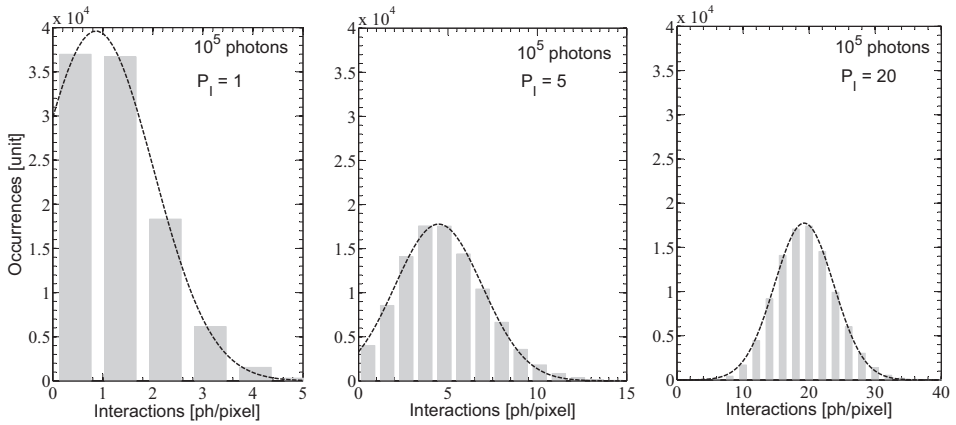

Figure 1.6: gaussian fitting of Poisson distributed photon-pixel interactions, for P_I=1 (left), P_I=5 (middle) and P_I=1 (right).

where σ_{FN} is the Fano noise (expressed in e^-_{RMS}), F_F is referred to as the $Fano\ factor$, which is defined by the variance in the number of electrons generated divided by the average number of electrons generated per interacting photon, h is is Planck's constant, ν is the wavelength and E_{e-h} is the energy per eletron-hole pair. The trend of Fano noise is depicted in Figure 1.7, where the Fano factor for silicon, 0.1, applicable for photon energies higher than 10 eV, has been used. It has to be noticed that Fano noise becomes appreciable in the soft X-ray regime.

1.3 State of the art in FEL instrumentation

In the following subsections, an overview in the area of electronic instrumentation for 2D X-ray imaging is given, limited to some of the most significant examples of the large set of technologies and circuit solutions proposed for experiments at FELs.

1.3.1 Detectors for the European XFEL

The European XFEL consortium is funding three independent detector development projects. Each of the three projects is proposing a different solution to the challenges set by the characteristics of the X-ray beams, in particular the wide signal dynamic range (from 1 to 10000 photons at 1 keV) and the high frame rate foreseen for the burst mode of operation, where each burst

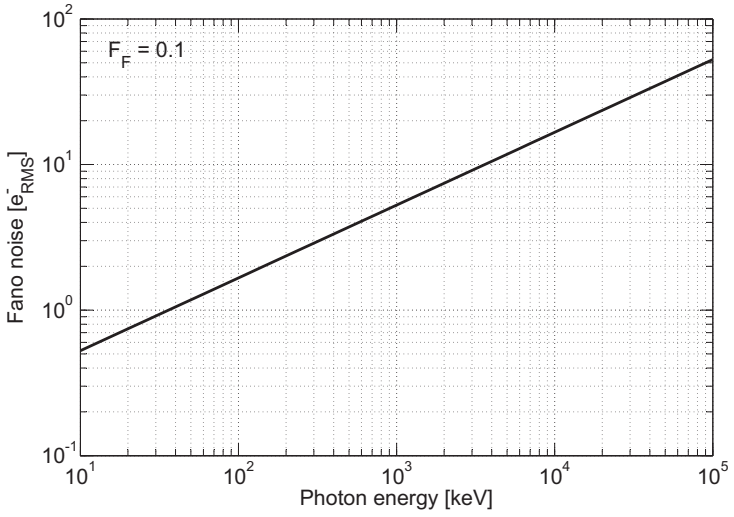

Figure 1.7: trend of Fano noise as a function of the photon energy

includes about 3000 bunches with an inter-bunch interval of about 220 ns, as shown before in Section 1.2.

Adaptive Gain Integrating Pixel Detector

The **AGIPD (Adaptive Gain Integrating Pixel Detector)** [7] consists of an array of 2 × 8 ASICs of 64 × 64 pixels bump bonded to a monolithic silicon sensor of 128 × 512 pixels to build a module. 8 × 2 modules will be used to achieve a 1 Mpixel camera. The schematic view of the front-end channel, designed in a 130 nm CMOS process, is depicted in Figure 1.8. As it can be noticed, the large dynamic range of the input signal is covered by means of a gain switching technique. The baseline configuration of such a pixel cell enables individual programming of the integrator gain to adapt to the expected photon intensity. In case the expected flux range is unknown, the feedback capacitors can be switched dynamically during the detector operation. In this adaptive gain switching (adaptive slope integration) mode, the used gain setting has to be stored along with the data. An in-pixel analog pipeline is used to store on sampling capacitors the integrator output voltages (i.e., the recorded images) during the 0.6 ms long pulse train. About 352 images per train can be recorded by the detector, corresponding to 352 storage capacitors. This feature sets the bounds for the pixel area, which is 200 μm×200 μm. Each

ASIC has 64 × 64 parallel readout channels, where the charge information of several pixel pipelines are chained together and fed into the 14 bit 50 $^{Mb}/_{s}$ ADC of the XFEL data acquisition system. One of the major concerns in this approach is the design of the switches, which should be such to enable charging of the capacitors in the 200 ns inter-bunch period while preventing them from discharging through leakage during the 100 ms inter-train period. The main scientific applications are Coherent X-ray imaging and Photon Correlation Spectroscopy at 12 keV photon energies.

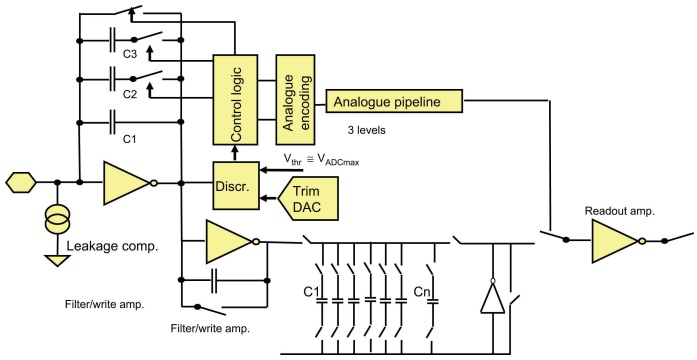

Figure 1.8: schematic view of the pixel cell for the AGIPD imager [7].

Large Pixel Detector

The approach of the **LPD (Large Pixel Detector)** [5] [8] project to the issue of a large input dynamic range involves employing three different channels in parallel, each with a different gain setting and followed by its own analog pipeline. The principle is depicted in Figure 1.9. In order for the pixel to incorporate three separate pipelines with 500 storage capacitors each, the cell pitch needs to be relatively large, about 500 μm (which may be too large for some applications). The LPD front-end module, fabricated in a 130 nm CMOS technology, will also include an interposer device in order to adapt the pitch difference between the silicon sensor and the ASIC. This solution makes it possible to use a different pitch on the two interconnected layers and offers the advantage of adding an extra radiation shield, therefore relaxing the radiation hardness requirements on the ASIC. However, it may contribute some parasitic capacitance at the channel input, resulting in a degradation of the noise performance. The three analog pipelines can also be linked together to form a single, 1500-deep pipeline, amounting to about half of the number of images that can be taken in a single pulse train at the European XFEL.

Each chip will contain 16 × 32 pixels and 8 × 1 chips will be bump-bonded to a monolithic silicon sensor giving 128 × 32 pixel tiles. 2 × 8 of these tiles will be used to construct the so called super modules with 256 × 256 pixels. These super modules can then be used to construct detectors of any size. The LPD focuses on the 12 keV photon energy range, optimally suited for the so-called liquid scattering experiments.

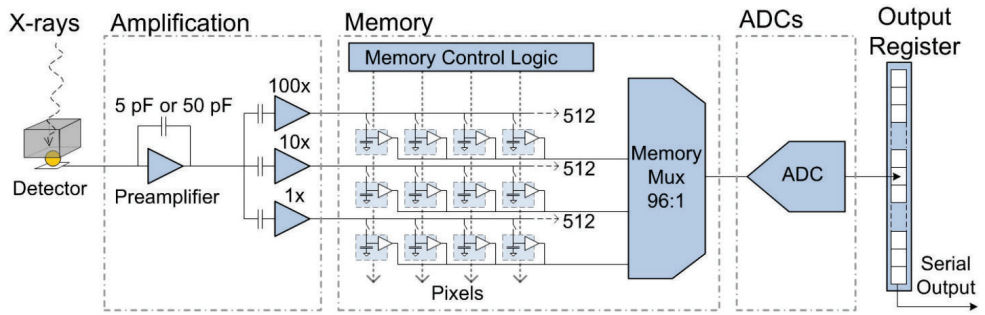

Figure 1.9: simplified schematic view of the pixel cell for the LPD imager [8].

DEPFET Sensor with Signal Compression

The **DSSC (DEPFET Sensor with Signal Compression)** [4] detector provides the non-linear response at the sensor layer by means of a DEPFET device [9] featuring an internal gate which extends into the region below the large area source. As depicted in the conceptual front-side view of Figure 1.10, small signal charges cumulate below the channel, thus full contributing to a transistor current increase. For larger signal charges, the effect on the transistor current will be lower, as the charges spill over into the region below the source. While being one of the original points of the proposal, implement-

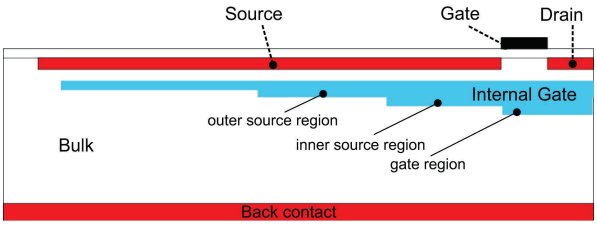

Figure 1.10: conceptual front-side view of the DSSC device [4].

ing the non-linear response in the DEPFET sensor requires quite a complex

fabrication process, resulting in fairly long turnaround times. On the other hand, the very low noise performance of the DEPFET makes it an excellent candidate for experiments using low energy X-rays, around 1 keV or smaller. The DSSC detector is made of hexagonal pixels with a 136 μm side, yielding a 200 μm bump bond pitch. The front-end chip is designed in a 130 nm CMOS process provided by IBM and will include 64 $\times$ 64 elements. As depicted in the simplified block diagram of Figure 1.11, the pixel level readout of the sensor can be carried out either in Drain Current (DC) mode, with the drain current driven into a virtual ground and sensed, or in Source Follower (SF) mode [4], with the DSSC arranged in source follower configuration and AC-coupled to a charge sensitive amplifier. Compared to AGIPD and LPD, the DSSC detector provides direct in-pixel digitization with a high speed, 8-bit, single-ramp (Wilkinson) A-to-D converter (ADC) operating with a 800 MHz clock (the content of the ADC counter is actually incremented on both fronts of the clock signal). Moreover, it features an in-pixel digital memory to store up to 600 events. 2 $\times$ 8 ASICs will be bump-bonded to a monolithic DSSC giving 128 $\times$ 512 pixels ladders. 16 ladders will be finally used to achieve a 1024 $\times$ 1024 pixels (1 Mpixel) imager.

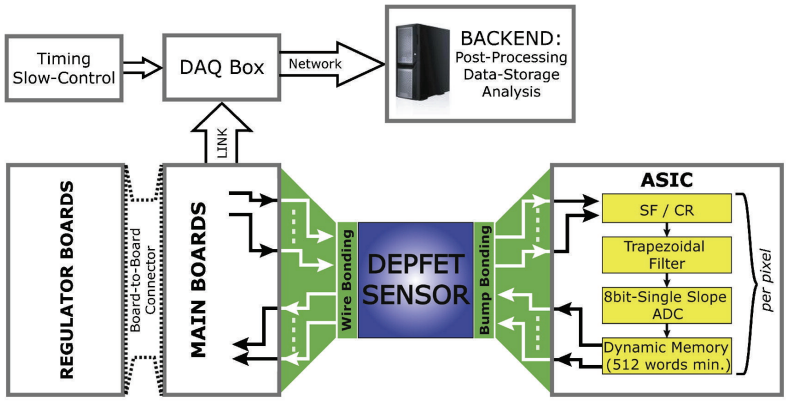

Figure 1.11: simplified block diagram of the DSSC detector [4].

1.3.2 Percival

The **Percival (Pixellated Energy Resolving CMOS Imager, Versatile and Large)** detector is a large pixellated imager featuring both a wide dynamic range and a good spatial resolution [10]. With respect to the solutions proposed at the European XFEL, operating with beam energies ranging from 1 keV to 14 keV, this detector aims to have characteristics compatible with

low-energy FEL and synchrotron sources. The core is a CMOS Monolithic Active Pixel Sensor (MAPS), depicted in Figure 1.12, embedding both charge collection junctions and signal processing circuitry. The design is based on a quadruple well 180 nm CMOS process, providing a 12 μm thick high resistivity epitaxial layer, which represents the sensitive volume of the detector. The Percival detector deals with the anticipated input dynamic range of 10^5 photons, with an energy between 250 eV and 1 keV, by means of a multi-gain approach based on the integration of three capacitors with increasing size inside each pixel, as depicted in Figure 1.13, and features an equivalent noise charge (ENC) of about 15 electrons, enabling single photon detection. The project is pursuing the ambitious goal to fabricate a 27 μm pitch, 4000 $\times$ 4000 pixel detector to be read at a frame rate of 120 Hz or lower, suitable for operation at the LCLS.

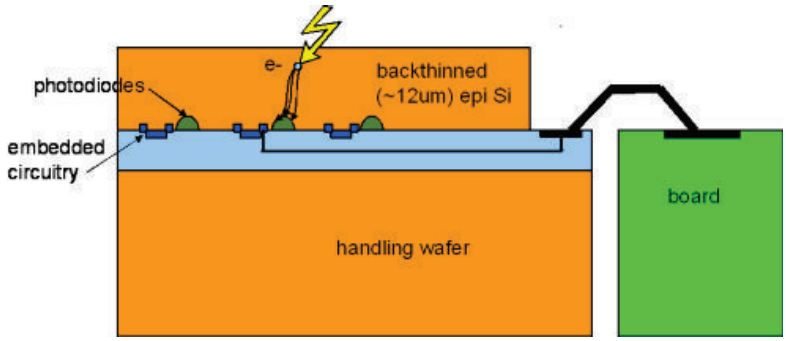

Figure 1.12: simplified front-side view of the Percival detector, with the sensor wire-bonded to the periphery board [10].

1.3.3 XAMPS

The **XAMPS (X-ray Active Matrix Pixel Sensor)** detector is a monolithic device built on high resistivity silicon arranged in a matrix fashion of 1024 $\times$ 1024 square pixels with a 90 μm pitch [11] [12]. Figure 1.14 shows the XAMPS pixel structure. Thanks to JFET switches integrated in the sensing layer, the system is operated in a data accumulation phase (JFET switch open) and a data readout phase (JFET switch closed). During the first phase, the charge released by a photon in the substrate of the sensor (400 μm thick) is stored on a capacitor which occupies most of the pixel area and which can store as many as 3.5 pC. In the readout phase, taking up to a few microseconds, the switches are closed, therefore allowing the charge to flow to the

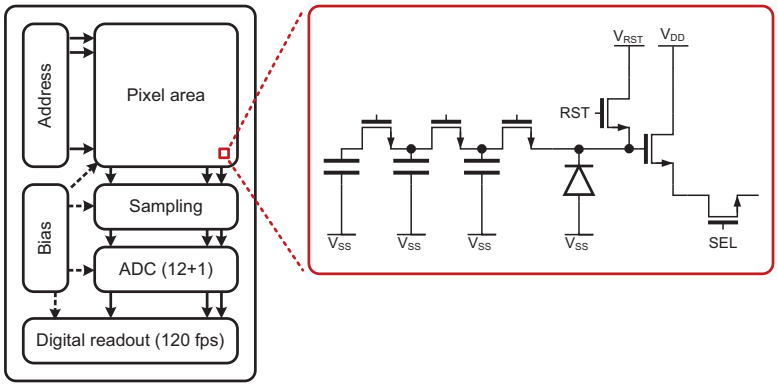

Figure 1.13: simplified diagram of the Percival detector.

readout lines. As depicted in Figure 1.15, the sensor is connected via wire

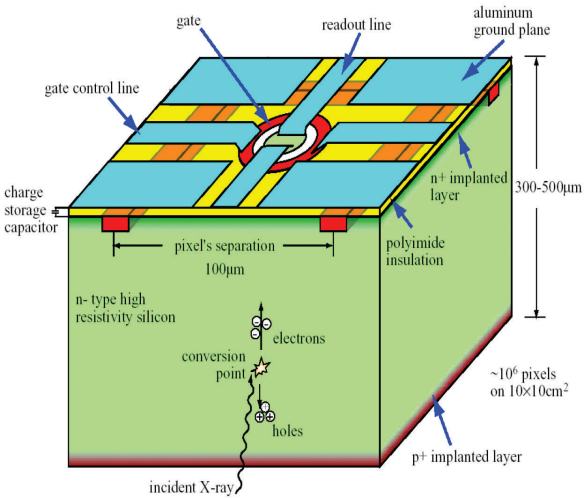

Figure 1.14: pixel structure in the XAMPS sensor [12].

bonding to 16 XAMPS front-end (XAMPSFE) ASICs of 64 channels each for a parallel readout of the pixels in the same row. Each channel, designed in a 250 nm CMOS technology, integrates a low-noise charge preamplifier with a programmable double polarity pulsed reset, a second order non-inverting programmable filter, two correlated double samplers and a discriminating charge pump. In order to cope with the wide input dynamic range of 10^4 photons with an energy up to 8 keV, amplitude measurements are performed in two

stages. A first, coarse digitization is performed on-chip. Residuals from the conversion are digitized with an external 14-bit ADC [12]. A few milliseconds are needed to readout the entire detector, making it suitable for applications at FELs continuously operated at rates in the 100 Hz range, like LCLS.

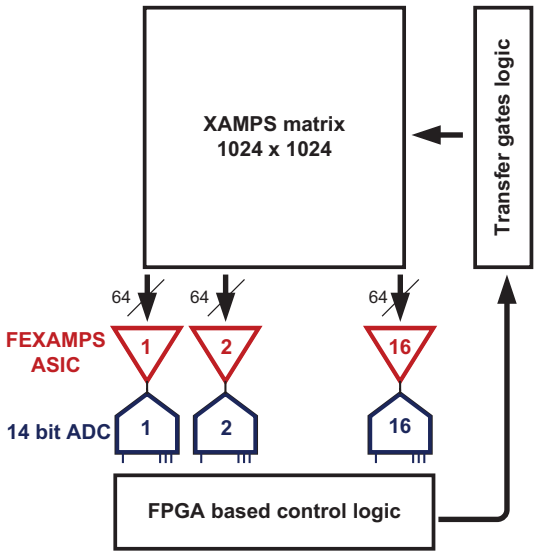

Figure 1.15: block diagram of the XAMPS detector system.

1.3.4 SOPHIAS

The **SOPHIAS (Silicon-On-Insulator PHoton Imaging Array Sensor)** is an X-ray pixel detector based on a CMOS silicon-on-insulator (SOI) technology targeting X-ray diffraction imaging experiments [13]. The detector, featuring a 30 μm pitch, is designed to be sensitive to single photons in the 5.5-7 keV energy range and to perform frame readout at a 60 Hz rate, suitable for operation at the SCSS. Charge is processed using a typical CMOS MAPS scheme. The relatively low degree of radiation hardness typical of this technology is strongly mitigated by the shielding action of the 500 μm thick handle wafer also acting as the sensitive volume of the detector. A dual-gain concept is used in the SOPHIAS detector to address the issue of wide input dynamic range, similarly to the case of the Percival detector. The basic chip includes as many as about 1.9 Mpixels.

1.3.5 CCD based detectors

In general, Charge Coupled Devices (CCDs) represent a natural choice for imaging applications. However, for X-ray FEL cameras, suitable architectures have to be envisioned to overcome the limited readout rates (of the order of a few frames per second) typical of sequentially read out structures. For this purpose, almost-fully or fully-column-parallel readout architectures have been proposed for applications at the LCLS FEL experiments. Front-end chips may be needed to provide amplification, sampling and fast digitization of the charge collected by the detector.

For example, in [14], the development of a soft X-ray camera based on compact, fast CCD (cFCCD) is presented. The cFCCD camera is based on a custom, highly parallel, thick, high-resistivity, fully-depleted direct detection CCD arranged in a matrix of 480 $\times$ 480 square pixels of 30 μm pitch. The sensor is 200 μm thick, for a high detection efficiency up to 8 keV, and has an "almost column parallel" readout architecture, in which each group of 10 columns has an individual output stage for both top and bottom halves of the CCD, giving a total number of 96 output ports, with an overall readout time of about 6 ms. The sensor is connected to 16-channel ASICs, called Fast CCD Readout IC (FCRIC). Each channel integrates a preamplifier, a multi-gain integrator and correlated double sampler, followed by a 14-bit pipelined ADC operating with a conversion period of about 1 $^{\mu s}/_{pixel}$.

The High-speed Image Preprocessor with Oversampling (HIPPO) is a column-parallel CCD readout ASIC designed in a 65 nm CMOS technology, featuring a 1 $^{Gpixel}/_{\mathrm{s}}$ pixel rate and thus enabling 10000 fps for a 1 Mpixel camera [15]. The ASIC consists of 16 channels subdivided in four modules of four channels each. Each module includes 4 analog front-end blocks and four sample-and-hold circuits. A-to-D conversion is performed through a pipeline ADC shared among four channels. Data from the ADC are sent off chip at a 480 Mb/s rate.

1.3.6 Summary of state-of-the-art FEL instrumentation

As a reference for comparison between state-of-the-art electronic instrumentation developed for X-ray FEL applications, Table 1.2 summarizes the main specifications of the detectors proposed by research collaborations working worldwide at FEL facilities.

Name	**Technology**	**Pitch** [μm]	**Number of pixels**	**Input range** [ph]	**Energy** [keV]	**Noise** [e^-_{RMS}]	**Facility**
AGIPD	130 nm	200	1 M	10^4	12	300	Eu XFEL
LPD	130 nm	500	1 M	$10^4 \div 10^5$	5÷20	1000	Eu XFEL
DSSC	130 nm	200	1 M	6×10^3	0.5÷20	70	Eu XFEL
Percival	180 nm	27	10÷16 M	10^5	0.25÷1	15	LCLS
XAMPS	250 nm	90	1 M	10^4	up to 8	650	LCLS
SOPHIAS	200 nm SOI	30	1.9 M	3.6×10^3	5.5÷7	150	SCSS

Table 1.2: main specifications of state-of-the-art X-ray FEL detectors.

Chapter 2

Analog blocks for pixel-level calibration of detector front-end circuits

In this chapter, the activity carried out in the framework of the DSSC collaboration is presented. First, an overview about the project is given in Section 2.1, by focusing on the sensing element of the detector and on the building blocks of the readout ASIC. Then, the characterization activity on a prototype of the readout ASIC is described and discussed in Section 2.2. Section 2.3 concerns the design optimization of the injection circuit employed in the readout ASIC for pixel-level calibration purpose, carried out on the basis of the results from the characterization of the prototype chip. Finally, the development of the test system for the main functionality tests of the bare modules of the DSSC detector is presented in Section 2.4.

2.1 Overview of the DSSC project

As already mentioned, the DSSC collaboration is developing a detector for X-ray FEL applications able to cope with the demanding requirements set by the European XFEL. The main specifications of the DSSC detector are summarized in Table 2.1. To pursue such a goal, the project is developing a system with a pixellated silicon sensor based on a new DEPFET device, connected via bump-bonding to an ASIC for the parallel readout of the full matrix. As depicted in Figure 2.1, each quadrant of the focal plane consists of 4 ladders and 8 monolithic sensors of 128 $\times$ 256 pixels, with an overall sensing area of 21 cm $\times$ 21 cm. Each ASIC integrates 64 $\times$ 64 readout channels,

with an array of 2 × 4 ASICs bump bonded to one sensor. In the following subsections, a description of the DSSC device and the readout ASIC is given.

Parameter	Value
Energy range	0.5 keV÷6 keV
Number of pixels	1024 × 1024
Pixel size	204 × 236 μm
Input dynamic range	$\geq$ 10000 ph for E$\geq$ 1 keV $\geq$ 4000 ph for E = 0.5 keV
Resolution	1 ph
Frame rate	0.9 ÷ 4.5 MHz
Average power consumption	400 W in vacuum
Operating temperature	253 K

Table 2.1: summary of the DSSC main specifications.

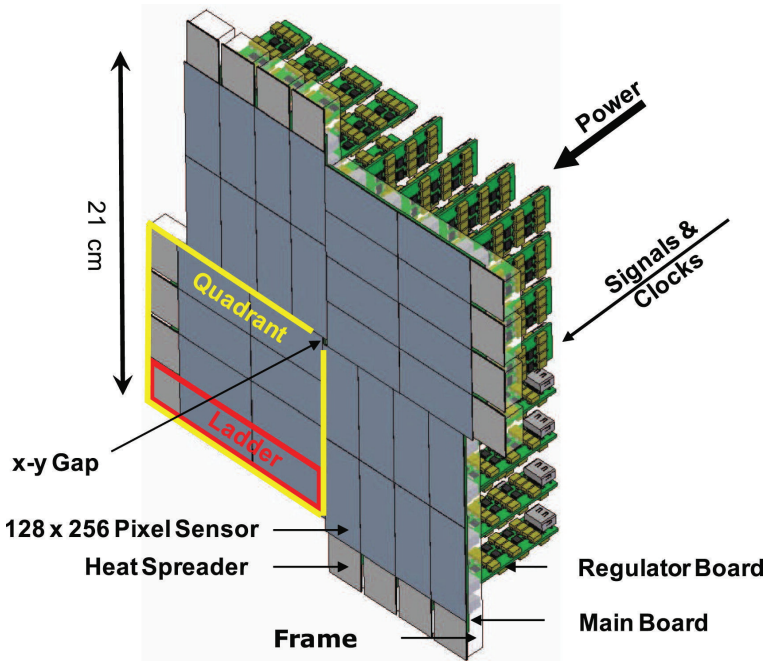

Figure 2.1: 3D view of the DSSC focal plane [4].

2.1.1 The DEPFET Sensor with Signal Compression

The sensing element of the DSSC detector is a new type of DEPFET device, the so called DEPFET Sensor with Signal Compression (DSSC). As depicted in Figure 2.2, a DEPFET device is a Field Effect Transistor (FET) with an electrode on the bottom surface acting as radiation entrance window [16]. The n-doped bulk contact is reversed biased with respect to the p-doped source, drain and back contacts. With the proper doping concentration and bias voltage, a potential maximum below the channel of the transistor is created. This region, called internal gate, collects signal electrons generated within the depleted bulk thus increasing the channel conductivity. The collected charge can be measured with one of the following solutions:

- Source follower (SF) mode: the current is imposed by means of a current source, and the device is operated in source follower configuration. A collected charge in the internal gate leads to a voltage step at the source (output) terminal, which is usually AC-coupled to a preamplifier.

- Drain current (DC) mode: the terminals of the device are kept to a fixed potential and the drain current, which is proportional to the collected signal charge, is read out. For a proper measurement, the bias current of the device corresponding to no signal collection is read out and subtracted.

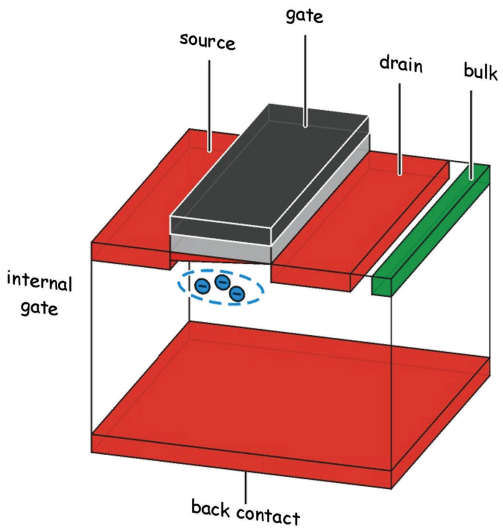

Figure 2.2: simplified view of a DEPFET device [16].

The charge collected in the internal gate can be removed by applying a positive voltage pulse to the clear (bulk) contact, thus restoring the initial condition. It has to be noticed that the DEPFET is a natural building block for a pixel detector as it combines the properties of detector, amplifier and storage cell in a single structure.

The DSSC consists of a DEPFET device with a strongly non-linear current-charge characteristic, able to cope with both the single photon resolution for small signals and the wide input dynamic range requirements set by the European XFEL [16]. This feature has been achieved by extending the internal gate into the region below the large area source region, as depicted in Figure 2.3. Small signal charges are collected below the channel, fully contributing to an increase in the transistor current. On the other hand, as a large amount of charge is collected and spilled underneath the source region, the increase in the transistor current is less effective, resulting in the non-linear behavior of the charge-current characteristic shown in Figure 2.4. In order to optimize a signal collection time, the pixel has the shape of a regular hexagon with a side length of 136 μm, minimizing the distance from the centre to the edge, and features a pitch of 204 μm along the x direction and a pitch of 236 μm along the y direction. The device is enclosed by two drift rings that are biased in such a way that signal electrons are guided towards the centre of the pixel. Moreover, the hexagonal shape of the drift rings provides a more homogeneous drift field with respect to a conventional square pixel and is more effective in focusing the collected charge into the internal gate. The DSSC is operated in drain current readout mode with a gain, defined as $g_q = {}^{dI_{drain}}/_{dQ_{in}}$, of about 288 pA per signal electron in the linear region. For large input signals, a compression factor of 17.5 is achieved, thus resulting in a gain of about 34 pA per

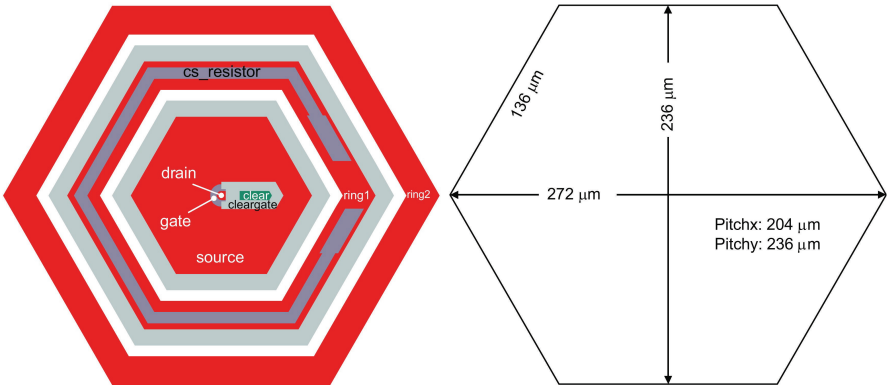

Figure 2.3: top view of the DSSC pixel cell [4].

signal electron.

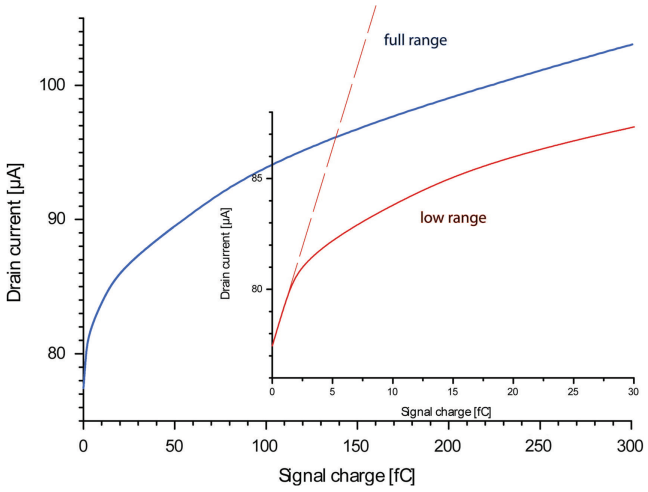

Figure 2.4: non-linear response of the DSSC sensor [4].

2.1.2 The DSSC Chip

The readout ASIC, also known as the DSSC Chip, is designed in a 130 nm CMOS technlogy by IBM and is powered with a supply voltage of 1.2 V. It is arranged in a matrix fashion of 64 $\times$ 64 pixels featuring a low-noise readout channel with integrated digitization of the DSSC output current at a rate between 0.9 MHz and 4.5 MHz. Each channel, designed to match the DSSC pixel without any interposer, have a form factor of 204 μm $\times$ 236 μm. A total of 256 chips will be used to readout the full 1 Mpixel camera. The single readout channel, depicted in Figure 2.5, is based on the following main building blocks [17]:

- An input cascode stage to keep the drain of the DSSC at constant potential, thus enabling the drain current mode operation. The drain of the input cascode is connected to the virtual ground of the front-end filter, and is set to a potential of 950 mV.

- A pixel-level adjustable current source for the DSSC bias current cancellation [18]. This circuit is based on a 5-bit DAC (with pixel-wise settings) and an additional continuous regulation which is operated in a closed loop before the arrival of the X-ray macro bunch.

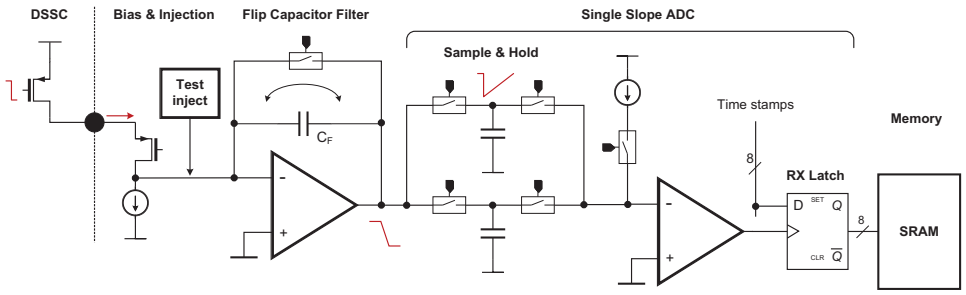

Figure 2.5: conceptual schematic of one DSSC readout channel.

- A time variant filter, also known as the Flip Capacitor Filter (FCF), acting as gated integrator and performing correlated double sampling with a trapezoidal weighting function. In order to compensate the signal measurement for the bias current contribution, both the baseline and the signal are integrated in a single stage by flipping the feedback capacitance [19] of the amplifier. The gain of the stage can be adjusted by changing the feedback capacitance, depending on the input photon energy. The reference voltage of the FCF is 950 mV.

- An injection circuit for pixel-level calibration of the readout channel and for functional test purposes [20]. The circuit is based on an 8-bit binary weighted current steering DAC topology, and integrates a coarse current DAC for the emulation of the bias current from the DSSC.

- A pair of Sample-and-Hold (S&H) capacitors for an interleaved readout operation.

- An 8-bit Wilkinson type (single slope) ADC [21], based on a ramp current, started with a precise strobe, which charges the S&H capacitors and latches 8 gray coded differentially distributed time stamps once the threshold voltage is reached. A fast 800 MHz external clock is used to toggle the counter on both edges, giving a time resolution of 625 ps. The ramp current is pixel-level adjustable for a fine tuning of the gain of the readout channel. Moreover, a programmable time delay on the ramp signal allows to individually adjust the ADC offset with a granularity equal to 1 tenth of the bin size. An additional bit can be used with operation at frequencies lower than 4.5 MHz. The ADC covers an input voltage ranging from 0.2 V to 1 V, respectively for high and low signals at the input of the front-end.

- A SRAM to store 640 words of 9 bits during the X-ray pulses train period. The size of the memory is such that all the events occurring in a 600 μs bunch train period with a 0.9 MHz burst mode operation can be stored. At higher frequencies, further events can be stored thanks to a vetoing mechanism which discriminates whether a successfull hit has occured or not.

- Additional auxiliary blocks, like static control registers, a large switchable decoupling capacitor, monitoring lines and a debug readout circuit.

2.2 Characterization activity on the MM3 prototype

In the framework of the DSSC collaboration, a characterization activity has been carried out on a prototype of the DSSC Chip, the so called MM3 matrix, integrating 16 $\times$ 8 readout channels. In this section, an overview about the prototype chip is first given. Then, the test system used to perform the measurements is briefly decribed. Finally, the results from the characterization activity, mainly focused on the injection circuit for pixel-level calibration and test purpose, are presented.

2.2.1 Overview of the MM3 prototype chip

The MM3 is the third generation of ASICs integrating smaller matrices (Mini-Matrix) with respect to the final DSSC Chip of 64 $\times$ 64 pixels. The layout of the chip is depicted in Figure 2.6, along with the layout of the single readout channel. The matrix is divided in two sub-matrices of 16 $\times$ 4 pixels, according to the block diagram shown in Figure 2.8. One 16 $\times$ 4 matrix uses an asynchronous binary Grey Code Counter (GCC) generated in-pixel from a global clock, whereas the other matrix uses a global GCC distributed from the periphery of the chip. This choice has been made in order to evaluate the performance of the ADC with both the solutions. As depicted in Figure 2.8, the power supply is distributed with in a snake-like fashion which emulates the column based distribution in the final chip, with 64 pixels powered by the same line. The bottom half of the matrix, counting 8 $\times$ 8 pixels, can be bump bonded to a sensor. The architecture of the single readout channel is shown in Figure 2.9. Besides the main blocks already described above, additional logics and test points have been integrated for monitoring and characterization purposes:

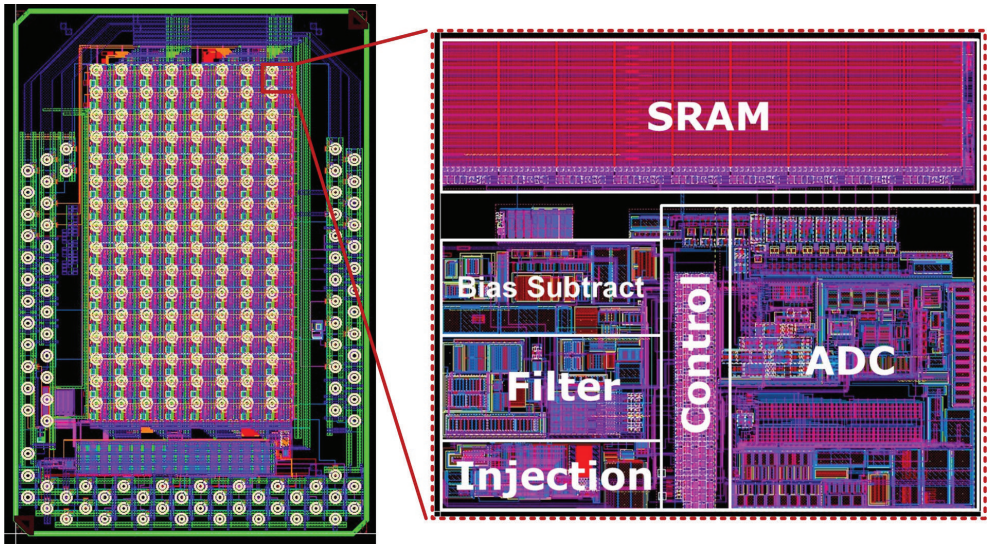

Figure 2.6: layout view of the MM3 chip prototype matrix (right) and of the integrated readout channel (left).

- An external signal can be fed into each pixel through the inject bus, labelled as `IN_Injectbus`. Either a voltage or a current can be applied by enabling the bit number 13 or 11 of the pixel control register, respectively.
- The adjustable current source, sinking the DSSC bias current, can be tested by setting the voltage at the `VP_BBusInjection` node, externally accessed, which change a DC current, generated with a PMOS transistor, in the input branch. An additional test point, `OUT_Inject_Ibias`, enables to monitor such current.
- The in-pixel injection circuit can be used with bits number 19 and 20, enabling the signal injection and the DC current, respectively.
- The voltage at the output of the FCF of pixel number 63 can be monitored with the test point labelled as `MON_TestFilter`, providing a buffered version of the signal.
- A 2:1 multiplexer (MUX), controlled by bit number 14 of the pixel control register, provide either the FCF output voltage or a voltage applied to the inject bus at the input of the ADC. This block is of crucial importance for bypassing the front-end and performing a characterization

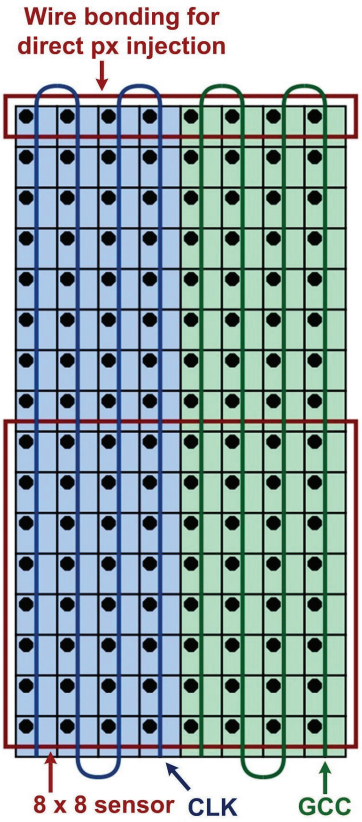

Figure 2.7: pixel numbering, arrangement of transmission lines and input connections.

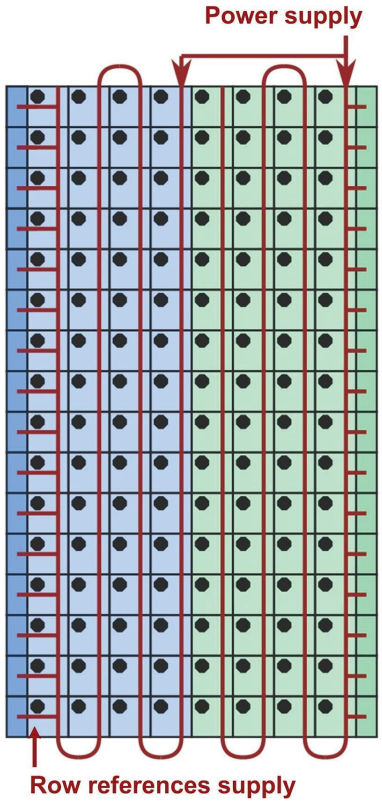

Figure 2.8: Distribution of the power supply for the two pixel matrices.

of the ADC only.

- The ramp current of the ADC can be measured by enabling bit number 15, which steers the current from the S&H capacitors branch towards the inject bus.

- A 2:1 multiplexer (MUX), controlled by bit number 31 of the pixel control register, enables to test the GCC and the memory storage with the dynamic signal `DDYN_SwCap`.

The dynamic control signals, indicated with a signal name starting with `DDYN`, are generated by the front-end sequencer starting from a 700 MHz clock and

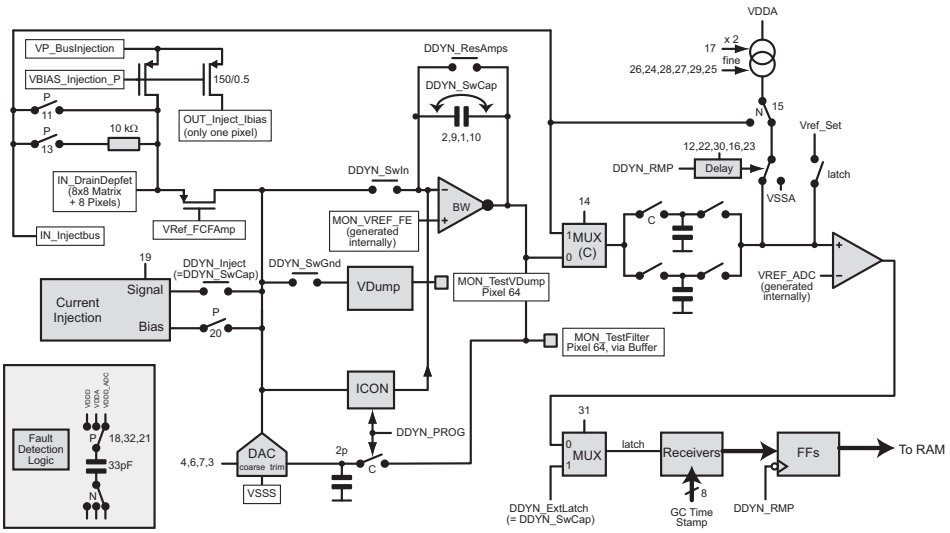

Figure 2.9: Conceptual schematic view of the single readout channel integrated in the MM3 prototype. Signals in boxes are chip pins. The numbers on the switches indicate the bit position in the pixel control register, whereas switches having names starting with `DDYN` are for dynamic control.

a 100 MHz clock, provided off-chip. Figure 2.10 depicts the time diagram of the dynamic control signals, which are described in the following list:

- `DDYN_RMP`, which triggers, on the rising edge, the ADC conversion by transferring the FCF output voltage to the S&H capacitor and by starting the ramp current.
- `DDYN_SwIn`, which closes the path toward the feedback capacitance of the

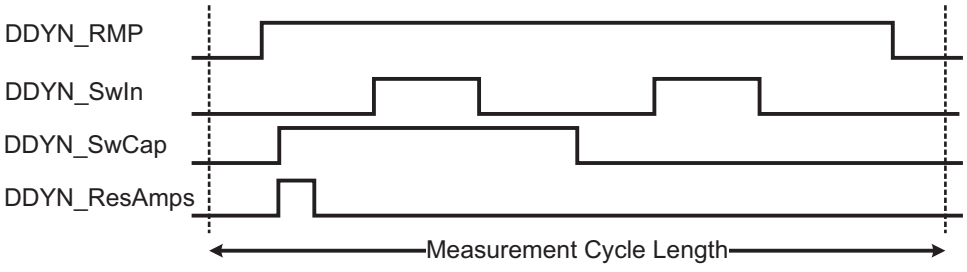

Figure 2.10: Dynamic control signals for the front-end operation.

FCF stage thus enabling either the baseline or the integration phases.

- `DDYN_SwCap`, which flips the FCF feedback capacitance..
- `DDYN_ResAmps`, which enables the reset of the FCF.

The operation of the chip is managed by the global digital control block, outlined in Figure 2.11. The Master Finite State Machine (FSM) is triggered by the control telegram decoder and handles the coarse control of the chip, triggering the operation of all the other main modules for the control of the front-end, SRAM and readout chain. Each module has its own configuration register.

- **Command telegrams**: The command telegrams are 5 bits, sent serially over the `XSTART` line, summarized in 2.2. The telegram decoder samples `XSTART` on the rising edges of `XCLK` and starts receiving a telegram on a

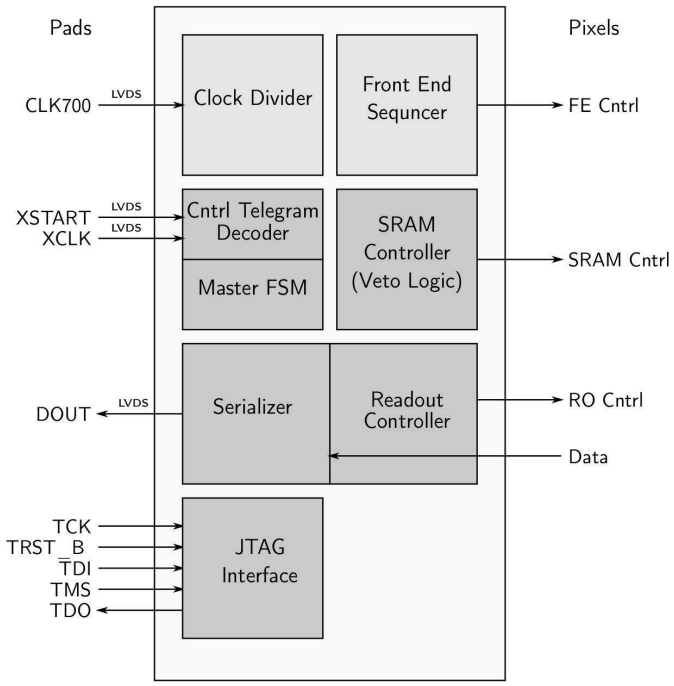

Figure 2.11: Block diagram of the global digital control block. The signals on the left are connected to the I/O pads, the signals on the right control the chip.

rising edge at XSTART. The telegrams trigger certain cycles in the Master FSM.

Bit config	Command name	Description
10000	cmd_START_BURST	Starts a new burst
10001	cmd_START_READOUT	Starts the readout
10010	cmd_VETO	Vetoes an event with a fixed latency
10011	cmd_SEND_TEST_PATTERN	Starts sending the test data pattern
10100	cmd_STOP_TEST_PATTERN	Stop sending the test data pattern

Table 2.2: Summary of the command telegrams.

- **Master FSM**: The Master FSM is the supervising instance of the chip, triggered by the 100 MHz. According to the state machine summarized in Figure 2.12, the states of the chip can be sSEND_TEST_PATTERN, during which the chip continuously sends a programmable test pattern, sIPROG, during which the programmable current source for the DSSC is finely tuned, sBURST, during which the matrix processes the input signals, sVETO, during which the veto signal is forwarded to the SRAM controller, and sREADOUT, during which the chip is read out.

- **Front-end sequencer:** the front-end sequencer generates the 4 dynamic digital signals required to operate the front-end properly. The sequencer is based on a 700 MHz clock (CLK700), referred to as fast clock, and a 100 MHz clock signals, referred to as slow clock, both provided externally. The slow clock has a fixed phase relation with respect to the fast clock, from which it is derived. The mechanism for generating the sequences is summarized in Figure 2.13. It is based on various short partial sequences in a fast clocked serial shift register repeated using the slower clocked counter. The partial sequences concatenated with their repetition counts are stored in a shift register that runs with the slow clock. The partial sequences are repeated until the repetition count is reached, and, then, the next partial sequence is loaded into the fast serial shift register. The initial state of the slow shift register is programmed via slow control. All of the entries of the slow shift register receive their initial state from the JTAG slow control. For measurements using external input signals, it is necessary to program long flat

tops for the trapezoidal filter in the front-end. The sequencer features a module which generates a hold signal which is common for all tracks. When the hold signal is active, none of the repetition counters and slow shift registers in the sequencer tracks are advanced. The current partial sequences are repeated until the hold signal becomes inactive. The hold signal is obtained from a shift register which holds a count and the hold bit. The count is decremented each clock cycle and the shift register is advanced when the count has reached zero, thus making it possible to program phases in which the hold is active and phases in which the hold is inactive.

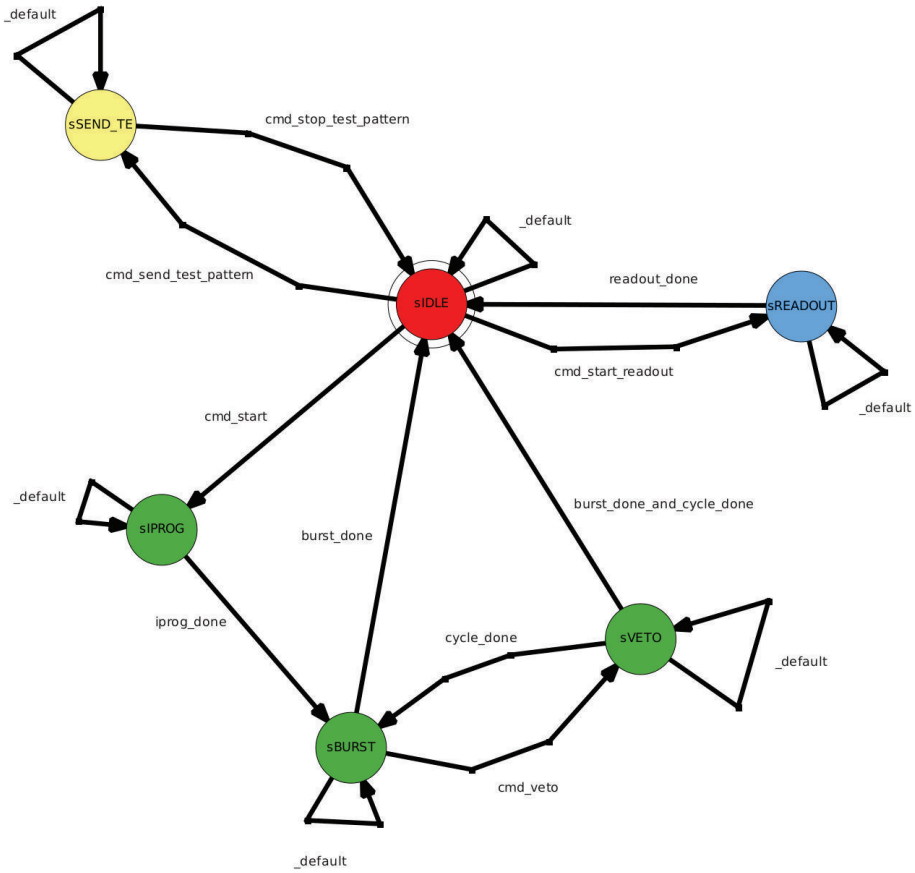

Figure 2.12: Master FSM of the MM3 chip.

- **SRAM Controller and Readout Controller:** the state machine located in the SRAM controller generates the required signals from the 100 MHz clock, in order to have it synchronous with the analog front-end during the burst. During the readout, the SRAM Controller loads the data from the SRAM cells, whereas the Readout Controller loads the data from the bit busses to the internal pixel readout register chain and shifts them out. The synchronization between the SRAM Controller and the Readout Controller is realized through a handshake.

2.2.2 The MM3 chip injection circuit

The injection circuit integrated in the MM3 chip, designed during a previous Ph.D. program [22] within the framework of the same research group this Ph. D. activity has been involved, is intended for use as a calibration block of the front-end electronics as well as for test purpose of the detector once it

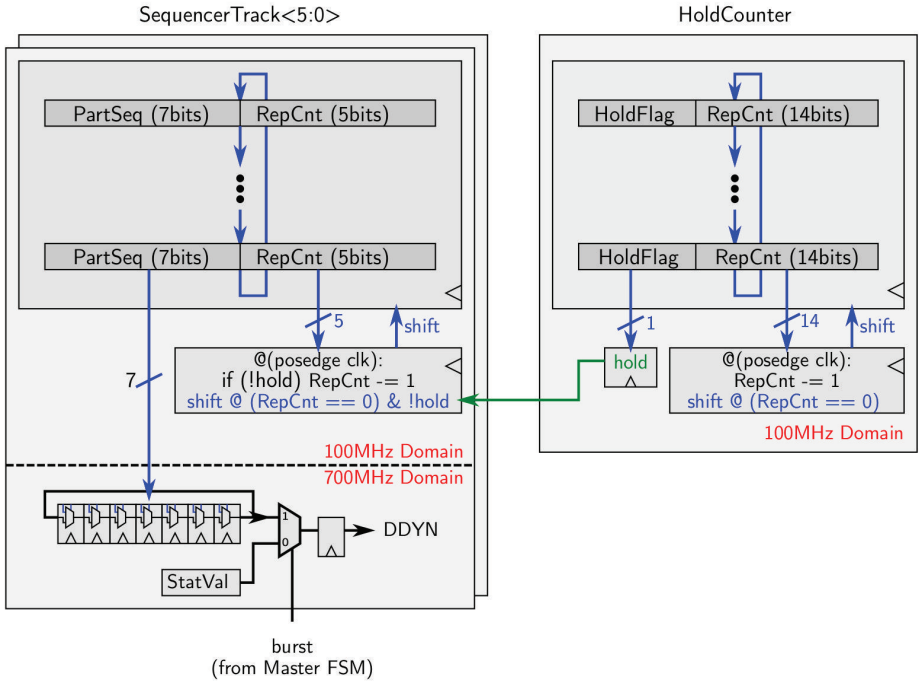

Figure 2.13: The front-end sequencer mechanism. The Hold Counter is common for all tracks and also stops the cycle counter in the Master FSM which determines the length of a measurement cycle.

will become operational. The main requirements of the injection circuit are summarized in the following list:

- **Output:** both a DC current, emulating the DSSC bias, and a current signal.
- **DC current range:** 10 μA $\div$ 150 μA.
- **DC current resolution:** 10 μA
- **Current signal range:** 0 μA $\div$ 25 μA.
- **DC current resolution:** far better than 1 photon with an energy of 1 keV, corresponding to 80 nA. A resolution of 10 nA has been chosen.
- **Output characteristic:** Straigth and monotonic characteristic. No particular constraints concerning the integral-non-linearity (INL).
- **Output noise:** lower than the input referred noise of the front-end, corresponding to an Equivalent Noise Charge (ENC) of about 30 e^- RMS.
- **Injection control:** pixel-level habilitation of the signal injection.
- **Voltage room at the output:** since the voltage room to inject the signal at the source of the input cascode would be too low for a proper circuit operation, the signal is fed at the drain of the input cascode, which is a low impedance virtual ground thanks to the FCF amplifier and kept a potential of 950 mV.

As depicted in Figure 2.14, the circuit consists of two main sections. In the periphery of the chip, a Current Steering DAC and a coarse current DAC provide the references for the DC current and the signal to be appliead at the input of each front-end, respectively. Inside each pixel of the matrix, a pulser, fed by the periphery references, provides the DC current and the signal at the input of the front-end. The output can be enabled by means of a dedicated bit.

The Coarse Current DAC is based on a 4-bit binary weighted current network, as depicted in Figure 2.15. Since no particular constraints in terms of accuracy and linearity are set for such stage, the DAC has been designed using scaled MOS devices as current sources, with an input reference current of 1 μA. The DC current can be enabled in each pixel with a dedicated bit.

The Current Steering DAC is responsible for setting the amplitude of the signal to be injected. It is based on a binary weighted architecture of k groups

of 2^{k-1} unity current sources, with k integer and $1 \leq k \leq N$, where N is the number of bits for the DAC. To meet the requirements of range and resolution of the injected signal, 12-bits are mandatory to set the amplitude. However, in order to reduce the complexity and the area of the Current Steering DAC, only 8-bit have been used with an additional bit (HG) for setting the gain. In low-gain (LG) configuration, one tenth of the dynamic range is covered with a fine resolution, whereas in high-gain (HG) mode, the full output dynamic range is covered with a lower resolution. Since a 10:1 current mirror is used between the periphery and the pixels, the LSB of the Current Steering DAC is 100 nA and 1 μA, respectively in LG and HG. The 8 groups of current sources are switched toward the output node or a dummy load according to the 8-bit input code. Figure 2.16 gives an overview about the architecture of the block. An external 1 μA reference current, is either 1:1 or 10:1 mirrored according to the HG bit configuration, providing the current reference for the 8-bit Current Steering DAC. The output current of the DAC is mirrored into each pixel of the matrix with a 10:1 factor thus achieving the proper dynamic range set by the requirements. Moreover, the same output is fed to a variable resistance

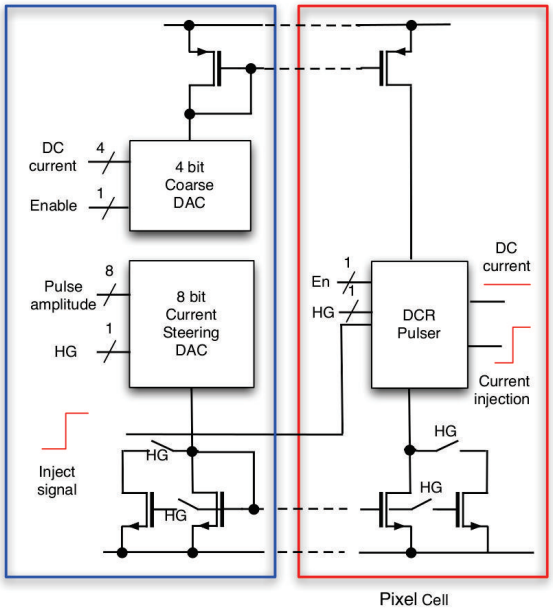

Figure 2.14: Architecture of the injection circuit, with the 8-bit current steering DAC and the 4-bit coarse current DAC located in the periphery of the chip, and the current pulser inside each pixel of the matrix.

controlled by the 8-bit input code of the DAC, in such a way that a constant reference voltage of 100 mV, to be provided into each pixel, is achieved.

As depicted in Figure 2.17, the current injection pulser located inside each pixel is based on a first branch where the Current Steering DAC output is first mirrored with a 10:1 factor, in such a way to achieve the current to be injected in the range of 10 nA ÷ 2.5 μA and 100 nA ÷ 25μA, respectively for the LG and HG configurations. The current is then mirrored once again into a steering branch controlled by the pixel-level enable bit and sent either to the drain of the input cascode or to a dummy device. According to the selected gain, the current mirror stages, located in both the periphery and in the pixel, may switch on an additional transistor, as depicted in Figure 2.18.

In the DSSC chip, the power lines are distributed by rows. If a separate ground line is assumed for the current mirror of the injection circuit, it can be demonstrated that the voltage drop over such line can be up to 30 mV for the farthest pixel [22], resulting in a sistematic mismatch of the mirrored current due to a variation of the gate-to-source voltage (V_{GS}) of M_1. In the proposed injection circuit, this issue has been overcome by means of the voltage drop compensation circuit [20] [22], shown in Figure 2.19. The reference voltage, generated in the periphery by means of the variable resistor technique presented in Figure 2.16, is used to set the source of M_1 to a constant potential, thus avoiding any systematic mismatch due to the power lines. An additional

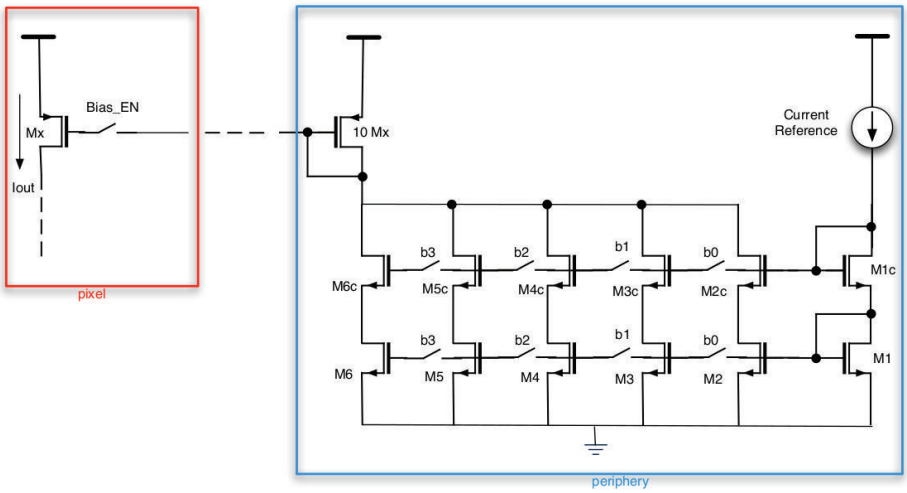

Figure 2.15: Architecture of the 4-bit Coarse Current DAC.

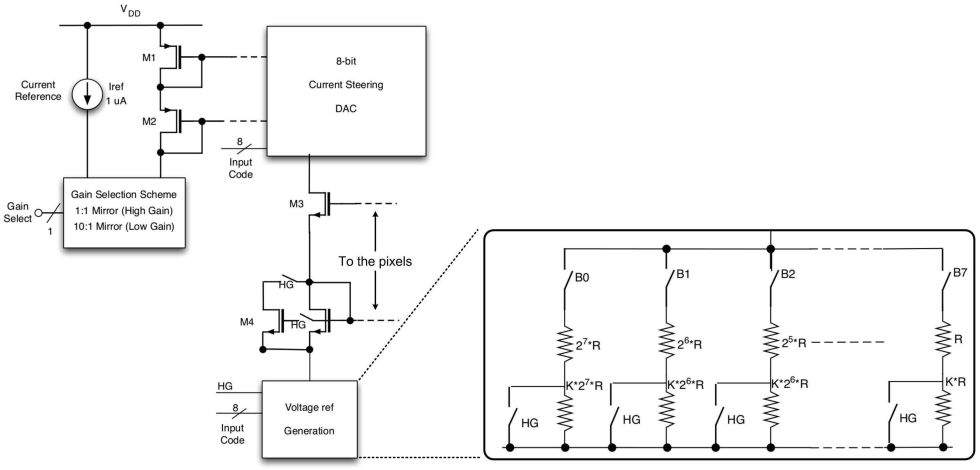

Figure 2.16: block diagram of the 8-bit Current Steering DAC.

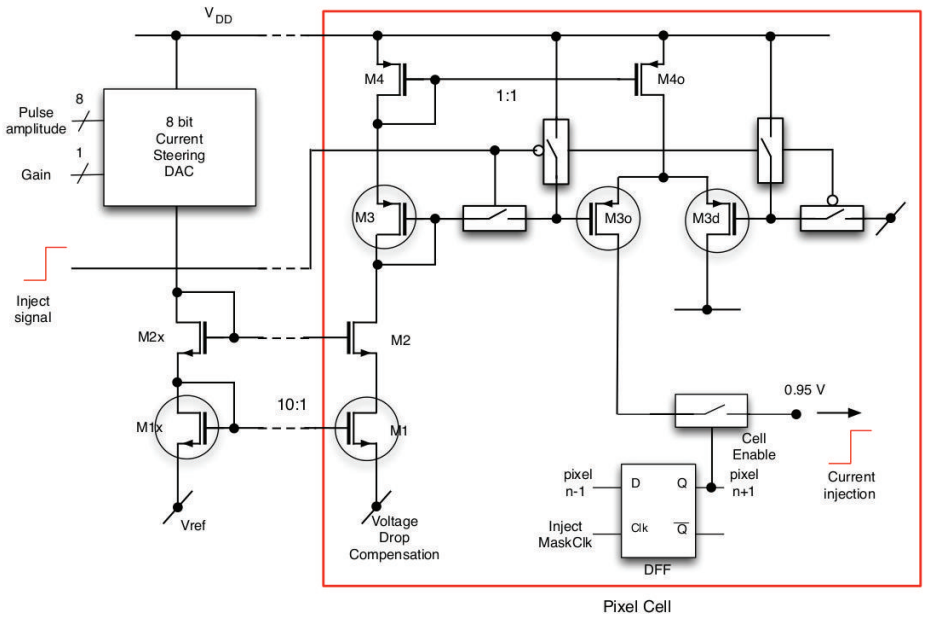

Figure 2.17: Architecture of the current pulser located inside each pixel of the matrix.

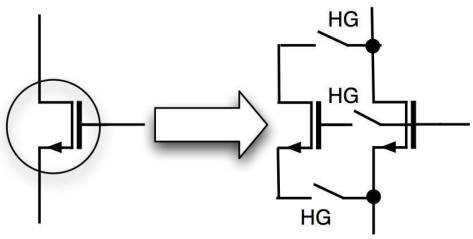

Figure 2.18: Architecture of single cell, controlled by the gain selection bit, used to mirror the current.

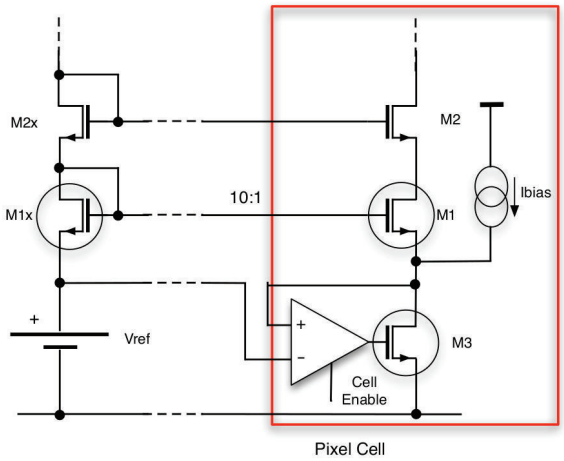

Figure 2.19: Conceptual schematic of the voltage drop compensation circuit integrated inside each pixel.

current source is used to bias the circuit in LG configuration. A detailed description about the performance of the circuit as a stand-alone block can be found in [20].

2.2.3 The MM3 test system

The test system used to perform the measurements on the MM3 matrix is depicted in Figure 2.20. It consists of the following blocks:

- An FPGA board, hosting the FPGA for the control of the ASIC as well as for data acquisition. The board is interfaced with a computer by means of an FTDI USB-RS232 data link.

- A power regulator board, connected on-top of the FPGA board and providing the digital, analog and ADC supply voltages.

- A main board, integrating all the electronics needed for applying signals at the injection bus of the ASIC as well as for buffering the clocks from the FPGA board.

- An ASIC carrier, hosting the MM3 ASIC, connected on-top of the Main board.

- A software for data acquisition and analysis, executed on the computer connected to the FPGA board and based on the `C++` programming language and the CERN ROOT data analysis framework.

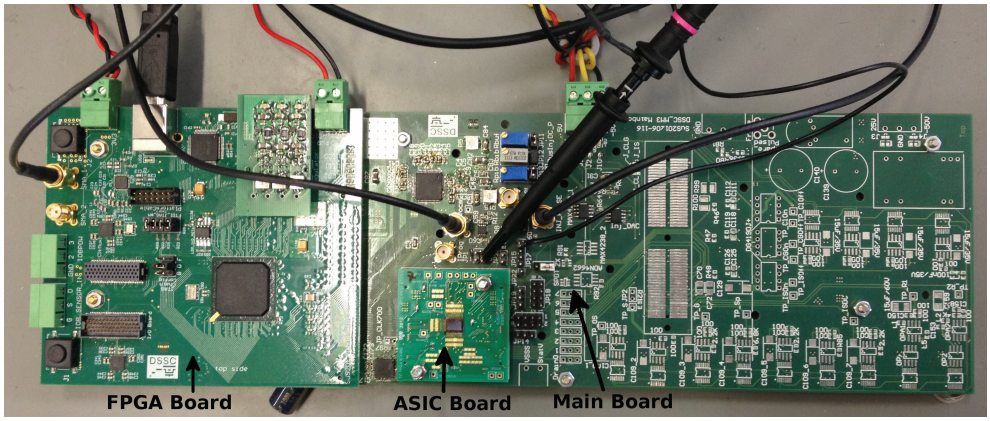

Figure 2.20: Picture of the test system used for the characterization of the MM3 chip.

2.2.4 Performance of the MM3 injection circuit

The characterization activity, while mainly focusing on the injection circuit described in Subsection 2.2.2, was also concerned with other blocks of the MM3 prototype. In particular, an assessment of the output dynamic range and linearity for all the pixels of one chip has been performed. Since in the final DSSC chip the GCC will be shared by all the pixels of the matrix, the measurements have been carried out on the right-hand side 16 $\times$ 4 matrix integrated in the chip.

The input-output characteristic of the readout channel can be described by the following equation:

$$ADC_{out} = i_{IN} \cdot \frac{\tau}{C_f} \cdot g_{ADC} + o_{ADC} \tag{2.1}$$

where ADC_{out} is the ADC output code, i_{IN} is the current at the input of the front-end during the signal integration phase, τ is the duration of both the baseline and the signal integration phases, g_{ADC} is the gain of the ADC and o_{ADC} is the offset of the ADC. In order to evaluated the injection circuit output current, i_{INJ}, which corresponds to the current at the input of the front-end during the signal integration, i_{IN}, both the FCF feedback capacitances and the ADC characteristic for each pixel have first been measured.

The gain of the ADC has been measured by means of the commercial 16-bit DAC (MAX544) integrated on the Main board. The output voltage of the DAC has been applied to the input of the ADC through the `IN_Injectbus`, by enabling the bit number 14 of the control register of each pixel. Figure 2.21 and Figure 2.22 depict an example of the ADC output and the related Differential Non Linearity (DNL), for pixel number 7 and with a particular configuration of the ramp current. The gain and the DNL of the ADCs integrated in the right-hand side matrix of the MM3 chip have been measured with the standard configuration of both the ramp current setting (code of 32 in decimal notation, control register bit 17 enabled) and with no time delay in the ramp current control. The results are shown in Figure 2.23 and Figure 2.24, where the gain and the DNL are reported in a matrix fashion as the pixel are laid out in the chip. As it can be noticed, there is an increase of the gain, as well as a

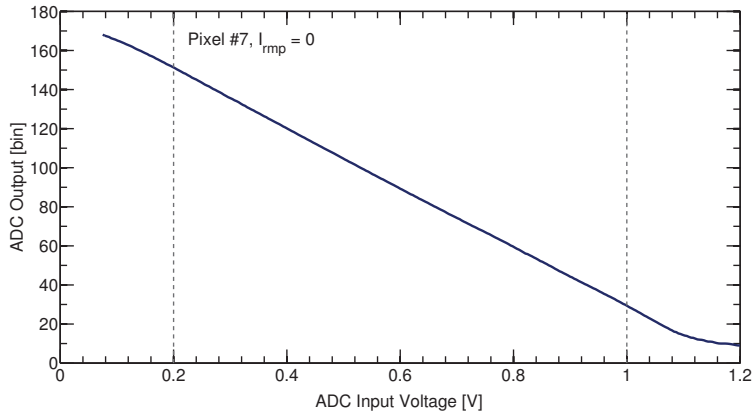

Figure 2.21: ADC output characteristic for pixel number 7.

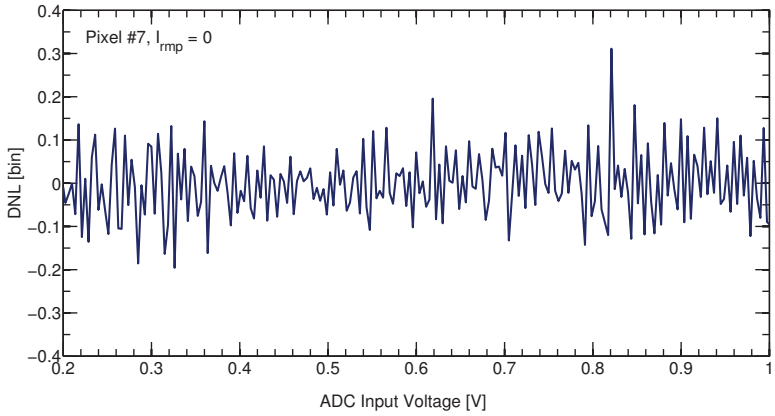

Figure 2.22: Trend of the DNL for pixel 7.

worsening of the maximum DNL, as the distance of the pixel from the power supply entrance, in proximity of pixel number 127, increases. This is mainly due to a voltage drop across the power line, with an estimated value of 50 mV between two pixels at the two ends of the line.

The feedback capacitances of the FCF are arranged in a binary weighted fashion and are based on a 4-bit architecture, resulting in 4 feedback capacitances, one with twice the value of the previous one. Once the ADC gain of each pixel was measured, the values of the feedback capacitances of the FCF

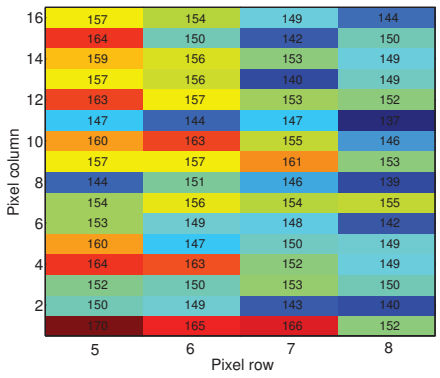

Figure 2.23: Gain of the measured ADCs, expressed in $^{ADC\,count}/_{V}$.

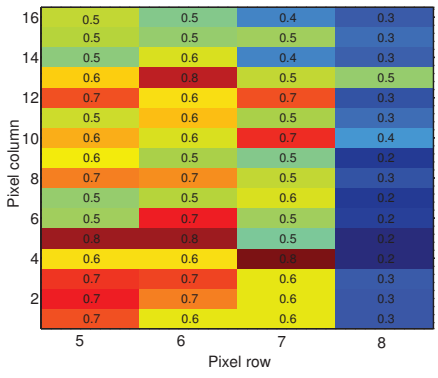

Figure 2.24: Maximum DNL of the measured ADCs, expressed in LSB.

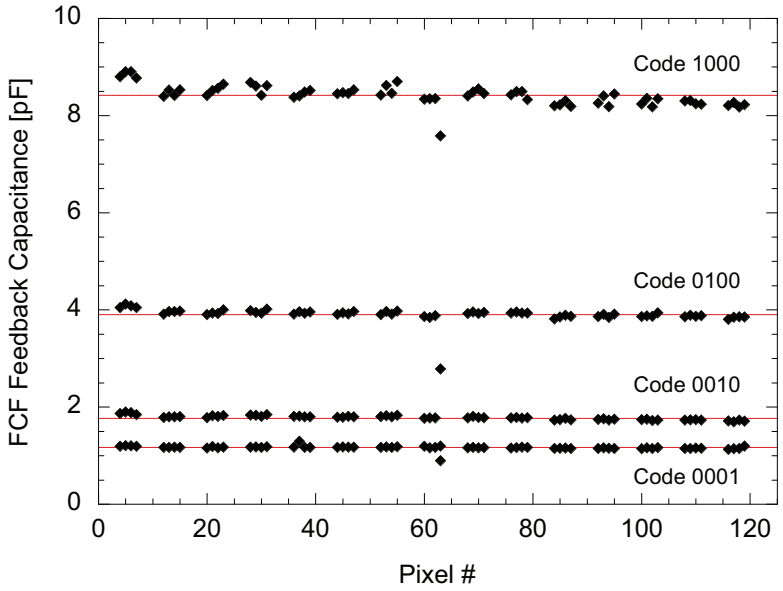

Figure 2.25: Measured values of the FCF feedback capacitances for the pixels of the right-hand side matrix.

have been estimated starting from the following equation:

$$C_f = \frac{i_{IN}}{(ADC_{out} - o_{ADC})}\tau \cdot g_{ADC} \tag{2.2}$$

In order to get rid of the ADC offset as well as to avoid the need for an accurate measurement of the input current absolute value, a differential measurement with increasing steps of the input current has been performed, thus leading to the following equation:

$$C_f = \frac{\Delta i_{IN}}{\Delta ADC_{out}}\tau \cdot g_{ADC} \tag{2.3}$$

The input current, achieved with an external pulse generator (Tektronics AFG3101) and a series 100 kΩ resistor integrated on the Main board, has been fed through the `IN_Injectbus`, by enabling the bit number 11 of the pixel control register. The integration time, τ, has been set to 100 ns. Figure 2.25 shows the 4 values of feedback capacitances achieved for the pixels of the right-hand side matrix, whereas a comparison with the design values is reported in Table 2.3. The low value achieved for pixel number 63, especially with the bits number 2,3 and 4, can be ascribed to the monitor bus at the output of the filtering stage.

Code	**Value** [pF]	
	Design	Measurement
1	1	1.14 ±0.10
2	1.5	1.74 ±0.04
4	3.4	3.84 ±0.06
8	7.9	8.28 ±0.2

Table 2.3: Comparison of the values of the FCF feedback capacitances from design and measurement.

Once both the ADC gains and the values of the FCF feedback capacitances are known, the current provided by the injection circuit can be computed according to the following equation:

$$i_{IN} = \frac{(ADC_{out} - o_{ADC})}{g_{ADC}} \cdot \frac{C_f}{\tau} \tag{2.4}$$

The characterization of the injection circuit has been performed by measuring the ADC output with the standard configuration of both the ramp current setting (code of 32 in decimal notation, control register bit 17 enabled), with an integration time of 180 ns, with no time delay in the ramp current control and for all the 256 input codes of the Current Steering DAC. In order to cover the overall output dynamic range of the ADC, two different FCF feedback capacitances have been used for the LG and HG configurations of the circuit. As an example, the output characteristic, the DNL and the INL, as a function of the 8-bit Current Steering DAC input code, for pixel number 7, are shown in Figure 2.26, Figure 2.27 and Figure 2.28, respectively. The LSB and the dynamic range for all the pixels are depicted in Figure 2.29, whereas the overall performances are summarized in Table 2.4. As it can be noticed, the circuit features a maximum DNL which is lower than 1 LSB, thus ensuring a monotinic transfer function in both the gain modes. The output dynamic range is well covered in HG configuration, with an average LSB current of about 90 nA. However, the dynamic range in LG operation is quite reduced, with a LSB current of 7 nA. Moreover, the circuit features a quite high LSB dispersion in both the configurations.

Parameter	Low Gain	High Gain
I_{MIN} [nA]	6.1 ± 0.9	87.2 ± 5.0
I_{MAX} [μA]	1.8 ± 0.2	23.0 ± 1.2
I_{LSB} [nA]	6.9 ± 0.8	90.1 ± 4.7
$\sigma_{I_{LSB}}/\overline{I_{LSB}}$ [%]	12	5
DNL_{MAX} [I_{LSB}]	0.3 ± 0.1	0.9 ± 0.4
INL_{MAX} [I_{LSB}]	2.1 ± 1.0	1.6 ± 0.7

Table 2.4: Overall performance of the injection circuit.

2.3 Optimization of the injection circuit

On the basis of the results achieved from the MM3 chip characterization, an optimization activity has been carried out on the injection circuit. As described in the following subsections, design changes aimed to reduce the LSB dispersion, increase the output dynamic range in LG mode and simplify the circuit architecture. The new version of the circuit has been integrated in a prototype of the DSSC chip based on 64 × 64 pixels, the F1 matrix.

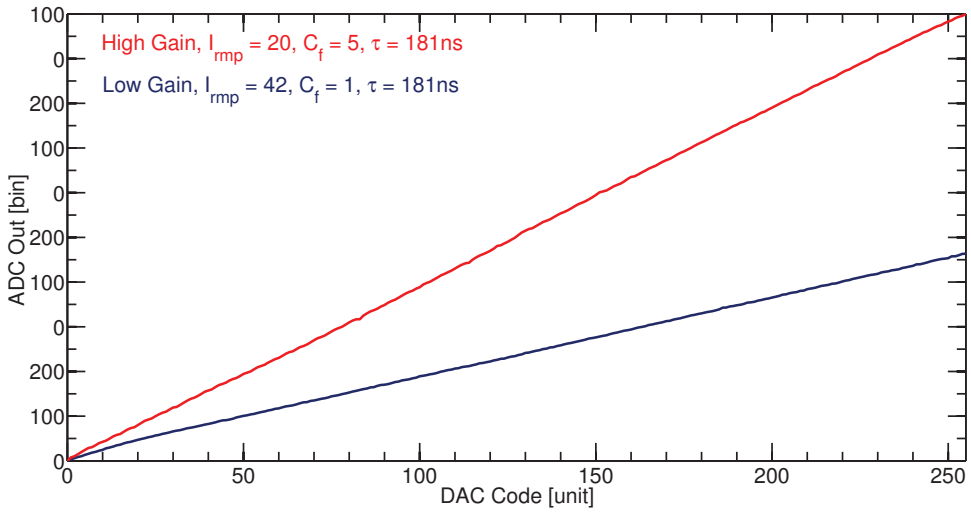

Figure 2.26: Injection circuit characteristic for pixel number 7.

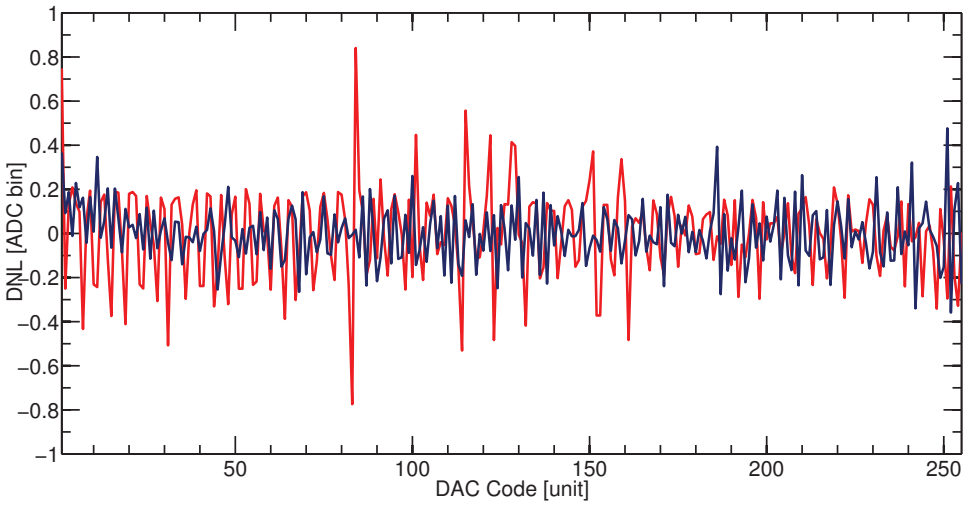

Figure 2.27: DNL for pixel number 7.

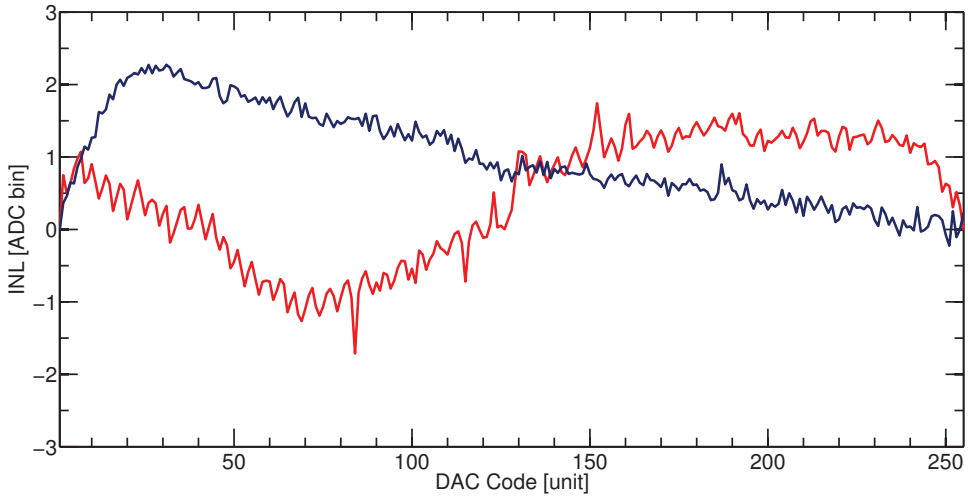

Figure 2.28: INL for pixel number 7.

2.3.1 Current reference for the 8-bit periphery DAC

In the MM3 matrix, the reference current for both the 8-bit Current Steering DAC and the 4-bit coarse DAC, located in the periphery, is obtained starting from a 1 μA current, provided externally from the Main board by means of a PCB resistor, as shown in Figure 2.30. The current is then mirrored in the

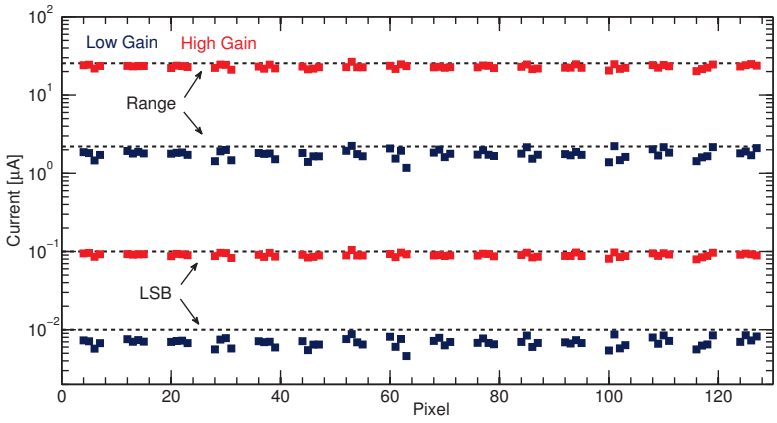

Figure 2.29: LSB and output dynamic range of the injection circuit for the pixels in the right-hand side matrix.

8-bit Current Steering DAC with either a 1:1 or a 10:1 factor for the LG and HG configurations, respectively, whereas it is mirrored with a 1:1 factor in the 4-bit Coarse Current DAC. Since in the F1 chip all the reference currents will be achieved on-chip, starting from a 6 μA current reference, a 6:1 current mirror, providing the current for both the DACs, has been integrated, as depicted in Figure 2.31. In order to reduce the complexity of the periphery architecture and decrease the number of mismatch sources, the gain selection has been completely removed from the periphery. This results in a simpler architecture of the input current mirror, which is not controlled by the gain selection bit anymore, as depicted in Figure 2.31. The 6:1 mirroring stage consists of a cascode current mirror. In order to reduce the current mismatch,

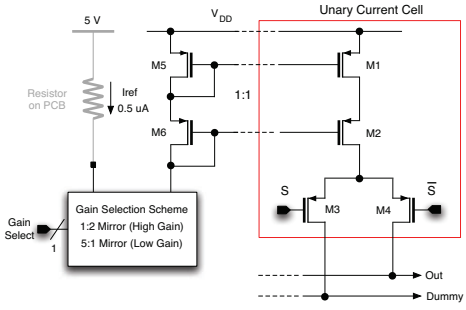

Figure 2.30: Reference current mirror in the MM3 matrix.

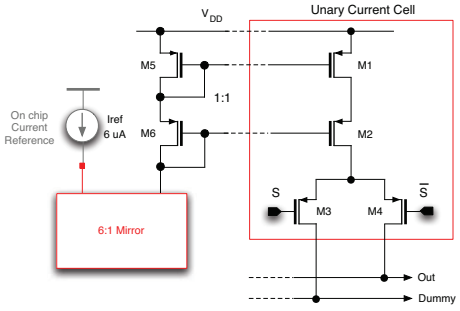

Figure 2.31: 1 μA reference current mirror in the F1 matrix.

dummy transistors have been introduced and the following aspect ratios have been used:

- **Cascode devices:** $^{120}/_{0.2}$ and $^{20}/_{0.2}$, respectively for the left-hand side and right-hand side branches.
- **Mirror devices:** $^{240}/_{2}$ and $^{40}/_{2}$, respectively for the left-hand side and right-hand side branches.

With such improvements, the normalized standard deviation of the output current from Monte Carlo simulation is about 1.7%.

2.3.2 Voltage drop compensation circuit reference

As shown in Figure 2.32, the 100 mV reference voltage for the voltage drop compensation circuit, employed in the MM3 chip, is obtained by feeding the current at the output of the 8-bit Current Steering DAC into a variable resistor with a value controlled by the same 8-bit input code of the DAC:

$$V_{ref} = I_{DAC} \cdot R_{ref} \tag{2.5}$$

where:

$$I_{DAC} = k \cdot I_{DAC,LSB} \quad R_{DAC} = \frac{R_0}{k} \tag{2.6}$$

and $0 \leq k \leq 255$. This quite complicated logic occupies lot of the periphery area and results in a reference voltage which is not constant in the overall input

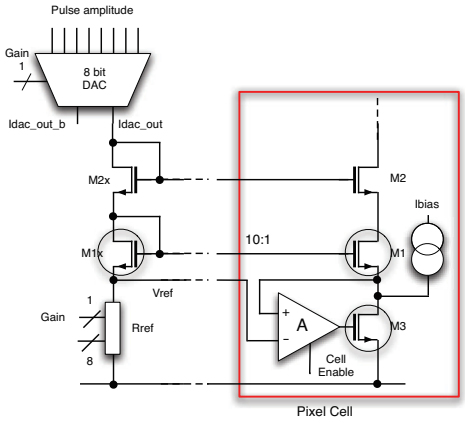

Figure 2.32: Voltage drop compensation circuit in the MM3 matrix.

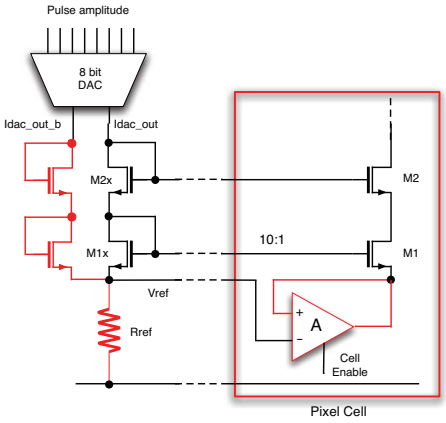

Figure 2.33: Voltage drop compensation circuit in the F1 matrix.

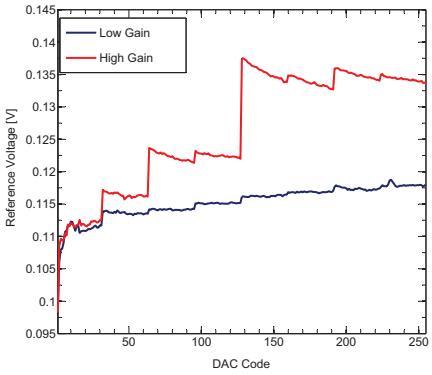

Figure 2.34: Reference voltage measured in the MM3 injection circuit as a function of the 8-bit input code.

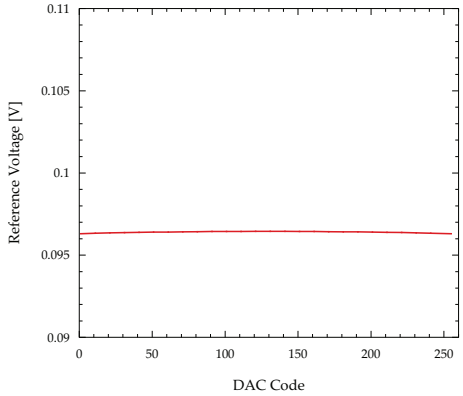

Figure 2.35: Reference voltage simulated in the F1 injection circuit as a function of the 8-bit input code.

range, with more than 30 mV of variation between 0 and 255 as depicted in 2.34. The solution adopted in the F1 version of the circuit, shown in Figure 2.33, takes advantage of the complementary current which, along with the desired output current, is always available at the output of the Current Steering DAC. The sum of such currents is always constant and has been exploited to provide a voltage reference throughout a fixed resistor:

$$V_{ref} = \left(I_{DAC} + \overline{I_{DAC}}\right) \cdot R_{ref} \tag{2.7}$$

where $\left(I_{DAC} + \overline{I_{DAC}}\right)$ is 255 μA and R_{ref} is a 400 Ω resistor, achieved with a standard voltage NMOS with an aspect ratio $^{W}/_{L}$ of $^{8.6}/_{1}$ biased in triode region ($V_{GS} = 1.2$ V). With such a solution, the reference voltage is almost independent of the DAC input code, as shown in Figure 2.35, and the mismatch, evaluated for 100 Monte Carlo simulations with a DAC input code of 128, is lower than the 2% of the average voltage (96 mV).

2.3.3 Periphery-to-pixel mirror

In the MM3 matrix, the 8-bit Current Steering DAC output is mirrored inside each pixel according to the schematic in Figure 2.32, with the dimensions of $M_{1,x}$ and M_1 adjusted depending on the gain configuration in order to cope with the output current range. Since in the F1 matrix the 8-bit Current Steering DAC output does not depend on the gain configuration anymore, $M_{1,x}$ and M_1 aspect ratios are fixed and are the same as the ones used in HG configuration in the MM3 version ($^{W}/_{L} = {}^{60}/_{4}$).

2.3.4 In pixel amplifier

The voltage drop compensation circuit used in the MM3 matrix, depicted in Figure 2.32, is based on a simple differential stage and an output transistor, acting as the second stage. This solution presents two main drawbacks:

- **Systematic offset:** the current flowing through M_3 is not constant, since it changes according to the Current Steering DAC input code and therefore the signal to be injected, leading to a systematic mismatch in the amplifier. Moreover, the high output impedance and the limited DC gain of the stage represent two systematic offset sources.
- **Random offset:** The amplifier bias current is achieved in-pixel with a transistor featuring small dimensions, therefore leading to a high channel-to-channel mismatch, resulting in a wide variation of the offset voltage.

Moreover, in the F1 matrix, the amplifier bias current should be generated from the same 6 μA reference used in the periphery. Taking this requirements and the above limitations, a new version of the in-pixel amplifier, depicted in Figure 2.36, has been designed:

- A two stage architecture, based on a differential input stage and an additional inverter with active load, has been adopted to improve the DC gain.

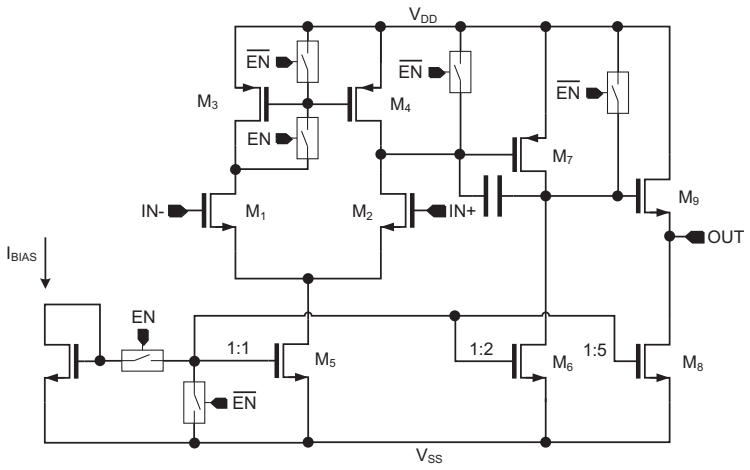

Figure 2.36: Simplified schematic of the F1 matrix in-pixel amplifier for the voltage drop compensation.

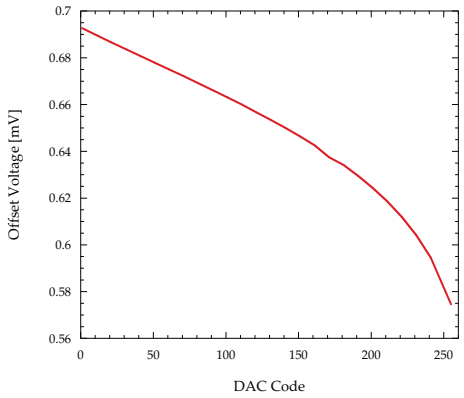

Figure 2.37: F1 in-pixel amplifier offset voltage as a function of the 8-bit input code.

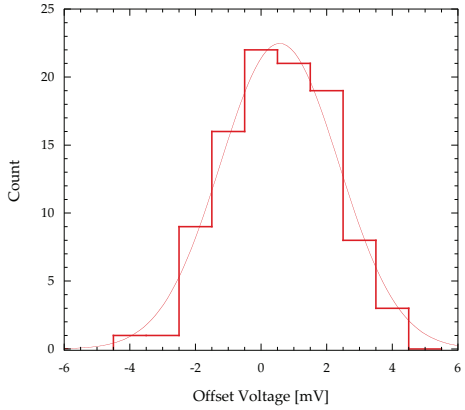

Figure 2.38: Distribution of the F1 in-pixel amplifier offset voltage from Monte Carlo simulations.

- Dimensions of devices in the two gain stages have been chosen in order to cancel the systematic offset:

$$\frac{W_{3,4}}{L_{3,4}} \cdot \frac{W_6}{L_6} = \frac{1}{2} \cdot \frac{W_5}{L_5} \cdot \frac{W_7}{L_7} \tag{2.8}$$

- An additional source follower output stage has been included, to sink the current from the in-pixel mirror without introducing a systematic offset and to reduce the output impedance.
- A long channel and a large gate area have been used for current mirrors, in order to reduce random offsets.
- The dimensions of M_1 and M_2 have been chosen in such a way that they are operated in the weak-inversion region, in order to reduce the contribution from current mirror active load mismatch thanks to the high $^{gm}/_{I_D}$ ratio.

With such improvements the offset voltage of the amplifier is now almost independent of the DAC code, as shown in Figure 2.37, and features a random offset variation of about 2 mV, as depicted in Figure 2.38.

2.3.5 In pixel PMOS mirror

In the MM3 matrix, the current mirrored inside the pixel is then mirrored once again with a 1:1 factor, in order to obtain the proper polarity of the

signal to be injected. According to the schematic of Figure 2.17, the injection control bit, `InjectSignal`, switches the mirrored current from the right-hand side branch of the differential stage, terminating on a dummy device, to the left-hand side one, connected to the drain of the input cascode and to the virtual ground of the front-end amplifier. To comply with the wide range of current to be injected, the switching architecture proposed in Figure 2.18 has been used for transistors M_3, $M_{3,o}$ and $M_{3,d}$. The output current in F1 matrix

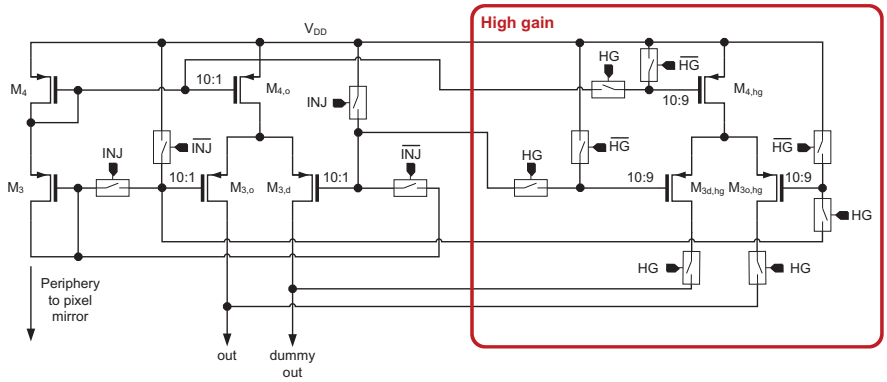

Figure 2.39: Simplified schematic of the F1 matrix in-pixel current pulser.

is provided according to the schematic in Figure 2.39. The new circuit is based on two PMOS current mirrors with 10:1 and 10:9 factors for the LG and HG configurations, respectively. The 10:1 mirror is always connected to either the output node or the dummy output, while the other one is enabled in HG mode only.

2.3.6 Performance of the F1 injection circuit

The performance of both the F1 and MM3 injection circuits, evaluated by means of schematic simulations, have been compared in terms of minimum current, LSB current, dynamic range, maximum DNL and maximum INL. The output characteristics of the circuits as a function of the 8-bit Current Steering DAC input code are depicted in Figure 2.40 and Figure 2.41, respectively for the LG and HG configurations. As it can be noticed, the output dynamic range of the circuit in LG mode has been increased from 2.2 μA (1.8 μA from the MM3 measurements) to 2.5 μA, while it remains sufficiently high to test the front-end linear region in HG configuration. Concerning the mismatch effects on the both the versions of the circuit, as depicted in the Monte Carlo simulation results of Figure 2.42 and Figure 2.43, the dispersion of the LSB

current has been reduced by a factor of 2, thus proving the effectiveness of the new design. The same conclusion can be drawn from the overall performance of the circuits, summarized in Table 2.5.

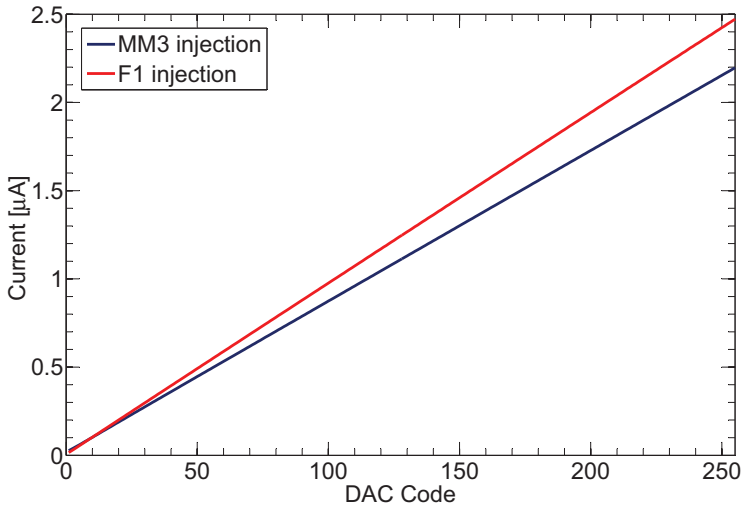

Figure 2.40: Output characteristics of the MM3 and F1 injection circuits in LG mode.

Parameter	**High Gain**	
	MM3	F1
I_{LSB} [nA]	88.6 ± 9.0	91.0 ± 4.2
$\sigma_{I_{LSB}}/\overline{I_{LSB}}$ [%]	10	5
I_{MIN} [nA]	113.5 ± 30.0	115.5 ± 6.9
$\sigma_{I_{MIN}}/\overline{I_{MIN}}$ [%]	26	6
I_{MAX} [μA]	22.6 ± 2.3	23.2 ± 1.1
DNL_{MAX} [LSB]	0.11	0.05
INL_{MAX} [LSB]	0.1	0.4

Table 2.5: Performance of the MM3 and F1 injection circuits in HG mode.

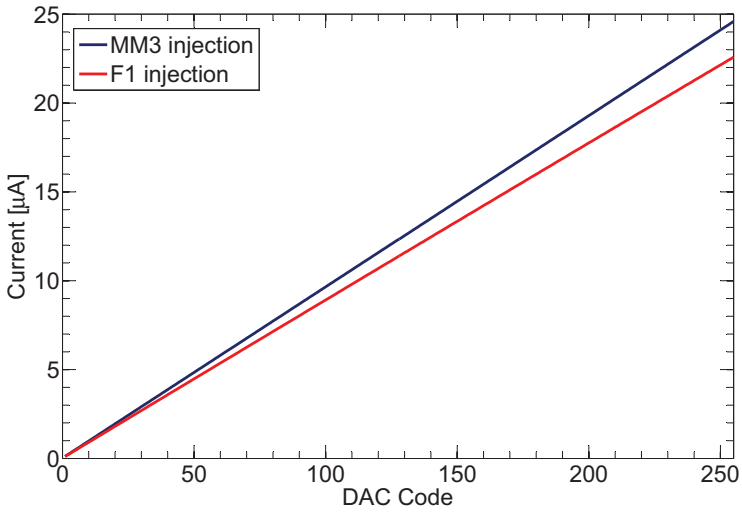

Figure 2.41: Output characteristics of the MM3 and F1 injection circuits in HG mode.

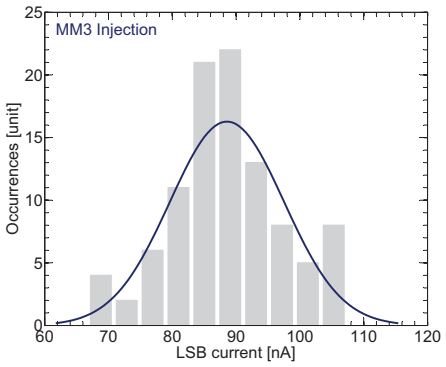

Figure 2.42: LSB distribution in HG mode for the MM3 injection circuit.

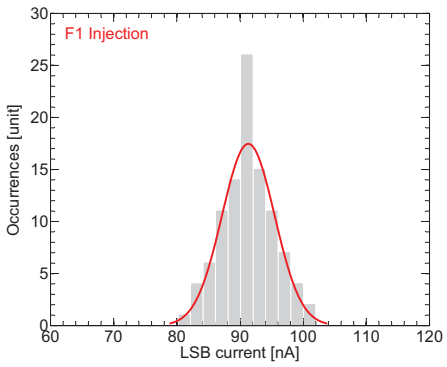

Figure 2.43: LSB distribution in HG mode for the F1 injection circuit.

2.4 DSSC bare modules test activity

In the framework of the DSSC collaboration, a validation activity, aimed to check the proper operation of the single ladders, will be performed during the assembly of the full Megapixel detector. In particular, a series of tests is foreseen on the bare module systems, each one assembled with 2 × 4 F1

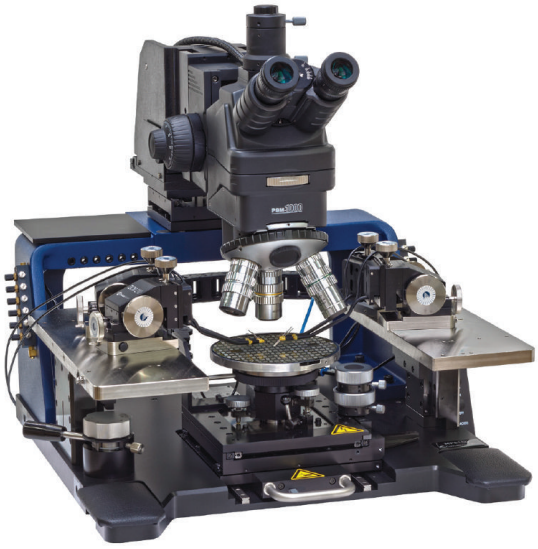

Figure 2.44: Picture of the probe station which will be used for the test of the bare modules.

chips bump bonded to a monolithic sensor of 128 × 256 DSSC pixels. In this section, a brief description of the activity carried out to set up the test system for the bare modules is given.

The tests on the bare modules include the validation of each ASIC, with standard measurements on the single microelectronic building blocks, the measurement of the I/V characteristic of the sensor, and an optical inspection of the sample. The test setup will include a 150 mm probe station (EPS150FA provided by Technoprobe), depicted in Figure 2.44, a probe card holder, a 3 Megapixel digital videocamera and a vibration isolation table. Figure 2.45 shows how the ASICs are arranged in one bare module. Each ASIC will be contacted by means of 80 wire bonding pads, with an area of 130 × 256 μm^2 each and a pitch of 150 μm. 10 contacts in the middle of the row will be dedicated to the sensor voltages (e.g. biasing, clear). The bare module will be hosted in a storage container, shown in Figure 2.46, which will be vacuum clamped to the chuck of the probe station. Each ASIC of the bare module will be clamped with a holder mechanism, as depicted in Figure 2.47. The pads on the ASIC will be contacted according to the diagrams of Figure 2.48 and Figure 2.49, with 80 tungsten-rhenium probe tips descending for about 3.65 mm from the probe card. The contact with each ASIC will be achieved

by finely shifting the chuck, along the x and y axes. The probe card which has been designed for the bare module test activity is depicted in the 3D sketch of Figure 2.50. It features an array of 80 vias, with a diameter of 0.9 mm and a through hole diameter of 0.5 mm, which will be used for the connection of the 80 tips to the ASIC through a rectangular aperture in the middle of the PCB (see Figure 2.48). The probe card will be connected, by means of a high speed edge card connector, to the same FPGA board used for the characterization of the MM3 chip prototype. Moreover, the following circuitry has been integrated on-board:

- A buffer for the 700 MHz clock.
- A LVDS buffer.
- Test points for the JTAG and the power supply.
- A 14-bit DAC, with the output connected to the `IN_Injectbus`, for ADC testing purpose.
- A SMA connector, in order to test the front-end through the `IN_Injectbus` by means of external intruments (e.g. pulse generator).

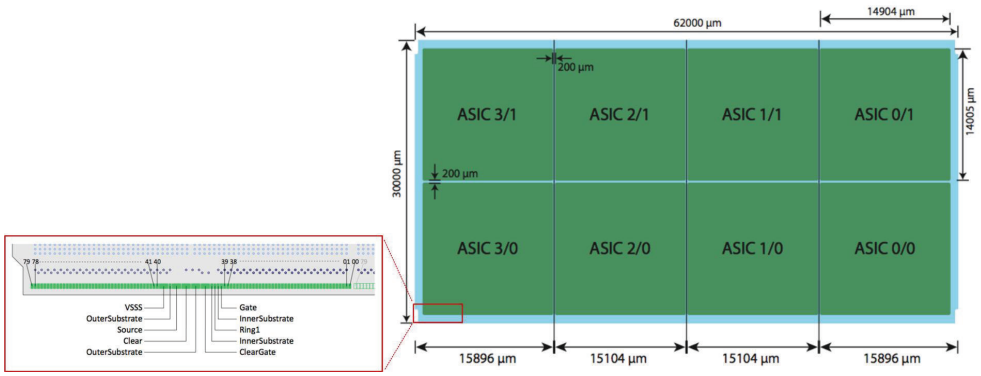

Figure 2.45: Block diagram of a bare module, with the row of 80 contacts on the ASIC.

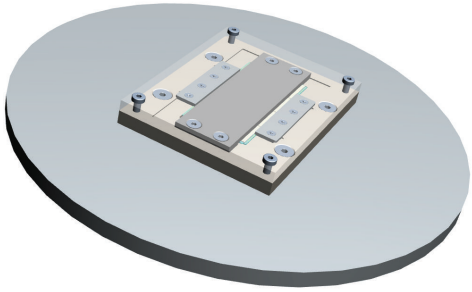

Figure 2.46: Storage container for a bare module.

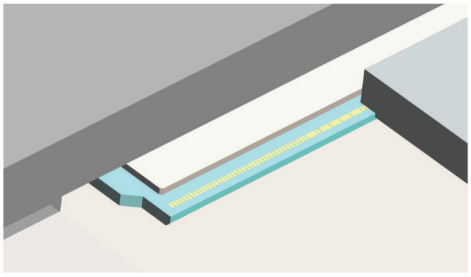

Figure 2.47: Clamping of the bare module within the storage container.

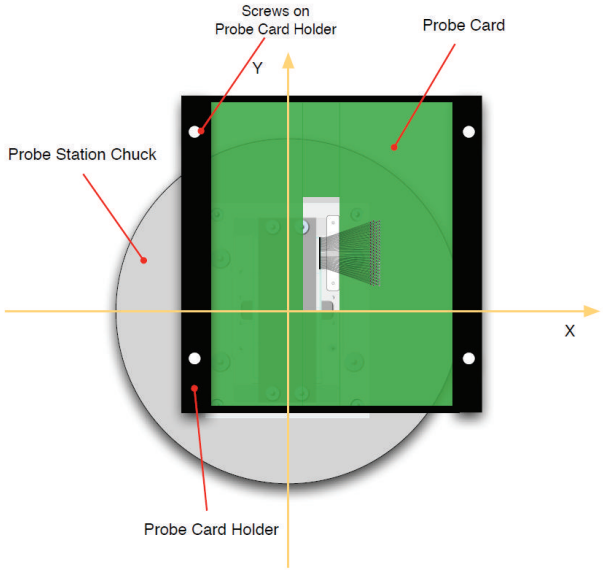

Figure 2.48: Connection of the ASIC to the probe-card with an orientation along the y-axis of the probe station.

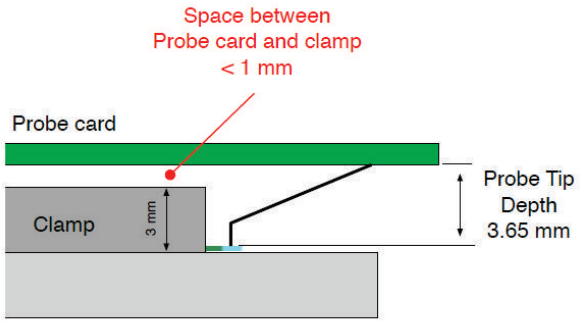

Figure 2.49: Side view of the connection between the ASIC and the probe-card.

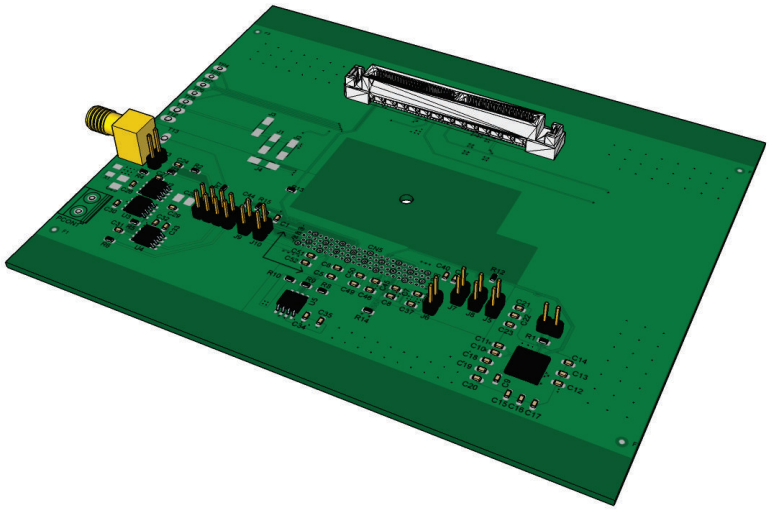

Figure 2.50: 3D sketch of the probe card designed for the bare modules test activity.

Chapter 3

Analog front-end for X-ray imagers

This chapter is dedicated to the activity carried out in the framework of the PixFEL project, a research program aiming to advance the state-of-the-art in 2D imagers for X-ray FEL. In Section 3.1, an overview about the project is given, with a particular focus about the specfications and the long term goal. Section 3.2 concerns the design of the microelectronic building blocks for the analog front-end of the readout channel for the PixFEL detector. Finally, the measurement results from the characterization activity of the first prototype chips, will be presented in Section 3.3.

3.1 Overview of the PixFEL project

The PixFEL project is conceived as the first stage of a research program aiming to advance the state-of-the-art in X-ray imaging instrumentation for applications at FEL facilities [23]. The project, funded by Istituto Nazionale di Fisica Nucleare (INFN) from early 2014, is a three years collaboration activity between University of Pavia, University of Bergamo, University of Pisa, University of Trento, Trento Institute for Fundamental Physics and Applications (TIFPA) and INFN. The groups involved in the research program are exploring cutting-edge solutions in manufacturing technologies and detector readout architectures, in order to lay the foundations for the future fabrication of a complete system to be used in the experiments at X-ray free electron laser facilities. This imager will comply with the very demanding specifications of the European XFEL, operating in burst mode with a frequency up to 4.5 MHz, and will retain, at the same time, the necessary flexibility to be

compatible with the continuous operation mode typical of other FEL facilities:

- **Pixel shape and dimensions:** square, with about 100 μm pitch.
- **Input signal dynamic range:** from 1 to 10^4 photons, with an energy from 1 keV to 10 keV.
- **Resolution:** single photon resolution for input signals smaller than 20 photons, a resolution much better than the Poisson limit for a larger number of input photons.
- **In-pixel analog-to-digital conversion:** 10 bit resolution ($\geq$ 9 bit effective resolution).
- **Readout operation:** burst mode up to 4.5 MHz with 1% duty cycle (as in the case of the European XFEL), or continuous mode.
- **In-pixel memory:** 1 kframe/pixel, which can be exploited whenever the pulse rate exceeds the chip readout rate.
- **Dead area of the detector:** $\leq$5%.
- **Radiation hardness:** tolerance to 1 GGy for the sensitive layer, tolerance to 10 MGy for the readout electronics.

In order to pursue such a goal, the PixFEL project is focusing on the following topics:

- Enabling technologies potentially leading to a 4-side buttable elementary chip and to a zero or almost zero dead-area detector.
- Microelectronic building blocks to be included in the front-end chip for a 2D X-ray camera.
- Investigation of the architectures for high performance in-pixel storage and readout of the data.

The sensing layer will be based on a fully depleted p-on-n silicon pixel sensor, which can guarantee remarkably high quantum efficiency in hard X-ray conversion if a suitable thickness is used. This choice lends itself to the design of an X-ray imager with excellent sensitivity also in the high energy range of the signals at FELs, of the order of 10 keV. On the other hand, noise performance of the system sets a limit for the low energy end to about 1 keV or slightly below. The front-end chip will be fabricated in a 65 nm CMOS technology by TSMC, in order to embed the required amount of intelligence in the target pitch of about 100 μm.

3.1.1 Enabling technologies

Cutting-edge microelectronic fabrication technologies are the key for advancing the state-of-the-art in 2D imager for X-ray FEL applications. An overview of such technologies is given in Figure 3.1, showing a matrix (part of a more complex and larger area detection system) of 9 four-side buttable blocks, each consisting of a multilayer device resulting from the vertical interconnection of the sensor to a dual-tier front-end chip. The chip, in turn, is bump bonded to a hybrid board. In the following, a description of a few key technologies, enabling the vertical integration of a four-side buttable chip, is presented.

Active edge pixel sensors

One interesting option to minimize the dead area in the sensing layer is represented by active edge pixel sensors. This technology was proposed as a possible solution to minimize the gap between the active area and the edge of the detector [24] [25]. In an active edge sensor, deep trenches are etched around the active area by Deep Reactive Ion Etching (DRIE) and then heavily doped to act as wall (ohmic) electrodes. A support wafer is needed to hold different sensors together, once the trenches have been etched, and has to be removed at the end of the process. With this approach, planar detectors with an insensitive region of about 5 μm from the physical edge were fabricated and successfully tested. One of the key points of the technology lies in the

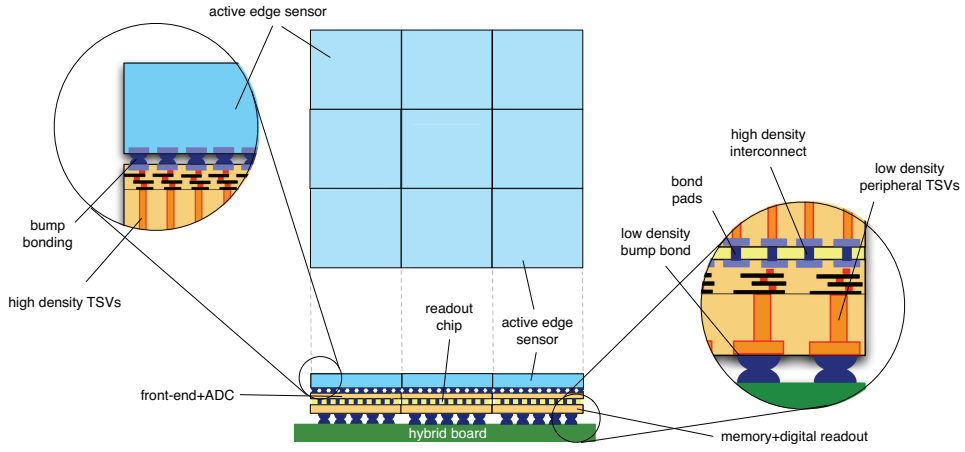

Figure 3.1: Conceptual view of a 3 × 3 detector matrix made of 9 four-side buttable elementary blocks.

capability of achieving a high aspect ratio ($\geq$ 20:1) in the trench excavation step. Typical trench depth is of the order of 200 μm. To achieve a quantum efficiency larger than 90% at 10 keV, a thickness in excess of 400 μm is needed. Therefore, trench etching has to be optimized together with the steps mentioned above in view of using an active edge sensor in an X-ray camera. Moreover, the following topics have to be investigated:

- **Plasma effect:** the so called plasma effect, takes place in silicon sensors when a large amount of energy is released in a relatively small volume, leading to extremely high densities of holes and electrons which determine a change in the electric field lines inside the detector and an increase in the collection time and distance [26].

- **Radiation hardness:** as already mentioned, the total amount of ionizing radiation dose expected for a 2D X-ray imager is in the order of 1 Grad. Toward the development of a thick, 100 μm pitch active edge pixel sensor, several irradiation campaings for the qualification of the sensors need to be carried out.

Vertical interconnection

Interconnection between the sensing layer and the front-end chip, given the relatively large pitch of 100 μm, can be easily achieved through bump-bonding techniques. Use of a dual-tier approach for the design of the front-end chip, besides the obvious benefit of doubling the effective area as compared to the case of a single tier circuit, represents the minimum requirement for a true four-side buttable structure. Indeed, if in-pixel A-to-D conversion and data storage are envisioned, the upper layer can be used to accommodate the analog front-end channel and the ADC, while the memory cells and the readout electronics can be integrated in the bottom layer. The two front-end chip layers may be interconnected using a small pitch vertical integration technique. With respect to standard bump bonding, vertical integration processes ensure enough mechanical stability for the chip to tolerate substrate grinding and mechanical polishing, which are needed to access the face-to-face bonded circuits through the substrate by means of Through Silicon Vias (TSVs).

Through Silicon Via (TSV) technology

As shown in Figure 3.1, through silicon vias with a pitch of 100 μm are needed to interconnect the sensor to the analog processor input. With an aspect ratio not exceeding 10:1 and a TSV diameter of the order of 1 μm (required to

minimize the parasitic contribution to the input capacitance of the channel), very aggressive thinning of the upper side of the 3D front-end chip structure is required. A process with these characteristics is available from Tezzaron Semiconductor in conjunction with the semiconductor manufacturer Globalfoundries [27]. On the other side of the vertically integrated structure, low density TSVs represent another key technology of a four-side buttable chip. By accessing the input/output pads through the substrate, use of wire bonds can be avoided and a tight side-by-side placement of the elementary tiles can be achieved. A less aggressive thinning step than in the previous case is required here, since the TSV diameter can be of the order of a few tens of micrometers.

3.1.2 Building blocks

In the following, a brief list about the fundamental microelectronic building blocks of the front-end chip for the 2D X-ray camera, based on a 65 nm CMOS technology, is given. The front-end channel is responsible for the parallel readout of the 100 μm pitch sensors and employs a non-linear response in order to deal with the wide input dynamic range of 10^4 photons.

Charge preamplifier

The charge preamplifier is responsible for the readout of the charge collected by the sensor. One photon with an energy of 1 keV corresponds to about 280 electron-hole pairs. In order to address the single photon detection requirement for small input signals, the first stage of the signal processing chain must feature a noise performance resulting in an ENC not exceeding 80 electrons RMS. The low-power consumption is a minor requirement in X-ray FEL applications, for the system in its final installation will be relatively easy to access and cool down. Hence, the noise performance can be improved by acting on the power dissipated in the very first stage of the chain. Another demanding requirement set by applications at FEL facilities, is the capability to cover the wide (10^4 photons) input dynamic range, while preserving the single photon detection at small signals. As already mentioned in Chapter 1 and Chapter 2, to cope with such requirement, several solutions have been proposed in the framework of the collaborations active in research programs for current X-ray FEL facilities. In the PixFEL project, the charge preamplifier features a novel non-linear response, in order to fit the large input dynamic range into a reasonable output swing.

Shaping stage

The shaping stage is a standard component of an optimum channel for charge signal processing [28]. In X-ray FEL applications, the front-end chip operation is synchrounus with the FEL beam, providing trains of pulses with inter-bunch periods which could be very short (as in the case of the European X-FEL) and with a known repetition rate. Hence, the charge preamplifier of the front-end chip of the PixFEL project is followed by a time variant filtering stage. This solution provides advantages with respect to continuous time processing in terms of time to return to base and Signal-to-Noise Ratio (SNR). Moreover, if in-pixel digitization is employed for amplitude measurement, a time variant shaper can be designed in such a way to provide the sample to convert directly at its output, like in the case of the DSSC Chip.

ADC

As mentioned in the previous chapters, several solutions based on either in-pixel ADC or analog readout have been proposed in the X-ray FEL community. However, the analog approach to data storage seems to provide a lower storage capacity than digital memories. Moreover, off chip transmission of analog data, or transfer of analog samples from the pixel to the periphery of the chip for digitization before data output, is more prone to corruption as compared to the case of in-pixel conversion, besides being more demanding in terms of power dissipation. The downside of immediate digitization of amplitude information is the need for an ADC inside each pixel, resulting in fast clock signals running dangerously close to the most sensitive points of the front-end circuit. In the PixFEL project, the voltage at the output of the shaping stage will be directly digitized in-pixel. Given the non-linear response of the very first stage of the front-end, the resolution of the ADC results from the following requirements:

- Small signal input range, which is the part of the input dynamic range where single photon detection is required.
- Number of ADC bins to be attributed to each photon in the single photon detection input range.
- Input dynamic range, which is 10^4 photons in the case of the PixFEL project.

Figure 3.2 shows the quantization error as a function of the input signal range intended for single photon detection, for different number of resolution bits and for two different ADC gains in the small signal region. In the case of an

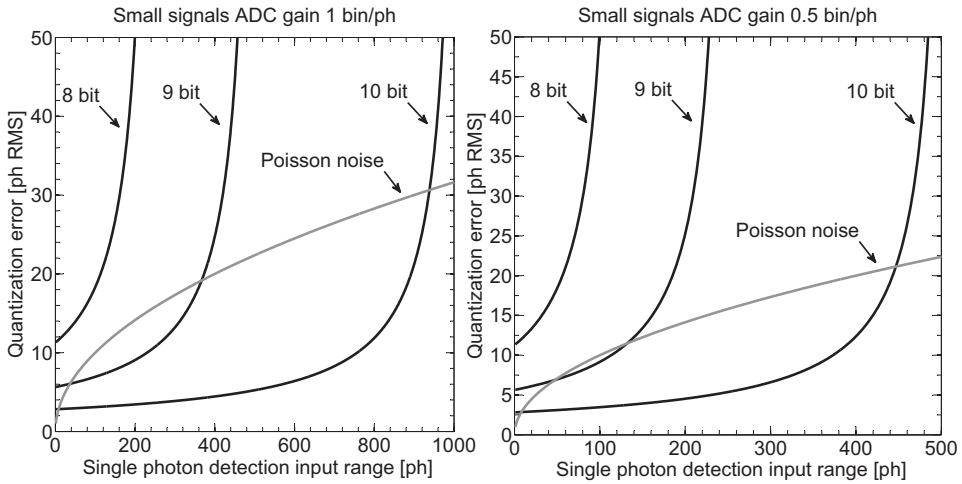

Figure 3.2: quantization error for an ADC with 8, 9 and 10 resolution bits and with an input dynamic range of 10^4 photons, as a function of the single photon detection input range. The quantization error is shown for an ADC gain of 1 bin/ph (left) and 0.5 bin/ph(right).

almost bi-linear transcharacteristic, a resolution of at least 9 bits is mandatory, in order to cope with the wide input dynamic range of 10^4 photons. Given the ADC resolution, the clock frequency is set according to the ADC architecture. The PixFEL front-end will integrate a Successive Approximation Register (SAR) ADC, featuring a suitable trade-off between clock frequency and resolution, with respect, for example, to the Wilkinson solution adopted in the DSSC. Moreover, in the case of a SAR ADC, one new conversion bit becomes available at each clock cycle, and transfer of the numerical data can start directly at the beginning of the sample conversion, without the need to wait for the end of the operation. The main drawback of SAR ADCs is the large area. Power consumption may also be an issue at fast conversion rates. Fortunately, the event rate in continuously operated FELs is quite low, slightly exceeding 100 Hz in the worst case, and so would be the conversion rate. In the case of burst mode operations, as in the European XFEL, while the event rate and the required conversion frequency may be as high as 4.5 MHz during the pulse train period, the average rate, hence the average dissipated power, becomes relatively low if the large intertrain period during which the converter is inactive is taken into account. The SAR ADC integrated in the PixFEL readout channel features 10 bit resolution, with a 0.5 bin/ph small signals

gain, and a target sampling and conversion frequency of 5 MHz.

Calibration circuit

The correct interpretation of the digital data sent off chip relies upon the accurate knowledge of the non linear input-output characteristics, or transcharacteristics, of the front-end channel. As the transcharacteristic may change from channel to channel due to process parameter dispersion, gain calibration has to be performed for each individual channel. This requires that a programmable signal generator circuit be integrated in each pixel. The granularity of the generated signal amplitude should be chosen to provide a significant number of experimental points also in the high gain portion of the input-output front-end curve with a resolution higher than the ADC one.

Other ancillary blocks

Other circuits may be needed to complete the set of fundamental building blocks. To mention a few: I/O circuits (transmitters and receivers, CMOS to LVDS and LVDS to CMOS converters) are needed to transfer data off-chip and to feed the clock to the ADC, the time variant shaper, the memory and the readout circuits. Power supply/temperature independent band-gap reference circuits are also required to provide stable voltage references to in-pixel blocks (e.g., the ADC). Other stages may be necessary to minimize the voltage drop across power and ground lines serving in-pixel circuits in a large matrix.

3.1.3 Readout architecture

The choice of the readout architecture is mostly dependent on the beam structure of the specific FEL facility. As already mentioned, a FEL can be operated either in continuous mode or in burst mode.

3.1.4 Continuous operation mode

The relatively low repetition rates, of the order of 100 Hz at most, foreseen in FELs to be operated in continuous mode, makes direct readout of a megapixel matrix a task within reach of present technology. For each million of pixels, with a 10 bit resolution, a 100 Hz frame readout rate will correspond to a bandwidth of 1 Gbit/s.

3.1.5 Burst mode operation

When the FEL is operated in burst mode with a very high repetition rate inside the train of photon pulses, direct and complete data readout would require impractical bandwidths. Note that in the case of imaging applications like the ones considered for this project, no sparsification techniques can be used to reduce the transmission bandwidth, as a large fraction of the pixels in the detector are expected to have a hit to report on for each pulse of the train. The common practice in this case, is to store as much information as possible in the pixel during the pulse train period and to send it off chip during the long inter-train period. For this purpose, the second layer in the dual-tier structure of the front-end chip, envisioned for the future evolution of the PixFEL project, is devoted to the integration of a large memory, with a capacity close to 1 kword, in a 65 nm CMOS process. A versatile design of the architecture may include the possibility of selecting the readout method between a direct readout mode (for continuous operation FELs) and an accumulate & read-out-later mode (for applications at the Eu-XFEL). This option might come at the cost of slightly smaller room available for memory cells.

3.2 Design of the analog front-end

This section is concerned with the design of the analog blocks for the readout channel to be used in the framework of the PixFEL project. First, the signal compression principle, exploited in the Charge Sensitive Amplifier (CSA) to cope with the wide input dynamic range, is described. Then the design of the CSA is presented. Finally, a description of the time variant shaping stage is given.

3.2.1 Signal compression principle

In the following, a detailed description about a novel front-end solution to dynamically adjust the gain of a CSA amplifier is given.

Inversion mode MOS capacitor

In the design of microelectronic circuits, MOS transistors may be used for the implementation of capacitive elements. For this purpose, drain and source of the device are shorted together to form one capacitor terminal whereas the gate forms the other. The value of the resulting capacitance, C_{gs}, depends on the voltage between the gate and the source-drain terminal V_{gs} and varies

non-linearly as the MOSFET is biased through accumulation, depletion and inversion region. In order to ensure a monotonic behavior of C_{gs}, the bulk can be connected to the lowest voltage available in the circuit (the GND reference) for an NMOS device or the n-well to the highest voltage (the power supply V_{DD}) for a PMOS, thus avoiding the accumulation region for all the values of V_{gs}. In this way, the device can only operate in inversion mode [29]and yields the qualitative C_{gs}-V_{gs} characteristic shown in Figure 3.3. This characteristic is non-linear and monotonic, with a relatively sharp transition occurring for V_{gs} values approaching the threshold voltage of the device, V_{Th}. For $0 < V_{gs} \ll V_{Th}$, the value of C_{gs} is set to its minimum and is mainly due to the overlap of the gate terminal with the source and drain diffusions. For $V_{gs} \gg V_{Th}$, a conductive channel appears under the gate oxide. Therefore, C_{gs} shows a maximum value which is mainly given by the gate-to-channel capacitance, C_{gc}. The values of $C_{gs,min}$ and $C_{gs,max}$ depend on the device geometry, whereas the V_{gs} value at which the transition occurs depends on the threshold voltage V_{Th} [30].

Dynamic signal compression

In response to a delta-like current signal, a CSA with a capacitive feedback network generates an output voltage step with an amplitude proportional to the input charge and with a sensitivity given by the inverse of the feedback

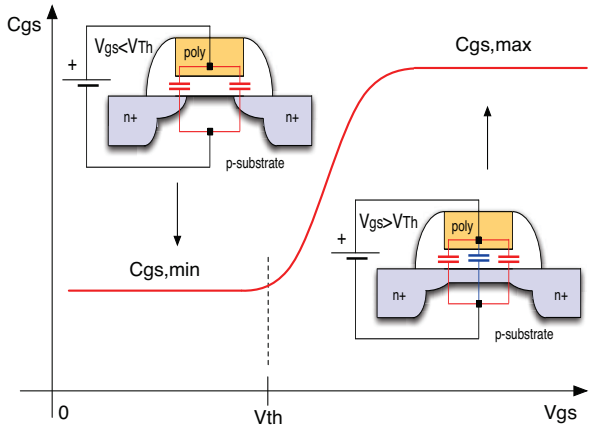

Figure 3.3: qualitative behaviour of the C_{gs} capacitance as a function of the V_{gs} voltage for an inversion-mode NMOS capacitor with fixed gate width W. The substrate contact (not shown) is at the GND potential.

capacitance. Therefore, the non-linear feature of the inversion-mode MOS capacitor can be exploited to dynamically change the gain of a CSA with the input signal amplitude, thus providing a dynamic signal compression. For this purpose, the MOS capacitor is used as the feedback network of the charge sensitive amplifier, as shown in Figure 3.4. In the following, an ideal block for the forward gain stage of the CSA is considered, to focus on the design of the feedback network. Moreover, a large resistance is included in the feedback network for DC restoration, setting to zero the gate-to-source voltage of the feedback device when no input signal is applied.

In principle, either a PMOS or an NMOS can be used in the feedback network. Moreover, the gate terminal can be connected either to the input or to the output of the gain stage. Device polarity and orientation must be chosen according to the detector characteristics, to obtain a capacitance which increases with the input signal amplitude, thus leading to a gain which decreases as the detected charge increases. For a detector collecting electrons, a positive voltage step is expected at the amplifier output in response to an input pulse charge. Hence, either a PMOS with the gate terminal connected to the amplifier input, Figure 3.4.a), or an NMOS with the gate connected

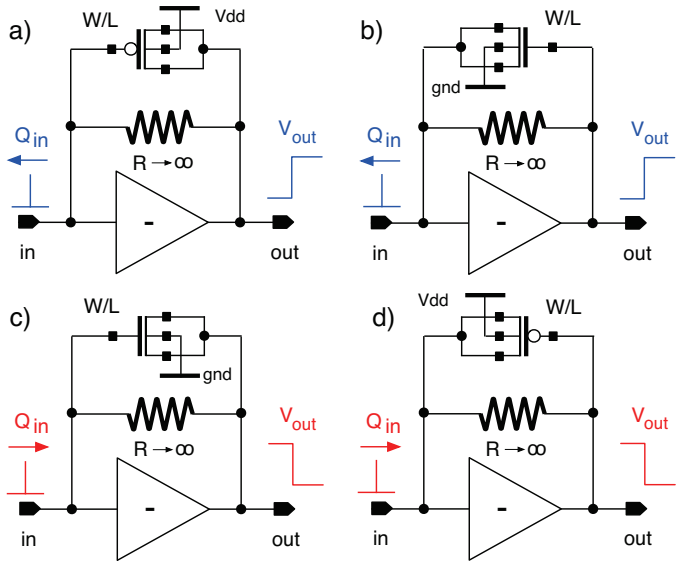

Figure 3.4: charge sensitive preamplifier with MOS non-linear feedback capacitor. The device type (NMOS or PMOS) is determined by the gate connection and by the detector signal polarity.

to the amplifier output, Figure 3.4.b), can be used. On the other hand, since a detector collecting holes generates a negative voltage step at the amplifier output, either an NMOS with the gate terminal connected to the amplifier input, Figure 3.4.c), or a PMOS with the gate connected to the amplifier output, Figure 3.4.d), are needed. With such configurations, the gate connection of the feedback device is always at a higher, for NMOS, or lower, for PMOS, potential with respect to the source-drain one. It is worth noting that, to fully exploit the output dynamic range of the CSA, the input DC voltage must be properly fixed: close to GND for PMOS and close to V_{DD} for NMOS feedback devices. For this purpose, the polarity of the preamplifier input device must be chosen accordingly, resulting in an NMOS for a detector collecting electrons and a PMOS for a detector collecting holes. For the sake of simplicity, in the following, only the solution proposed in Figure 3.4.a) is considered. However, the results can be easily extended to the other proposed configurations.

An example of the simulated input-output transcharacteristic for a CSA with an SVT PMOS feedback device with W/L=20 μm/5 μm is shown in Figure 3.5. The CSA output voltage V_{out} is the amplitude of the voltage step occurring at the amplifier output in response to a delta-like input current signal. The inset shows the initial high gain portion of the characteristic. As it can be noticed, the transfer function is almost bilinear with a higher sensitivity region for low values of the injected charge and a lower sensitivity for higher values of the injected charge. The transition starts to occur for values of the output voltage approaching the threshold voltage of the feedback MOS. The gain of the Charge Sensitive Amplifier is not constant any more and depends on the value of the injected charge Q_{inj}. By referring to the definition of charge sensitivity:

$$S_q(Q_{inj}) = \frac{dV_{out}}{dQ_{inj}} \tag{3.1}$$

an equivalent feedback capacitance C_{ef} can be derived as the inverse of the CSA gain:

$$C_{ef}(Q_{inj}) = S_q(Q_{inj})^{-1}. \tag{3.2}$$

The plots of the amplifier charge sensitivity and of the relevant equivalent feedback capacitance, obtained for the transfer function of Figure 3.5, are reported in Figure 3.6. For low values of the injected charge, the feedback device exhibits an equivalent capacitance of 10 fF with an amplifier sensitivity of 100 mV/fC. At the highest values of the injected charge, the capacitance reaches a maximum value of 1 pF and the sensitivity of the amplifier falls to 1 mV/fC.

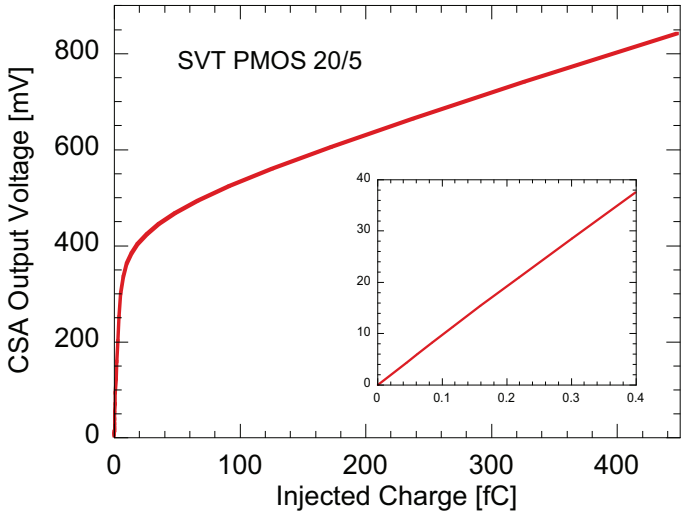

Figure 3.5: simulated input-output transcharacteristic of a CSA with a W/L=20 μm/5 μm SVT PMOS feedback device. The inset shows the initial, high gain portion of the characteristic.

Feedback network design methodology

In the design of a charge amplifier, the input-output transfer function must be chosen to comply with the requirements of the specific application. These requirements may concern:

- the sensitivity for low values of the injected charge;
- the maximum input dynamic range;
- the maximum voltage headroom at the amplifier output.

To comply with these specifications, the feedback device dimensions, W and L, must be properly chosen. Moreover, the most suitable threshold voltage, V_{Th}, must be chosen among the ones commonly available for nanoscale CMOS technologies.

Sensitivity for low input charge (S_{lq}): if we assume that low values of the injected charge generate an output voltage step with amplitude V_{out} much lower than the device threshold V_{Th}, then the equivalent feedback capacitance

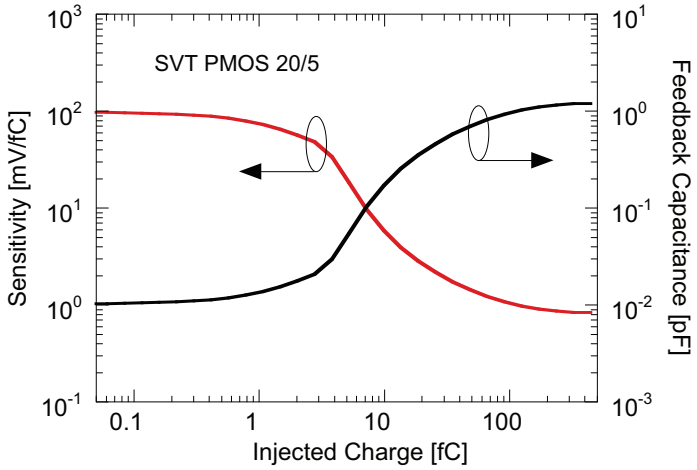

Figure 3.6: Simulated CSA sensitivity and equivalent feedback capacitance as a function of the injected charge for a CSA with a W/L=20 μm/5 μm PMOS feedback device.

C_{ef} is set at its minimum and it is mainly due to the parallel of the overlap gate-to-source $C_{gs,ov}$ and gate-to-drain $C_{gd,ov}$ capacitances:

$$C_{ef,min} \approx C_{gs,ov} + C_{gd,ov} = 2W\Delta LC_{ox} \tag{3.3}$$

where W is the channel width, ΔL is the extension of the overlap region and C_{ox}=ε_{ox}/t_{ox} is the gate oxide capacitance per unit area. According to Equation 3.2, the relevant sensitivity of the amplifier for low values of the input charge, S_{lq}, is given by the following equation:

$$S_{lq} = \frac{1}{2\Delta LC_{ox}}\frac{1}{W}. \tag{3.4}$$

Therefore, in this region, the gain of the preamplifier is independent of the MOS channel length L and can be adjusted by carefully choosing the channel width W. Figure 3.7 shows the simulated S_{lq} sensitivity for SVT PMOS feedback devices, as a function of the channel length (for a fixed width) and as a function of the channel width (for fixed lengths). As expected, the gain is independent of the channel length, whereas it is proportional to the inverse of the channel width.

Sensitivity for high input charge (S_{hq}): for high values of the injected charge, the amplitude of the output voltage step is expected to exceed the

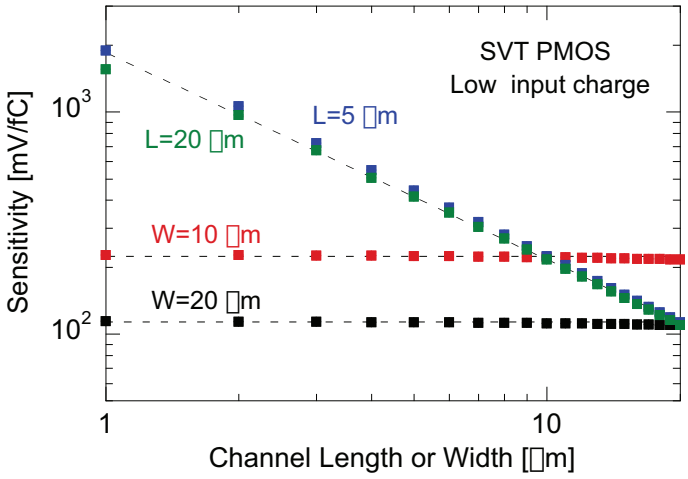

Figure 3.7: simulated sensitivity at low input charge, for SVT PMOS feedback devices, as a function of the channel length (for a fixed width) and as a function of the channel width (for fixed lengths).

threshold, thus leading to a maximum of C_{ef} which is mainly given by the gate-to-channel C_{gc} capacitance:

$$C_{ef,max} \approx C_{gc} = WLC_{ox}. \tag{3.5}$$

The relevant amplifier sensitivity is given by:

$$S_{hq} = \frac{1}{C_{ox}} \frac{1}{WL}. \tag{3.6}$$

Therefore, for high values of the injected charge, the gain depends on the MOS gate area WL and can be set with a suitable design of the MOS channel length L, once W has been properly chosen to set the sensitivity for small input charges. In Figure 3.8 the simulated gain for SVT PMOS feedback devices is reported as a function of the device gate area, for different values of the channel length and width. In agreement with the behaviour reported in equation Equation 3.6, the gain is proportional to the inverse of the device gate area.

It is useful to define a signal compression factor, k, as the ratio of the sensitivity at small and large values of the input signals:

$$k = \frac{S_{lq}}{S_{hq}} = \frac{L}{2\Delta L}. \tag{3.7}$$

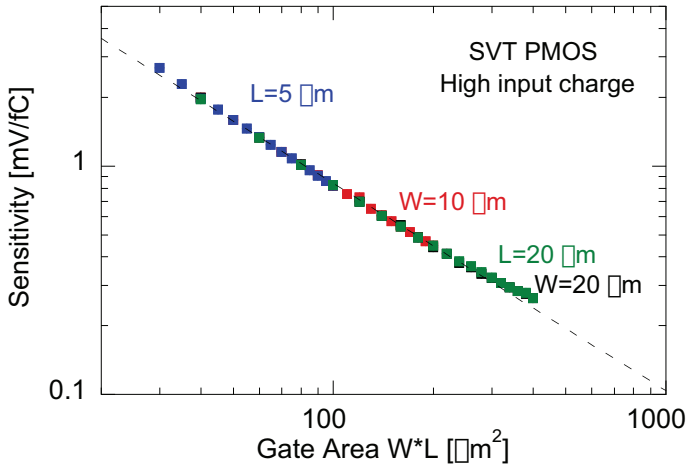

Figure 3.8: simulated sensitivity in the high input charge region, for SVT PMOS feedback devices, as a function of the device gate area for different values of the device channel length and widths.

According to the definitions of S_{lq} and S_{hq}, reported in Equation 3.4 and Equation 3.6, respectively, k depends on the channel length, L, only. If we approximate the transfer function with a piecewise linear characteristic with the slopes given by S_{lq} and S_{hq}, the signal compression factor must be fixed according to the following equation, to comply with the input and output dynamic range requirements:

$$k = \frac{Q_{inj,max} - Q_{inj,k}}{V_{out,max} - V_{out,k}} S_{lq} \approx \frac{Q_{inj,max}}{V_{out,max} - V_{Th}} S_{lq} \tag{3.8}$$

where $V_{out,max}$ is the voltage headroom at the CSA output, $V_{out,k} \approx V_{Th}$ is the voltage at which the kink, i.e., the change in slope, occurs, $Q_{inj,max}$ is the input dynamic range and $Q_{inj,k}$ is the value of the input charge at the kink ($Q_{inj,k} \ll Q_{inj,max}$). As a consequence, once S_{lq} has been fixed to comply with the required sensitivity, S_{hq} must be fixed in agreement with the following equation:

$$S_{hq} = \frac{V_{out,max} - V_{Th}}{Q_{inj,max}}. \tag{3.9}$$

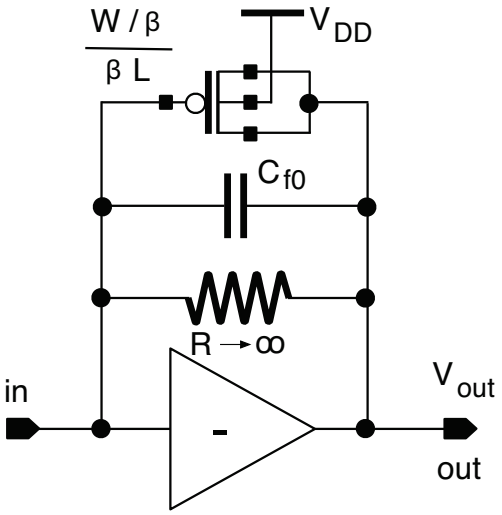

Figure 3.9: improved feedback network with a MOS device, scaled by a factor of β, and an additional fixed capacitance C_{f0}.

A remark about the gain precision

Since the sensitivities S_{lq} and S_{hq} depend on W, L and t_{ox}, the gain might be affected by parameter mismatch. This effect is critical, in particular, for the sensitivity at low input charge S_{lq}. In order to improve the precision of the gain for small input signals, an additional capacitance in parallel to the feedback MOS, C_{f0}, can be introduced, as shown in Figure 3.9. Among the different passive capacitances available in nanoscale processes, the one adopted for the implementation of C_{f0} must be of a type which is less sensitive to parameter mismatch with respect to the MOS capacitance. Its value can be chosen in agreement with the following equation:

$$C_{f0} = \left(1 - \frac{1}{\beta}\right) C_{ef,min} \tag{3.10}$$

where β>1 is a free parameter to be set by the designer. To preserve the value of the sensitivity in both the high and low gain regions, the dimensions of the feedback MOS must be scaled according to the following equations:

$$W_{new} = \frac{W}{\beta} \tag{3.11}$$

$$L_{new} = \beta \cdot L \tag{3.12}$$

As an example, Figure 3.10 shows the mismatch occurring for a feedback network achieved with an SVT PMOS only with W/L=100 μm/1 μm, and the one obtained for an improved version designed with β=5, that is with an additional C_{f0}=35 fF MIM capacitor and a scaled MOS with W=20 μm and L=5 μm. While the mean value of the gain is almost unchanged, the dispersion on the simulated sensitivity is improved by about a factor of 4. The passive capacitance provides an additional benefit. Since C_{f0} is insensitive to the bias conditions, which is not the case for the MOS capacitance, it improves the linearity of the transfer function in the low input charge region where C_{f0} is dominant on the overall feedback capacitance.

Transition between high and low sensitivity region

The transition between the high and the low sensitivity regions starts to occur for values of the output voltage approaching the threshold of the device. V_{Th} is a parameter which, apart from the slight dependence on the channel length, is almost constant. Nonetheless, for nanoscale CMOS technology, manufacturers usually supply MOS transistors with low, standard and high threshold voltage.

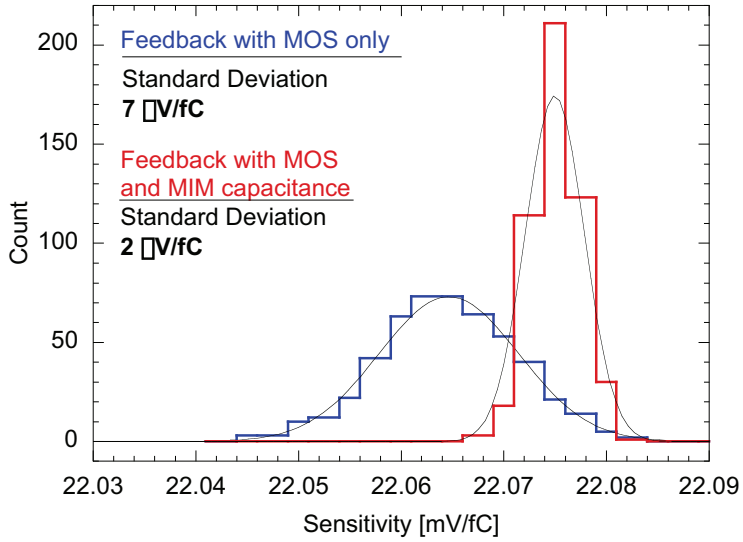

Figure 3.10: dispersion of the sensitivity at low injected charge, for a feedback SVT PMOS with W/L=100 μm/1 μm and for an improved network with an additional C_{f0}=35 fF MIM capacitor and a scaled MOS with W=20 μm and L=5 μm.

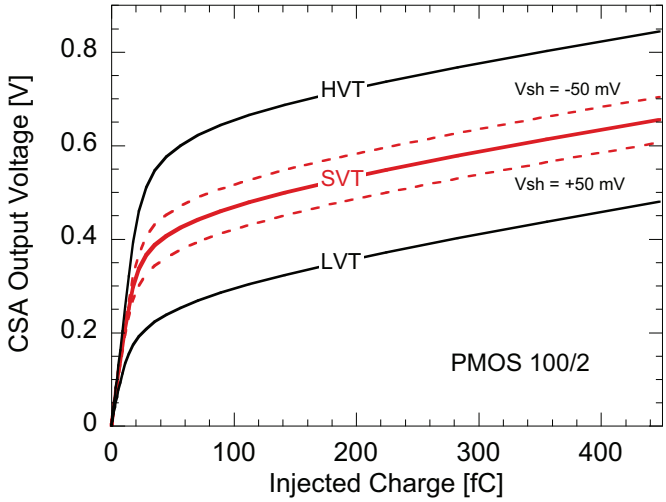

Figure 3.11: simulated transcharacteristic of a CSA with a W/L=100 μm/2 μm PMOS feedback device. Results for low, standard and high threshold voltage devices are reported. The effect of a ±50 mV voltage shift applied by a transconductor is also shown for the SVT device.

This feature provides an additional degree of freedom in the choice of the feedback device, which can be exploited, in particular, in the shift of the value of the input charge at which the kink between high and low sensitivity occurs. This is shown in Fig. 3.11, where the simulated transfer function of a CSA with a W/L=100 μm/2 μm PMOS feedback device is reported for LVT, SVT and HVT options.

In addition, for applications where the reset of the feedback capacitance is performed by a continuous time network implemented with a transconductance amplifier, as shown in Fig. 3.12, an additional voltage shift can be applied to the feedback MOS, which enables a precise trimming of the voltage at which the kink occurs. As an example, the effect of a ±50 mV shift is shown in Fig. 3.11 for the SVT device.

3.2.2 Charge sensitive amplifier with dynamic signal compression

The CSA is the very first stage of the signal processing chain of the PixFEL readout channel, and will be connected via bump-bonding to a fully depleted p-on-n silicon pixel sensor collecting holes. The main requirements of the stage

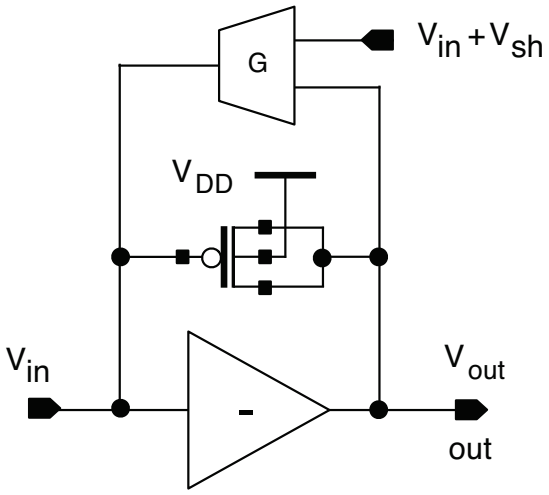

Figure 3.12: feedback network with additional transcondutance amplifier for continuous time reset. One terminal of the device can be used to apply a voltage shift on the feedback MOS. This shift enables a precise variation of the voltage at which the kink occurs.

are reported in the following:

- **Input dynamic range:** from 1 photon up to 10^4 photons, with an energy between 1 keV and 10 keV. Since one photon at 1 keV generates approximately 280 electron-hole pairs, the input charge ranges between 44 aC and 44 pC, respectively for 1 photon with an energy of 1 keV and 10^4 photons with an energy of 10 keV.

- **Output voltage range:** in order to properly exploit the almost bilinear transcharacteristic provided by the signal compression principle of an inversion mode MOS capacitor, the output voltage swing should exceed the threshold voltage of the MOS transistor, which could be roughly estimated in 350 mV for an LVT NMOS the 65 nm CMOS technology by TSMC. On the other hand, in order to avoid saturation and nonlinearity effects in the cascaded shaping stage, the output swing should be lower than 800 mV. Therefore, a value of about 500 mV has been chosen for the output swing of the CSA.

- **Noise:** in order to provide single photon detection capabilities at an energy of 1 keV, a minimum SNR of 6 is needed. By assuming that

the major contribution to the noise of the overall signal processing chain comes from the very first stage, and taking into account the minimum shaping time, which corresponds to about 50 ns for a 5 MHz operation, the noise of the CSA must be such that an ENC lower than 80 electrons RMS is achieved.

- **Power consumption:** no particular constraints are set for the power consumption, since the final application of the PixFEL detector has not yet been envisioned. As a rule of thumb, the power consumption can be reckoned by referring to the one of the DSSC detector, expected in about 1.5 mW per pixel. Considering the target pixel pitch of about 100 μm of the PixFEL project, a power consumption of about 350 μW per pixel can be estimated. This power budget should be allocated to the different blocks of the readout channel, including the CSA, in such a way to minimize the noise performance.

- **Area occupancy:** the CSA must be accomodated, along with the shaping stage and the ADC, in a pixel with an area of about 100 μm $\times$ 100 μm.

It has to be noticed that the overall capacitance of the detector, C_D, due to the sensor, the inter-pixel parasitic capacitance and the bump-bonding, is estimated at about 100 fF.

Feedback network design

The device used in the feedback network of the CSA, M_f, is an LVT NMOS transistor. In order to cope with either 1 keV and 10 keV input signals, two different configurations of the feedback network have been foreseen:

- **1 keV configuration:** the sensitivity for small input signals, S_{lq}, has been set to about 1 mV/ph, leading to a minimum value for C_{ef} of about 45 fF. The width of the feedback transistor can be computed from Equation 3.3:

$$W_f = \frac{1}{S_{lq} \cdot 2 \cdot \Delta L \cdot C_{ox}} \approx 100\,\mu\text{m} \tag{3.13}$$

  As far as large input signals are concerned, the sensitivity S_{hq} can be computed from Equation 3.9. By taking into account a threshold voltage, V_{Th}, of about 320 mV (extracted from simulations for an LVT NMOS transistor), the large signal sensitivity, S_{hq}, results in about 20 μV/ph,

whereas the maximum value of C_{ef} is about 2.5 pF. The feedback transistor length, L_f, can be computed as follows:

$$L_f = \frac{1}{S_{hq} \cdot C_{ox} \cdot W} \approx 1.7\,\mu\text{m} \tag{3.14}$$

In order to improve the dispersion of S_{lq}, a MIM capacitance, C_{f0} of 25 fF has been added in parallel to M_f. Hence, the final dimensions of the feedback transistor have been scaled by a β factor of 2.3:

$$W_f = \frac{100\,\mu\text{m}}{\beta} \approx 40\,\mu\text{m} \tag{3.15}$$

$$L_f = 1.7\,\mu\text{m} \cdot \beta \approx 4\,\mu\text{m} \tag{3.16}$$

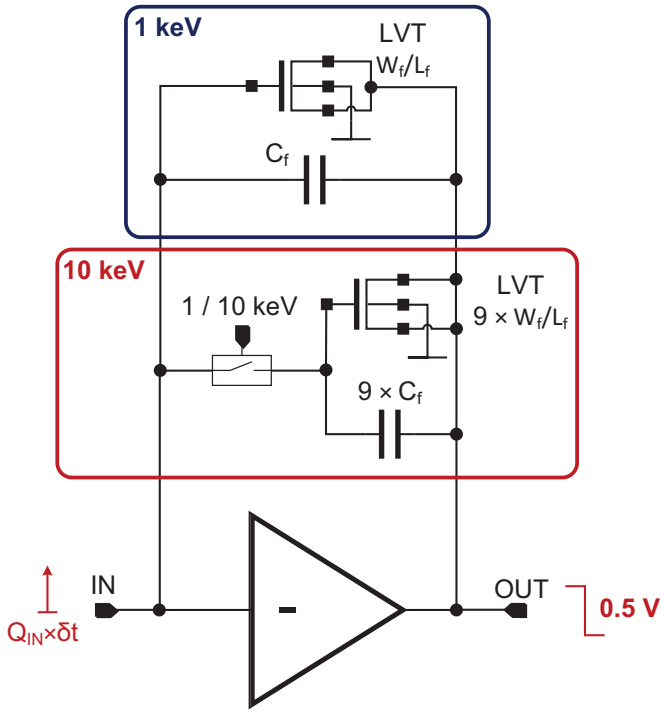

Figure 3.13: schematic of the feedback network for the CSA with dynamic signal compression. The network for 1 keV input signals is coloured in blue, whereas the network to be used for 10 keV input signals is coloured in red.

- **10 keV configuration:** the same consideration carried out for the feedback transistor to be used in 1 keV configuration can be done for input signals with an energy of 10 keV. As the energy of the input signal increases by a factor of 10, so does the equivalent feedback capacitance, leading to a feedback transistor width of 400 μm, and a value of the MIM capacitor of 250 fF. The length of the feedback transistor, L_f, is unchanged (4 μm).

The feedback network featuring the dynamic signal compression is based on 2 blocks, as depicted in Figure 3.13. For input signals with an energy of 1 keV, only the corresponding block (coloured in blue) is connected in feedback to the CSA, and the equivalent feedback capacitance is C_{ef}. To deal with 10 keV input signals, an additional network (coloured in red), scaled up by a factor of 9, is connected in parallel to the other one by means of a switch, resulting in an equivalent feedback capacitance equal to $10 \cdot C_{ef}$.

Forward stage

In the following, a description about the design of the forward stage of the CSA with dynamic signal compression is given.

Gain-bandwidth product analysis: in response to a delta-like input current, the CSA must be able to provide a negative voltage step at the output with a fall time lower than 25 ns. Hence, the Gain-Bandwidth Product (GBP) must be properly set to satisfy such a requirement in the wide range of values of the equivalent feedback capacitance (45 fF $\div$ 25 pF). The CSA can be approximated by the simplified schematic shown in Figure 3.14. Besides the equivalent feedback capacitance, C_{ef}, and the detector capacitance, C_D, a feedback resistance, R_f, modeling the reset switch, has been introduced. The forward stage is described by means of a first order model:

$$A(s) = \frac{A_0}{1 + s \cdot \tau_0} \tag{3.17}$$

where A_0 is the DC gain and τ_0 is the dominant pole time constant. The input and feedback impedances of the stage are the following:

$$Z_{in} = \frac{1}{s \cdot C_D} \tag{3.18}$$

$$Z_f = \frac{R_f}{1 + s \cdot C_f R_f} \tag{3.19}$$

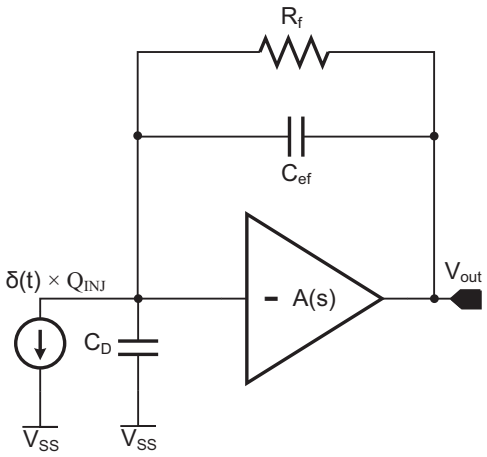

Figure 3.14: simplified schematic of the CSA.

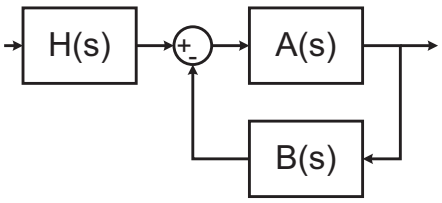

Figure 3.15: block diagram of the dynamic system modeling the CSA.

By referring to the dynamic system shown in Figure 3.15, the transfer function of the CSA amplifier can be computed as follows:

$$H\left(s\right) \;=\; Z_{in} \parallel Z_f \tag{3.20}$$

$$B\left(s\right) \;=\; \frac{Z_{in}}{Z_{in} + Z_f} \tag{3.21}$$

$$G(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{A(s) \cdot H(s)}{1 + A(s) \cdot B(s)} = \\ = \frac{A_0 \cdot R_f}{(1 + A_0)(\tau_0 + R_f(C_D + C_f) + A_0 C_f R_f)\, s + R_f \tau_0 (C_D + C_f)\, s^2} \tag{3.22}$$

If both A_0 and R_F are high enough, the first order term in the denominator of Equation 3.22 can be approximated by $A_0 \cdot C_f \cdot R_f \cdot s$, and the CSA transfer function becomes the following:

$$G(s) \approx \frac{R_f}{1 + C_f R_f s + (C_D + C_f) R_f \frac{\tau_0}{A_0} s^2} \tag{3.23}$$

The denominator of Equation 3.23 can be modeled as follows:

$$1 + C_f R_f s + (C_D + C_f) R_f \frac{\tau_0}{A_0} s^2 = (1 + \tau_A)(1 + \tau_B) = \\ = 1 + \tau_A s + \tau_B s + \tau_A \tau_B s^2 \tag{3.24}$$

where τ_A and τ_B are the two time constants of the system. If it is assumed that $\tau_A \gg \tau_B$, the denominator can be approximated as follows:

$$1 + \tau_A s + \tau_B s + \tau_A \tau_B s^2 \approx 1 + \tau_A s + \tau_A \tau_B s^2 \tag{3.25}$$

and the two time constants of the CSA can be computed:

$$\tau_A = C_f \cdot R_f \tag{3.26}$$

$$\tau_B = (C_D + C_f) R_f \frac{\tau_0}{A_0} \cdot \frac{1}{R_f \cdot C_f} = \frac{\tau_0}{A_0} \cdot \left(\frac{C_D}{C_f} + 1 \right) \tag{3.27}$$

Therefore, the CSA transfer function can be written as follows:

$$G(s) \approx \frac{R_f}{1 + \tau_A s + \tau_A \tau_B s^2} \tag{3.28}$$

where τ_A is the time constant describing the discharge of the feedback capacitance, whereas τ_B is the time constant modeling the charging of the feedback capacitance (i.e. the response time of the CSA when a delta like input signal is applied). The GBP of the forward stage of the CSA can be computed by taking into account that the fall time, t_f, must be lower than 25 ns. The worst case is given when the equivalent feedback capacitance is at the minimum (i.e.

the smallest signal is applied at the input of the CSA), and the minimum GBP can be computed as follows:

$$2.2 \cdot \tau_B = 2.2 \cdot \frac{\tau_0}{A_0} \cdot \left(\frac{C_D}{C_f} + 1\right) = 2.2 \cdot \frac{1}{2\pi \cdot GBP} \cdot \left(\frac{C_D}{C_f} + 1\right) \leq 25\,\text{ns} \leftrightarrow$$
$$\leftrightarrow GBP \geq 2.2 \cdot \left(\frac{C_D}{C_f} + 1\right) \frac{1}{2\pi \cdot 25\,\text{ns}} = 45\,\text{MHz} \tag{3.29}$$

In conclusion, the forward stage of the CSA must feature a GBP greater than 45 MHz.

CSA gain stage: the gain stage of the CSA forward block, shown in Figure 3.20 together with a cascaded ideal output stage, is based on a single-ended folded cascode topology, which is a common choice for low-voltage and low-noise, high gain ampliers. For a detector collecting holes, a negative voltage swing at the output of the CSA is obtained when an input signal is applied. Therefore, an LVT PMOS input transistor is needed in order to set the DC value of V_{in} as close as possible to V_{DD}, thus ensuring enough voltage room for a proper operation of the CSA output stage in the overall 0.5 V voltage swing. The folded cascode configuration is based on transistors M_0 and M_2.

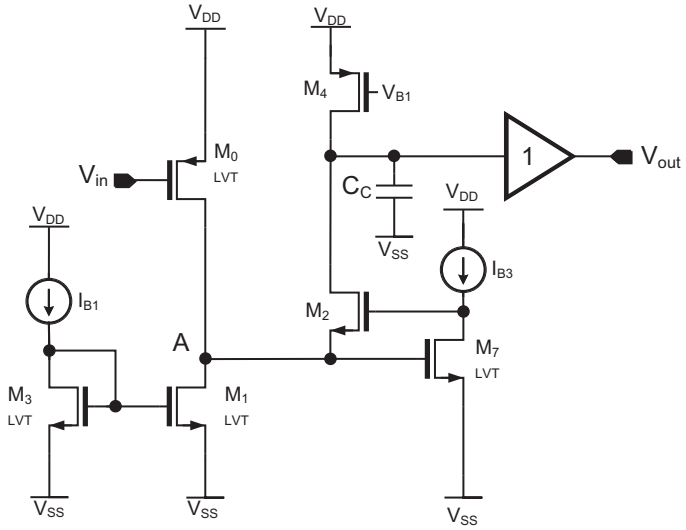

Figure 3.16: schematic view of the gain stage of the CSA forward block.

In order to increase the impedance from the drain of M_1, a local feedback based on M_7 has been employed. The active load is provided by transistor M_4, properly biased. A compensation capacitance, C_c, achieved by means of a MOS transistor biased in strong inversion, has been connected at the output of the gain stage in order to reduce the bandwidth and increase the phase margin. The aspect ratios of the transistors as well as the values of the other components of the stage are summarized in Table 3.1.

Name	**Value**
M_0	$40/0.15$
M_1	$5/2$
M_2	$2/0.15$
M_4	$8/1$
M_7	$5/0.15$
I_{B1}	45 μA
I_{B3}	5 μA
V_{B1}	800 mV
C_c	600 fF

Table 3.1: summary of the CSA gain stage components. Transistor dimensions are expressed in μm.

As far as the low frequency small signal response is concerned, it can be shown that the DC gain of the stage is the following:

$$\frac{v_o}{v_{in}} = \frac{g_{m,0}\, r_{d,0}\, (1 + g_{m,2}\, r_{ds,2}\, (1 + g_{m,7}\, r_{ds,7}))\, r_{ds,4}}{r_{d,0} + r_{ds,4} + g_{m,2}\, r_{d,0}\, r_{ds,2}\, (1 + g_{m,7}\, r_{ds,7}) + r_{ds,2}} \tag{3.30}$$

where $r_{ds,i}$ and $g_{m,i}$ represent the drain-to-source resistance and the transconductance of the i-th transistor, respectively, and $r_{d,0}$ is the resistance as seen from the source terminal of M_2:

$$r_{d,0} = r_{ds,0} \parallel r_{ds,1} \tag{3.31}$$

In this case, the output resistance of the stage is mainly given by $r_{ds,4}$, for the resistance seen from the output node downward is enhanced by the local feedback network. Hence, Equation 3.30 can be approximated as follows:

$$\frac{v_o}{v_{in}} = g_{m,0}\, r_{d,4} \tag{3.32}$$

The frequency response of the stage is limited by the dominant pole of the stage, τ_c, which is given by the output impedance, Z_{out}:

$$Z_{out} = r_{out} \parallel Z_c = \frac{r_{out}}{1 + r_{out}\, C_c\, s} \tag{3.33}$$

where Z_c is the impedance of the compensation capacitance and r_{out} is the output resistance of the stage. The latter contribution is given by the following equation:

$$r_{out} = (r_{d,0} + r_{ds,2} + g_{m,2}\, r_{d,0}\, r_{ds,2}\, (1 + g_{m,7}\, r_{ds,7})) \parallel r_{ds,4} \tag{3.34}$$

Since the output resistance, r_{out}, can be approximated to $r_{ds,4}$, the output impedance of the stage becomes the following:

$$Z_{out} \approx \frac{r_{ds,4}}{1 + r_{ds,4}\, C_c\, s} \tag{3.35}$$

CSA output stage: as already mentioned above, the equivalent feedback capacitance spans almost three orders of magnitude, resulting in high current pulses to be sunk by the CSA output stage when large signals are applied at the input. The maximum amplitude of the current pulse can be roughly computed as follows:

$$I_{pulse,max} \approx \frac{C_{ef,max} \cdot \Delta V_{out,max}}{t_{fall}} \tag{3.36}$$

where $\Delta V_{out,max}$ is the maximum voltage variation at the output of the CSA (0.5 V) and t_{fall} is the fall time of the signal at the output of the CSA (25 ns). For 10^4 photons, an equivalent feedback capacitance of 2.5 pF and 25 pF is achieved, respectively for a photon energy of 1 keV and 10 keV, leading to current pulses of about 62.5 μA and 625 μA. In order to deal with such high values of current, an improved output stage, based on the White follower configuration [31], has been cascaded to the gain stage of the CSA, as shown in Figure 3.17. The circuit operates in such a way that the current flowing through M_{10} is kept at its equilibrium point during transients, thus avoiding a further decrease of the output voltage but for the gate-to-source voltage contribution of M_{10}. When a negative voltage step occurs at the output of the gain stage, the equilibrium working point of the output stage is shifted and the current through M_{10} tends to decrease. As the current through M_{11} increases, due to the charging of the feedback network, its gate-to-source voltage, $V_{GS,11}$ increases, thus decreasing the current through M_{12} and restoring the equilibrium. According to the schematic shown in Figure 3.18, the low

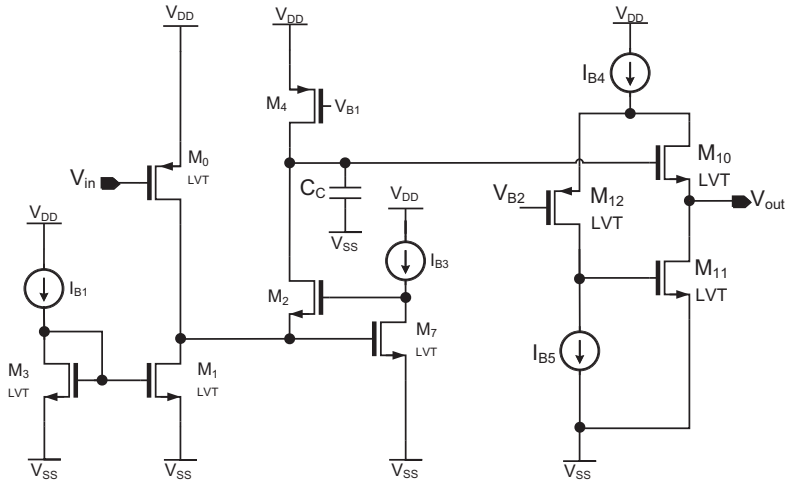

Figure 3.17: schematic view of the CSA output stage.

frequency small signal response is the following:

$$v_{out} = \frac{g_{m,1}\, r_{ds,1}\, r_{ds,2}\, (1 + g_{m,2}\, r_A)}{g_{m,1}\, r_{ds,1}\, r_{ds,2}\, (1 + g_{m,2}\, r_A) + g_{m,2}\, r_A\, r_{ds,2} + r_3 + r_A + r_{ds,1} + r_{ds,2}}\, v_{in} \approx$$
$$\approx \frac{g_{m,1}\, g_{m,2}\, r_{ds,1}\, r_{ds,2}\, r_A}{g_{m,1}\, g_{m,2}\, r_{ds,1}\, r_{ds,2}\, r_A}\, v_{in} = v_{in} \tag{3.37}$$

The loop gain of the stage has been computed by opening the loop on the

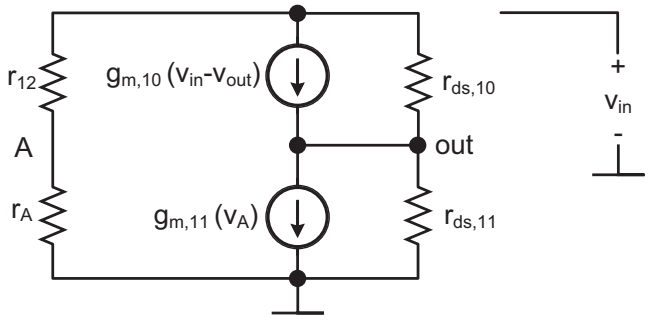

Figure 3.18: schematic view of the small signal circuit of the CSA output stage.

gate of M_{11} and restoring the impedance at node A. It can be shown that the loop transfer function is the following:

$$G_{loop}(s) = \frac{V_A(s)}{V_{G,11}(s)} = -\frac{g_{m,10}\, g_{m,11}\, r_A\, r_{ds,11}}{(1 + C_{11}\, r_A\, s)\,(1 + r_{ds,11}\, g_{m,11} + C_{out}\, r_{ds,11}\, s)} \tag{3.38}$$

where C_{11} is the gate-to-source capacitance of M_{11} and C_{out} is the output capacitance. Hence, the output stage must be properly designed in order to ensure the stability of the system.

The aspect ratios of the transistors as well as the values of the other components of the stage are summarized in Table 3.2.

Name	Value
M_10	$^{50}/_{0.06}$ DNW
M_11	$^{5}/_{0.06}$
M_12	$^{5}/_{0.06}$
I_{B4}	30 μA
I_{B5}	7 μA
V_{B2}	500 mV

Table 3.2: summary of the CSA output stage components. Transistors dimensions are expressed in μm.

CSA reset network: in order to comply with timing requirements up to 5 MHz, the CSA must be able to restore the charge of the feedback network within some tens of nanoseconds. Hence, in order to overcome the slew rate limitation at the output of the gain stage, due to the small current flowing through M_4 (refer to Figure 3.20), an additional reset network has been introduced in the CSA, as shown in the overall schematic of Figure 3.19. The network has been designed in such a way that M_x is switched off during the normal CSA operation. When a large amount of charge is collected by the detector and the CSA output voltage approaches its minimum, so does the voltage at node B. As the reset is carried out by means of the `SR` signal, closing the switch in the feedback network, current $I_{B,0}$ charges the capacitance at node B. Since current $I_{B,0}$ is kept at a low value (about 400 nA) to maximize the gain of the stage, the voltage at node A increases, for the current flowing through M_2 drops to almost 0. When the voltage at node A exceeds

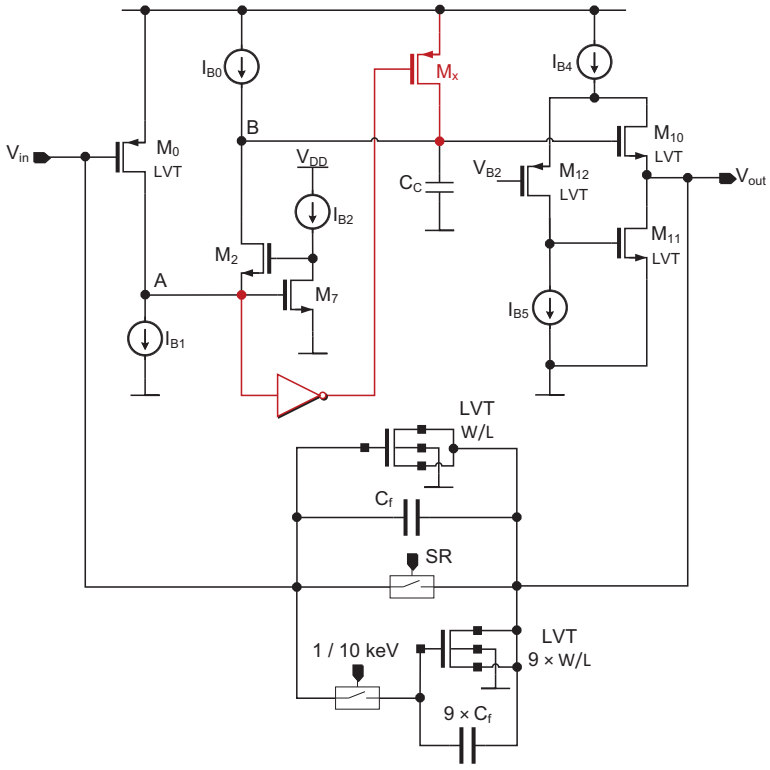

Figure 3.19: schematic view of the CSA. For the sake of simplicity, some transistors have been replaced with ideal current sources. The reset network is depicted in red.

the threshold voltage V_{IH} of the inverter, M_x is switched on, thus providing an additional current to restore the voltages at node A and B. M_x remains active as long as the voltage at node A is not restored at the DC operating point.

Performance of the CSA

Figure 3.20 shows the magnitude of the frequency response of the overall forward stage obtained from simulation (red) and from the expression of Equation 3.30 (blue). As it can be noticed, the two responses are in fair agreement, with the dominant pole given by the parallel between the compensation capacitance, C_c, and the output resistance, $r_{ds,4}$. The simulation shows a second

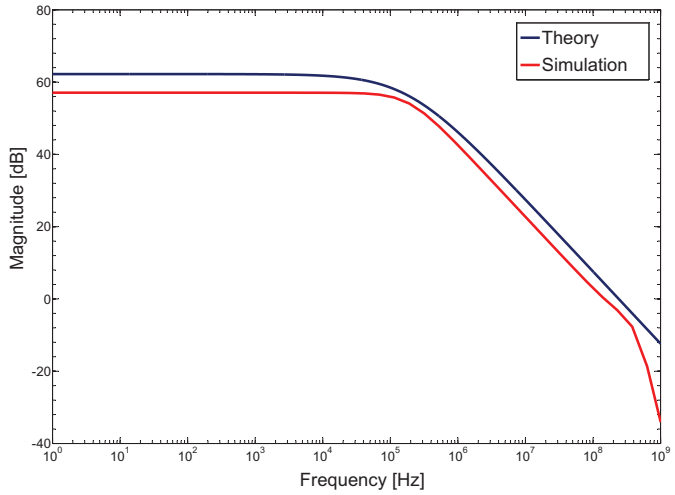

Figure 3.20: magnitude of the CSA forward stage transfer function from simulation and theory.

high frequency pole, due to the overall capacitance at node A. The simulated GBP corresponds to about 140 MHz, whereas the phase margin, evaluated with an ideal feedback capacitance varied in the range between 10 fF and 20 pF, is always higher than 60 degrees, as shown in Figure 3.21. As far as the output stage loop frequency response is concerned, the magnitude and phase are shown in Figure 3.22. As it can be noticed, the transfer function features two poles. The low frequency one is due to the gate-to-source capacitance of $M11$, whereas the high frequency one is related to the output capacitance. The system features a phase margin of about 30 degrees.

The transient response of the CSA has been simulated by applying a current pulse at the input node, in a range of values corresponding to the charge generated by signals between 1 photon and 10^4 photons, for both the 1 keV and 10 keV configurations. To simulate a realistic operation, the duration of the current pulse is equal to the signal collection time of the detector, estimated at 15 ns. Figure 3.23 shows the output of the CSA in the 1 keV configuration. The figure emphasizes the signal compression featured by the stage, able to detect up to 10^4 photons in a 500 mV output swing. The fall time (10-90% of the swing) is always lower than the specification value of 25 ns. The benefit of the output stage, based on the white-follower configuration, can be noted in Figure 3.24, where a comparison with a classic source follower based solution

is shown. The PMOS based source follower is affected by the high current peak occurring for 10^4 photons, in such a way that the voltage room available for M_2 drops to almost zero. On the other hand, the proposed White follower solution is able to sink the current without affecting the amplifier operation. As far as the reset of the stage is concerned, Figure 3.25 shows the transient response without (blue) and with (red) the reset network that has been introduced to speed up the discharging phase. As it can be noticed, thanks to the proposed solution, the reset can be carried out in a very small time period (20 ns), enabling operation at frequencies up to 5 MHz.

The transcharacteristic of the stage is shown in Figure 3.26, for both the 1 keV and 10 keV configurations. As it can be noticed from the inset, the CSA features a high linearity in the small input signal region, with a non-linearity error lower than 0.025 ph. The sensitivity of the CSA, computed according to Equation 3.1 and expressed in mV/ph, is shown on the left hand side of Figure 3.27, for both the energy configurations. Starting from a value of 1 mV/ph for small input signals, it begins to drop with 300 input photons, and settles at about 20 μV/ph for an input signal approaching 10^4 photons. In the right hand side of Figure 3.27, the equivalent feedback capacitance is shown for both the energy configurations. Starting from a value of about 30 fF (300 fF in the 10 keV mode), the equivalent feedback capacitance increases up to about 1.3 pF (13 pF in the 10 keV mode). As expected, by switching from the 1 keV to the 10 keV configuration, the equivalent feedback capacitance is

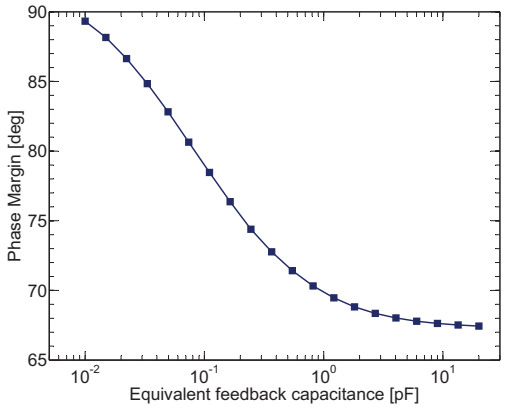

Figure 3.21: phase margin of the CSA as a function of the equivalent feedback capacitance.

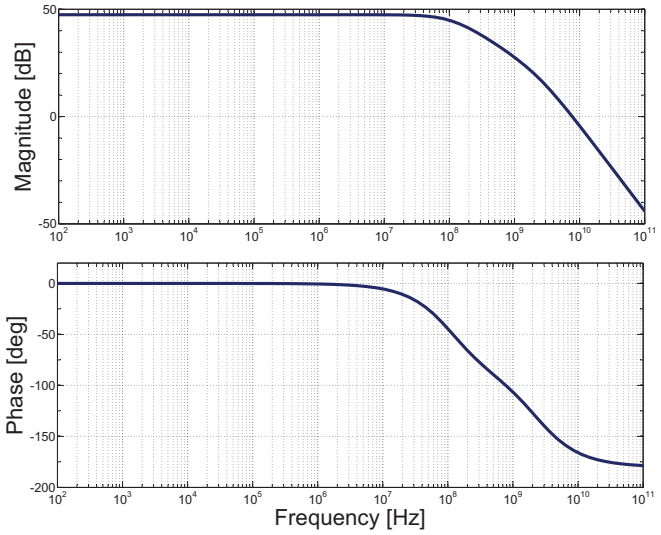

Figure 3.22: magnitude and phase of the loop transfer function of the CSA output stage.

scaled up by a factor of 10.

The noise of the CSA has been simulated in the frequency range between 1 Hz and 100 MHz. As depicted in Figure 3.28, the noise voltage spectrum exhibits a flicker noise component at low frequencies and a white noise contribution at high frequencies. For frequencies higher than 100 MHz, the noise contribution of the cascaded stages become relevant. In the simulated frequency range, the input voltage noise spectrum can be modeled as follows:

$$S_v(f) = a_w + \frac{a_f}{f} \tag{3.39}$$

where the first term, a_w, accounts for the frequency independent contribution and the second one represents the flicker noise, depending on the power coefficient a_f. The input referred noise of the CSA has been estimated by taking into account a cascaded time variant filter implementing a trapezoidal weighting function with a flat top duration equal to the integration phase, as in the case of the PixFEL project. As expressed in [28], the ENC is given by the following equation:

$$ENC^2 = C_{eq}^2 \left(\frac{a_w}{\tau} \cdot A_1 + 2 \cdot \pi \cdot a_f \cdot A_2 \right) \tag{3.40}$$

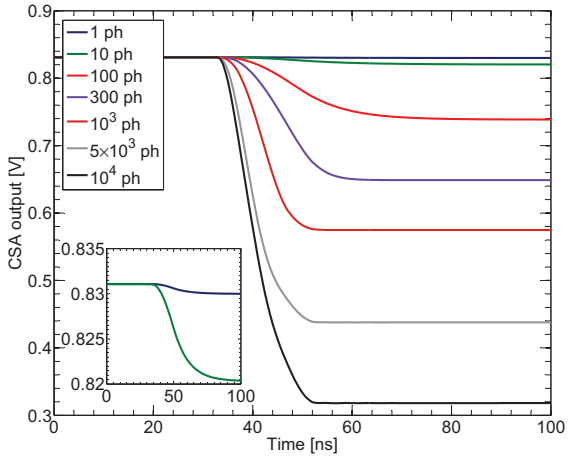

Figure 3.23: transient response of the CSA for different input signals. The input current pulse duration is 15 ns. The inset shows the response for small input signals.

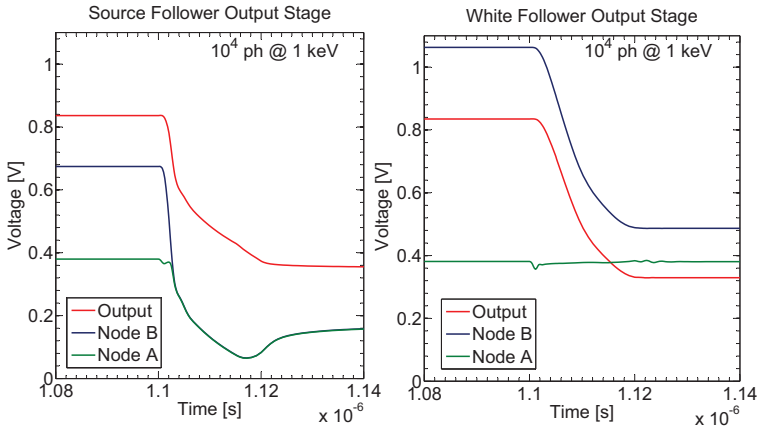

Figure 3.24: transient response of the voltages at the output, at node B and at node A, with a PMOS based source follower (left) and the proposed White follower configuration (right).

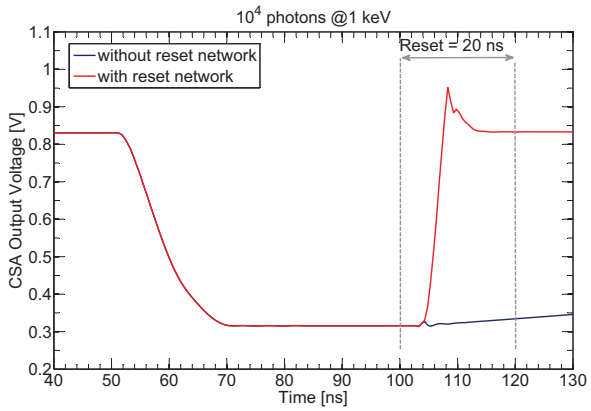

Figure 3.25: transient response of the CSA without (blue) and with (red) the reset network.

where C_{eq} is the total capacitance shunting the input node, A_1 and A_2 are the filter parameters depending on the shape of the weighting function ($A_1 = 2$ and $A_2 = 1.38$ for a trapezoidal weighting function) and τ is the shaping time.

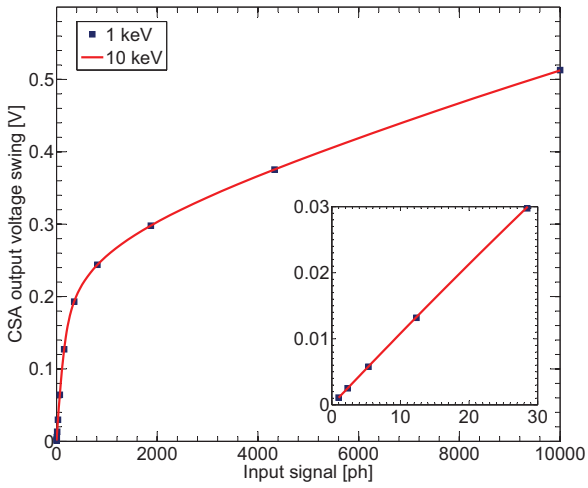

Figure 3.26: transcharacteristic of the CSA with dynamic signal compression. The inset shows the characteristic for small input signals.

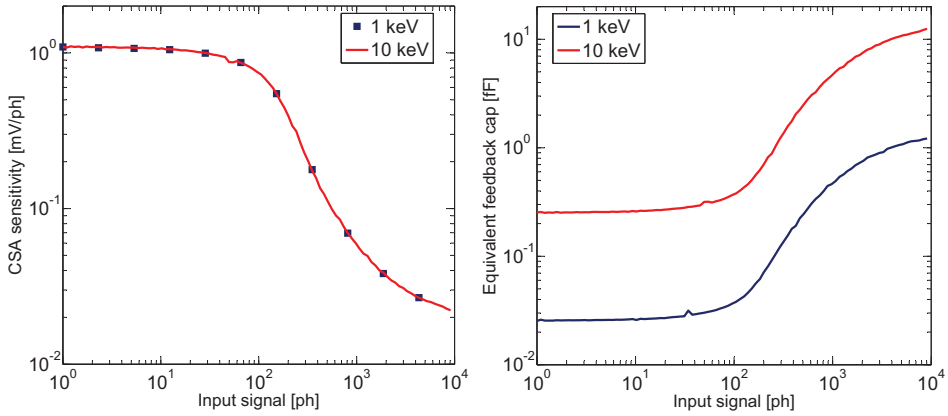

Figure 3.27: CSA sensitivity (left) and equivalent feedback capacitance (right) as functions of the input signal.

In order to evaluate the ENC in the worst case condition, given by the highest conversion rate limit of 5 MHz, the shaping time τ, which is the duration of both the rising and falling edge of the trapezoidal weighting function, is 50 ns.

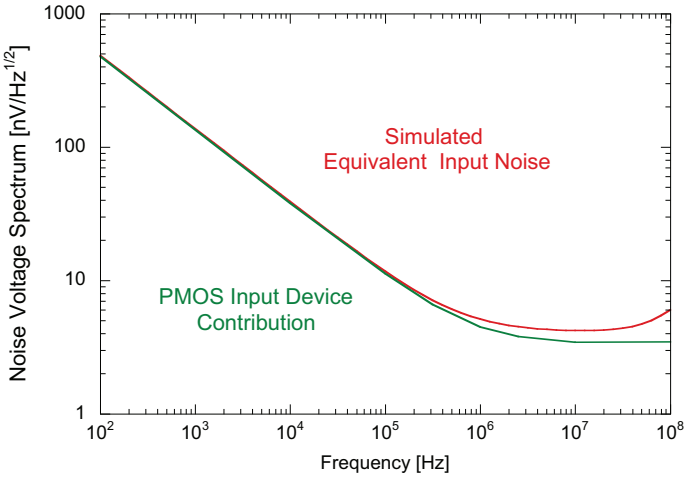

Figure 3.28: input noise voltage spectrum of both the CSA and the input device, M_0.

The equivalent input capacitance term is given by the following contributions:

$$C_{eq} \approx C_D + C_{in} + C_{ef} + C_{stray} \tag{3.41}$$

where C_D is the detector capacitance, about 70 fF for a $100\,\mu\text{m} \times 100\,\mu\text{m}$ pixel area, C_{in} is the input device capacitance, about 50 fF, C_{ef} is the equivalent feedback capacitance and C_{stray} is the parasitic capacitance due to the bonding, around 50 fF. The worst case is given by the minimum input signal of 1 photon at 1 keV, where the total feedback capacitance is about 45 fF. The ENC for an input signal of 1 photon at 1 keV, computed by taking into account noise sources in the CSA only, results to be close to 50 e^- RMS, leading to a minimum SNR of 5.6.

Schematic of the CSA

The schematic view of the overall CSA is shown in Figure 3.29, whereas the aspect ratios, the passive components values, the DC currents and DC voltages are summarized in Table 3.3.

Layout of the CSA

The layout of the CSA has been carried out in order to fit the stage into the reference area of the PixFEL project, that is a squared pixel with a pitch of 100 μm. As shown in Figure 3.30, the CSA has been laid out in the bottom

Name	Value	Name	Value	Name	Value	Name	Value
M_0	40/0.15	M_{72}	6/1.5	$M_{x,1}$	10/1	$I_{B,1}$	45.5 μA
M_1	5/2	M_{73}	1/5	$M_{x,2}$	5/0.2	$I_{B,2}$	800 nA
M_2	2/0.15	M_{10}	50/0.06	M_f	40/4	$I_{B,3}$	4 μA
$V_{B,0}$	600 mV	M_{11}	5/0.06	C_f	25 fF	$I_{B,4}$	32 μA
M_4	8/1	M_{12}	5/0.06	$M_{f,he}$	360/4	$I_{B,5}$	25 μA
M_{41}	20/1	M_{121}	2/4	$C_{f,he}$	250 fF	R_s	80 Ω
M_{42}	1/10	M_{122}	2/2	M_{he}	100/0.06	C_c	800 fF
M_7	5/0.15	M_{13}	12/2.3	$M_{sr,D}$	9.2/0.06	V_A	400 mV
M_{71}	6/1.5	M_{14}	1.5/4	M_{sr}	20/0.06	V_B	1 V

Table 3.3: Aspect ratios, passive components values, DC currents and DC voltages of the CSA.

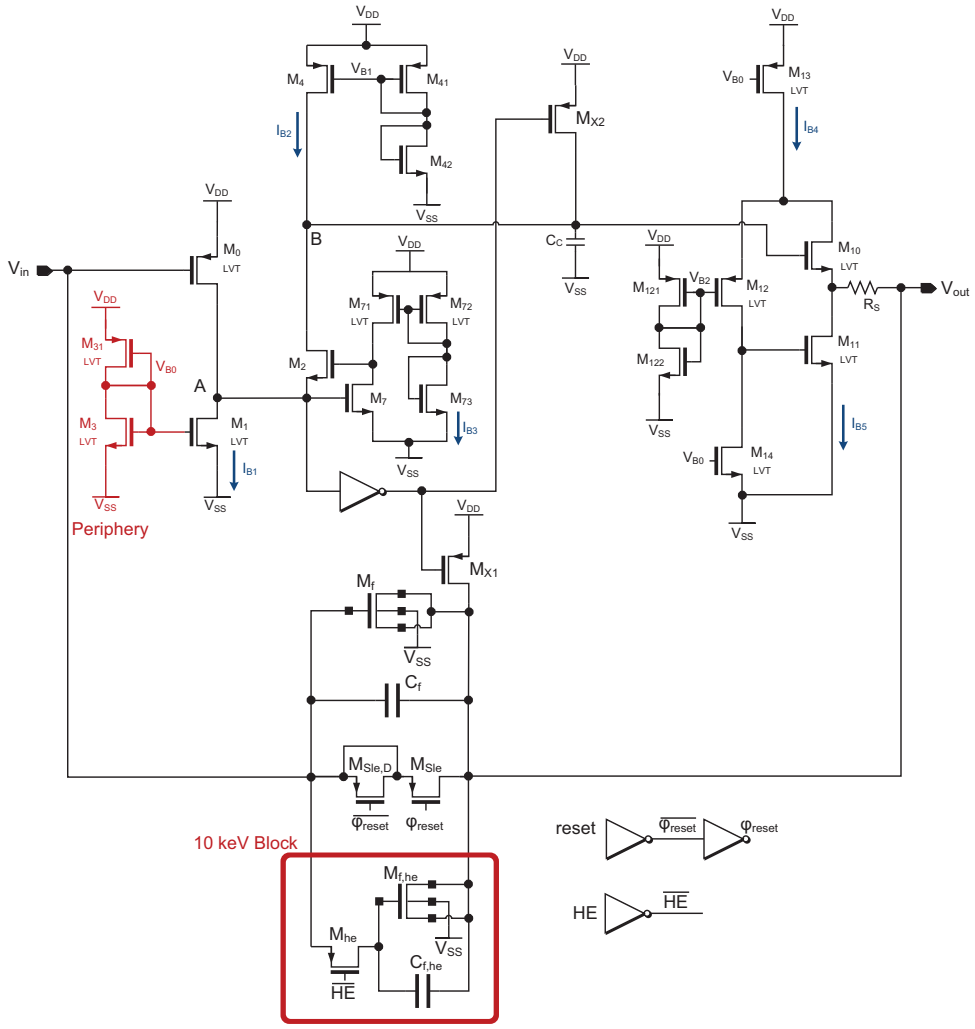

Figure 3.29: schematic view of the overall CSA. The current reference located in the periphery of the chip is depicted in red.

of the feedback transistor providing the signal compression. 10 elementary devices, with an aspect ratio of $^{40}/_{4}$, have been arranged in a 2×5 array fashion. The MIM capacitances improving the sensitivity precision for small input signals have been placed above the feedback device. Finally, forward

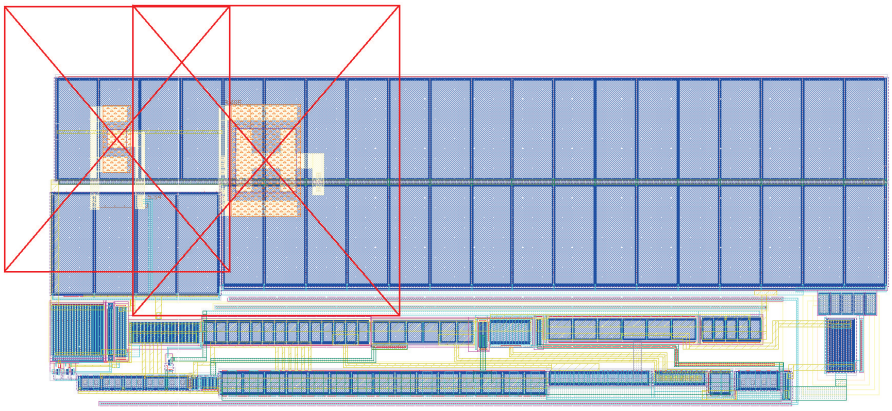

Figure 3.30: layout view of the CSA.

stage transistors have been laid out at the bottom, with the input device on the left hand side and the output one on the right hand side. The CSA occupies an area of 85×33 μm^2.

CSA specifications

The overall specifications of the CSA are summarized in Table 3.4.

3.2.3 The PixFEL analog front-end

Figure 3.31 shows the conceptual schematic view of the analog front-end for the PixFEL project. As already mentioned, the CSA is followed by a time variant shaping stage, which consists of a transconductance amplifier converting the CSA output voltage into a current, and a gated integrator performing correlated double sampling. In the following, a description about the building blocks of the shaping stage is given, along with a summary of the main performance of the overall analog channel.

[1]Computed by taking into account an ideal time variant filtering stage operating with a shaping time of 50 ns and a trapezoidal weighting function.

Voltage to current conversion

The CSA output voltage is converted into a current to be fed at the input of the gated integrator performing correlated double sampling. The archiecture of the voltage-to-current conversion stage is shown in Figure 3.32. It is based on a transconductance amplifier, with an additional network (depicted in red) inserted with the purpose of improving the linearity for the input dynamic

Specification	Value
GBP	140 MHz
Phase margin	$\geq$ 60 deg
Fall time	$\leq$ 25 ns
Output swing	500 mV
S_{lq}	1 mV/ph
S_{hq}	20 μV/ph
ENC [1]	$\approx$ 50 e^- RMS
SNR	$\geq$ 5.6
Power consumption	90 μW
Area occupancy	2805 μm^2

Table 3.4: main specifications of the CSA.

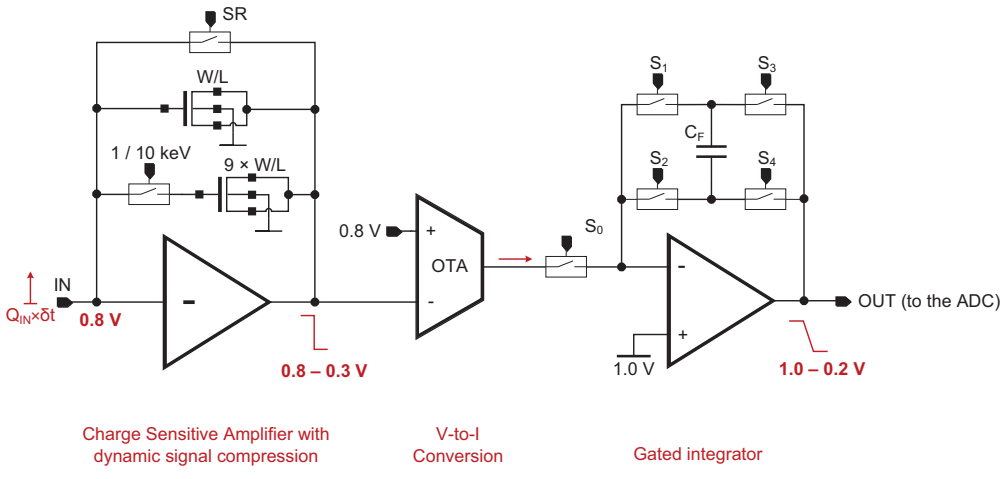

Figure 3.31: simplified schematic of the PixFEL analog front-end.

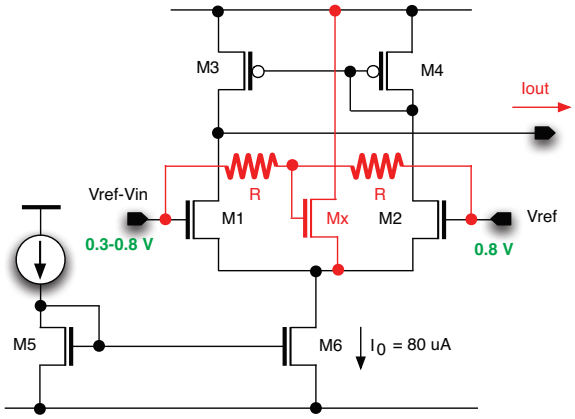

Figure 3.32: schematic view of the transconductance amplifier performing the voltage-to-current conversion.

range of 0.5 V, and therefore leaving unchanged the almost bi-linear characteristic of the CSA. It can be shown that the output current of the stage is given by the following equation:

$$I_{out} = \frac{\sqrt{2 \cdot \beta_{1,2} \cdot I_0}}{A} \cdot \sqrt{1 - \frac{\beta_{1,2} \cdot V_{in}^2}{2 \cdot I_0}} \cdot V_{in} \tag{3.42}$$

where $\beta_i = 1/2 \cdot \mu_0 \cdot C_{ox} \cdot W_i/L_i$ is the transconductance parameter, i denotes the i-th transistor, and A is defined as follows:

$$A = \sqrt{1 + \frac{\beta_X}{2 \cdot \beta_{1,2}}} \tag{3.43}$$

The bias current of the stage, I_0, has been set to 80 μA, whereas the reference voltage at the inverting input, V_{ref}, corresponds to the CSA DC output voltage, that is 0.8 V. The aspect ratios of the transistors, as well as the value of the resistor R, are summarized in Table 3.5. The circuit has been designed in order to set A to 5 and achieve a transconductance of about 30 μA/V. The benefit of the linearization network is highlighted in Figure 3.33, where a comparison with respect to a classic transconductance amplifier is shown. As it can be noticed, the circuit features a linear response over the input voltage range of 0.5 V. The layout of the transconductance stage is shown in Figure 3.34. In order to reduce any mismatch effect between the two input transistors and the two active loads, interdigitation as well as dummy devices have been used. The stage occupies an area of about 35 $\times$ 18 μm^2.

Name	Value
M_1, M_2	$^{0.7}/_{1}$
M_3, M_4	$^{20}/_{1.5}$
M_6	$^{20}/_{0.5}$
M_X	$^{4.8}/_{0.2}$
R	12 $k\Omega$

Table 3.5: values of the components of the transconductance amplifier.

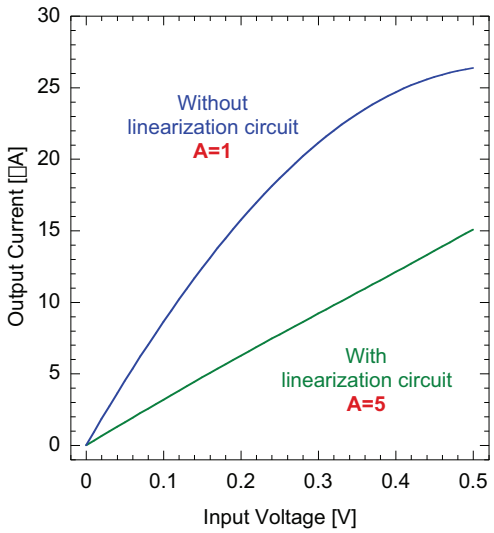

Figure 3.33: transcharacteristic of the transconductor amplifier without (blue) and with (green) the linearization network.

Gated integrator

The voltage-to-current conversion stage is followed by a gated integrator performing correlated double sampling in a single compact stage, based on the same solution proposed for the DSSC [19], the Flip Capacitor Filter (FCF). As shown in the schematic of the overall analog front-end of Figure 3.31, the basic idea is to exploit a feedback network, arranged in an H-bridge fashion, to flip the feedback capacitance, and integrate first the baseline (i.e. the current at the output of the transconductance amplifier when no signal is collected

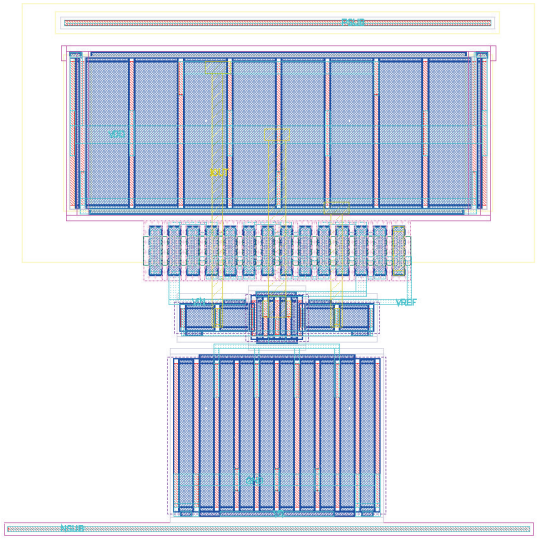

Figure 3.34: Layout view if the transconductance amplifier.

at the input electrode) and then the signal (i.e. the current at the output of the transconductance amplifier when a signal has been collected at the input electrode and a negative step has occured at the CSA output). As shown in Figure 3.35, the circuit operation consists of 4 phases:

1. **Baseline integration:** the baseline of the CSA is sampled on the feedback capacitance of the FCF. Switches S_0, S_1 and S_4 are closed, whereas switches S_2 and S_3 are open.

2. **Signal settling and capacitance flipping:** the charge is collected at the input electrode and a negative step occurs at the output of the CSA. In the meantime, the feedback capacitance of the FCF is flipped by simultaneously opening S_1 and S_4 and closing S_2 and S_3, respectively. Switch S_0 is always open, for no current needs to be integrated.

3. **Signal integration:** once the CSA output has settled, the signal is integrated. Since the capacitance is flipped, the baseline contribution is subtracted and only the signal contribution is stored. Switches S_0, S_2 and S_3 are closed, whereas switches S_1 and S_4 are open. The FCF output voltage is stored in the capacitive DAC of the SAR ADC.

4. **Reset:** both the CSA and the FCF are reset. To restore the charge in

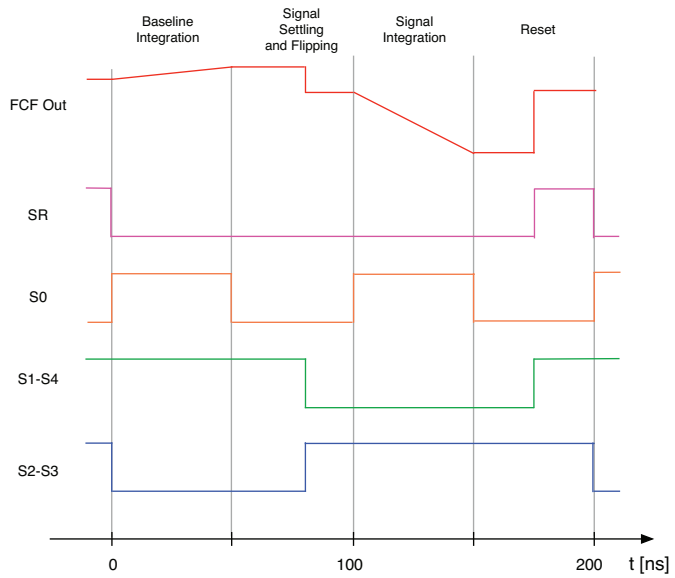

Figure 3.35: timing diagram of the FCF operating at 5 MHz. Operation at lower frequencies can be obtained by scaling properly the signals duration.

the CSA, signal SR is hold high, whereas the FCF is reset by closing all the feedback switches, S_1, S_2, S_3 and S_4. Switch S_0 is open.

The forward stage of the FCF, shown in Figure 3.36, consists of a two stages class AB Operational Transconductance Amplifier (OTA) [32]. Thanks to the source follower stage based on M_8 and M_9, the output of the first differential stage drives both M_6 and M_5 in a push-pull fashion, thus enabling the overall stage to drive the large capacitive DAC of the SAR ADC, estimated in about 2.5 pF. It can be shown that the small signal transfer function of the circuit is given by the following equation:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{2} \cdot g_{m,2} \cdot r_{ds,4} \cdot \frac{\left(1 - \frac{C_c \cdot s}{g_{m,5}+g_{m,6}}\right)}{1 + R_{eq} \cdot (C_c + C_L) \cdot s} \cdot R_{eq} \cdot (g_{m,5} + g_{m,6}) \quad (3.44)$$

where $R_{eq} = r_{ds,5} \parallel r_{ds,6}$. The DC gain of the stage can be achieved by studying Equation 3.44 for $s \to 0$, thus leading to the following DC small signal response:

$$v_o = \frac{1}{2} \cdot g_{m,2} \cdot r_{ds,4} \cdot (g_{m,5} + g_{m,6}) \cdot (r_{ds,6} \parallel r_{ds5}) \cdot v_{in} \quad (3.45)$$

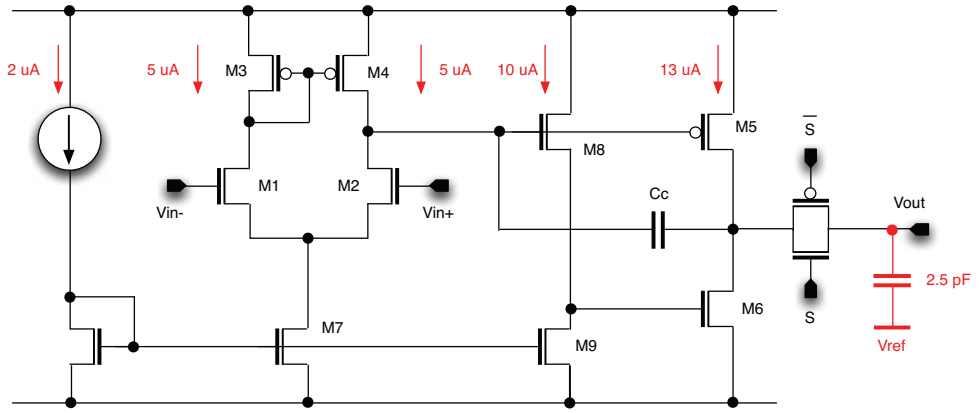

Figure 3.36: schematic view of the FCF forward stage.

Figure 3.37 shows the Bode diagrams of magnitude and phase of the stage, achieved from both simulations and Equation 3.44. Despite the contribution of the zero in the right hand side s-plane, which may jeopardize the stability of the system, the stage features a phase margin higher than 60 degrees and a DC gain of about 50 dB. The aspect ratios of the transistors and the value of C_c are summarized in Table 3.6.

Name	Value
M_1, M_2	$^{2.5}/_{0.5}$
M_3, M_4	$^{5}/_{1}$
M_5	$^{10}/_{0.1}$
M_6	$^{2.5}/_{0.2}$
M_7	$^{4}/_{1}$
M_8	$^{2.5}/_{0.12}$
M_9	$^{4}/_{1}$
C_c	30 fF

Table 3.6: values of the components of the FCF forward stage.

The feedback network of the FCF has been designed in order to fit 1 photon into 2 ADC bins for the small input signal region, with a 5 MHz operation and therefore an integration time, τ, of 50 ns. Since 1 ADC bin corresponds,

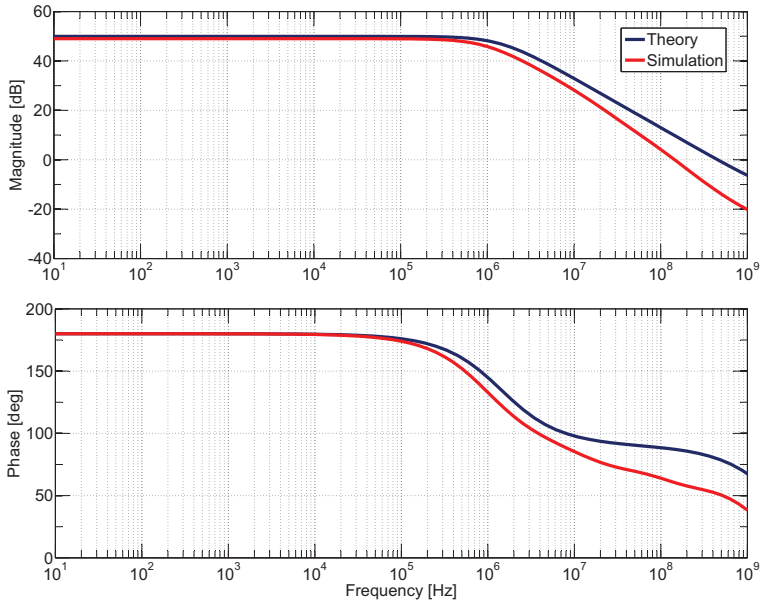

Figure 3.37: Bode plot of the FCF forward stage.

by design, to about 800 μV, the value of the feedback capacitance can be obtained from the following equation:

$$C_f = \frac{G_m \cdot S_{lq,CSA} \cdot \tau}{g_{FCF}} = 940 \text{ fF} \tag{3.46}$$

where G_m is the gain of the transconductance amplifier, 30 μA/V, $S_{lq,CSA}$ is the CSA sensitivity for small input signals, 1 mV/ph, and g_{FCF} is the expected FCF gain, 1.6 mV/ph. With such a configuration, the analog front-end of the PixFEL project features a sensitivity of 1.6 mV/ph and an output dynamicr range of 800 mV.

The layout view of the FCF is shown in Figure 3.38. The forward stage and all the switches have been laid out in the top section. The current mirrors, the input transistors and the active loads have all been laid using interdigitated and dummy devices.

The main specifications of the FCF, achieved in closed loop configuration, are summarized in Table 3.7.

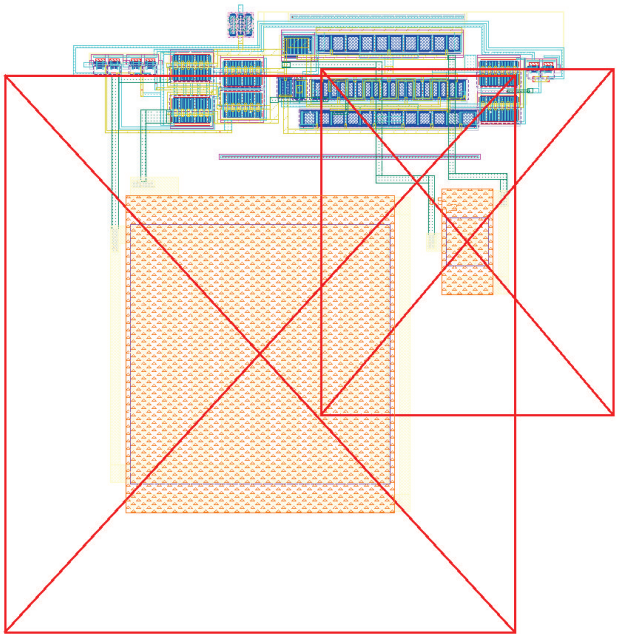

Figure 3.38: layout view of the FCF.

Name	Value
DC gain	53 dB
GBP	400 MHz
Phase margin	60 deg
Power consumption	42 μW
Area occupancy	1000 μm^2

Table 3.7: main specifications of the FCF.

Simulation results of the analog front-end

The analog front-end has been simulated in a 5 MHz operation with the same timings presented in Figure 3.35.

The time response to different input signals are shown in Figure 3.39, highlighting the signal compression at the output of the FCF. Figure 3.40 shows the characteristic between the input of the CSA and the FCF output (left)

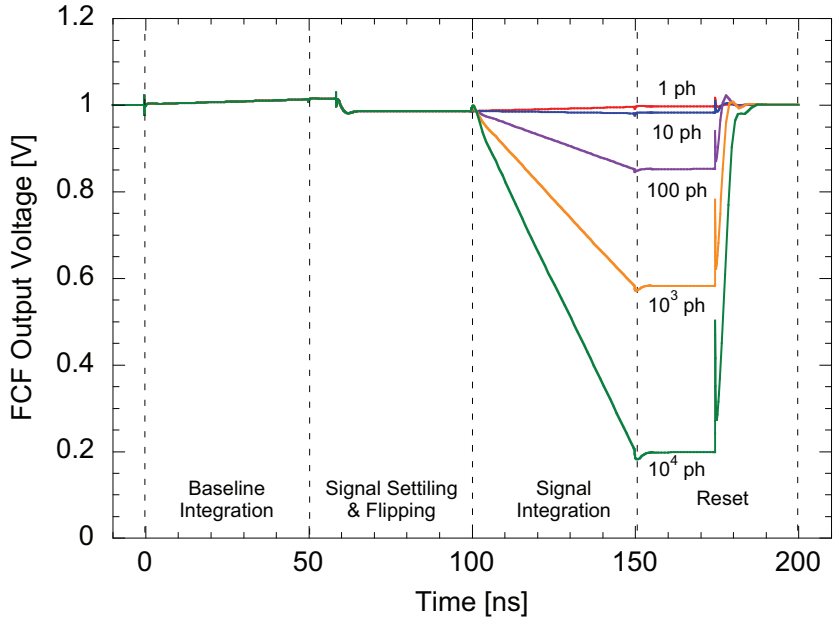

Figure 3.39: FCF output voltage operated at 5 MHz.

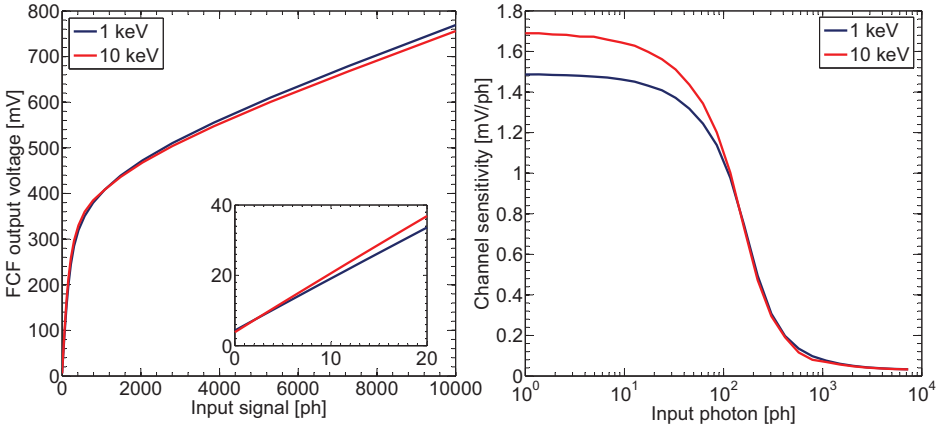

Figure 3.40: transcharacteristic (left) and sensitivity (right) of the analog front-end.

and the sensitivity of the channel as a function of the input signal amplitude (right), for both the energy configurations. For small input signals, the channel features a sensitivity of 1.5 mV/ph and 1.65 mV/ph, respectively for the 1 keV and the 10 keV configuration, and a non-linearity lower than 0.08 ph. The weighting function of the analog front-end has been simulated by applying an input signal with an increasing delay time starting from 0 to the end of the 200 ns processing period. Figure 3.41 shows the simulated weighting function with the FCF only and with all the analog blocks at both 1 keV and 10 keV. The deviation from the ideal weigthing function, which can be detected in the case of the complete channel at the two different photon energies, is due to the finite response time of the CSA, which is shorter in the 10 keV case. The actual ENC of the analog channel has been computed by performing iterated transient noise simulations for different input signals, with the same time constraints of Figure 3.35. Then, the standard deviation of the FCF output voltage at the end of the conversion, $\sigma_{v,out}$, has been evaluated and referred

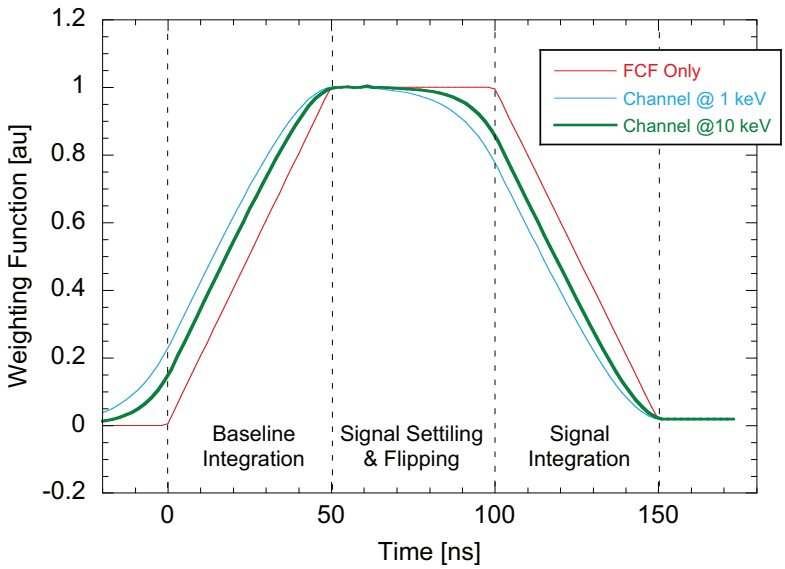

Figure 3.41: comparison between the weighting function simulated with the flipped capacitor filter only and with the overall analog blocks at both 1 keV and 10 keV.

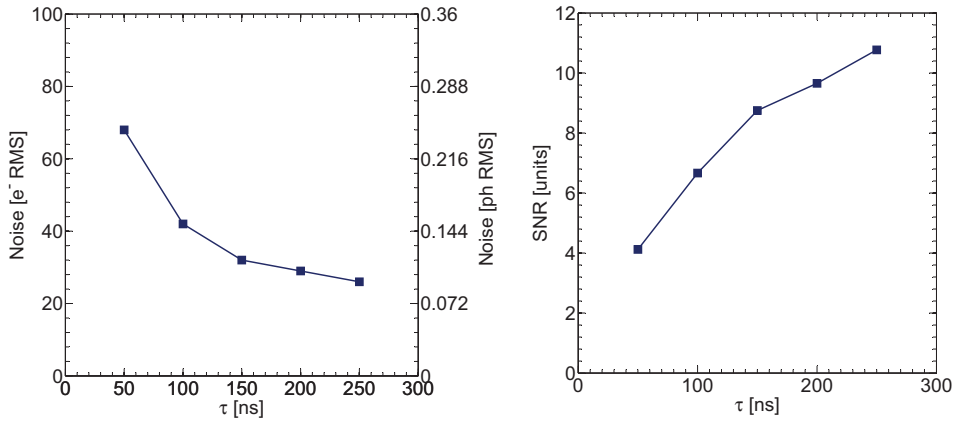

Figure 3.42: ENC (left) and SNR (right) of the analog front-end for 1 photon input signal at different integration times.

to the input of the channel, according to the following equation:

$$ENC = \sigma_{v,out} \cdot \frac{C_f}{S_{CSA} \cdot G_m \cdot \tau} \tag{3.47}$$

where C_f is the FCF feedback capacitance, S_{CSA} is the CSA sensitivity for the applied input signal and G_m is the gain of the transconductance amplifier. The results achieved for the minimum input signal, that is 1 photon with an energy of 1 keV, are shown in Figure 3.42 (left), for different integration times between 50 ns and 250 ns. In such conditions, an ENC lower than 70 electrons RMS, has been obtained. This value of ENC corresponds to about 0.25 photons RMS, and therefore a SNR higher than 4, as shown in Figure 3.42 (right). With such performance, the analog front-end of the PixFEL project is able to provide single photon detection. Figure 3.43 shows the input RMS noise for small input input signals (left) and in the overall input dynamic range (right). The results, achieved with an integration time of 50 ns, show that the noise is dominated by the Poisson photon generation process, and therefore prove the suitability of the designed analog front-end for high resolution X-ray FEL applications. As a last remark, the main specifications of the analog front-end designed for the PixFEL project are summarized in Table 3.8, along with the deviations obtained from Monte Carlo simulations.

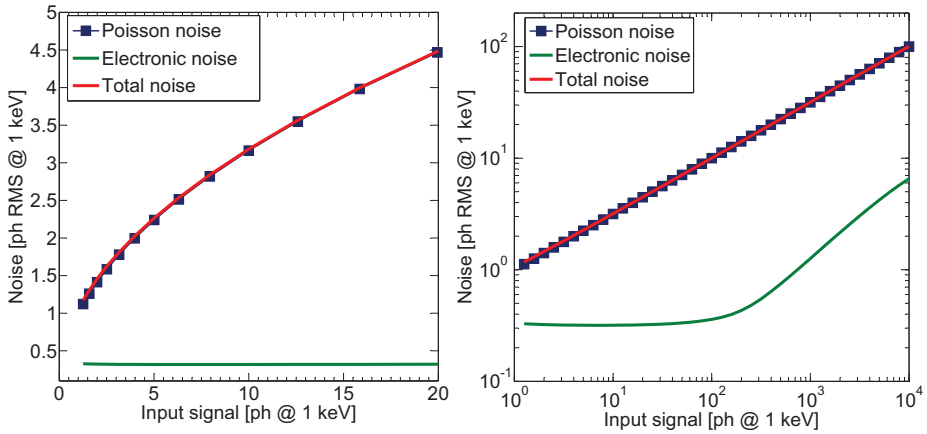

Figure 3.43: SNR achieved with a 50 ns integration time in the 10^4 photons input dynamic range.

Specification		Value
S_{lq}	1 keV	1.5 ± 0.03 mV/ph
	10 keV	1.65 ± 0.03 mV/ph
S_{hq}	1 keV	33 μV/ph ± 0.24 μ/ph
	10 keV	33 μV/ph ± 0.25 μ/ph
INL (0÷20 ph)	1 keV 10 keV	0.06 ph 0.08 ph
Input range		10000 ph
Output swing		800 ± 10 mV
SNR		$\geq$ 4.5
Power consumption		230 μW
Area occupancy		4492 μm^2

Table 3.8: main specifications of the analog front-end.

3.2.4 First submission of the PixFEL readout channel

The first submission of the chip designed in the framework of the PixFEL project took place during Fall of 2014. In order to test the readout channel

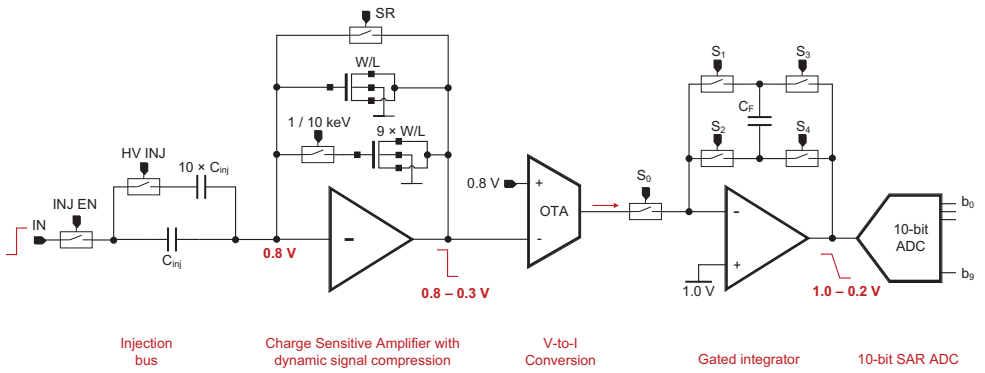

Figure 3.44: schematic of the submitted PixFEL readout channel.

without bump bonding the sensor, an injection bus has been inserted before the CSA. As shown in the readout channel schematic view of Figure 3.44, the injection bus consists of an injection capacitance, C_{inj}, with a value of about 50 fF. In order to perform tests in the wide input dynamic range of 10^4 photons without applying an excessively high voltage step at the input, an additional injection capacitance of 450 fF, selectable by means of the `HV_INJ` signal, has been inserted. The injection bus can be enabled by means of the `INJ_EN` signal.

The layout of the analog front-end is shown in Figure 3.45. The shaping stage has been placed on the top-right side of the CSA, whereas the injection bus has been laid out on the top-left of the CSA. The first prototype chip submitted in the framework of the PixFEL collaboration, shown in Figure 3.46 (left), consits of an 8×8 pixels readout ASIC, integrating the analog front-end, the SAR ADC, digital readout circuits, and some blocks at the periphery providing the bias and control signals. The layout of the single pixel is depicted in Figure 3.46 (right). The SAR ADC, occupying most of the pixel area (74×97 μm^2), has been placed on top, the analog front-end on the bottom-left and the digital readout logic on the bottom-right. The pixel size is 110×110 μm^2. Along with the 8×8 pixels matrix, a test structures matrix has been submitted. The chip, shown in Figure 3.47, integrates the single building blocks of the analog front-end and several versions of the SAR ADC. As far as the analog blocks are concerned, the following structures have been integrated:

- A CSA with an NMOS feedback transistor for the dynamic signal com-

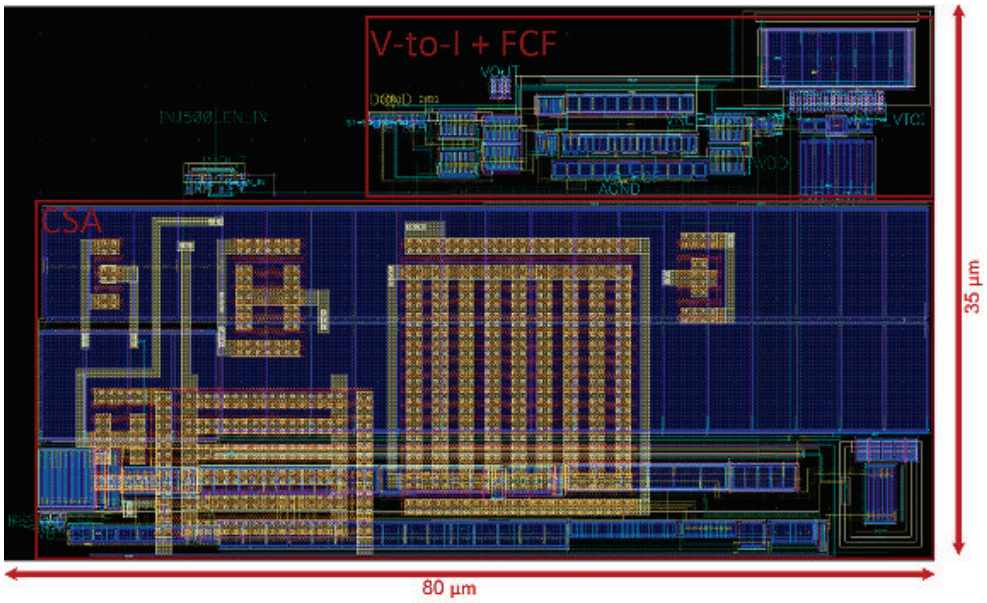

Figure 3.45: layout of the analog front-end.

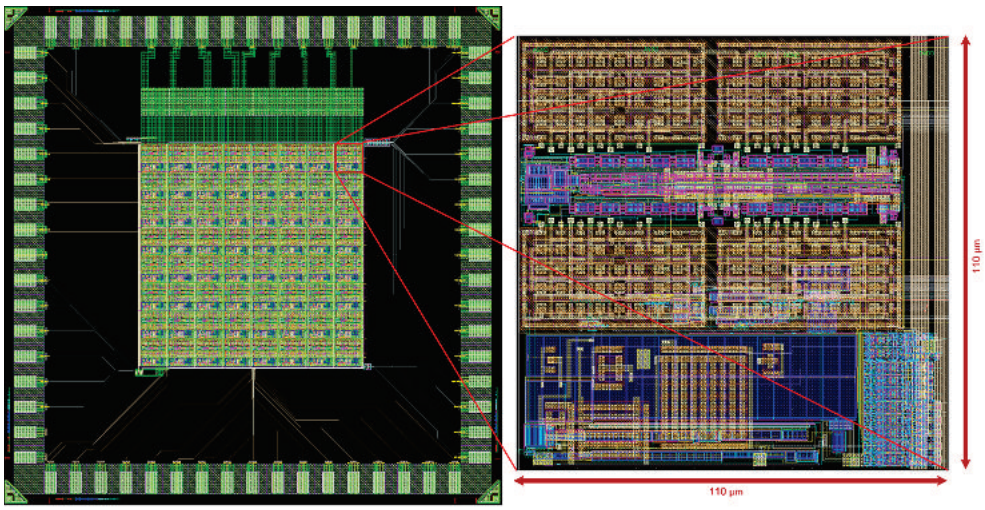

Figure 3.46: layout view of the submitted 8 × 8 readout channels matrix.

pression.

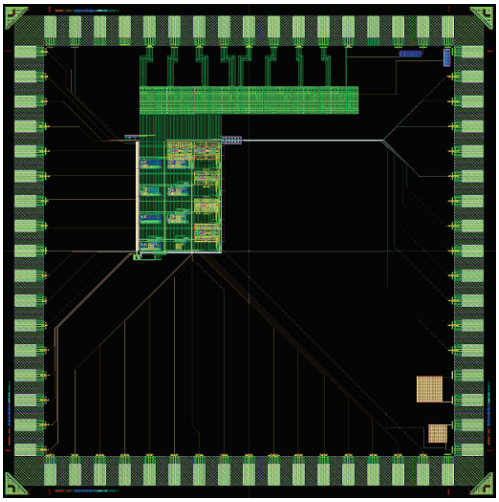

Figure 3.47: layout view of the submitted matrix with the test structures.

- A CSA with a PMOS feedback transistor for the dynamic signal compression.
- A CSA with an NMOS feedback transistor for the dynamic signal compression and without the injection bus. In this case, an external injection capacitance has to be used.
- An analog front-end with an NMOS feedback transistor in the CSA.
- An analog front-end with a PMOS feedback transistor in the CSA.
- An analog front-end with an NMOS feedback transistor in the CSA and without the injection bus. In this case, an external injection capacitance has to be used.
- A standalone shaping stage, with the transconductance amplifier followed by the FCF.

3.3 Characterization of the analog front-end

In this section, the characterization activity, carried out on the submitted test structures, is described. First, an overview about the test system used to perform automated tests is given. Then the measurement results are presented, starting from the single building blocks toward the overall analog front-end.

3.3.1 Test setup

In order to carry out automated and systematic measurements, a proper test system has been developed. The hardware of the test system consists of two Printed Circuit Boards (PCBs):

- **Main board:** the *Main board* hosts all the circuitry providing the bias and the digital fast and slow control signals to the chip, as well as the analog inputs for the injection bus. In particular, the following blocks are employed:
  - Adjustable voltage regulators for the power supply (analog and digital V_{DD}).
  - Voltage references for the analog front-end blocks and for the SAR ADC.
  - Current references for the analog front-end blocks.
  - 16-bit DAC, to be controlled via SPI, for the characterization of the SAR ADC.

  It embeds 4 arrays of terminal strips, placed in the center of the board and arranged in a squared fashion, which enables the connection to the

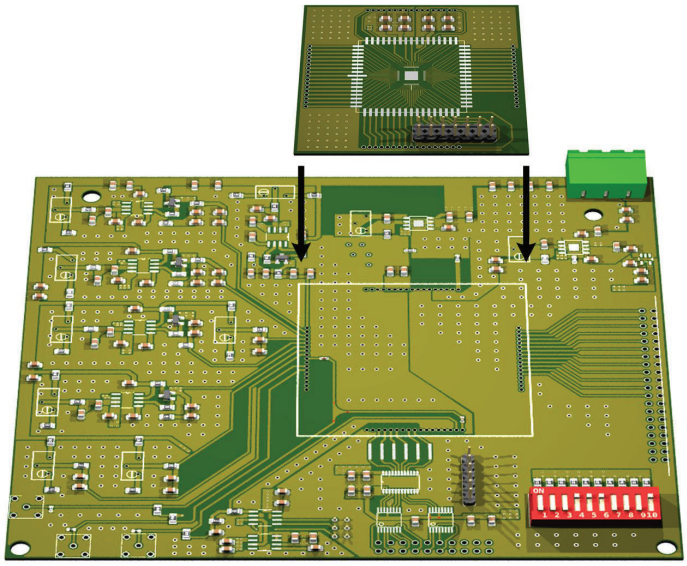

Figure 3.48: 3D sketch of the *Main board* and the *ASIC carrier*.

board hosting the ASIC. The PCB has been designed in a 4 layers FR4 technology with through all vias.

- **ASIC carrier:** the *ASIC carrier* hosts the test structures chip (to be either soldered or wire bonded to the board). It plugs to the main board by means of 4 arrays of terminal sockets arranged in a squared fashion and placed at the edges of the board. The *ASIC carrier* receives all the bias and digital control signals from the *Main board* and hosts a 7×2 terminal strip providing the analog output signals.

Figure 3.48 shows the 3D sketch of both the *Main board* (bottom) and the *ASIC carrier* (top). As shown in Figure 3.49, the test system is based on the following blocks:

- A pattern generator (Agilent 1673G), providing the fast digital control signals for the CSA, FCF and ADC operation.
- A function generator (Agilent 33220A), providing the voltage pulse to be applied at the input of the inject bus.
- A STM32F4 evaluation board for the programming of the 16-bit DAC via SPI.

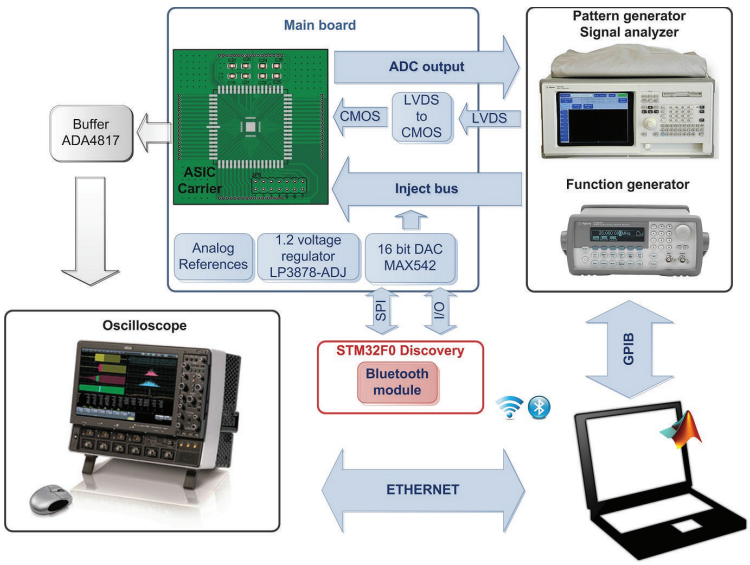

Figure 3.49: Block diagram of the test system.

- A low-noise, low input capacitance, low bias current buffer board (based on the ADA4817 OpAmp), to be connected to the analog outputs available on the *ASIC carrier* and able to drive large capacitive loads (like the passive probe of an oscilloscope).
- An oscilloscope (Lecroy WavePro 735Z), to be connected to the buffer board and to perform measurements on the output signals (e.g. amplitude, fall time).
- A computer running the Matlab environment, controlling the instruments and collecting the output data. It is connected via GPIB to both the pattern generator and the signal generator, via Bluetooth V3 to the microcontroller board, and via ethernet to the oscilloscope.

3.3.2 Measurement results

In the following, the measurement results achieved on the analog front-end are presented, by focusing first on the single building blocks and then on the overall signal processing chain.

Charge sensitive amplifier

The characterization activity on the CSA has been focused on the NMOS based test structures integrating the injection bus. A proper voltage step has been applied at the input of the injection bus by taking into account the following relation between the amplitude of the voltage step and the equivalent signal in photons, ph_{in}:

$$ph_{in} = \frac{C_{inj} \cdot \Delta V_{inj} \cdot \varepsilon_i}{q \cdot E} \tag{3.48}$$

where ΔV is the amplitude of the voltage step, q is the elementary charge, E is the energy of the incoming photons and ε_i is the average energy required for generating one electron-hole pair in silicon (3.6 eV). Depending on the purpose of the measurement, the following injection capacitances have been used:

- The 50 fF injection capacitance has been used to measure the CSA output for small input signals, for both the 1 keV and 10 keV configurations. In this case, a voltage step of 1 mV and 10 mV needs to be applied at the input of the injection bus in order to collect a charge corresponding to 1 photon, respectively for the 1 keV and 10 keV configurations.
- The 500 fF injection capacitance has been used to measure the CSA output in the overall input dynamic range in 1 keV configurations. In

10 keV configuration, it is possible to study the response up to about 1200 photons, for the input pads of the chip accept voltages up to V_{DD}, that is 1.2 V.

Figure 3.50 shows the transient response of the CSA during both the injection of a signal corresponding to 1200 photons and the reset phase. As it can be noticed, the fall time is within the specification of 25 ns (23 ns from measurement), and the reset is carried out as expected. The same results in terms of fall time and reset time have been achieved in the overall input range of 10^4 photons, and for all the measured chips. The transcharacteristic of the CSA in 1 keV configuration, is shown in Figure 3.51, as the average value of the results from the measured chips, along with the results obtained from simulation. Error bars on the blue curve show the standard deviation in the measurement results. As it can be noticed, the transition between the high and the small sensitivity regions is sharper in the measurement than in the simulation. This point does not represent a concern, for the sensitivities in both the regions are within the expected values, as it can be noted from the insets. As far as the 10 keV configuration is concerned, Figure 3.52 shows the measured characteristics together with the simulation results for small input signals (left) and in the 1200 photons input range (right). Besides the difference in the transition, it can be noticed that the measured small signal

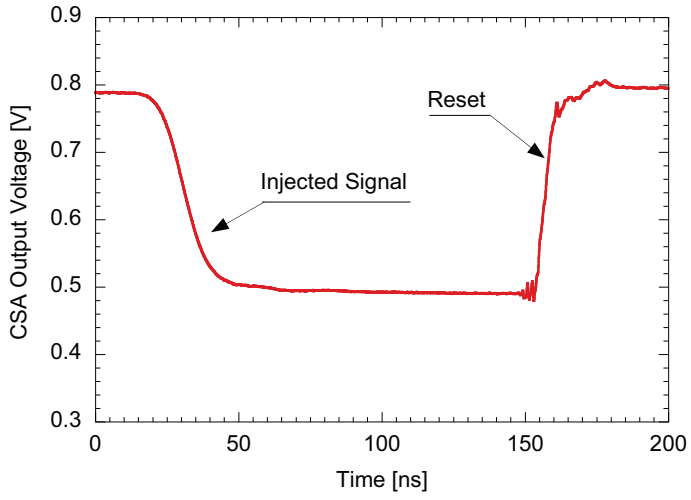

Figure 3.50: transient response of the CSA for an input signal corresponding to 1200 photons.

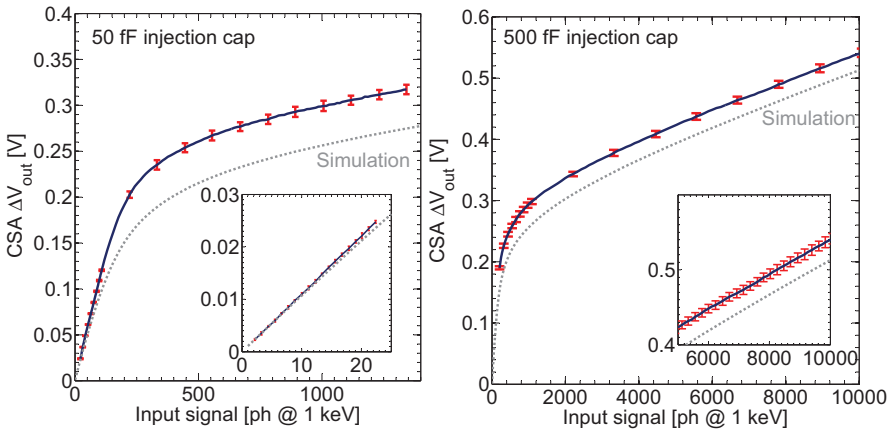

Figure 3.51: average value and standard deviation of the transcharacteristic of the CSA at 1 keV with the 50 fF (left) and 500 fF (right) injection capacitances. The inset shows the response in the first 20 photons input range (left) and between 5000 photons and 10000 photons (right).

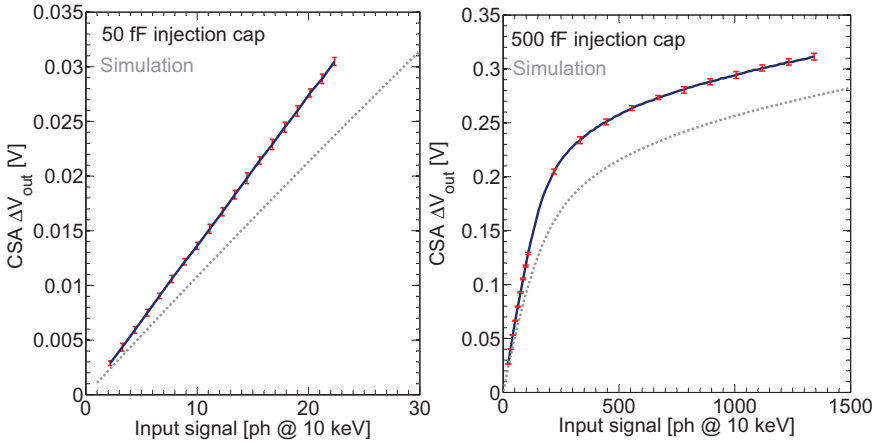

Figure 3.52: average value and standard deviation of the transcharacteristic of the CSA at 10 keV with the 50 fF (left) and 500 fF (right) injection capacitances.

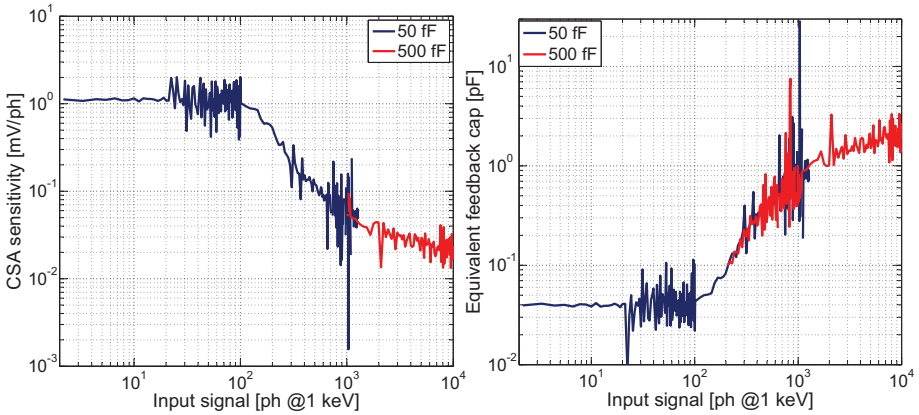

Figure 3.53: CSA sensitivity (left) and equivalent feedback capacitance (right) in both the 1 keV and 10 keV configurations and with both the injection capacitances (chip #7).

sensitivity is higher than the expected value. This represents a minor concer, for X-ray imagers tipically integrate in-pixel circuitry for the calibration of the readout channels. The sensitivity and the equivalent feedback capacitance at 1 keV, computed according to Equation 3.1 and Equation 3.2, are shown in Figure 3.53, for a single chip. The spikes in the plots are due to the derivative operation on the high resolution measurements in the transition region. It can be noticed that the sensitivities at 1 keV are very close to the specification values of 1 mV/ph for small signals and 20 μV/ph for large signals, with equivalent feedback capacitance values of about 35 fF and 20 pF. As summarized in Table 3.9, the CSA performance are in good agreement with the specifications.

Shaping stage

The shaping stage has been characterized by means of the function generator and with the same timings of the channel operation. During the baseline integration, a voltage close to the value of the non-inverting input reference of the transconductance amplifier (0.8 V) has been applied. Then, in order to emulate the CSA output voltage, a negative voltage step has been applied and the voltage at the end of the signal integration phase was measured. Figure 3.54 shows the voltage measured at the output of the FCF with the

Specification		Value
S_{lq}	1 keV	1.1 ± 0.01 mV/ph
	10 keV	1.35 ± 0.01 mV/ph
S_{hq}	1 keV	22.6 ± 0.5 μV/ph
	10 keV	n.a.
INL (0÷20 ph)	1 keV	0.1 ph
	10 keV	0.1 ph
Fall time		$\leq$ 25 ns
Input range		10000 ph
Output swing		≈500 mV

Table 3.9: performance of the CSA.

buffer board, for increasing amplitudes of the input voltage step and with a 1 MHz operation. The operation frequency is limited by the buffer board time

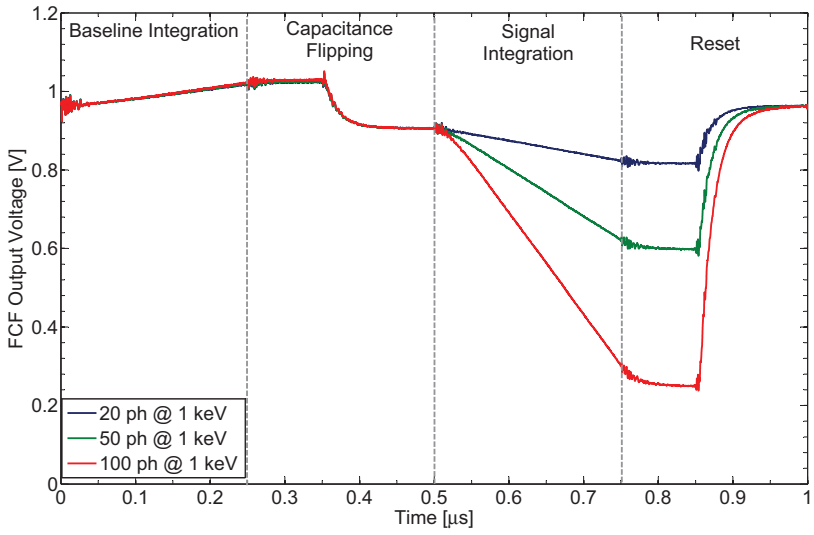

Figure 3.54: FCF output voltage for different input signals measured with an integration time of 250 ns, corresponding to an operation frequency of 1 MHz.

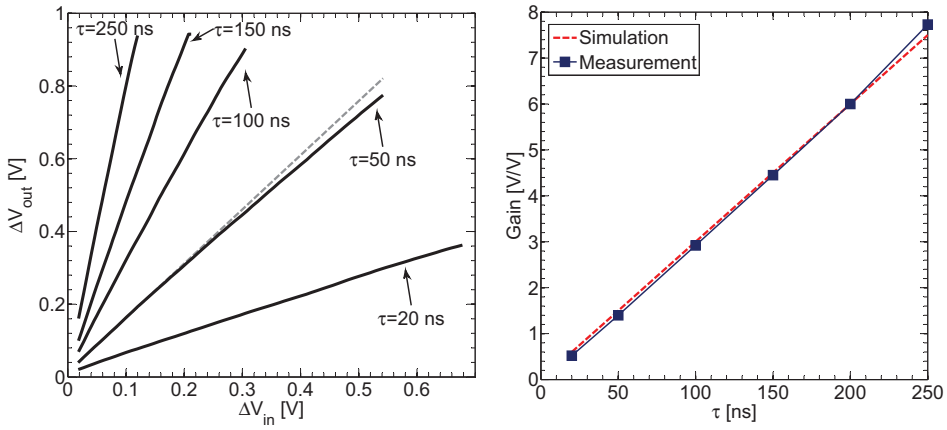

Figure 3.55: characteristic of the FCF for increasing values of the integration time (left) and gain of the stage as a function of the integration time (right).

constant, as it can be noted from the slow transients during the flipping of the capacitance and the reset of the stage.

The expected gain of the stage can be computed from Equation 3.46:

$$\frac{\Delta V_{out}}{\Delta V_{in}} = \frac{G_m}{C_f} \cdot \tau \tag{3.49}$$

Figure 3.55 (left) shows the characteristic of the shaping stage for different integration times. As it can be noticed, the stage operates properly with an output voltage even higher than the expected 0.8 V. However, as it can be observed from the deviation between the characteristic at 50 ns of integration time and the straight line (in dotted grey), obtained by fitting the characteristic in the small input voltages region, the gain decreases when the amplitude of the input voltage increases, thus deteriorating overall the non-linearity and leading to an output dynamic range of the overall channel lower than the expected 0.8 V with 10^4 photons. Figure 3.55 (right) shows the gain of the stage as a function of the integration time, computed by fitting the characteristic in the small input voltages range ($0 \div 0.2$ V). The results are in agreement with the expected values, and prove the proper operation of the stage even with an integration time of 20 ns.

Analog front-end

The analog front-end has been characterized by applying a voltage step at the input of the CSA during the signal settling phase and by measuring the FCF output voltage at the end of the signal integration phase. Figure 3.56 shows the transcharacteristic in 1 keV configuration, as the average value and the standard deviation of the measured chips, together with the simulation results. As it can be noticed from the picture on the left hand side, showing the response for small signals achieved with the 50 fF injection capacitance, the channel features a sensitivity close to the expected value. Again, the measurements differ from the simulations in the transition between the high sensitivity and small sensitivity regions. The output dynamic range is lower than the expected 0.8 V. This behavior is mainly due to the decreasing gain in the shaping stage as the amplitude of the input voltage increases, and lead to a large signal sensitivity smaller than the expected 33 μV. The sensitivity of the channel in 1 keV configuration as a function of the input signal is shown in Figure 3.57. As it can be noticed, the measurement results in the small input signal region are in good agreement with simulations, with a sensitivity S_{lq} of

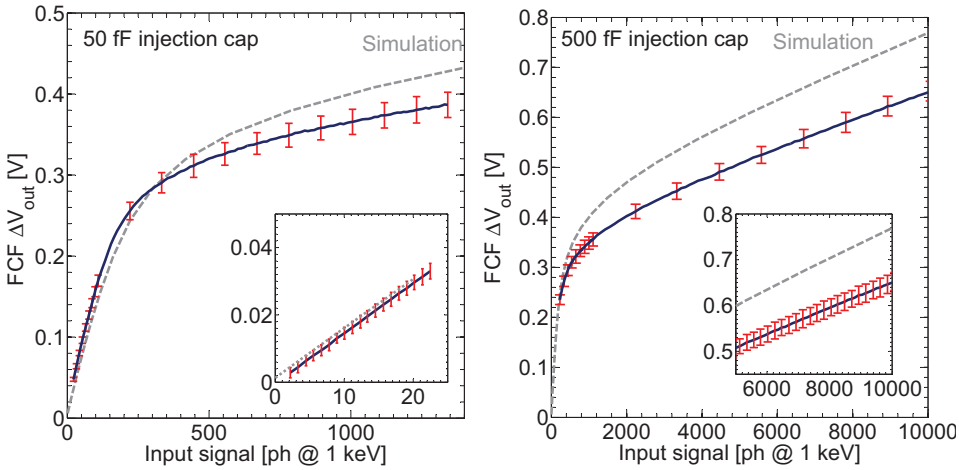

Figure 3.56: average value with errorbar of the transcharacteristic of the analog front-end in the 1 keV operation with the 50 fF (left) and 500 fF (right) injection capacitances. The inset shows the response in the first 20 photons input range (left) and between 5000 photons and 10000 photons (right).

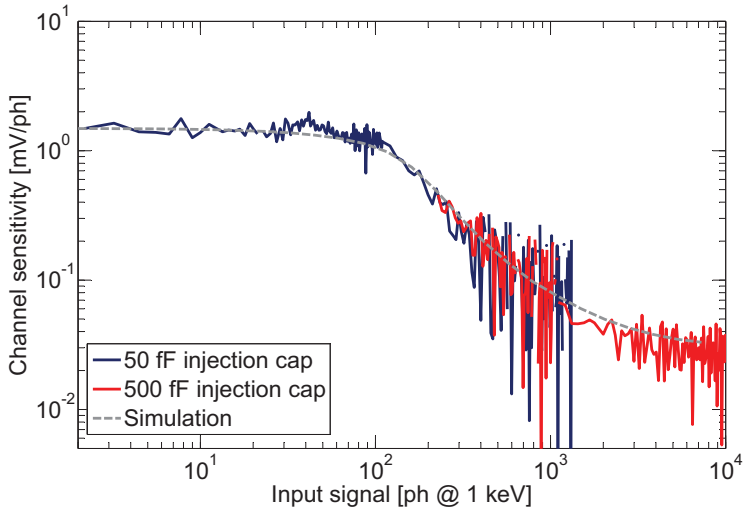

Figure 3.57: sensitivity of the analog front-end measured with both the injection capacitances and from simulation.

about 1.5 mV/ph. As the input signal increases, the gain of the FCF decreases and the measured sensitivity drops below the expected value, settling at about 29 μV/ph.

In 10 keV mode, the transcharacteristic has not been fully explored, due to limitations in the amplitude of the input voltage step. Figure 3.58 shows a comparison between the measurement results, summarized as the average and the standard deviation over the measurements performed on different chips, and simulations. In the small input signals region, the measurements feature a sensitivity higher than the expected 1.65 mV/ph, as a result of the larger CSA sensitivity. Even though the overall characteristic is not available, the results obtained with the 500 fF injection capacitance suggest the same reduction of the output dynamic range already assessed for the 1 keV mode.

The noise of the channel has been evaluated by measuring the standard deviation of the signal at the output of the FCF at the end of the signal integration phase, and by computing the ENC according to Equation 3.47. In order to evaluate possible contributions of the CSA reset, the ENC has been computed also with the reset signal not enabled (i.e., no signal was applied and the FCF output voltage was sampled). Moreover the analog front-end integrating the PMOS based signal compression has been considered. The preliminary

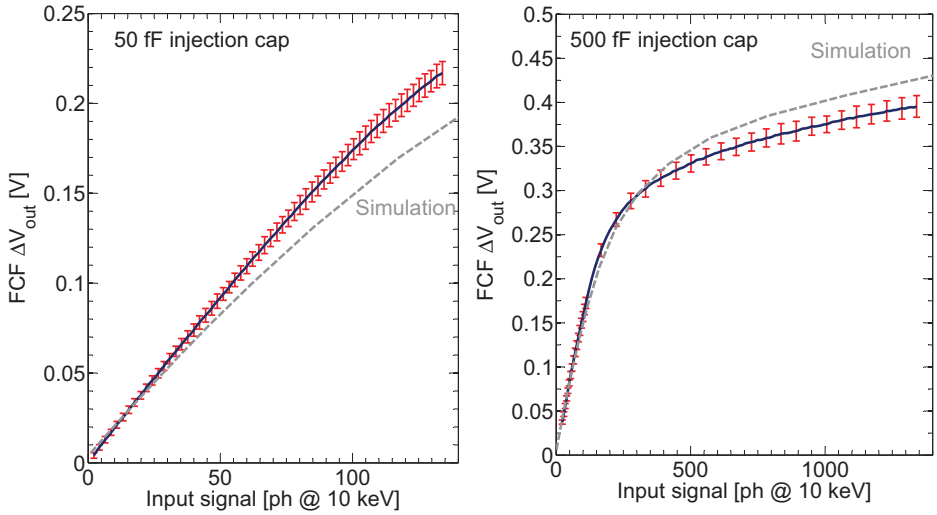

Figure 3.58: average value and standard deviation of the transcharacteristic of the analog front-end in the 10 keV operation with the 50 fF (left) and 500 fF (right) injection capacitances. The inset shows the response in the first 20 photons input range (left) and between 5000 photons and 10000 photons (right).

results, achieved in the 1 keV configuration for a single chip, are shown in Figure 3.59. The ENC at 50 ns has been evaluated in about 125 e^- RMS and 170 e^- RMS, respectively for the analog front-end based on the PMOS and NMOS feedback capacitors, resulting in a SNR of 2.2 and 1.6. Thanks to the n-well of the PMOS feedback device, the rejection of the noise induced from the bulk to the output of the CSA may be higher with respect to the case of the NMOS based CSA. Moreover, improvements may be found in finely adjusting the timings of the FCF and by improving the test setup.

As a last remark, Table 3.10 summarizes the overall performance of the analog front-end of the PixFEL project.

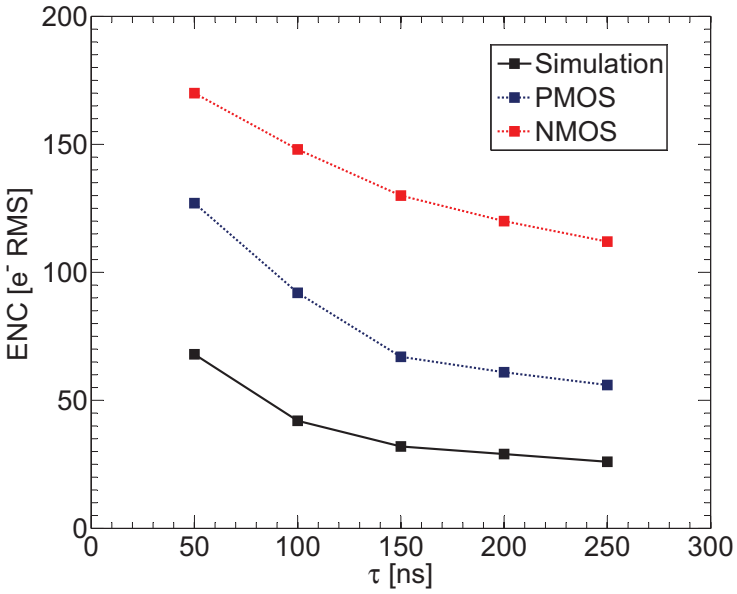

Figure 3.59: Noise performance of the analog front-end obtained from simulations (black) and from measurements on a single chip from both the PMOS (blue) and NMOS (red) based analog front-ends.

Specification		**Value**
S_{lq}	1 keV	1.49 ± 0.04 mV/ph
	10 keV	1.87 ± 0.03 mV/ph
S_{hq}	1 keV	29 ± 0.6 μV/ph
	10 keV	n.a.
INL (0÷20 ph)	1 keV 10 keV	0.2 ph 0.2 ph
Input range		10000 ph
Output swing		≈650 mV
ENC		125 e^- RMS
SNR		$\geq$ 2.2

Table 3.10: performance of the analog front-end.

Conclusions

In this thesis work, the design and the characterization of microelectronic systems for applications at next generation X-ray Free Electron Lasers have been discussed.

In the framework of the DSSC consortium, an ancillary block, to be used for pixel-level calibration of the readout electronics, has been described. The performance of the circuit, designed in a 130 nm CMOS technology by IBM, have been evaluated from a characterization activity carried out on a prototype of the DSSC Chip, integrating 8×8 readout channels. Thanks to the measurement results obtained, the injection circuit, has been optimized. Then, the design of the test setup for the DSSC detector bare modules has been briefly presented. Currently, the very first bare module has been received from the provider and measurements are ongoing. A characterization campaign for all the bare modules is foreseen by the end of 2015.

In the framework of the PixFEL project, a novel signal compression principle, capable of fitting the wide input dynamic range of 10^4 photons with energies up to 10 keV, has been proposed and employed in the first version of the readout channel, integrating a Charge Sensitive Amplifier, a gated integrator, performing correlated double sampling with a trapezoidal weighting function, and a SAR ADC. The analog front-end, designed in a 65 nm CMOS technology by TSMC, has been successfully tested, showing the effectiveness of the proposed signal compression principle at both 1 keV and 10 keV energies. The main issues arised from the characterization activity are related to the output swing, which is lower than the expected 0.8 V, and to the noise performance. Ongoing activities are focusing on the optimization of the shaping stage, which is the main responsible of the reduced output range, and on possible solutions to improve the Signal-to-Noise Ratio, toward a 32×32 pixels matrix prototype chip submission foreseen by the end of 2015.

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