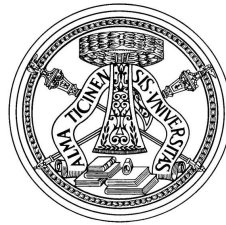


UNIVERSITY OF PAVIA

PH.D. THESIS IN MICROELECTRONICS

# Characterization and Modeling of Phase Change Memories



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To my family

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# Introduction

Nowadays, non-volatile storage technologies play a fundamental role in the semiconductor memory market due to the widespread use of portable devices such as digital cameras, MP3 players, smartphones, and personal computers, which require ever increasing memory capacity to improve their performance. Although, at present, Flash memory is by far the dominant semiconductor non-volatile storage technology, the aggressive scaling aiming at reducing the cost per bit has recently brought the floating-gate storage concept to its technological limit. In fact, data retention and reliability of floating-gate based memories are related to the thickness of the gate oxide, which becomes thinner and thinner with increasing downscaling [1].

The above limit has pushed the semiconductor industry to invest on alternatives to Flash memory technology, such as magnetic memory (MRAM), ferroelectric memory (FeRAM), oxide memory (OxRAM) and phase change memory (PCM) [2, 3]. The last technology is one of the most interesting candidates due to high read/write speed, bit-level alterability, high data retention, high endurance, good compatibility with CMOS fabrication process, and potential of better scalability. However, it still requires strong efforts to be optimized in order to compete with Flash technology from the cost and the performance viewpoints.

In PCMs, information is stored by exploiting two different solid-state phases (namely, the amorphous and the crystalline phase) of a chalcogenide alloy, which have different electrical resistivity (more specifically, the resistivity is high for the amorphous phase and lower for the crystalline phase). Phase transition is a reversible phenomenon, which is achieved by stimulating the cell by means of adequate thermal pulses induced by applying electrical pulses. Reading the resistance of any programmed cell is achieved by sensing the current flowing through the chalcogenide alloy under predetermined bias voltage conditions. The read window, that is, the range from the minimum (amorphous state, RESET) and the maximum (crystalline state, SET) read current, is considerably wide, which allows safe storage of an information bit in the cell and also opens the way to the multi-level (ML) approach to achieve low-cost high-density storage. ML storage consists in programming the memory cell to one in a plurality of intermediate resistance (i.e., of read

current) levels inside the available window, which allows storing more than one bit per cell (the number of bits that can be stored in a single cell is  $n = \log_2 m$ , where  $m$  is the number of programmable levels). The programming power and the read window depend on the electrical properties of the cell materials as well as on the architecture and the size of the memory cell. As the fabrication technology scales down the cell dimensions, new challenges arise to accurately program the cell to intermediate states and discriminate adjacent resistance levels.

In this framework, the aim of this Thesis is to investigate ML programming capabilities in PCM cells. Chapter 1 introduces the working principles and basic properties of PCM cells. In Chapter 2, experimental characterization is carried out to optimize the ML programming procedure, whereas an analytical model for partial-RESET programming with the capability of evaluating the effects of various parameters in this programming approach is developed in Chapter 3. The stability issues in intermediate states are studied in Chapter 4. In Chapter 5, the dependence of programming and read performances on the key geometrical parameters of the cell is addressed, in order to investigate the effects of technology scaling on the memory cell performance.



# Phase Change Memories

Besides Flash memory technology, which is based on the floating gate concept [4, 5], alternative non-volatile memory technologies based on innovative materials have been developed in last years. Among them, it is worth citing magnetic memory (MRAM), ferroelectric memory (FeRAM), and phase change memory (PCM) [2, 3].

The characteristics of such new memory technologies are compared to the features of Flash memories in Table 1.1 [2].

From this Table, PCM technology turns out to be one of the most interesting candidates among innovative memory technologies. In fact, PCMs present very small cell size with respect to MRAMs and FeRAMs, and much better scalability. The endurance, although lower than in the cases of FeRAM and MRAM, is still high if compared to Flash memories. In addition, it is

*Table 1.1: Non-volatile memories characteristics*

	Flash NOR	Flash NAND	FeRAM	MRAM	PCM
Cell feature size ( $F^2$ )	10-12	4-5	18	10-20	5-8
Endurance (cycles)	$10^5$	$10^5$	$10^{16}$	$10^{14}$	$10^{12}$
Additional mask step	6-8	6-8	2	4	3-4
Read speed	10 ns	50 ns	40 ns	50 ns	50 ns
Write speed	$2 \mu s$	500 ns	40 ns	50 ns	50 ns
Read voltage	2 V	5 V	1.5 V	3.3 V	0.4 V
Write voltage	12 V	18 V	1.5 V	3.3 V	1 V
Direct overwriting	No	No	Yes	Yes	Yes
Programming energy	High	Medium-High	Low	Medium	Medium

worth remembering that PCM technology has a good compatibility with CMOS fabrication process, unlike FeRAM and MRAM technologies, which require the integration of ferroelectric and magnetic materials within the CMOS process. Few mask steps are required for PCM technology. Regarding the programming performances, PCM increases the write speed by at least one order of magnitude with respect to Flash memories, and is suitable for very low-voltage technologies.

The above described properties of PCM technology promise a wide range of potential applications. For instance, PCM may well address the NOR Flash market. In fact, PCM has about half the cell size, much faster programming, read time on the same order of magnitude and better endurance than NOR Flash. Concerning NAND Flash applications, such as solid-states drives, more efforts are needed to reduce the cell size and improve the multilevel capabilities of PCM, in order to reduce the cost per bit. However, PCM may also be used in DRAM applications, since non-volatility helps to reduce power consumption. The choice of a suitable memory architecture has been demonstrated to mitigate the main drawbacks of PCM technology as a DRAM alternative, such as high latency, high energy required for writing, and limited endurance [6].

Among the companies that have invested in PCM technology it is worth mentioning Micron (formerly Numonyx, STMicroelectronics), Samsung Electronics, IBM, NXP, BAE Systems, and Hitachi. The developed PCM chips are shown in Fig. 1.1 [7, 8, 9, 10, 11, 12, 13, 14, 15].

## 1.1 Working principle of the PCM cell

---

The working principle of a PCM cell relies on the physical properties of chalcogenide materials, that can switch from the amorphous to the crystalline phase and vice versa when stimulated by suitable electrical pulses. Basically, a PCM cell is composed of a thin chalcogenide film (usually  $Ge_2Te_2Sb_5$ , or GST), a resistive element named heater (typically made of  $TiN$ ), and two metal electrodes, i.e., the top electrode contact (TEC) and the bottom electrode contact (BEC). Since phase transitions are thermally assisted, in PCM devices Joule heating is exploited to raise the temperature inside the chalco-

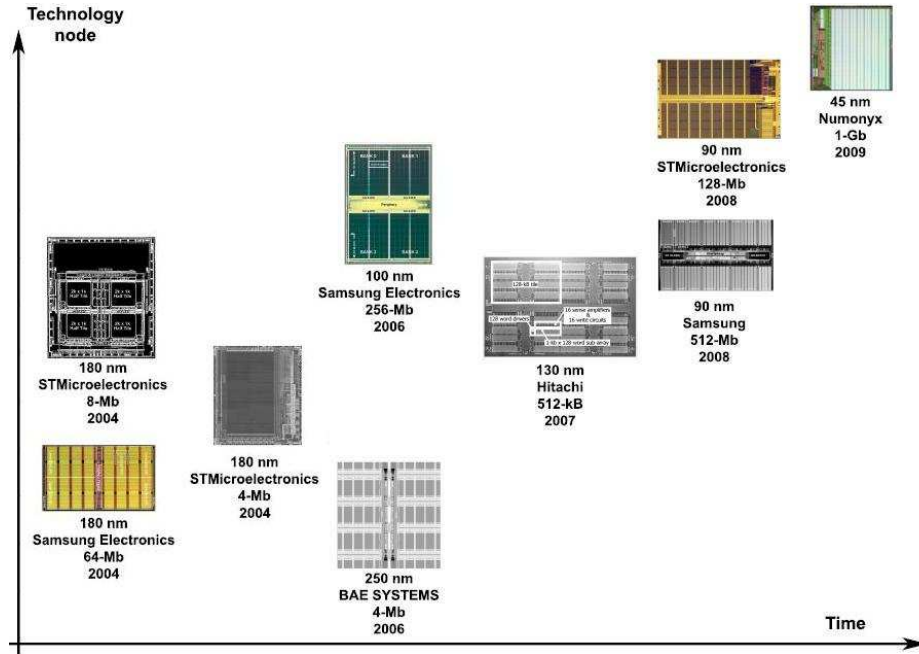


Figure 1.1: Technology roadmap for PCM development.

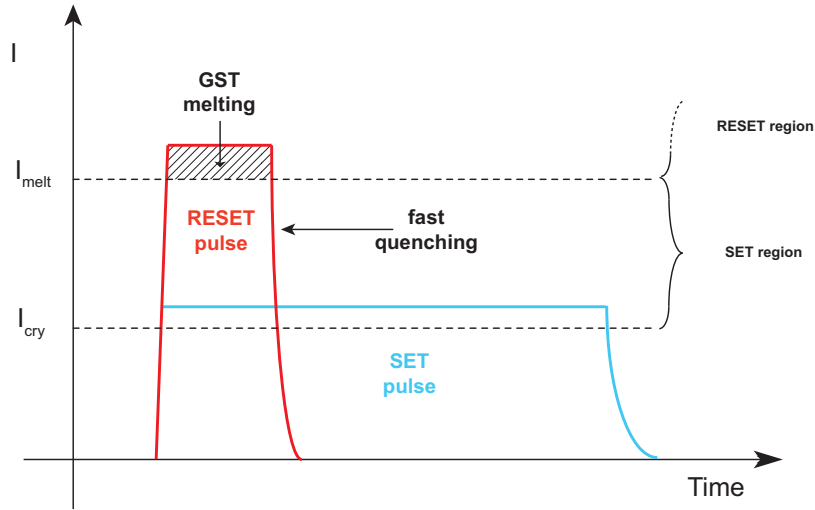


Figure 1.2: Standard pulses for bi-level PCM programming.

genide material to the required value. The crystalline-to-amorphous phase

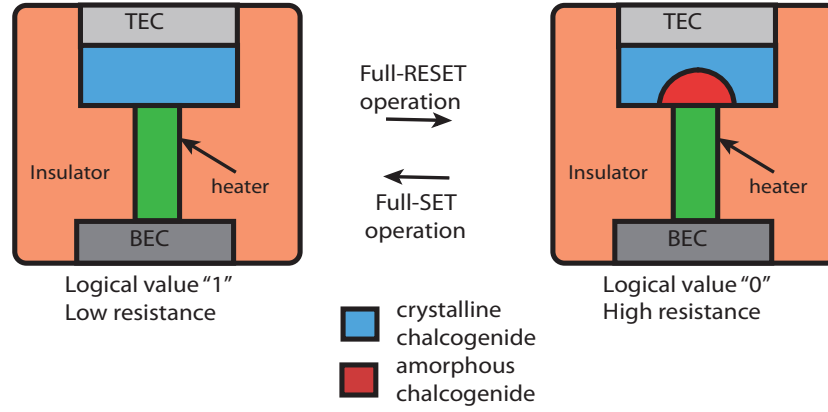


Figure 1.3: Conceptual scheme of a PCM cell in the full-SET and full-RESET states.

transition is obtained by applying a high-amplitude electrical pulse to the cell so as to bring the temperature of the active phase-change material above the melting point  $T_{melt}$  (about 600 °C for the GST alloy) [16], and then quickly cooling the memory cell, in order to freeze the chalcogenide material into a disordered (i.e., amorphous) structure. A pulse duration on the order of few tenth of ns is typically sufficient to crystallize the chalcogenide [17]. The amorphous-to-crystalline phase transition is obtained by applying an electrical pulse with a lower amplitude and a longer time duration than in the previous case. Then, the amorphous chalcogenide is heated to a temperature below the melting point but above the crystallization temperature, that is the temperature required to activate the crystallization process within the required time scale (typically on the order of 100 ns). This way, the thermal energy enables to restore the crystalline lattice, which is a minimum-energy structural configuration. Typical electrical pulses for SET and RESET operations are shown in Fig. 1.2. The obtained phase configuration is schematically depicted in Fig. 1.3.

Only a portion of the phase-change layer, which is located close to the GST-heater interface and is referred to as active chalcogenide, undergoes phase transition when the PCM cell is thermally stimulated. The phase state of the active chalcogenide determines the value of the memory cell resistance: the crystalline state corresponds to the minimum resistance (full-SET, logic

value 1), whereas the amorphous state corresponds to the maximum resistance (full-RESET, logic value 0) of the memory cell.

The typical V-I characteristics of the PCM cell in the SET and RESET states are shown in Fig. 1.4. Consider the case of a cell in its full-SET state: the differential resistance of the cell decreases as the applied voltage increases. This effect is due to the contribution of the crystalline chalcogenide to the cell resistance. In fact, typically the crystalline chalcogenide resistivity decreases with increasing electrical field inside the material.

The V-I curve of the cell in its RESET state shows an S-shaped behavior. This effect is due to the threshold switching phenomenon [18, 19, 20, 21], which consists in a sudden drop of the amorphous chalcogenide resistivity as the voltage across the PCM cell exceeds a critical value, typically referred to as threshold voltage,  $V_{th}$  (or, equivalently, when the current flowing through the cell exceeds the threshold value,  $I_{th}$ ). Thus, when low-amplitude voltage pulses are applied to the cell, a low current flows through the device, which is in its high-resistance state (OFF region in Fig. 1.4). On the other hand, when a high-amplitude voltage pulse is applied to the cell, threshold switching takes place and the device shows a much lower resistance (ON region in Fig. 1.4). Threshold switching in chalcogenide alloys is crucial for the feasibility of PCM technology. In fact, without threshold switching very high voltage pulses would be necessary to deliver enough power to the device to activate phase transition. Thanks to threshold switching, only few volts are required for programming despite the very high resistance of the cell in the OFF region. It is worth noticing that the V-I curves of the cell in the two states (SET and RESET) are essentially superimposed in the ON region, whereas they show substantial difference in the OFF region. Writing is carried out by operating the cell in the ON region, in order to provide the device with enough energy to induce phase change. On the other hand, readout must be carried out by operating the cell in the OFF region. Typically, a predetermined read voltage is applied to the cell and the current flowing through the device, referred to as read current, is sensed (current sensing approach). The read voltage must be low enough to avoid unintentional modification of the cell contents due to unintended heating during readout.

The read window, that is, the range from the minimum (RESET) and the

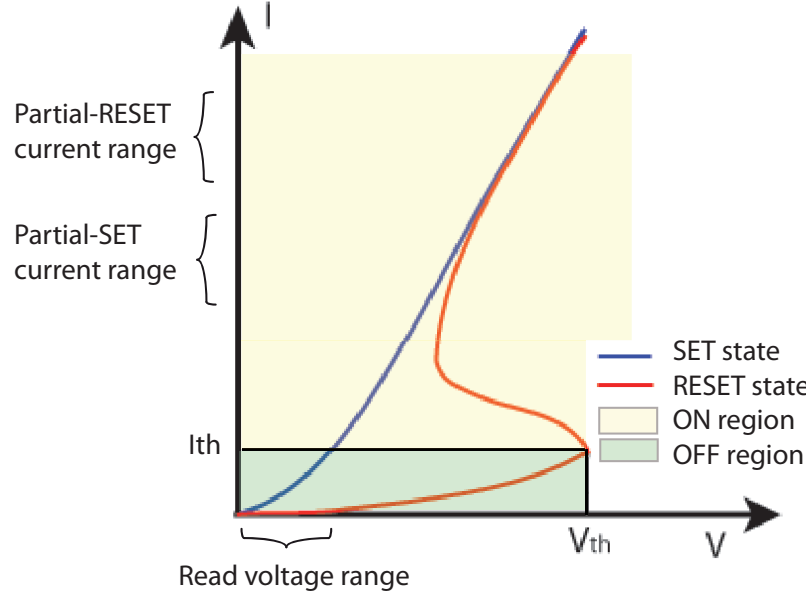


Figure 1.4:  $V$ - $I$  curve of a PCM device in the SET and the RESET state.

maximum (SET) read current, is considerably wide, which allows safe storage of an information bit in the cell and also opens the way to the multilevel (ML) approach to achieve low-cost high-density storage. However, critical issues must be addressed when implementing ML programming. Among them, it is worth mentioning the capability to program and read the memory cells with sufficiently high accuracy, the reproducibility of the programming operation, and the stability of programmed levels. Furthermore, an effective ML programming algorithm must be robust with respect to variations of parameters of the memory cell and the surrounding circuitry.

In fact, a PCM memory chip is made of a large number of PCM cells organized in a bi-dimensional array. As opposed to the case of Flash memories, in which the elementary storage consists of a floating-gate transistor, the PCM memory cell is a programmable resistor and, hence, is a two-terminal device. For this reason, a NOR type architecture is adopted as shown in Fig. 1.5(a). Each memory cell consists of a PCM storage element connected to a selection transistor, which can be either an MOS as depicted in Fig. 1.5(b),

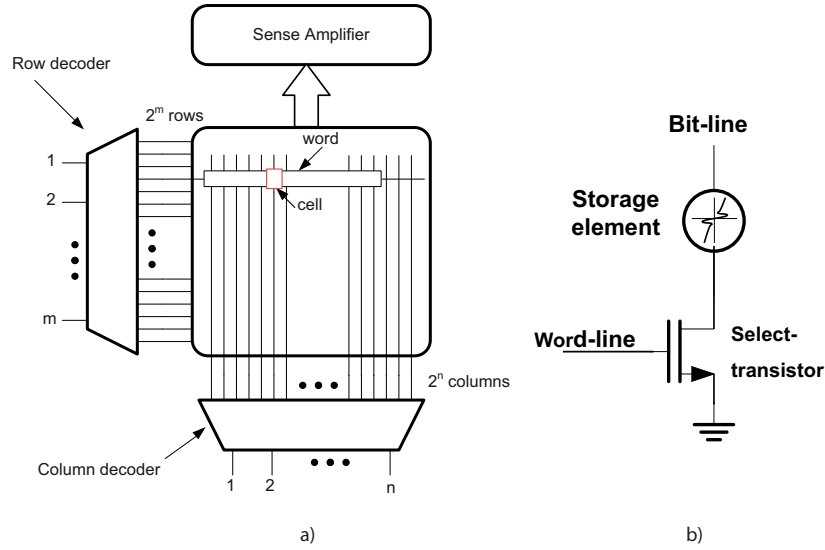


Figure 1.5: Architecture of a PCM array (a) and circuit scheme of a PCM cell (b).

or a bipolar device. The gate or the base of all select transistors of the same row are connected to the same word-line, while the TECs of the PCM cells belonging to the same column are connected to the same bit-line. The memory cell is selected by means of row and column decoders that generate the electrical control signals required for read and write operations.

## 1.2 PCM cell architectures

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Several memory cell architectures have been investigated to optimize the cell performance, the reproducibility of the device characteristics, and the scalability. Among the vertical structures, the simplest is the lance heater cell (Fig. 1.6), which is composed of a cylindrical heater above which a thin chalcogenide layer is deposited [22]. The required programming current and power depend on the electrical and thermal properties of the heater material and the chalcogenide, on the thermal properties of the surrounding materials and on the sizes of the cell. Since a small heater cross-section enables to reduce the RESET current, a sub-lithographic process is used for the heater

definition. For this reason, this type of cell geometry is referred to as contact minimized architecture. An improved contact minimized architecture is the ring-contact cell that was proposed to improve the reproducibility of the cell characteristics and further reduce the contact area [23, 24] (Fig. 1.7).

In the above cell architectures, the heater element may be considered the main responsible for the chalcogenide heating. However, some cell architectures have been proposed where Joule heating inside the phase change material (i.e., self-heating) significantly contributes to the active area heating, thus increasing the thermal efficiency of the device and reducing the programming current [25, 27, 28]. Typically, this effect is more relevant in the so-called volume minimized cells such as the pillar or pore cell (Fig. 1.8) [29, 25, 26, 28, 30] and the line cell (Fig. 1.9) which is a lateral structure [31, 32, 33]. In volume minimized architectures, the phase change material is laterally confined within sub-lithographic features, while the BEC and the TEC are quite large structures.

Finally, cell architectures combining the advantages of contact minimized and volume minimized structures have been proposed: the  $\mu$ Ttrench cell [35, 38] and the wall cell [15] (Fig. 1.10). In these cells, the chalcogenide is deposited in a trench which contacts a sidewall heater obtained by means of a sub-lithographic process.

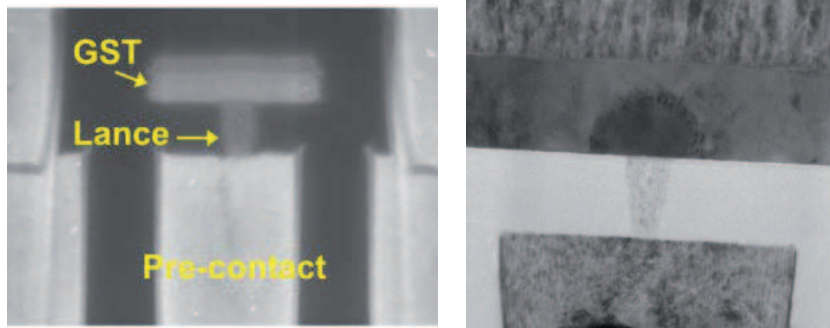


Figure 1.6: Lance heater cell structure realized by IBM/Macronix [22].



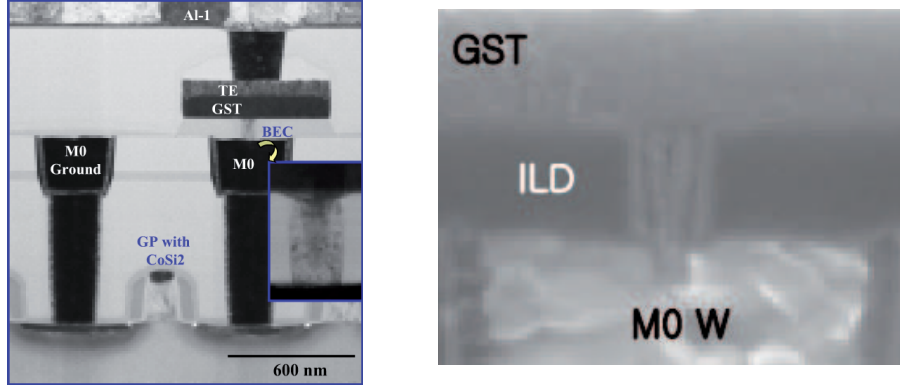


Figure 1.7: SEM picture of the ring contact cell realized by Samsung Electronics [23, 24].

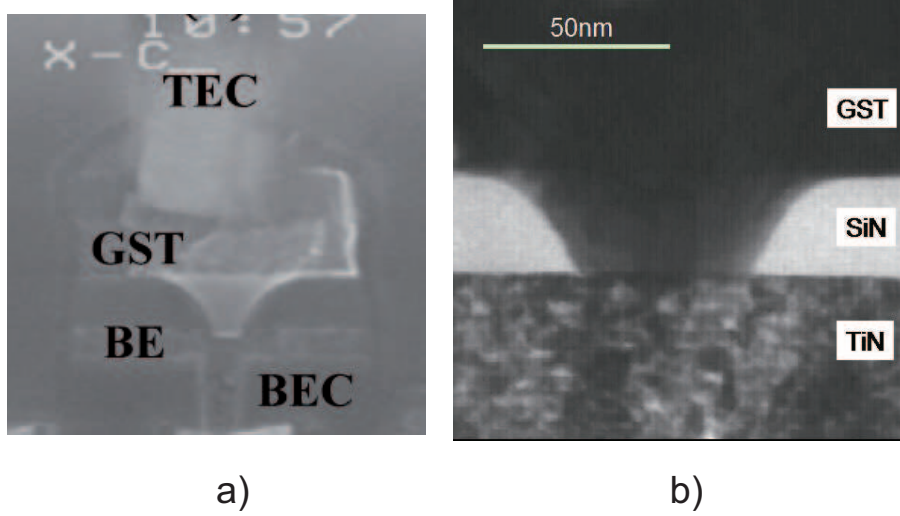


Figure 1.8: SEM picture of the pillar (or pore) cell structure realized by IBM/Infineon/Macronix PCRAM Joint Project [25] (a) and IBM/Quimonda/Macronix PCRAM Joint Project [26] (b).

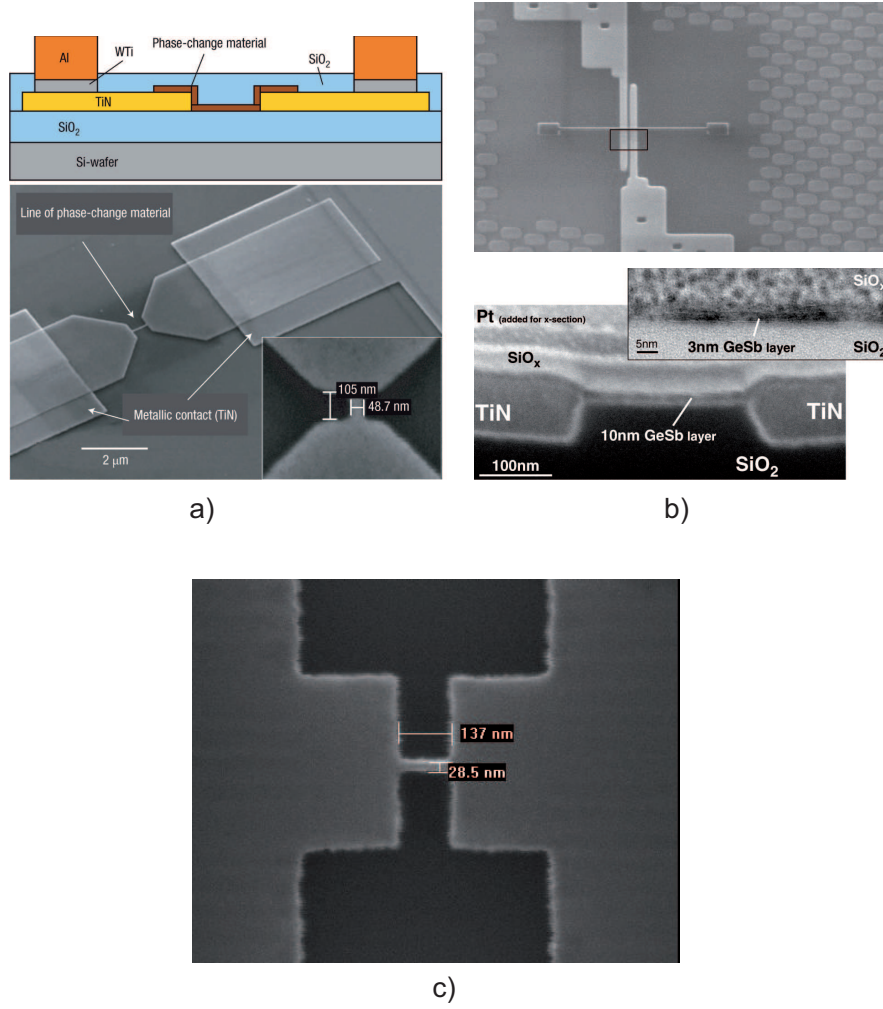


Figure 1.9: SEM picture of the line cell structure realized by Philips Research Laboratories [31] (a), IBM/Qimonda/Macronix PCRAM Joint Project [32] (b), and NXP [34] (c).

### 1.3 Phase change materials

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Phase-change materials have been widely employed in optical storage, like CD and DVD, whereas their application to solid-state memories is still under development. Among the alloys that have been studied for application

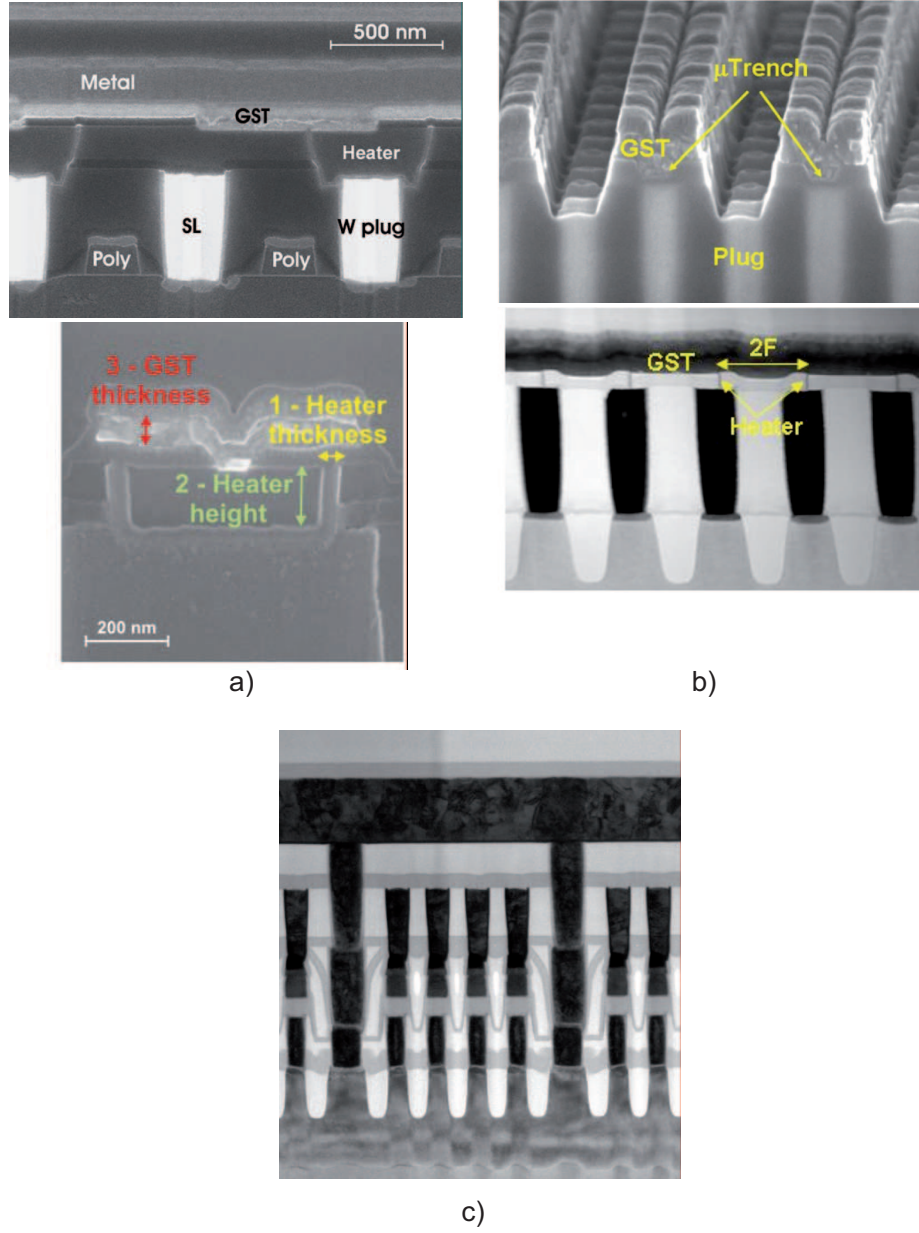


Figure 1.10: SEM cross sections of the devices realized by STMicroelectronics/Numonyx. The  $\mu$ Trench cell: 180 nm node [35, 36] (a), and 90 nm node [37] (b); the wall cell: 45 nm node [15] (c).

Table 1.2: Properties of Phase Change materials

Parameter	Performance affected
Crystallization temperature	Data retention, SET power
Crystallization speed	SET pulse duration, programming speed
Melting temperature	RESET power
Thermal conductivity in both phases	SET and RESET power, efficiency of the cell
Resistivity in amorphous and crystalline phases	ON/OFF ratio, read window
Threshold voltage	SET voltage and reading voltage

to PCM, the most common is GST ( $Ge_2Te_2Sb_5$ ). However, many chalcogenides alloys are still under study with the aim to improve the PCM cell performances by optimizing the alloy composition.

The most important properties of phase-change material for the use in nonvolatile memories are summarized in Table 1.2 [39]. The crystallization temperature,  $T_C$ , is related to the characteristics of the amorphous-to-crystalline phase transition, which determine the power required for the SET operation as well as data retention properties. The crystallization speed affects also the SET time and, thus, the achievable programming speed. GST presents a crystallization temperature of about 145 °C [40]. Among the alternative alloys that present improved data retention performances with respect to GST, it is worth mentioning  $GeTe$  [41, 40, 42] ( $T_C \simeq 180^\circ \text{C}$ ), N-doped  $GeTe$  [43] ( $T_C \simeq 220 - 270^\circ \text{C}$  depending on the doping amount), C-doped  $GeTe$  [44] ( $T_C \simeq 290 - 330^\circ \text{C}$  depending on doping amount), oxygen-doped  $GeSbTe$  [45], and  $GeSb$  [46] ( $T_C \simeq 250^\circ \text{C}$ ).

Regarding the crystalline-to-amorphous transition, the melting temperature,  $T_{melt}$ , is an important parameter which impacts on the power required for amorphization (RESET operation). GST has a melting temperature of about 620°C [47, 42], while  $T_{melt} \simeq 720^\circ \text{C}$  for  $GeTe$  [42] and N-doped  $GeTe$  [43]. The programming power may be reduced by choosing phase change materials having a lower melting point of a lower thermal conductivity, which improves the thermal efficiency of the memory cell.

Finally, the difference of electrical resistivity between the amorphous and the crystalline phase determines the width of the read window and also the ratio between the RESET state and the SET state cell resistance. The resistance ratio is about 3 orders of magnitude for the above mentioned alloys (slightly lower for GST and higher for *GeTe* [43]).

From the viewpoint of the threshold switching phenomenon, an important parameter is the threshold voltage of the memory cell. This threshold voltage must be low enough to enable low-voltage programming, but sufficiently high to allow the use of a reasonable read voltage which allows relaxing the accuracy of the readout operation.

# 2

## Multilevel programming strategies

Multilevel storage in PCM devices [48, 49] requires accurate programming of the cell resistance to predetermined intermediate levels. Two alternative ML programming strategies have been proposed in the literature, namely partial-SET and partial-RESET programming. In the former case, the PCM cell is first programmed to the full-RESET state and, then, partial-SET pulses are applied in order to partially crystallize the amorphous volume [49]. In the latter case, the PCM cell is first programmed to the full-SET state and, then, the GST material is partially amorphized by means of partial-RESET pulses [50]. The distribution of the amorphous and crystalline phases inside the GST layer depends on the programming approach which then determines the properties of the intermediate states from the viewpoint of stability over time.

In this Chapter, the characteristics of partial-RESET and partial-SET programming are analyzed and compared to investigate the feasibility of ML storage. All measurements were carried out on a 180-nm 4M-cell PCM experimental chip made of MOS-selected  $\mu$ Trench cells [51]. The architecture of the considered PCM array and the schematic of the cell biasing circuit are depicted in Figs. 2.1(a) and 2.1(b), respectively.

In voltage programming, the memory cell is biased by applying an adequate voltage level to the selected bit-line (BL) through a high-voltage natural NMOS transistor,  $Y_O$ , which works as a source follower. More specifically, voltage pulses having an amplitude  $V_{RST}$  ( $V_{SET}$ ) are applied to the gate terminal of  $Y_O$  for partial-RESET (SET) programming operations. In voltage programming, device  $Y_O$  is kept in saturation by applying a sufficiently high

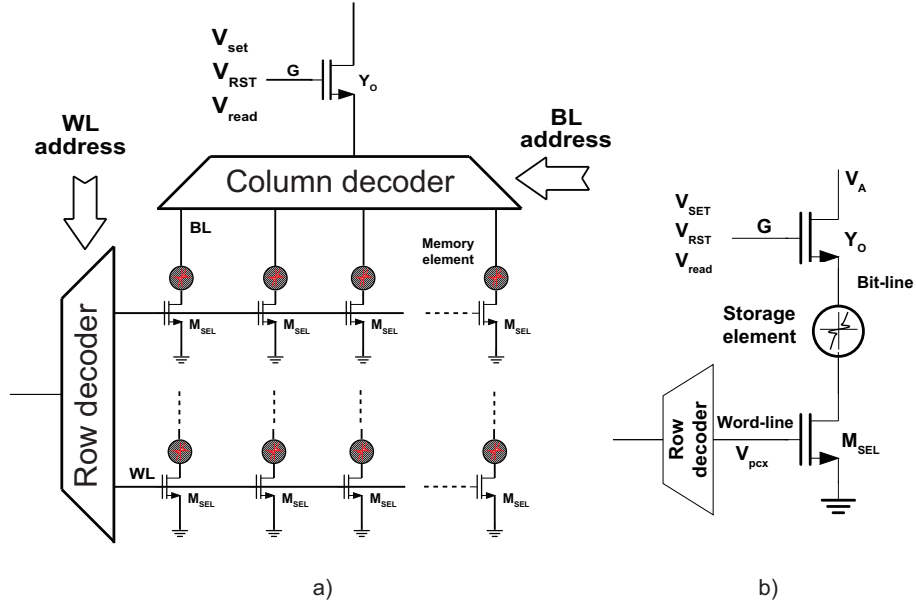


Figure 2.1: Architecture of the used PCM array (a) and schematic of the circuit used to program and read memory cells (b).  $M_{SEL}$  and  $Y_O$  are the word-line (WL) select transistor and the bit-line (BL) bias device, respectively.

voltage  $V_A$  to its drain terminal and the addressed word-line (WL) select transistor  $M_{SEL}$  is turned on by applying a high voltage level to its gate ( $M_{SEL}$  works in the triode region). In current programming, transistor  $M_{SEL}$  is operated in its saturation region and, hence, works as a voltage-controlled current source, whereas  $Y_O$  is forced in its triode region by applying a sufficiently high voltage to its gate terminal (5.2 V). The current forced through the PCM cell is controlled by means of the word-line voltage,  $V_{pcx}$ .

The stored information is read out by sensing the current,  $I_{cell}$ , flowing through the cell (hereinafter referred to as read current) when a suitable read voltage  $V_{read}$  is applied to the gate terminal of  $Y_O$ , which is forced in saturation and operates as a source follower.  $M_{SEL}$  is operated in its triode region with a sufficiently high value of the word-line voltage ( $V_{pcx} = 3$  V), which makes its on-resistance negligible. The read voltage is low enough to prevent un-intentional programming of the GST state (the bit-line voltage is set to about 0.4 V).

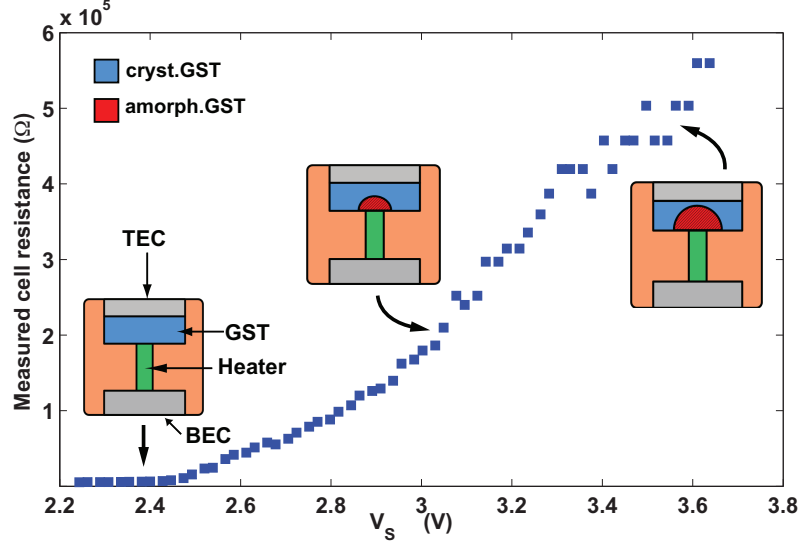


Figure 2.2: Partial-RESET programming curve: the volume of amorphous chalcogenide increases with the amplitude of the programming pulse.

In order to measure the read current  $I_{cell}$  with high accuracy, the PCM array can also be operated in direct memory access (DMA) mode. The cell resistance,  $R_{cell}$ , is calculated as the ratio between the read voltage across the cell,  $V_{cell}$ , and  $I_{cell}$ , where  $V_{cell} = V_{read} - V_{GS,Y_0}$  ( $V_{GS,Y_0}$  being the gate-to-source voltage of  $Y_0$ ). By setting  $V_{read}$  to 700 mV,  $V_{GS,Y_0}$  ranges from about 300 mV to 400 mV depending on the value of the cell current and, hence,  $V_{cell}$  varies from 300 mV to 400 mV. Each readout operation is carried out about 1  $\mu$ s after applying the programming pulse due to the used experimental setup. However, this delay can be in principle reduced to about 30 ns while still ensuring us to get rid of resistance recovery phenomenon that determines a remarkable variation of the GST resistance just after the programming operation [52]. The verify operation, where necessary, is performed under the same conditions of readout operation.



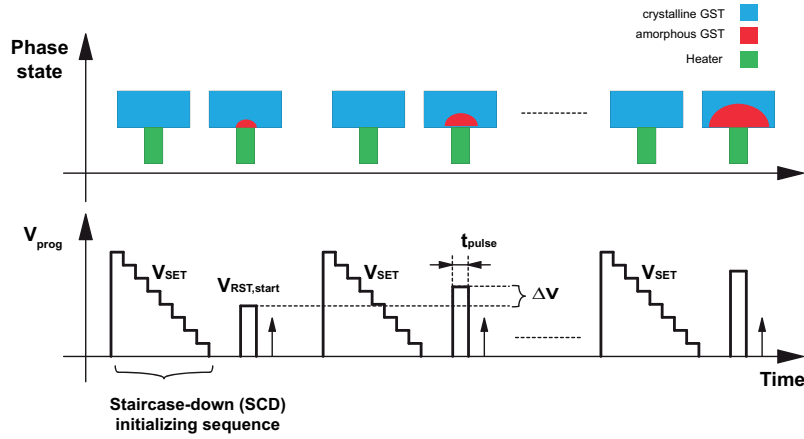


Figure 2.3: Sequence of program and read pulses used to obtain the single-pulse (SP) programming curve of PCM cells.

## 2.1 Partial-RESET programming

For the considered cell architecture, partial-RESET programming gives rise to a series phase distribution inside the active zone. The volume of chalcogenide amorphized by means of the partial-RESET pulse increases with the pulse amplitude, as schematically depicted in Fig. 2.2, thus determining an increase of the cell resistance.

### 2.1.1 Single-pulse partial-RESET programming

In single-pulse (SP) programming, only one partial-RESET pulse is applied to the PCM cell in its full-SET state to obtain a partial-RESET state. In partial-RESET programming, since the PCM cell is operated in the ON state and far from the threshold switching region, voltage programming and current programming are almost equivalent. In the following, only voltage programming will be considered. The sequence of program and read pulses used to obtain the single-pulse (SP) programming curve, which provides the achieved cell resistance as a function of the used programming voltage, is depicted in Fig. 2.3. The cell is first programmed to the SET state by means of a staircase-down (SCD) initializing sequence [53]. Then, a single partial-

RESET voltage pulse having predetermined amplitude ( $V_{RST}$ ) and duration ( $t_{pulse}$ ) is applied, which is followed by a readout operation in DMA mode. The above sequence is repeated with different values of  $V_{RST}$  and  $t_{pulse}$ , in order to obtain programming curves corresponding to different program pulse durations and highlight the impact of the dynamics of the RESET process over the obtained cell resistance for different programming pulse amplitudes. From Fig. 2.4, a significant dependence of the programming curve upon pulse duration is observed. As shown in Fig. 2.5, for any value of  $V_{RST}$ , the programmed cell resistance increases with increasing programming pulse duration, and approaches a saturation level for sufficiently high values of  $t_{pulse}$ . As the saturation resistance increases with  $V_{RST}$ , it is possible to achieve a reasonably high resistance level even with very short-duration pulses, provided that their amplitude is sufficiently high [7]. SP programming curve measurements have been repeated 4 times over the same cell. The obtained results, shown in Fig. 2.6 for the case  $t_{pulse} = 50$  ns, demonstrate a very good reproducibility of the programming curves. These results suggest that the randomness associated with the RESET process is minimum, as opposed to the case of partial-SET programming, where the randomness associated with the crystallization process has a severe impact, as will be shown in Chapter 4. In fact, crystallization takes place when stable crystalline nuclei are formed inside the amorphous array and, then, grow in size. The nucleation process is a stochastic phenomenon which heavily affects the characteristics of partial-SET programming. By contrast, in partial-RESET programming, each cell can be programmed to a predetermined resistance state with good accuracy once its corresponding optimum programming voltage and pulse duration values are determined.

A key aspect to be considered when developing an effective programming algorithm is that, as will be discussed in Section 2.1.3, the optimum voltage  $V_{RST}$  for any target value of cell resistance varies when considering different cells even inside the same array. This behavior suggests to use a Program and Verify technique to obtain the necessary accuracy for multilevel storage.

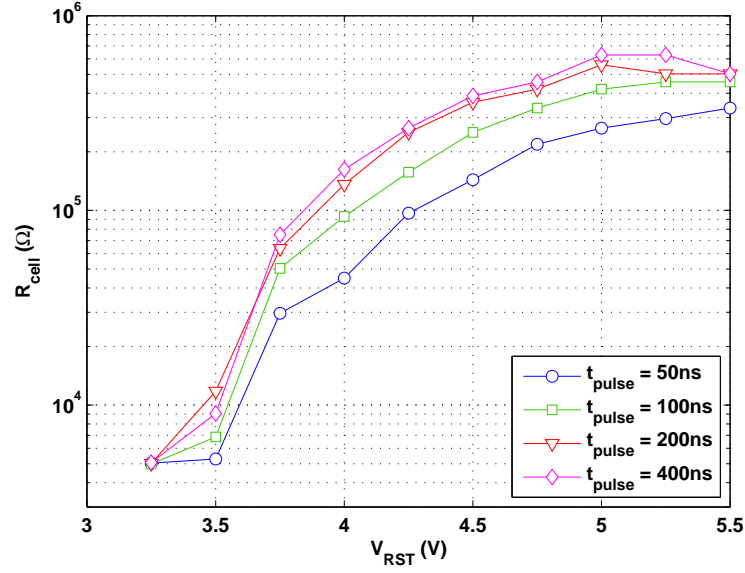


Figure 2.4: Single-pulse programming curve obtained by means of the programming procedure shown in Fig. 2.3 for different values of  $t_{\text{pulse}}$  (50 ns, 100 ns, 200 ns, 400 ns).

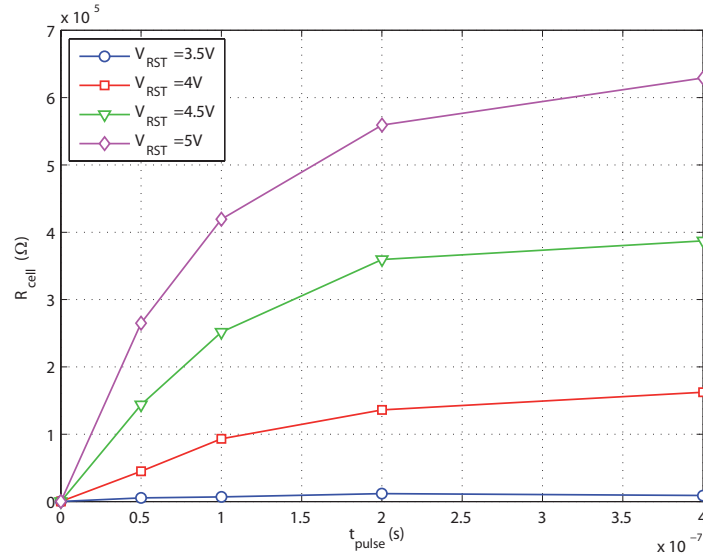


Figure 2.5: Dynamics of the RESET process in single-pulse partial-RESET programming for different values of  $V_{\text{RST}}$  (3.5 V, 4 V, 4.5 V, and 5 V).

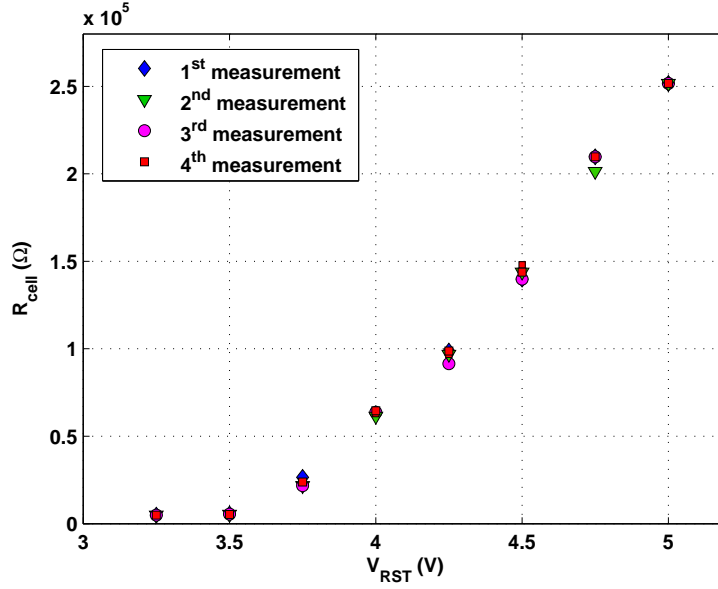


Figure 2.6: Measurements of the single-pulse partial-RESET programming curve repeated 4 times on the same memory cell ( $t_{pulse} = 50$  ns).

### 2.1.2 Staircase-up partial-RESET programming

To perform staircase-up (SCU) programming, a staircase-up sequence of partial-RESET voltage pulses (initial amplitude  $V_{RST,start}$ , increment at each step  $\Delta V$ , pulse duration  $t_{pulse}$ ) was applied after a staircase-down (SCD) initializing sequence, as depicted in Fig. 2.7. The read current  $I_{cell}$  was sensed in DMA mode after each programming pulse and the corresponding cell resistance was calculated, thus obtaining the programming curves in Fig. 2.8. The saturation of the programmed resistance for high values of  $V_{RST}$  is highlighted in the inset of Fig. 2.8. A slight increase of the minimum voltage required for amorphization is apparent when the pulse duration is decreased. Furthermore, the slope of the programming curves increases with increasing values of  $t_{pulse}$ .

As shown in Fig. 2.9, a similar effect is obtained by decreasing the value of  $\Delta V$ .

The phase state of the memory cell affects the programming operation only when fast pulses are used (for instance, 50 ns in Fig. 2.9), while when

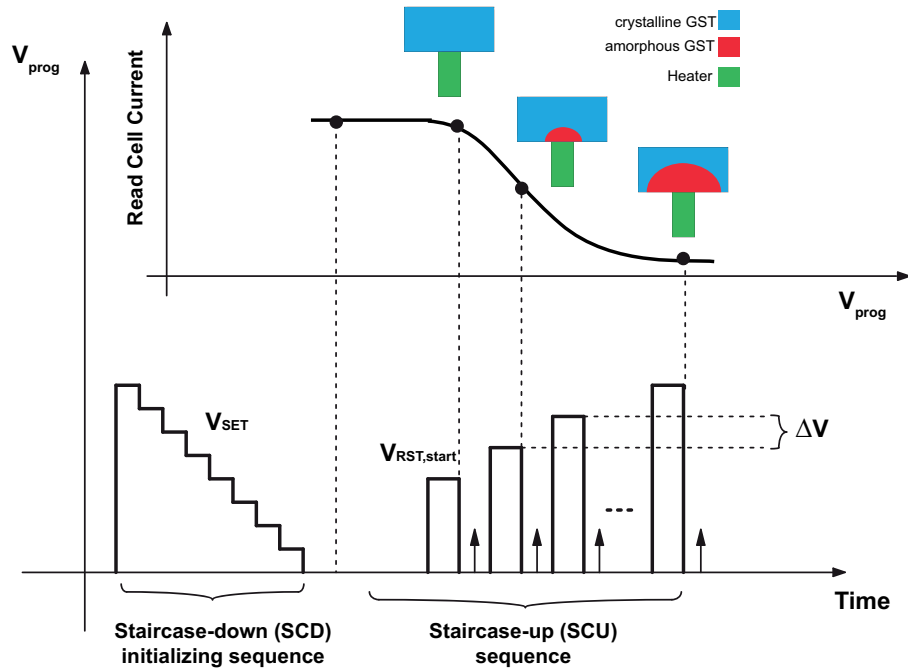


Figure 2.7: Sequence of programming pulses used to obtain the SCU partial-RESET programming curves.

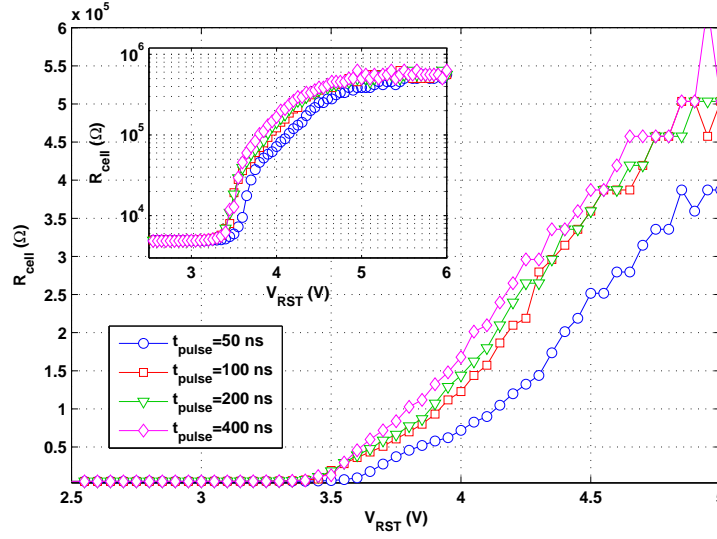


Figure 2.8: SCU partial-RESET programming curves obtained on the same cell with  $V_{\text{RST},\text{start}} = 2.5$  V,  $\Delta V = 50$  mV, and different values of  $t_{\text{pulse}}$  from 50 ns to 400 ns.

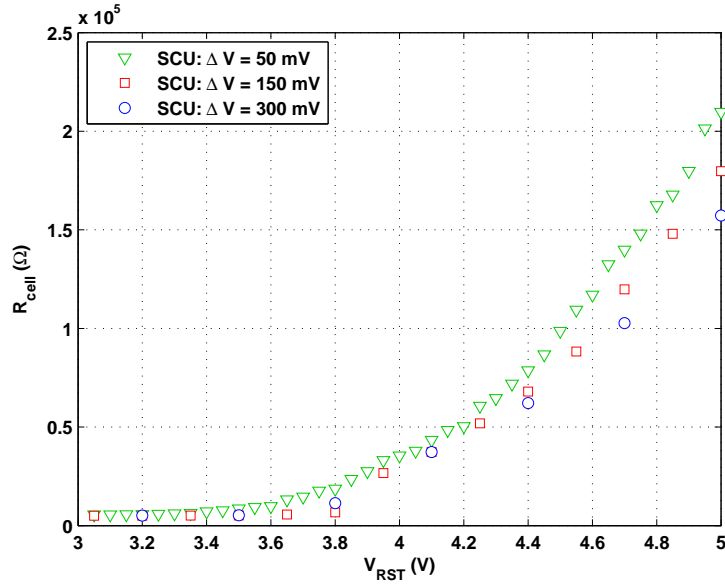


Figure 2.9: SCU partial-RESET programming curves obtained on the same cell with  $V_{\text{RST},\text{start}} = 3$  V,  $t_{\text{pulse}} = 50$  ns, and different values of  $\Delta V$ .

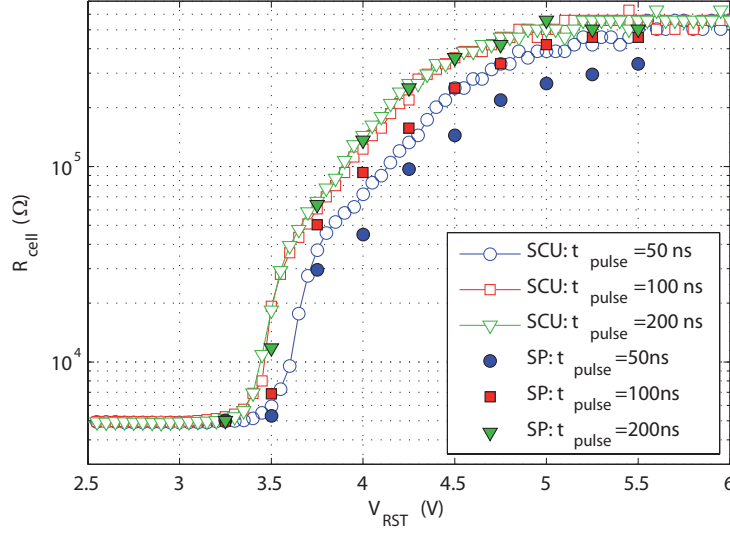


Figure 2.10: Single-pulse programming curve compared to SCU programming curve for different values of  $t_{pulse}$ .

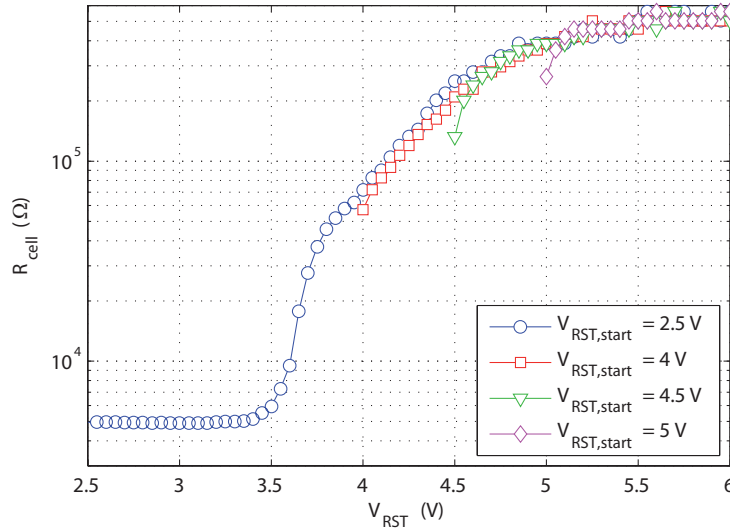


Figure 2.11: Programming curves obtained by means of the SCU algorithm in Fig. 2.7 with different values of  $V_{RST,start}$  ( $t_{pulse} = 50$  ns).

the pulse duration is increased, the obtained state becomes independent from the previous one. This behavior is apparent in Fig. 2.10, where staircase-up programming is compared to SP programming. A significant difference between the programming curves in the two cases can be observed only for low values of  $t_{pulse}$ . For high values of the pulse duration ( $t_{pulse} \geq 200$  ns), the programming curve is substantially independent of the considered programming procedures.

Finally, when SCU programming sequences with different values of the initial RESET voltage,  $V_{RST,start}$  are used, as in Figure 2.11, only few partial-RESET pulses are required to cancel the dependence of the programming curve on the value of  $V_{RST,start}$ . This property is beneficial from the viewpoint of ML programming speed, as will be explained in next Section.

### 2.1.3 Array analysis of SCU programming

In order to analyze the feasibility of ML partial-RESET programming, the performance of the SCU programming algorithm needs to be evaluated over an array of memory cells. To this end, the sequence of SCU programming pulses in Fig. 2.7 with  $V_{RST,start} = 3$  V,  $\Delta V = 25$  mV, and  $t_{pulse} = 50$  ns was applied to an array of 1K cells. The obtained programming curves greatly vary from cell to cell (see the highlighted region in Fig. 2.12) due to the intra-array variability of device parameters. In particular, since different cells reach different values of maximum resistance, a remarkable spread in the high resistance value of the programming curve is apparent. Therefore, in our case, the resistance window where programmed levels can be reliably allocated corresponds to the range from  $R_{min} \simeq 5$  k $\Omega$  to  $R_{max} \simeq 200$  k $\Omega$ .

The spread between different cells inside the array makes blind partial-RESET ML programming not applicable. Nevertheless, a Program & Verify (P&V) technique [54, 55] can be adopted to compensate for this spread and improve the accuracy of programmed resistance levels. In Program & Verify, when the read current corresponding to the programmed state decreases below a target value for the considered level, the staircase-up algorithm is stopped. The maximum voltage applied to the cell is named  $V_{RST,stop}$ . Since  $V_{RST,stop}$  depends on the cell characteristics, P&V is also beneficial for compensating the observed intra-array spreads.



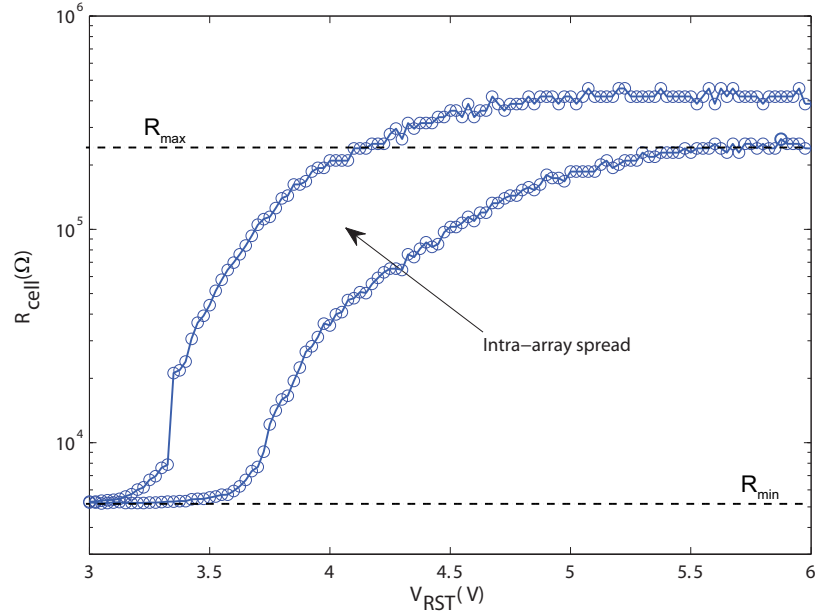


Figure 2.12: Spread of the measured SCU partial-RESET programming curves over the considered 1K-cell array with  $V_{RST,start} = 3$  V,  $\Delta V = 25$  mV, and  $t_{pulse} = 50$  ns.

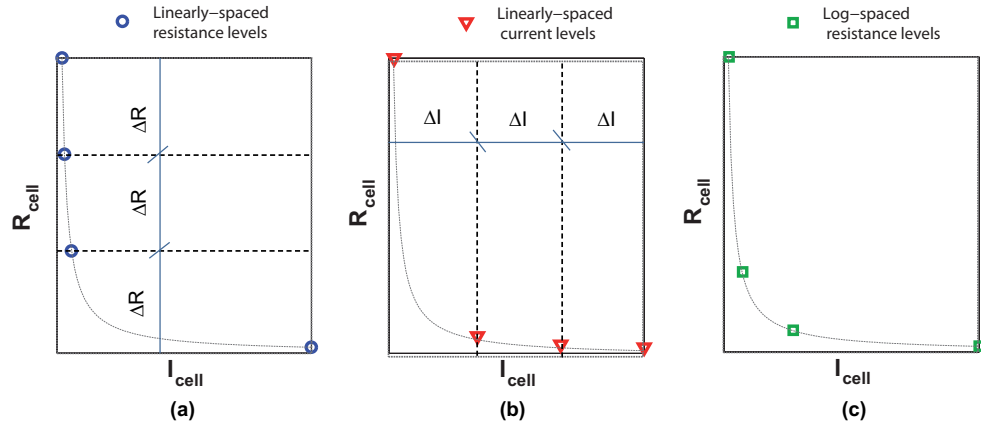


Figure 2.13: Multilevel spacing strategies: (a) linearly-spaced resistance levels, (b) linearly-spaced read current levels, and (c) log-spaced levels.

The choice of the spacing between adjacent programmed levels within the available window is driven by trade-off considerations between program and read operations. From the viewpoint of partial-RESET programming, the parameter which is directly controlled when applying a partial-RESET pulse to the cell is the thickness of the obtained amorphous cap that, to a first approximation, determines the cell resistance through a proportionality relationship inside a reasonable resistance range [56]. Then, the intrinsic mechanism of partial-RESET programming suggests to choose equally spaced levels within the available resistance window, as shown in Fig. 2.13(a). In this case, the obtained distributions and the corresponding histograms of  $V_{RST,stop}$  are shown in Fig. 2.14 and 2.15, respectively. However, when adopting a current sensing approach, like in our case, this choice results in current levels very close to one another in the lower part of the read current window, which implies long sensing time to achieve the necessary accuracy.

On the other hand, the optimum choice from the sensing viewpoint, that is to equally space the programmed levels within the available read current window [Fig. 2.13(b)], increases the programming accuracy required for low-resistance levels, which results in longer programming time.

A reasonable trade-off between programming and readout requirements is to choose log-spaced levels inside the available resistance window, as depicted in Fig. 2.13(c). This way, the intermediate read current levels are shifted toward higher values as compared to the case of equally-spaced resistance levels, thus relaxing the sensing accuracy requirements. In addition, the minimum required difference in the cell resistance (and, hence, in the amorphous cap thickness) between adjacent levels is higher with respect to the case of equally spaced read current levels, thus relaxing also the programming accuracy requirements.

Furthermore, using log-spaced levels is beneficial when considering the effect of the resistance drift phenomenon [57, 58, 59] which determines an increase of the cell resistance over time following a power-law.

In fact, as will be shown in Chapter 4, the drift coefficient increases for increasing values of the cell resistance, leading to a faster dynamics. Then, the resistance shift due to drift during a given time interval after programming increases with the programmed resistance value. This higher shift is

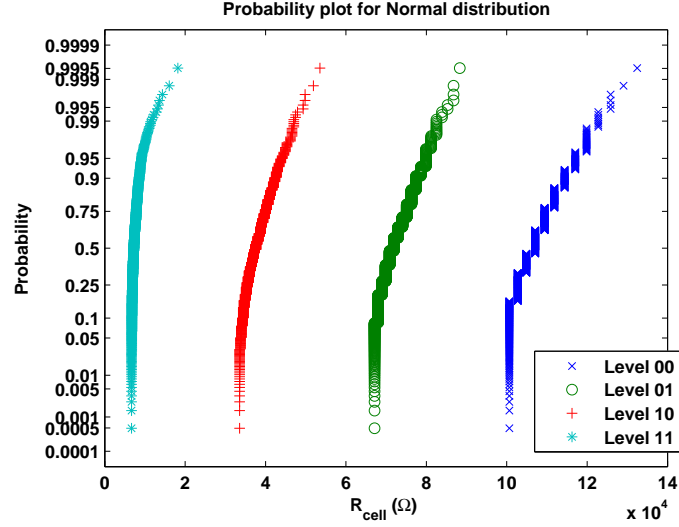


Figure 2.14: Cumulative distributions of the programmed resistance levels in linear resistance spacing. The intermediate levels are obtained by means of the SCU partial-RESET algorithm ( $V_{RST,start} = 2.5$  V,  $\Delta V = 50$  mV, and  $t_{pulse} = 50$  ns).

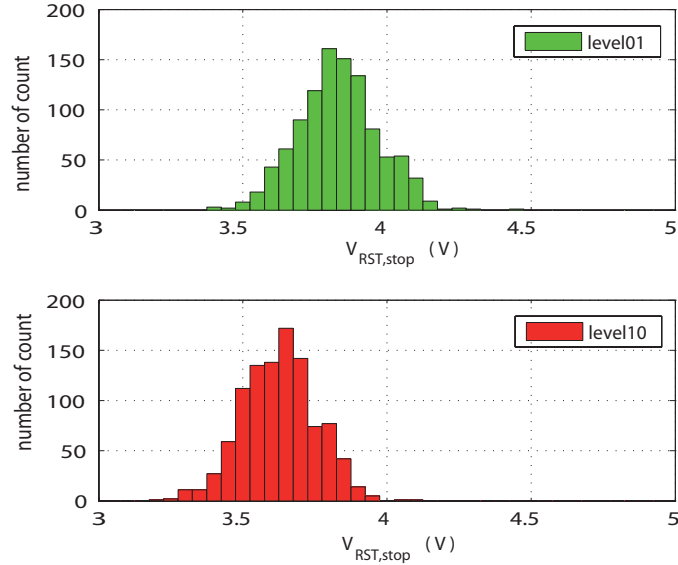


Figure 2.15: Histograms of the maximum programming voltage,  $V_{RST,stop}$ , required to achieve the intermediate levels of Fig. 2.14.

compensated for in log-spaced levels by the inter-level distance, which also increases with the programmed resistance level (high resistance levels are more distant from one another than low resistance levels), as schematically depicted in Fig. 2.16. In this respect, the log-spacing strategy represents an interesting solution to improve reliability, although a drift cancelation technique [52, 59, 60] may still be required when addressing high density ML storage in PCMs.

By adopting the log-spacing strategy in Fig. 2.13(c), it was possible to achieve the 4 resistance distributions in Fig. 2.17 (1K cells for each distribution). Level 11 was achieved by means of an SCD SET programming procedure. Level 00 was obtained by means of a single 50-ns RESET pulse whose amplitude (in our case  $V_{RST} = 6$  V) was chosen so as to guarantee that the read current of each RESET cell was lower than  $1.5 \mu\text{A}$ . The intermediate levels (10 and 01) were achieved by means of the SCU programming sequence in Fig. 2.7 ( $V_{RST,start} = 2.5$  V,  $\Delta V = 50$  mV, and  $t_{pulse} = 50$  ns). The target level for the P&V operation was set to  $5 \mu\text{A}$  for level 01 and  $21 \mu\text{A}$  for level 10. Figure 2.18 shows the histograms of the highest voltage ( $V_{RST,stop}$ ) of the SCU sequence required to obtain the intermediate levels in Fig. 2.17.

In SCU partial-RESET programming, once the initial programming voltage  $V_{RST,start}$  and the voltage step  $\Delta V$  are chosen, the worst-case programming time linearly increases with the maximum value of  $V_{RST,stop}$  over the array. Indeed, the maximum number of required programming pulses is in practice equal to  $n = \frac{V_{RST,stop} - V_{RST,start}}{\Delta V}$ . Nevertheless, the programming time may be reduced by adapting the value  $V_{RST,start}$  as a function of the target resistance level. In fact, as shown above (Section 2.1.2), the dependence of the SCU programming curve on  $V_{RST,start}$  vanishes after few programming pulses. Then, the value of  $V_{RST,start}$  for each target resistance level may be chosen as the minimum value of  $V_{RST,stop}$  of the corresponding histogram in Fig. 2.18 decreased by  $k\Delta V$ , where  $k$  is on the order of few units. This way, the maximum number of required programming pulses and, hence, the worst-case programming time for the considered resistance level turn out to be roughly proportional to the number of bins of the associated histogram of  $V_{RST,stop}$ . The number of bins is higher for the histogram of level 01, which

is therefore the slowest level from the programming viewpoint, whereas it is lower for level 10. This may be ascribed to the lower slope of the  $R_{cell}$  vs  $V_{RST}$  curve for high values of cell resistance due to the resistance saturation effects.

Programming time should be traded with the width of programmed resistance distributions. In fact, an increase in the programming voltage step  $\Delta V$  entails a lower number of SCU pulses on the one side and a lower programming accuracy on the other. To analyze this point, the considered 1K-cell array was programmed by means of the same P&V SCU algorithm as above with the following parameters:  $V_{RST,start} = 2.5$  V,  $\Delta V = 75$  mV, and  $t_{pulse} = 50$  ns. The verify current levels were set to  $3.5 \mu\text{A}$  for level 01 and  $20 \mu\text{A}$  for level 10. The obtained distributions and the corresponding histograms of  $V_{RST,stop}$  are shown in Fig. 2.19 and Fig. 2.20, respectively. It can be noticed that the number of pulses necessary to program levels 01 and 10 is significantly decreased with respect to the previous case, where  $\Delta V = 50$  mV (the average number of pulses is now  $n = 14$  for level 01 and  $n = 10$

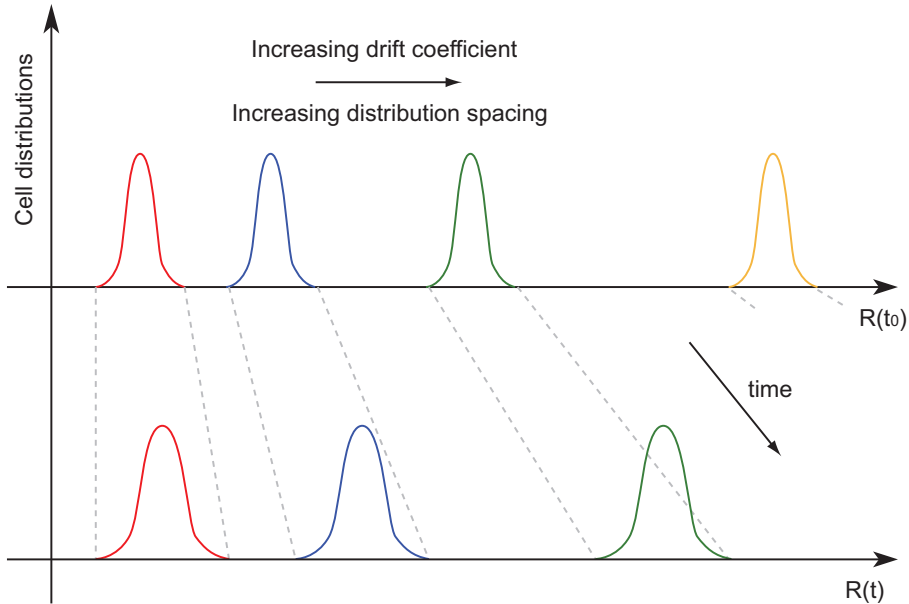


Figure 2.16: Effect of resistance drift on programmed cell distributions. The shift due to drift increases with the programmed resistance value.

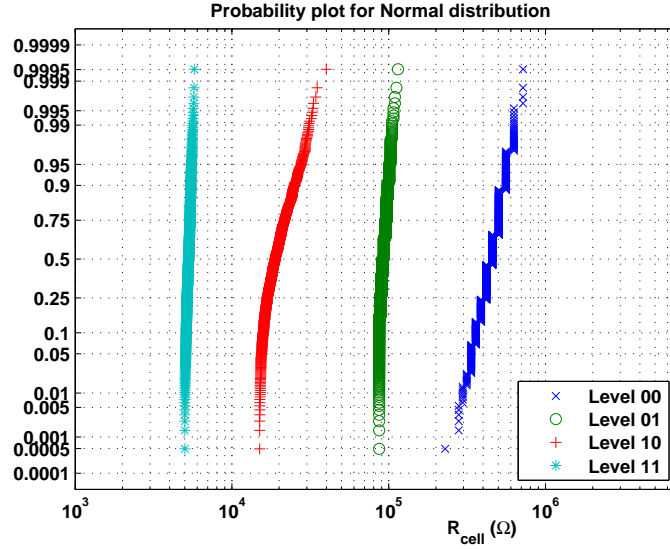


Figure 2.17: Cumulative distributions of the programmed resistance levels in log-spacing: level 01 and level 10 are obtained by means of the P&V SCU algorithm ( $V_{RST,start} = 2.5$  V,  $\Delta V = 50$  mV, and  $t_{pulse} = 50$  ns), while level 00 and level 11 are obtained by means of a single RESET pulse ( $t_{pulse} = 50$  ns,  $V_{RST} = 6$  V) and a SCD procedure, respectively.

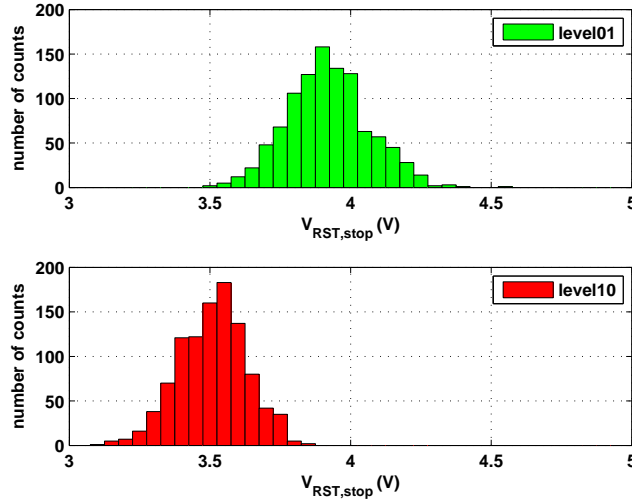


Figure 2.18: Histograms of the maximum programming voltage,  $V_{RST,stop}$ , used to obtain resistance levels 01 and 10 of Fig. 2.17.

for level 10). On the other hand, the width of the programmed resistance distributions is slightly increased.

A possible approach to conjugate high programming speed and high accuracy is to use the minimum programming pulse duration (50 ns in our case) and choose a specific value of  $\Delta V$  for each intermediate target resistance level. Once the target width of the intermediate resistance distributions is set, the number of programming steps can be minimized by first determining the minimum  $\Delta V$  required to program level 10 with the desired accuracy. Then, a higher value of  $\Delta V$  may be adopted for level 01 in order to compensate for the larger spread of  $V_{RST,stop}$ .

Another approach to reduce the number of required programming steps is to adopt a bi-directional programming algorithm [61] rather than the SCU algorithm. In partial-RESET SCU programming, the amorphous volume sizes are progressively increased until the desired resistance level is achieved. In the bi-directional approach, the amorphous volume sizes may be either increased or decreased at each programming step in order to rapidly converge to the target resistance value. Since with the bi-directional algorithm, the cell resistance converges to the desired range by overshooting and undershooting around the target value, two verify operations may be required in order to verify that the read current is close enough to the target level (one verify operation is required for the upper boundary and the other for the lower boundary of the resistance range for each programmed level). Then, bi-directional programming needs a more complex verify operation with respect to SCU programming, where the resistance distributions are obtained by only verifying if the read current decreases below a reference value. In fact, the maximum decrease of the read current (i.e., the cell resistance increase) given by a pulse of the SCU sequence is limited and can be reduced by decreasing the voltage step, thus tightening the resistance distributions as shown above.

To analyze the limits of bi-directionality in partial-RESET programming, the measurements shown in Fig. 2.21(a) were performed on a single cell. The PCM cell was first brought into the full-RESET state and, then, a sequence of identical partial-RESET pulses was applied to the device to re-crystallize a portion of the active area and reduce the cell resistance. As shown in Fig.

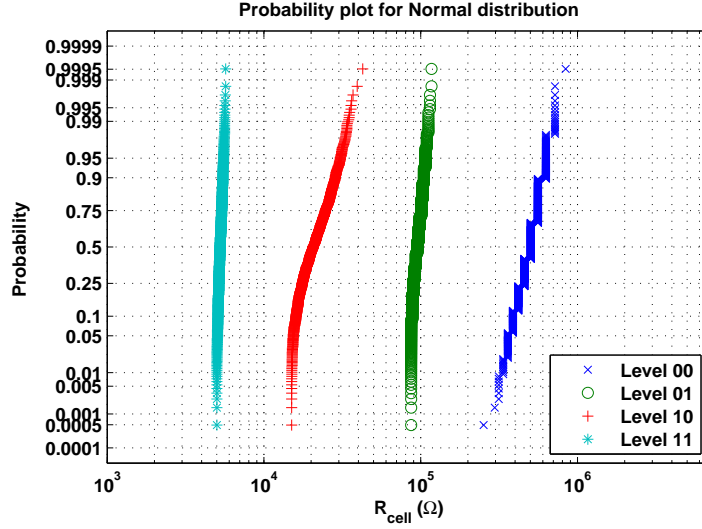


Figure 2.19: Cumulative distributions of the programmed resistance levels: level 01 and level 10 are obtained by means of the P&V SCU algorithm ( $V_{RST,start} = 2.5$  V,  $\Delta V = 75$  mV, and  $t_{pulse} = 50$  ns), while level 00 and level 11 are obtained by means of a single RESET pulse ( $t_{pulse} = 50$  ns,  $V_{RST} = 6$  V) and a SCD procedure, respectively.

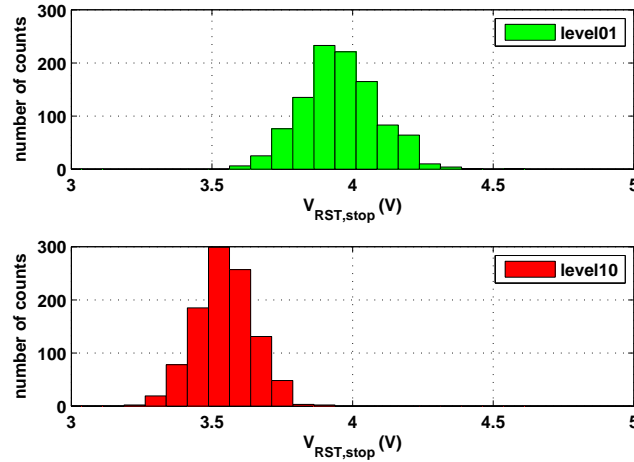
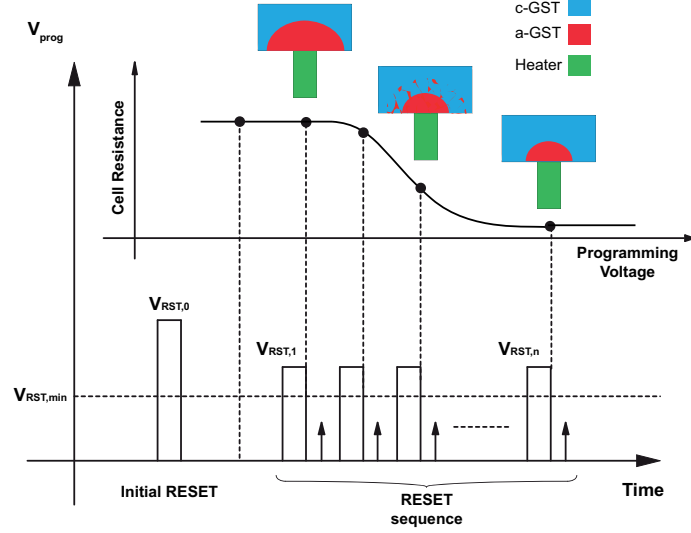
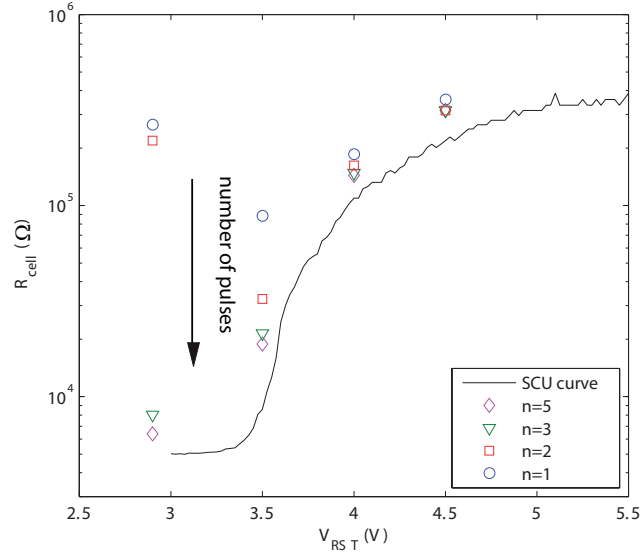


Figure 2.20: Histograms of the maximum programming voltage,  $V_{RST,stop}$ , used to obtain resistance levels 01 and 10 of Fig. 2.19.





(a)



(b)

Figure 2.21: Sequence of programming pulses used to investigate the bi-directionality of partial-RESET programming (a) and comparison of the obtained results with the SCU programming curve (b).

2.21(b), the obtained resistance values become closer to the values obtained in SCU programming with increasing number of pulses, which crystallize the region surrounding the GST melted zone.

Furthermore, since the crystallization process must be activated to reduce the amorphous volume size, the crystallization dynamics imposes a lower limit to the programming pulse duration (or to the minimum number of identical pulses) in the bi-directional approach, which impacts on the achievable programming time.

## 2.2 Partial-SET programming

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In SCU partial-SET programming, the memory cell first undergoes a full-RESET operation and, then, a sequence of partial-SET programming pulses is applied in order to partially crystallize the initially amorphous chalcogenide. The SCU sequence is applied to the gate of transistor  $Y_0$  for voltage programming, and to the gate of transistor  $M_{SEL}$  for current programming. Unlike partial-RESET programming, partial-SET programming is sensitive to the effects of threshold switching and, thus, different results are obtained when forcing current or voltage to program the memory cell.

The phase distribution achieved after a partial-SET pulse is substantially parallel, with a conductive path that shunts the remaining amorphous phase [62, 63, 64, 65]. Some evidence of incomplete filament formation in partial-SET states has also been provided in the literature [66], but concerning states having very high resistance close to the full-RESET state resistance, that corresponds to a small fraction of the programming window.

In order to better highlight the characteristics of partial-SET programming, in the following study programming curves plotting  $I_{cell}$  versus programming voltage will be provided.

### 2.2.1 Single-pulse programming

To investigate the feasibility of single-pulse programming for partial-SET ML storage, the single-cell programming characteristic (i.e., the curve which provides  $I_{cell}$  as a function of the programming pulse amplitude) was measured by means of the procedure depicted in Fig. 2.22 [67].

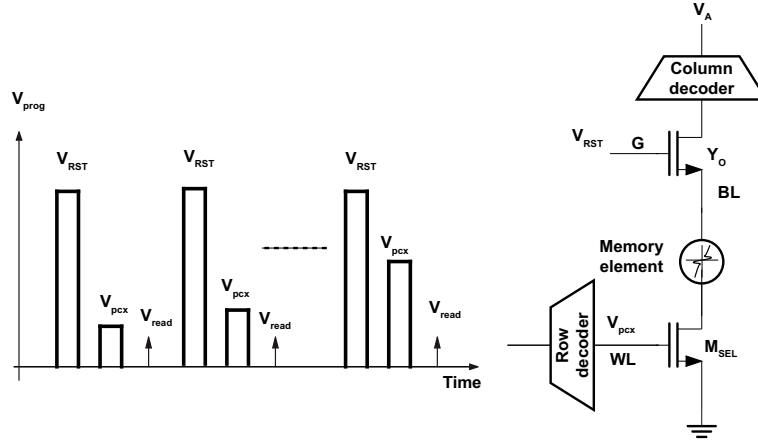


Figure 2.22: Sequence of voltage pulses applied to the gate of transistor  $Y_0$  ( $V_{RST}$ ) and to the gate of  $M_{SEL}$  ( $V_{pcx}$ ) during the characterization of the single-pulse programming (SPP) approach. Each current partial-SET pulse has an amplitude higher than the previous one and is preceded by a voltage RESET pulse. After each partial-SET pulse, a read operation is carried out so as to evaluate the read cell current, which allows the programming curve to be obtained.

The cell successively undergoes a voltage RESET operation, a SET operation (voltage pulse amplitude =  $V_{SET}$  applied to the gate of  $M_{SEL}$ ), and a DMA readout operation. The above sequence was repeated while increasing the SET programming pulse amplitude by an amount  $\Delta V$  at any step, until the complete programming curve was obtained. Since a single SET pulse was applied after a RESET pulse to program the cell to an intermediate resistance state, this programming sequence is referred to as single-pulse (SP) programming in the following. More in detail,  $\Delta V$  was set to 25 mV and the time length of each partial-SET program pulse,  $t_{pulse}$ , was varied from 100 ns to 500 ns.

The dependence of the programmed cell current on pulse duration is shown in Fig. 2.23. It can be observed that a pulse length of 100 ns is not sufficient to determine a significant increase of  $I_{cell}$ , even though the programming current for the considered values of  $V_{pcx}$  is higher than the threshold current. A 100-ns pulse turns out to be too short to crystallize a sufficient amount of chalcogenide to obtain a complete crystalline path that shunts the

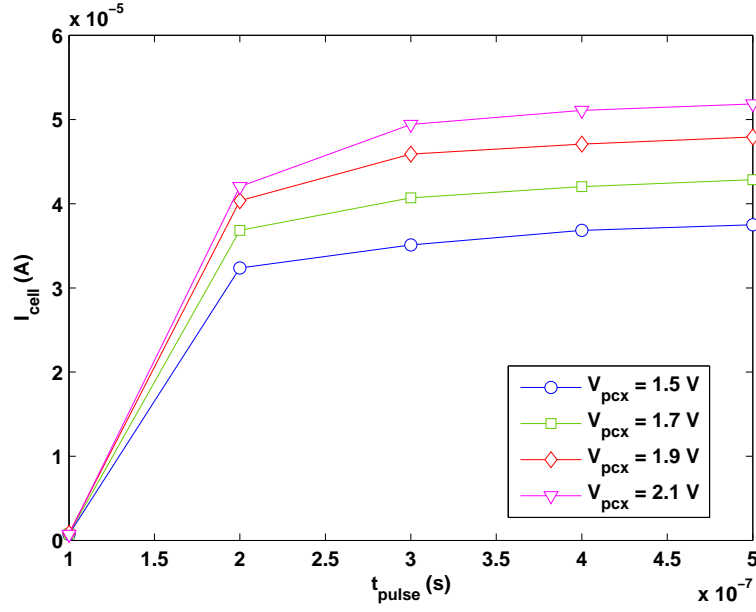


Figure 2.23: Dependence of  $I_{cell}$  on pulse duration for different values of  $V_{pcx}$ . For the initial RESET operation,  $V_{RST} = 5 V$  and  $t_{pulse} = 100 ns$ .

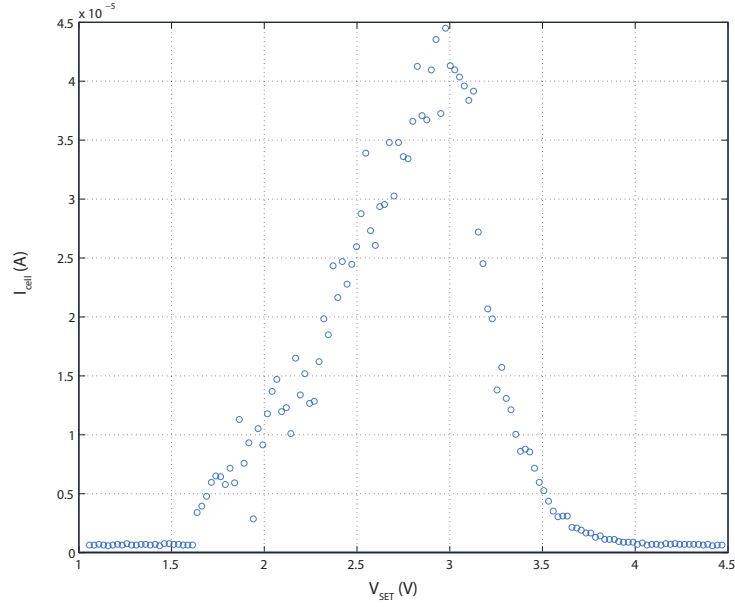


Figure 2.24: Programming characteristic of a PCM cell when following the partial-SET SP programming approach (program pulse length  $t_{pulse} = 500 ns$ ).

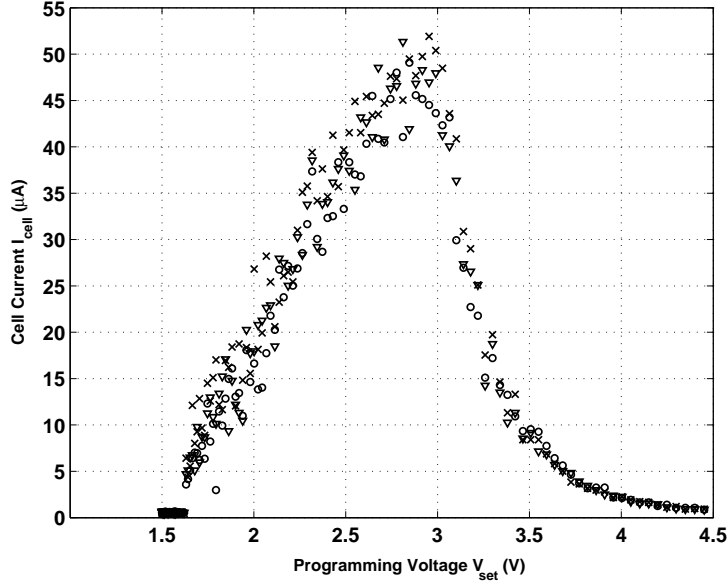


Figure 2.25: Repeated measurements of the programming characteristic of the same PCM cell when following the partial-SET SP programming approach.

resistance of the remaining amorphous volume (the fraction of crystalline phase inside the amorphous cap is lower than the critical value necessary to achieve a parallel phase configuration). The programming curve of a single cell is shown in Fig. 2.24. It can be noticed that a significant increase of the read cell current with respect to the value in the RESET state takes place when  $V_{SET}$  reaches about 1.6 V. This value is related to the electronic switching phenomenon in amorphous GST [21, 68], which is responsible for a sudden drop of the electrical resistivity of amorphous phase when the voltage across the memory cell exceeds the switching voltage  $V_{th}$ . When the voltage applied across the cell reaches  $V_{th}$ , the programming current raises, thus leading to a significant increase of the temperature inside the GST which strongly activates the amorphous-to-crystalline phase transition.

From Fig. 2.24, the programming characteristic shows a substantially linear average increase of  $I_{cell}$  for increasing values of  $V_{SET}$  (slope  $\Delta I_{cell} / \Delta V_{SET} \simeq 30 \mu\text{A/V}$ ). Nevertheless, the random nature of both the amorphization process (during the RESET pulse) and the crystallization process

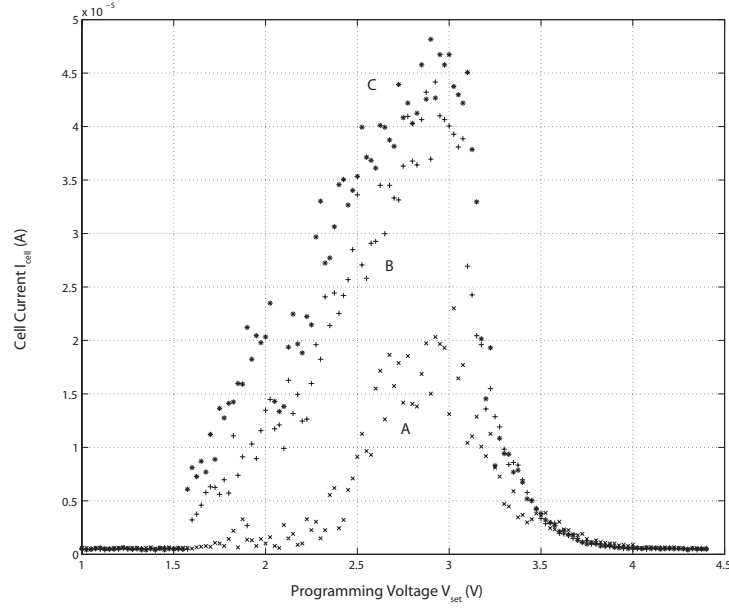


Figure 2.26: Programming characteristics obtained with the partial-SET SP programming technique for different values of program pulse time length  $t_P$ : 50 ns (A,  $\times$ ), 500 ns (B,  $+$ ), and 1  $\mu$ s (C,  $*$ ).

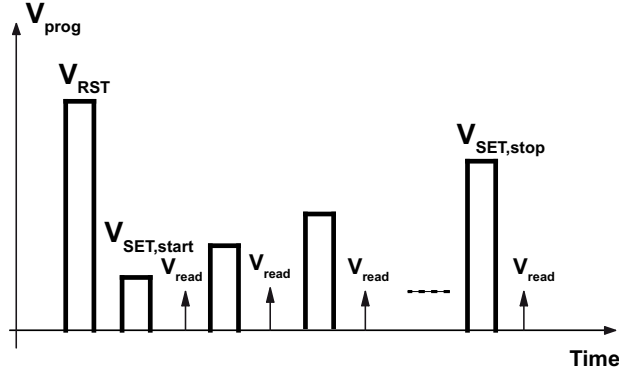


Figure 2.27: Voltage waveform applied to the gate of transistor  $Y_0$  during a voltage SCU programming routine. After an initial RESET, the cell current is read and, hence, a sequence of program pulses is applied. A read operation is carried out after each program pulse.

(during the partial-SET pulse) gives rise to a considerable statistical spread of the programmed cell resistance. Thus, if the measurements of Fig. 2.22 are repeated on the same cell a number of times, different programming curves are achieved, as shown in Fig. 2.25. Although the mean characteristic curve of a single cell can in principle be obtained by averaging repeated measurements, the mean programming curve of different cells shows non-negligible differences, due to the fabrication process spreads of the cell geometrical parameters between different chips and even within a memory array in a chip. Then, it is hardly possible to choose the optimum value of the pulse amplitude  $V_{SET}$  to be used for programming a RESET cell to obtain a given target read current level. Furthermore, no convergence towards the target read current value is observed when the programming sequence (RESET pulse followed by a single SET pulse) is repeated on the same cell. As a consequence, SP programming cannot take full advantage of Program-and-Verify technique implementation [54, 55].

From the above considerations, the SP programming algorithm appears to be inadequate to guarantee the high programming accuracy required for ML programming, mainly due to the stochastic nature of the phenomena involved in programming operations and to fabrication process spreads.

### 2.2.2 Staircase-up voltage programming

The drawbacks of SP partial-SET programming can be overcome by using a multi-pulse programming algorithm like in partial-RESET approach. In voltage SCU partial-SET programming, a sequence of programming voltage pulses with increasing amplitude is applied to the gate of  $Y_0$ , as shown in Fig. 2.27. The SCU procedure stops when the read current (measured after each programming pulse) exceeds the reference value for the considered level. The minimum and the maximum voltage applied to the gate of  $Y_0$  are named  $V_{SET,min}$  and  $V_{SET,max}$ , respectively.

In this case, the crystallization process takes place inside the active GST volume in a cumulative way, since each pulse increases the PCM cell conductance obtained with the preceding pulse by increasing the cross section of the crystalline path that is dug inside the initially amorphous active volume [62, 63, 64, 65]. As a consequence, the cell resistance gradually decreases as

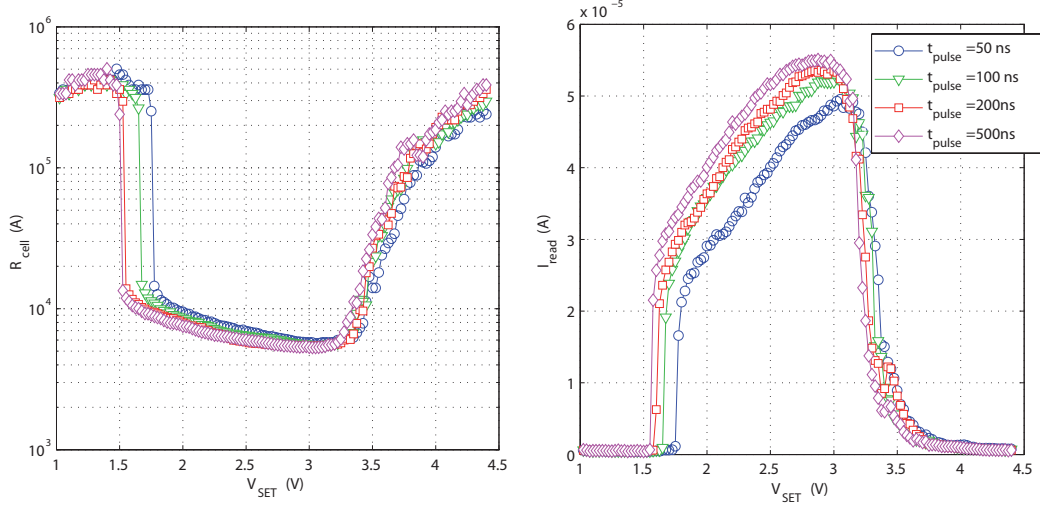


Figure 2.28: Experimental programming curves when using the voltage SCU algorithm for different values of  $t_{\text{pulse}}$  ( $\Delta V = 25$  mV).

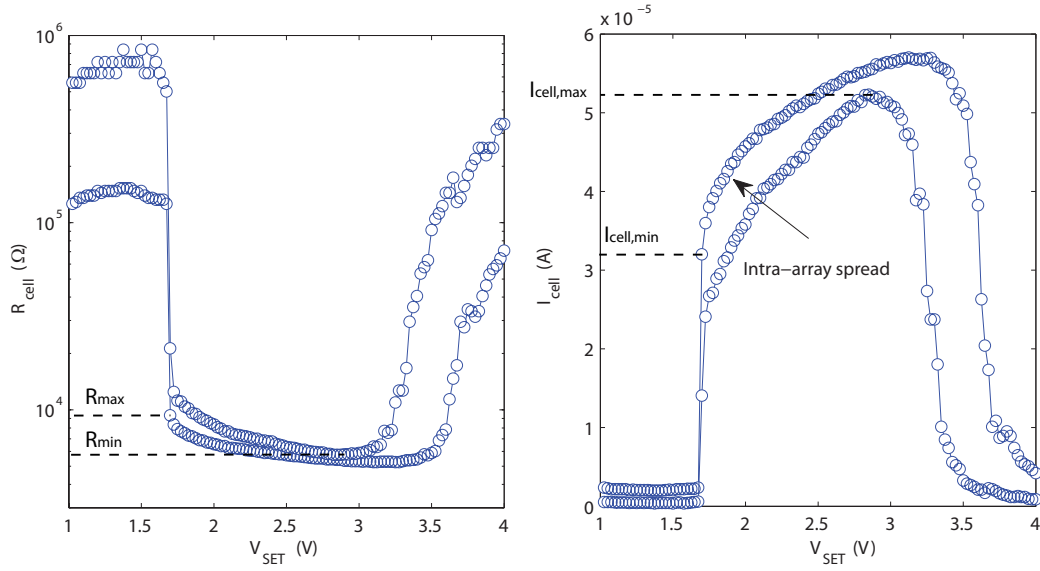


Figure 2.29: Spread of the measured partial-SET SCU voltage programming curves over the considered 1K-cell array ( $t_{\text{pulse}} = 100$  ns).



the number of cumulative SET pulses increases, and the programming curve is therefore inherently monotonic, as is apparent in Fig. 2.28.

The experimental characterization was carried out with the following parameters:  $V_{SET,start} = 1$  V,  $\Delta V = 25$  mV, and different values of  $t_{pulse}$  ranging from 50 ns to 500 ns.

It can be noticed that the monotonicity of the programming curve is preserved, although the obtained programming curve still varies from cell to cell (Fig. 2.29). Then, we can implement ML storage by adopting a conventional P&V approach, which allows the programming routine to be stopped when the target cell current value is reached, thereby ensuring the required programming accuracy. This has also been experimentally demonstrated in the literature [13].

From Fig. 2.28, it can be further noticed that a high variation of the read current is achieved with the first effective partial-SET pulses. Since a low slope of the programming curve is desired to program the cell state with high accuracy, it can be observed that voltage programming restricts the available programming range for intermediate levels. In fact, the intermediate levels may be reliably programmed to read current values higher than the highest value of  $I_{cell,min}$  in Fig. 2.29 (for the considered array of cells,  $I_{cell,min} \simeq 30$   $\mu$ A) and lower than the lowest value of  $I_{cell,max}$  (about 50  $\mu$ A for the considered cells), or equivalently, in the range from  $R_{min}$  to  $R_{max}$ .

### 2.2.3 Staircase-up current programming

The sequence of program and read pulses used to obtain the SCU current programming curve is shown in Fig. 2.30. After a RESET pulse, a sequence of SCU partial-SET pulses is applied to the cell starting from  $V_{pcx,min}$  (applied to the gate of  $M_{SEL}$ ), each one followed by a readout operation. The SCU procedure is stopped when the read current value exceeds the target value for the considered level. The maximum value of  $V_{pcx}$  is named  $V_{pcx,stop}$ , and corresponds to the programming current value  $I_{p,stop}$ .

The typical shape of a current-driven SCU programming curve is shown in Fig. 2.31 for different values of  $t_{pulse}$  ( $\Delta V = 25$  mV). It can be noticed that there is no significant restriction of the available programming range for the intermediate levels, provided that the pulse duration is sufficiently

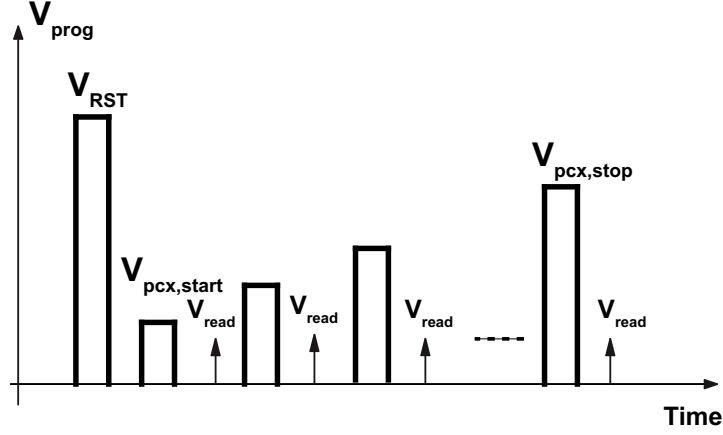


Figure 2.30: Programming pulses used to obtain the partial-SET SCU current programming curve. After an initial RESET, the cell current is read and, hence, a sequence of program pulses is applied to the gate of transistor  $M_{SEL}$ . A read operation is carried out after each program pulse.

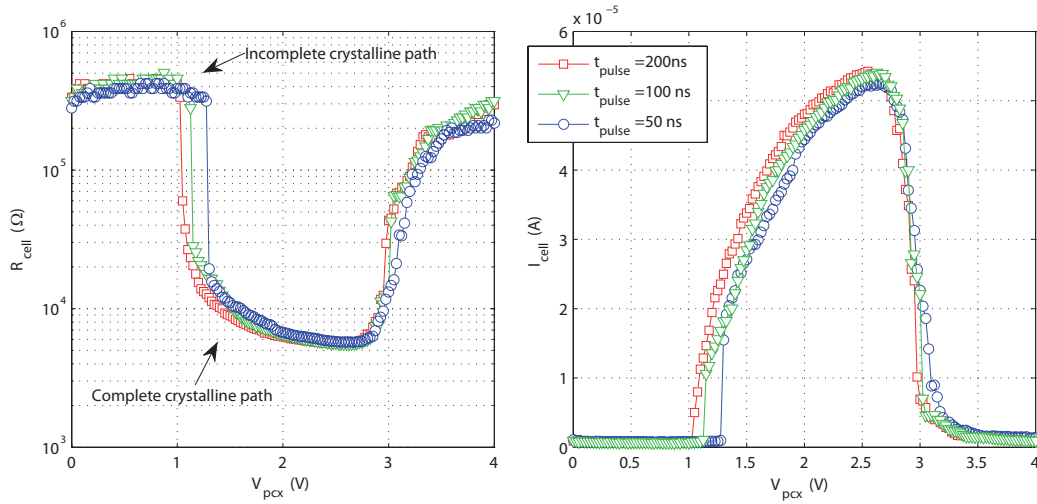


Figure 2.31: Measured programming curves when using the partial-SET current SCU algorithm for different values of  $t_{pulse}$  ( $\Delta V = 25$  mV).

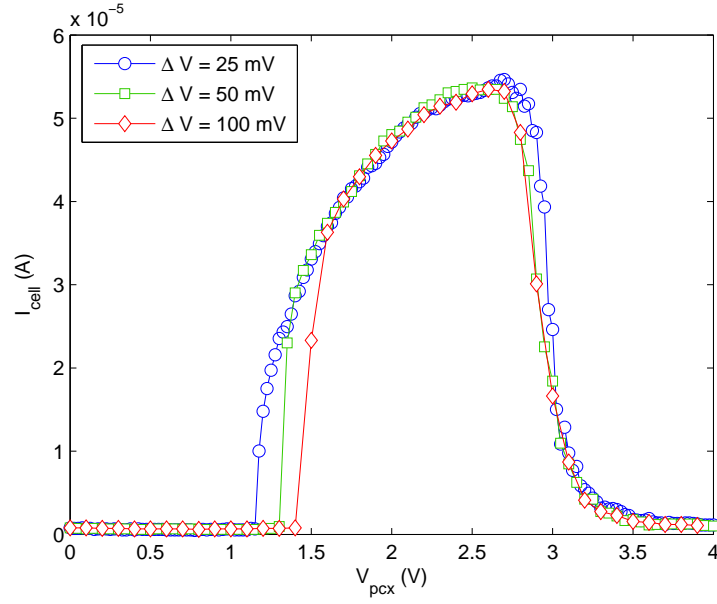


Figure 2.32: Programming curves when using the partial-SET current SCU algorithm for different values of  $\Delta V$  ( $t_{pulse} = 100$  ns).

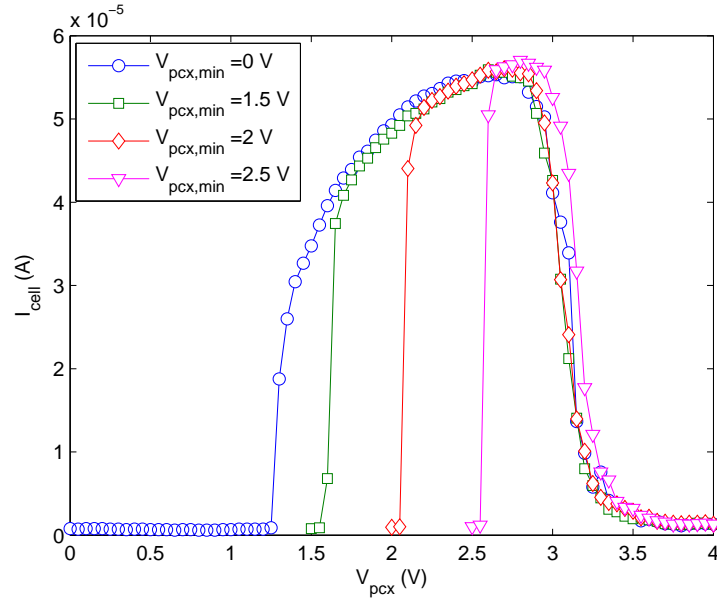


Figure 2.33: Programming curves when using the partial-SET current SCU algorithm for different values of  $V_{pcx,min}$  ( $t_{pulse} = 100$  ns,  $\Delta V = 25$  mV).

high. As  $t_{pulse}$  is decreased below a given value (100 ns in our case), the first effective pulse determines a significant increase of  $I_{cell}$ . This behavior is ascribed to the time required to form a complete crystalline path inside the amorphous volume, i.e. to the time required to crystallize a sufficient amount of chalcogenide to obtain a parallel phase configuration. As can be noticed from the plot on the left side in Fig. 2.31, the first pulses determine only a slight decrease of the cell resistance. This suggests that the crystallization process is activated but the crystallized GST is not sufficient to form a complete crystalline path [66]. As soon as a complete path is dug inside the active volume, the resistance suddenly drops.

The critical crystalline fraction for the formation of a complete path is reached at lower pulse amplitudes (i.e., lower temperatures inside the GST volume) if the programming pulse duration compensates for the lower temperature, thus explaining the observed experimental behavior.

It can be further noticed that, as shown in previous Section, an increase of the pulse duration does not help to enlarge the read current programming window in voltage programming. This difference in the cell behavior is ascribed to the threshold switching phenomenon. In fact, in voltage programming, the switching from the OFF to the ON region of the cell V-I curve determines a remarkable increase of the programming current. By contrast, in the current programming approach,  $V_{pcx}$  controls the programming current which, thus, can be gradually increased without any discontinuity.

However, a substantial restriction of the programming range available in current programming appears when  $\Delta V$  is increased, as shown in Fig. 2.32. In this case, the temperature reached during a programming pulse is significantly higher than the temperature obtained during the preceding pulse, thus speeding up the crystallization process. A similar behavior is observed when using the current partial-SET programming algorithm with different values of  $V_{pcx,min}$ , as depicted in Fig. 2.33. Few pulses are needed to dig a complete crystalline path inside the amorphous phase. When the path is complete, the programming current heats the filament and increases its cross-section, thus determining an increase of  $I_{cell}$ . It is worth noticing that, when the crystalline path is formed, the programming curves obtained with different values of  $V_{pcx,min}$  tend to superimpose. This feature enables

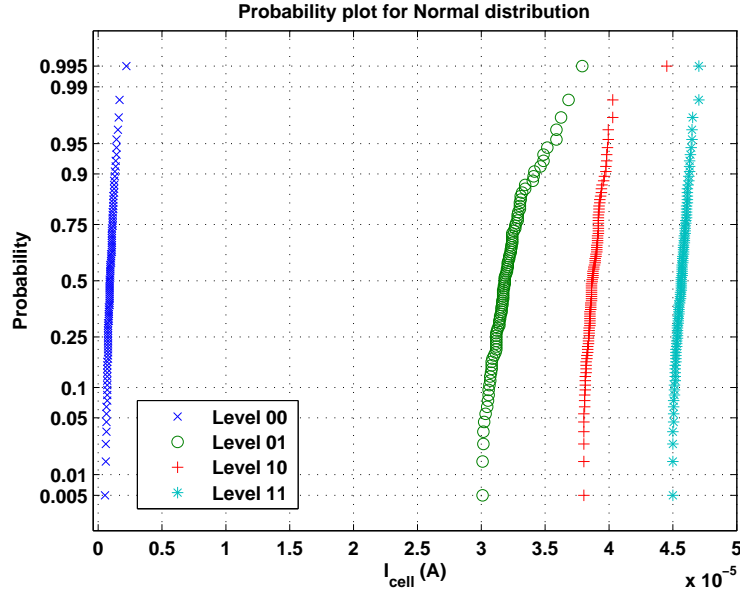


Figure 2.34: Cumulative distributions of the read current levels: level 01 and level 10 are obtained by means of the P&V voltage partial-SET SCU algorithm ( $V_{\text{SET,start}} = 0$  V,  $\Delta V = 50$  mV, and  $t_{\text{pulse}} = 100$  ns), whereas level 00 and level 11 are obtained by means of a single RESET pulse ( $t_{\text{pulse}} = 100$  ns,  $V_{\text{RST}} = 5.2$  V) and an SCD procedure, respectively.

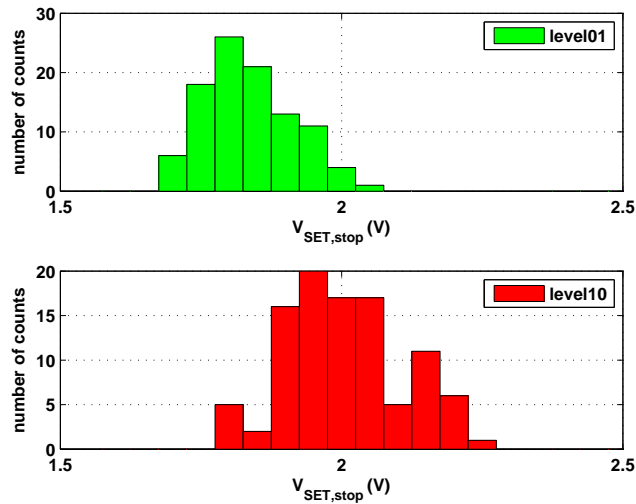


Figure 2.35: Histograms of the maximum programming voltage,  $V_{\text{SET,stop}}$ , used to obtain resistance levels 01 and 10 in Fig. 2.34.

to reduce the number of programming pulses required to reach the desired current level, as in the case of partial-RESET SCU programming.

#### 2.2.4 Array analysis of partial-SET programming

In order to evaluate the effects of the cell parameters spread over the array on partial-SET programming, a sub-array composed of 1K memory cells was considered. First, voltage programming was addressed by applying the sequence of programming pulses shown in Fig. 2.27 to every cell belonging to the array .

Figure 2.34 shows the obtained cumulative distributions of the programmed levels: levels 00 and 11 were obtained respectively, with a single RESET pulse ( $V_{RST} = 5.2$  V,  $t_{pulse} = 100$  ns) and a staircase-down procedure, respectively, whereas intermediate levels 01 and 10 were programmed with the voltage SCU partial-SET approach. The chosen programming parameters were the following:  $V_{SET,min} = 0$  V,  $\Delta V = 50$  mV, and  $t_{pulse} = 100$  ns. The histograms of the maximum values of the programming voltage  $V_{SET,stop}$  to obtain levels 01 and 10 are shown in Fig. 2.35. It can be noticed that the used  $\Delta V$  is not sufficiently small to achieve the necessary programming accuracy.

In order to obtain separate levels,  $\Delta V$  was decreased to 25 mV. The achieved cumulative distributions of the programmed levels are shown in Fig. 2.36, and the corresponding histograms of  $V_{SET,stop}$  are plotted in Fig. 2.37. Since the width of the histograms is roughly proportional to the time duration of the ML programming procedure, as in the case of partial-RESET programming, the worst case is represented by level 10 (more than 25 pulses). In fact, differently from partial-RESET programming, the slope of the  $I_{cell}$  vs  $V_{SET}$  programming curve is higher for low  $I_{cell}$  (i.e., high  $R_{cell}$ ) values. It can be noticed that levels 01, 10, and 11 are very close one to another (the read current spacing is less than 5  $\mu$ A) due to the reduction of the available range for intermediate levels in voltage programming (see Section 2.2.2). As a consequence of the low read margins, the accuracy constraints on current sensing circuits are very stringent.

In order to relax sensing accuracy requirements, partial-SET SCU current programming can be implemented. However, a suitable value of  $\Delta V$  (voltage

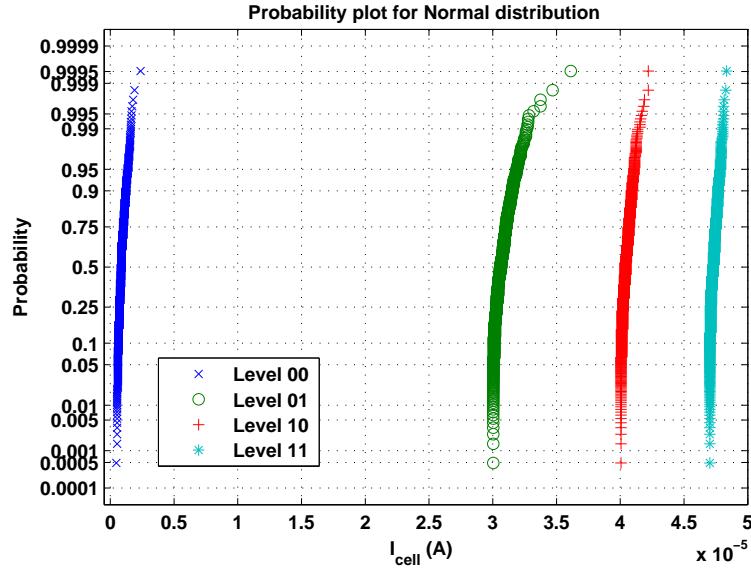


Figure 2.36: Cumulative distributions of the read current levels: level 01 and level 10 are obtained by means of the P&V voltage partial-SET SCU algorithm ( $V_{SET,start} = 0$  V,  $\Delta V = 25$  mV, and  $t_{pulse} = 100$  ns), while level 00 and level 11 are obtained by means of a single RESET pulse ( $t_{pulse} = 100$  ns,  $V_{RST} = 5.2$  V) and an SCD procedure, respectively.

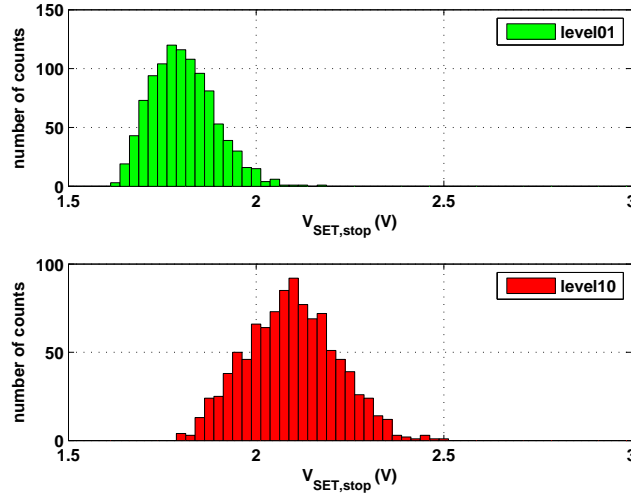


Figure 2.37: Histograms of the maximum programming voltage,  $V_{SET,stop}$ , used to obtain resistance levels 01 and 10 in Fig. 2.36.

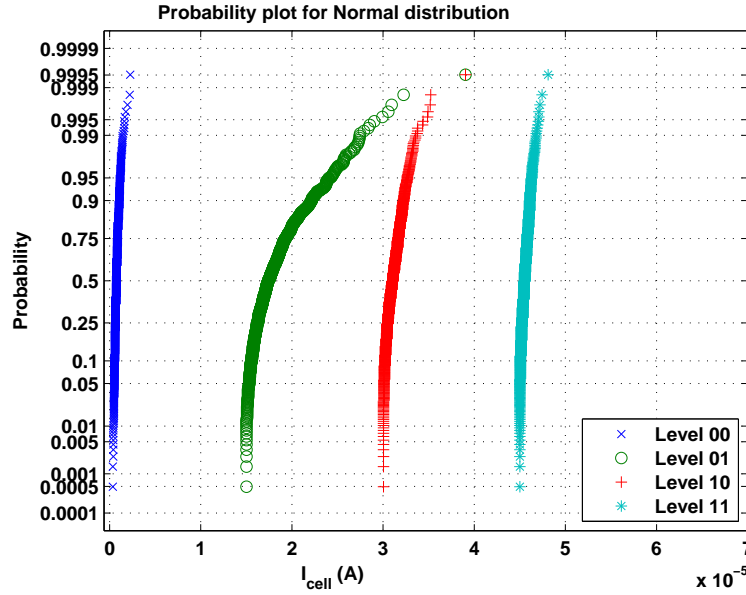


Figure 2.38: Cumulative distributions of the read current levels: level 01 and level 10 are obtained by means of the P&V current partial-SET SCU algorithm ( $V_{\text{pcx,start}} = 0$  V,  $\Delta V = 50$  mV,  $t_{\text{pulse}} = 100$  ns), whereas level 00 and level 11 are obtained by means of a single RESET pulse ( $t_{\text{pulse}} = 100$  ns,  $V_{\text{RST}} = 5.2$  V) and an SCD procedure, respectively.

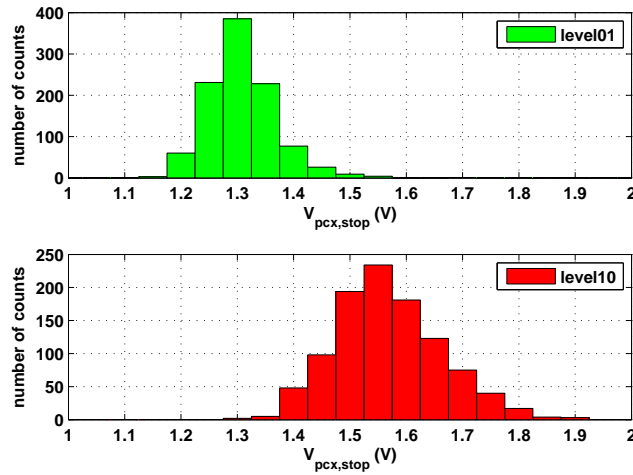


Figure 2.39: Histograms of the maximum programming voltage,  $V_{\text{pcx,stop}}$ , used to obtain resistance levels 01 and 10 in Fig. 2.38.



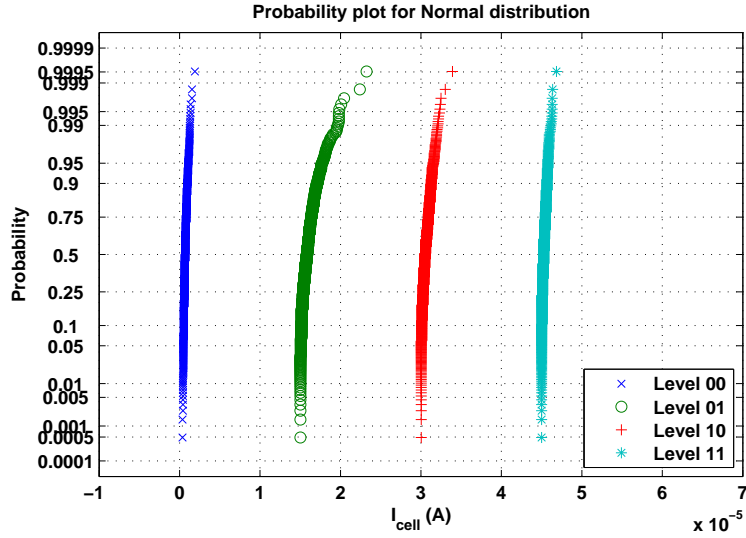


Figure 2.40: Cumulative distributions of the programmed resistance levels: level 01 and level 10 are obtained by means of the P&V current partial-SET SCU algorithm ( $V_{pcx,start} = 0$  V,  $\Delta V = 25$  mV,  $t_{pulse} = 100$  ns), whereas level 00 and level 11 are obtained by means of a single RESET pulse ( $t_{pulse} = 100$  ns,  $V_{RST} = 5.2$  V) and an SCD procedure, respectively.

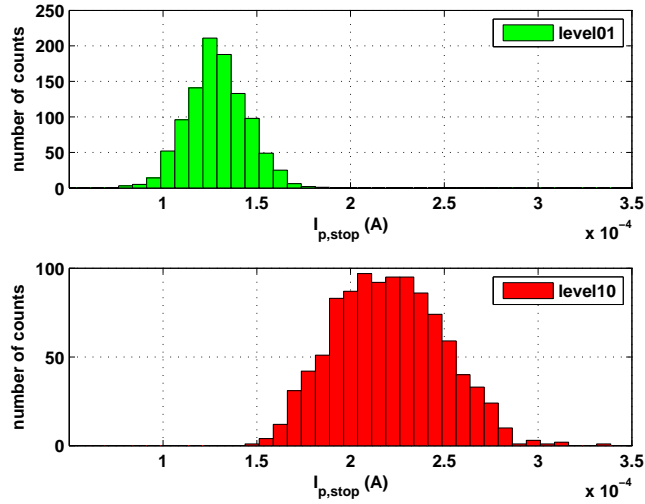


Figure 2.41: Histograms of the maximum programming voltage,  $V_{pcx,stop}$ , used to obtain resistance levels 01 and 10 in Fig. 2.40.

increment between adjacent pulses applied to the gate of  $M_{SEL}$  when performing current programming) must be chosen so as to exploit the whole read current window. For instance, the cumulative plot obtained with  $\Delta V = 50$  mV ( $V_{pcx,min} = 0$  V,  $t_{pulse} = 100$  ns) are plotted in Fig. 2.38, and the corresponding histograms of  $V_{pcx,stop}$  are depicted in Fig. 2.39. It can be observed that, although the number of pulses required for programming the intermediate levels is low,  $\Delta V$  is not small enough to achieve a sufficiently narrow distribution for level 01. Then,  $\Delta V$  was reduced to 25 mV, as in the case of partial-SET voltage programming, obtaining the cumulative distributions and the histograms of  $V_{pcx,stop}$  shown in Figs. 2.40 and 2.41, respectively. The width of level 01 distribution is significantly reduced, whereas the number of the programming pulses is roughly doubled.

# 3

## Compact modeling of a PCM cell

In both partial-SET and partial-RESET programming analyzed in Chapter 2, the resistance of the intermediate states depends on the distribution of the amorphous and crystalline phases inside the GST layer. In particular, the thickness of the amorphous cap obtained after the partial-RESET operation is a key parameter to control the resistance of the intermediate states in the case of partial-RESET programming. However, the amorphous cap thickness is also important in partial-SET programming since, in this case, it affects the maximum value of the cell resistance and, hence, the programmable window (i.e., the resistance range where all programmed states can be allocated).

The amorphous cap size and, as consequence, the cell resistance, are highly sensitive to the process spreads of device parameters (in particular, of the heater dimensions and the chalcogenide thickness). Optimized cell architectures have been proposed in the literature [23, 24, 69, 26] in order to limit the sensitivity of the programmed resistance values to fabrication process spreads. Nevertheless, since the sensitivity of the programmed resistance to device parameters varies with the pulse amplitude, effective and robust ML programming algorithms should be developed even when considering optimized cell geometries.

In this framework, the aim of this Chapter is to present an analytical model for the partial-RESET operation. Section 3.1 presents a physics-based model of partial-RESET which allows to estimate the expected thickness of the amorphous cap and, thus, the expected cell resistance, as a function of the applied RESET pulse amplitude [70]. Moreover, the model can be used to estimate the effect of fabrication process spreads on the amorphous cap

thickness, showing that the resistance sensitivity to device parameter spreads decreases with increasing amplitude of the RESET pulse.

Section 3.2 extends the analytical model to the dynamic case by taking into account the effects of the partial-RESET pulse duration on the phase-change layer resistance. The dynamic model is able to reproduce the memory cell behavior with good accuracy, considering both single-pulse and staircase-up partial-RESET programming.

The proposed models are validated by comparing the obtained relations with experimental data from the same PCM test chip used to investigate the performance of ML programming algorithms in previous Chapter [35].

### 3.1 Analytical model of the partial-RESET operation

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To develop an analytical model capable of estimating the thickness of the amorphous cap obtained after a partial-RESET pulse, the simplified cell geometry of Figure 3.1(a) is considered. The initially crystalline GST amorphizes when heated above the melting point and then quickly cooled down. Thus, the temperature distribution inside the PCM cell is crucial to determine the shape and the thickness of the amorphous cap. The maximum temperature inside the chalcogenide layer, which is achieved very close to the GST-heater interface for the considered  $\mu$ Trench cell architecture [71], is the result of two heating contributions, namely a term  $Q_h$  due to the power generated inside the heater and a term  $Q_{GST}$  generated within the GST (hereinafter, the two terms will be referred to as heater heating and self-heating, respectively). For the cell architecture under study, the self-heating contribution is much lower than the heater-heating contribution, especially when considering high-amplitude RESET pulses which operate the cell in the ON region [64]. In fact, since the crystalline GST shows a semiconductor-like behavior with temperature, the resistance of the fully crystalline layer during the RESET pulse is negligible with respect to the heater resistance  $R_h$ . Even though  $Q_h$  is generated inside the heater volume, for simplicity, we can consider a lumped thermal model in which  $Q_h$  is generated at the heater-GST interface and an equivalent thermal resistance ( $R_{th}$ ) takes the heater efficiency into account. More specifically,  $R_{th}$  is the lumped thermal

resistance of the memory cell as seen from the heater-GST interface to the thermal ground (which is represented by the top-electrode and the bottom-electrode contacts). Thus, we can simply express the maximum temperature at the GST-heater interface,  $T_{max}$ , as

$$T_{max} = R_{th}Q_h + T_0 = R_{th}\frac{V_{cell}^2}{R_h} + T_0, \quad (3.1)$$

where  $V_{cell}$  is the voltage applied across the PCM cell during the partial-RESET operation and  $T_0$  is room temperature.

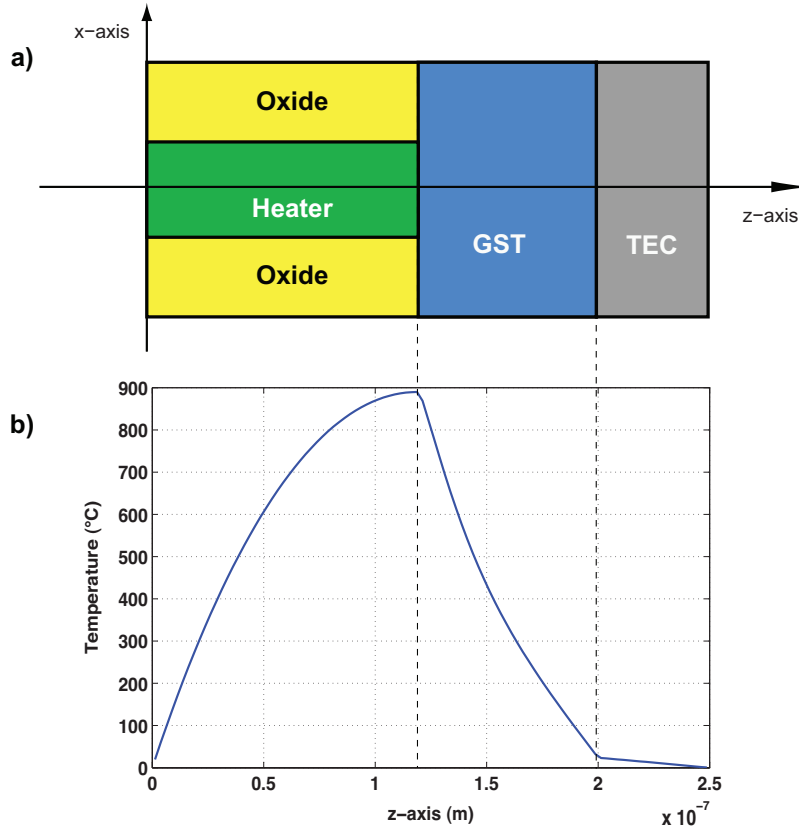


Figure 3.1: Simplified cell geometry for simulating the temperature distribution inside the PCM cell (a) and obtained temperature profile along the AA section of the upper figure (b).

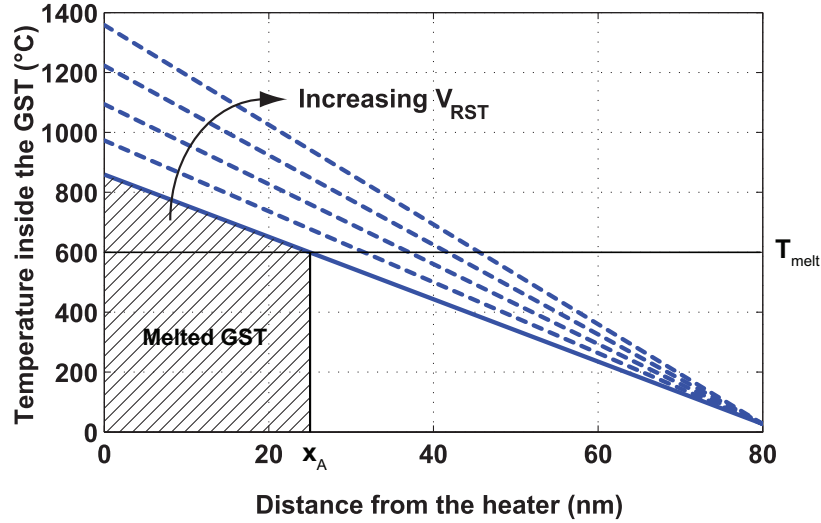


Figure 3.2: Linearized temperature profile inside the GST layer during a RESET operation.

The temperature inside the GST layer decreases along the  $z$ -axis from its maximum value to a minimum value (room temperature,  $T_0$ ) at the top electrode contact. In order to evaluate the temperature profile inside the PCM cell, a 3D electro-thermal model of the cell was developed [71]. The simulated temperature along the  $z$ -axis of the simplified cell geometry in Fig. 3.1(a) is shown in Fig. 3.1(b). The temperature profile inside the GST decreases almost linearly with the distance from the GST-heater interface, since the heat flow from the heater to the TEC is substantially parallel to the  $z$ -axis, as will be shown in the following.

Therefore, the simple linear model depicted in Fig. 3.2 was used to calculate the distance  $z_a$  from the heater-GST interface at which the temperature in the GST is equal to the melting point  $T_{melt}$ , thus obtaining

$$z_a = d \frac{(T_{max} - T_{melt})}{T_{max} - T_0} = d \left( 1 - \frac{(T_{melt} - T_0)R_h}{R_{th}V_{cell}^2} \right), \quad (3.2)$$

where  $d$  is the thickness of the GST layer. It is worth noticing that  $z_a$  does not depend linearly neither on  $V_{cell}$  nor on the RESET programming power ( $\frac{V_{cell}^2}{R_h}$ ): indeed, a sub-linear dependence of  $z_a$  upon  $V_{cell}$  is observed due to

the presence of the TEC, so that  $z_a$  asymptotically approaches  $d$  as  $V_{cell}$  approaches infinity.

Let us define  $V_{cell,min}$  as the lowest amplitude of the RESET pulse that, when applied to a PCM cell in the full-SET state, causes a significant increase of the cell resistance (under this condition, the volume of the GST alloy close to the GST-heater interface is heated just above the melting point). The equivalent thermal resistance  $R_{th}$  can be expressed as

$$R_{th} = \frac{(T_{melt} - T_0)R_h}{V_{cell,min}^2} \quad (3.3)$$

and, hence, by substituting Eq. (3.3) in Eq. (3.2), the following expression for  $z_a$  is obtained:

$$z_a = d \cdot \left(1 - \frac{V_{cell,min}^2}{V_{cell}^2}\right) = d \cdot f(V_{cell}), \quad (3.4)$$

where  $f(V_{cell}) = (1 - \frac{V_{cell,min}^2}{V_{cell}^2})$  can be seen as a thickness modulation factor: in fact, the distance  $z_a$  corresponds to the thickness of the amorphous cap obtained after the partial-RESET operation.

Some details about the shape of the amorphous cap are needed to calculate the amorphous cap resistance when the value of  $z_a$  is known. The shape of the obtained amorphous cap is determined by the melting-temperature isotherm obtained inside the GST layer with the used value of  $V_{cell}$ . From the simulated temperature map of Fig. 3.3, which was obtained by means of the above 3D model, it can be noticed that the temperature gradient and, thus, the heat flow just above the heater are roughly parallel to the  $z$ -axis. Then, the width of the amorphous cap along the  $x$ -axis and, for symmetry, also the width of the cap along the  $y$ -axis are much larger than its thickness ( $z$ -axis). As a consequence, the amorphous cap resistance depends approximately linearly on  $z_a$ . By neglecting, to a first order, the contribution of the remaining crystalline alloy to the GST layer resistance (which is much lower than the amorphous cap resistance, provided that  $\rho_A z_a \gg \rho_C d$ ,  $\rho_C$  and

$\rho_A$  being the low-field resistivity of the crystalline and the amorphous GST, respectively), the GST resistance is given by

$$R_{GST} \simeq \rho_A \frac{z_a}{A}, \quad (3.5)$$

where  $A$  is the area of the contact between the heater and the GST layer. By replacing Eq. (3.4) in Eq. (3.5), the following expression is obtained

$$R_{GST} \simeq R_{max} \cdot f(V_{cell}), \quad (3.6)$$

where

$$R_{max} = \frac{\rho_A d}{A} \quad (3.7)$$

is the asymptotic maximum resistance, which is achieved in the case of a fully-amorphous GST layer.

Now, Eq. (3.7) can be used to derive the effects of fabrication process spreads on the RESET process: if a RESET pulse of amplitude  $V_{cell}$  is applied

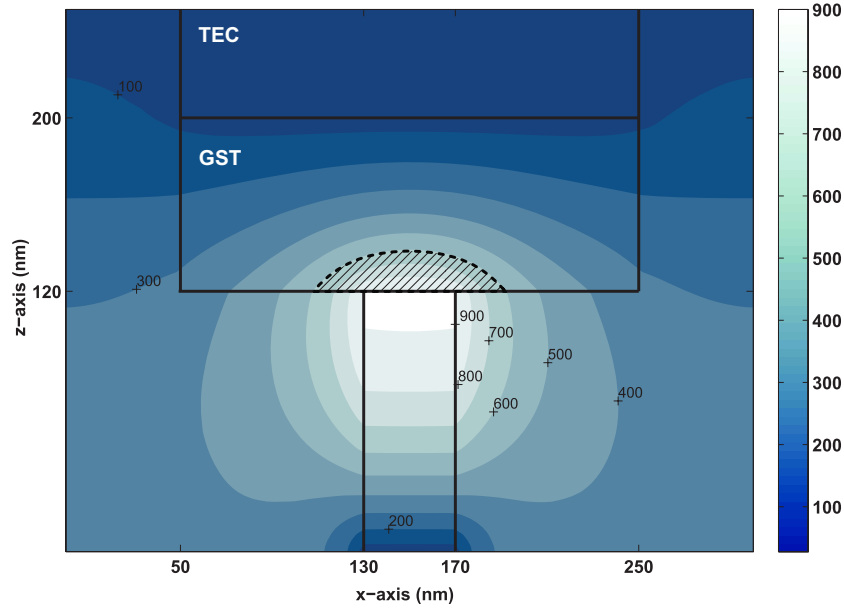


Figure 3.3: Simulated temperature map inside the simplified PCM cell of Fig. 3.1 [71].



to an array of PCM cells, a Gaussian resistance distribution is obtained, as shown in Fig. 3.4. By considering the possible causes of the resistance spread, the standard deviation,  $\sigma_{R_{GST}}$ , of  $R_{GST}$  can be written as

$$\sigma_{R_{GST}} = \mu_{R_{GST}} \sqrt{\left(\frac{\sigma_{R_{max}}}{\mu_{R_{max}}}\right)^2 + \left(\frac{\sigma_f}{\mu_f}\right)^2}, \quad (3.8)$$

where  $\mu_{R_{GST}}$ ,  $\mu_{R_{max}}$ , and  $\mu_f$  are the mean values of  $R_{GST}$ ,  $R_{max}$ , and  $f(V_{cell})$ , respectively, whereas  $\sigma_{R_{max}}$  and  $\sigma_f$  are the standard deviations of  $R_{max}$  and  $f(V_{cell})$ , respectively.

It is worth noticing, from Eq. (3.7), that  $R_{max}$  and, thus,  $\sigma_{R_{max}}$  are independent of the amplitude of the applied RESET pulse. The contribution of  $\sigma_{R_{max}}$  to the spread of  $R_{GST}$  for the considered process can be estimated to be in the order of few hundredths. As will be seen in the following, this contribution is small as compared to the spread introduced by the modulation factor  $f$  and, hence, it will be neglected in the following analysis. The sum of the contributions of the remaining process spreads can be modeled by using

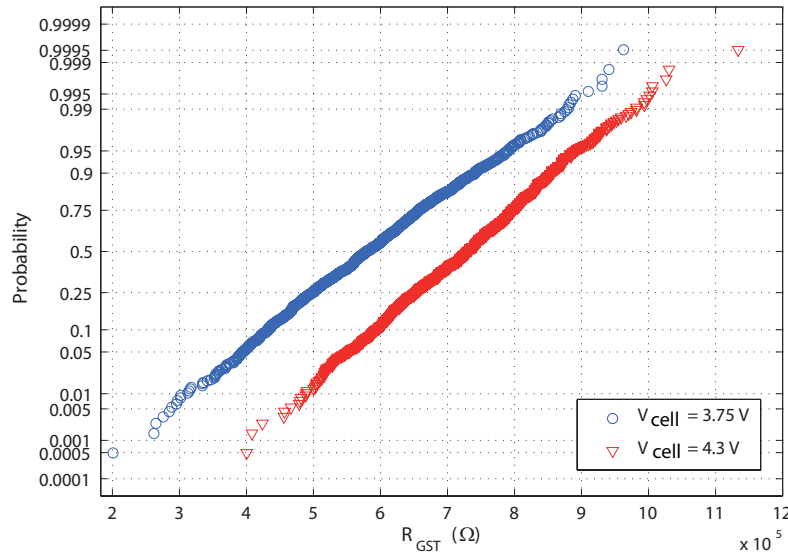


Figure 3.4: Normal probability plots of the measured  $R_{GST}$  obtained with two different values of  $V_{cell}$ .

an equivalent normally distributed random variable which, in this case, is  $V_{cell,min}$ . Then, by some hand calculations, the mean value and standard deviation of  $R_{GST}$  can be written as

$$\mu_{R_{GST}} \simeq \mu_{R_{max}} \left( 1 - \frac{\mu_{V_{cell,min}}^2}{V_{cell}^2} \right), \quad (3.9)$$

$$\sigma_{R_{GST}} \simeq \mu_{R_{GST}} \frac{\sigma_f}{\mu_f} \simeq \mu_{R_{max}} \frac{2\sigma_{V_{cell,min}}\mu_{V_{cell,min}}}{V_{cell}^2}, \quad (3.10)$$

where  $\mu_{V_{cell,min}}$  and  $\sigma_{V_{cell,min}}$  are the mean value and the standard deviation, respectively, of  $V_{cell,min}$ . The relative standard deviation  $e_{R_{GST}}$  is given by

$$e_{R_{GST}} = \frac{\sigma_{R_{GST}}}{\mu_{R_{GST}}} \approx \frac{2\sigma_{V_{cell,min}}\mu_{V_{cell,min}}}{V_{cell}^2 - \mu_{V_{cell,min}}^2}. \quad (3.11)$$

From Eq. (3.11), the larger the amplitude of the RESET pulse across the cell ( $V_{cell}$ ), the lower the relative standard deviation of the obtained resistance. In particular, when considering two RESET pulses with different amplitudes  $V_{cell,1}$  and  $V_{cell,2}$ , the corresponding relative deviations  $e_{R_{GST,1}}$  and  $e_{R_{GST,2}}$  are related as follows:

$$\frac{e_{R_{GST,1}}}{e_{R_{GST,2}}} = \frac{V_{cell,2}^2 - \mu_{V_{cell,min}}^2}{V_{cell,1}^2 - \mu_{V_{cell,min}}^2}. \quad (3.12)$$

### 3.1.1 Experimental validation

The experimental validation of the above model for the partial-RESET operation was carried out on a sub-array of 1024 memory cells in the PCM chip fabricated in 180-nm CMOS technology [35]. First, the value of the equivalent thermal resistance  $R_{th}$  of the PCM cell was estimated. To this end, the cells of the array were first programmed to the full-SET state, then the distribution of  $V_{cell,min}$  over the array was determined and, finally,  $R_{th}$  was calculated by means of Eq. (3.3). From these measurements, the mean value of  $V_{cell,min}$  turned out to be approximately equal to 2.8 V ( $t_{pulse} = 100$  ns).

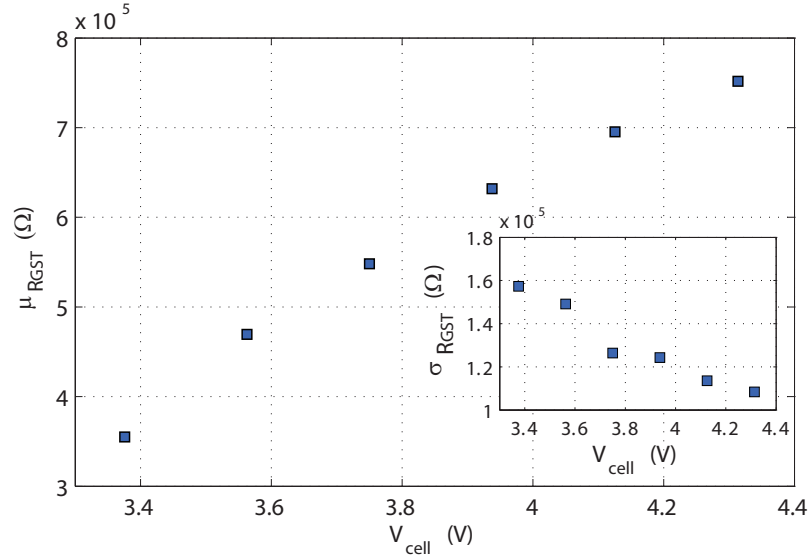


Figure 3.5: Mean value of the measured cell resistance after the RESET operation,  $\mu_{RGST}$ , as a function of the RESET pulse amplitude  $V_{cell}$ . The standard deviation of the resistance distribution,  $\sigma_{RGST}$ , is shown in the inset.

Since,  $R_h \simeq 5 \text{ k}\Omega$ ,  $T_{melt} = 600 \text{ }^\circ\text{C}$ , and  $T_0 = 20 \text{ }^\circ\text{C}$ , the equivalent thermal resistance  $R_{th}$  was calculated to be about  $360 \text{ k}^\circ\text{C/W}$ .

Next, the considered sub-array was programmed to the full-SET state, then a single RESET pulse ( $t_{pulse} = 100 \text{ ns}$ ) was applied to every cell and the obtained GST resistance was measured. The above measurements were repeated with different amplitudes of the RESET pulse across the cell in the range from about 3.4 V to 4.3 V, any amplitude value being used for all the considered cells after the re-initializing full-SET pulse. The experimental data obtained with the highest RESET pulse amplitude were used to calculate, from Eqs. (3.6), (3.7), and (3.10), the standard deviation of  $V_{cell,min}$  and the resistivity value of the amorphous GST,  $\rho_A$ , which turned out to be approximately 0.28 V and  $26 \text{ m}\Omega\text{m}$ , respectively. Then, these values were used in Eqs. (3.9) and (3.10) for every value of  $V_{cell}$  belonging to the considered range to predict the corresponding values of  $\mu_{RGST}$  and  $\sigma_{RGST}$ .

The mean value of the measured GST resistance as a function of  $V_{cell}$  is plotted in Fig. 3.5. It increases with the amplitude of the applied RESET

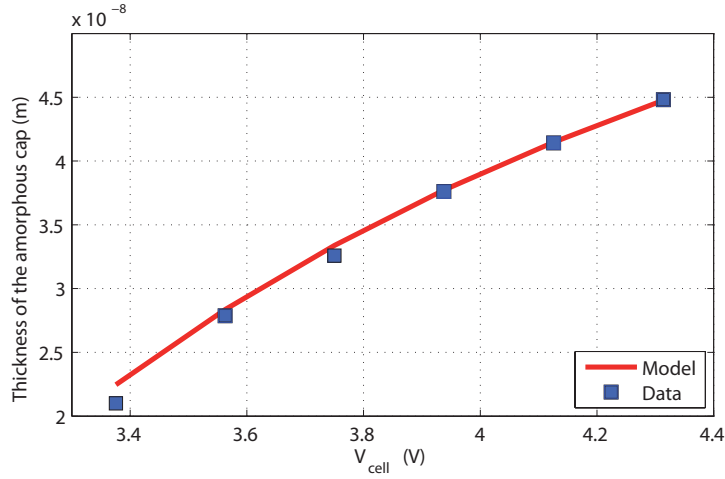


Figure 3.6: Experimental and predicted values of the amorphous cap thickness as a function of the RESET pulse amplitude.

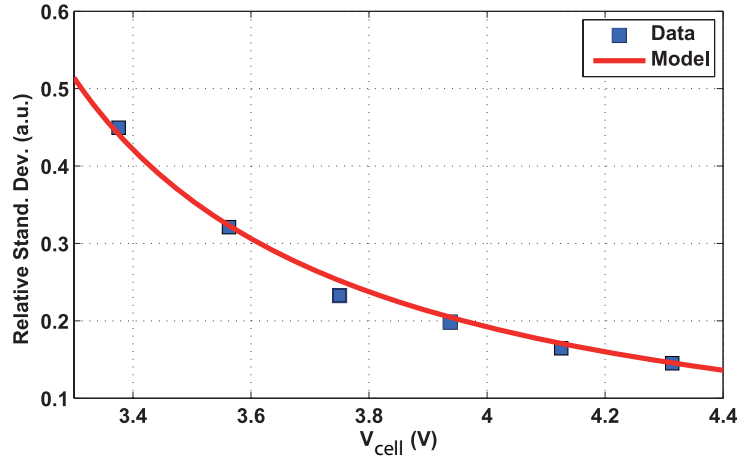


Figure 3.7: Experimental and predicted values of the relative standard deviation of  $R_{GST}$  as a function of  $V_{\text{cell}}$ .

pulse, since a higher portion of the GST alloy is melted and then amorphized, thus leading to an increase in the thickness of the amorphous cap. It can be noticed from the inset in Fig. 3.5 that the standard deviation of the GST resistance distribution decreases as the amplitude of the RESET pulse increases, as expected from Eq. (3.10). In particular, the standard deviation

of  $R_{GST}$  for the minimum considered  $V_{cell}$  is about 50% higher than that obtained with the highest value of  $V_{cell}$ .

Then, the values of  $z_a$  predicted by Eq. (3.4) for the considered range of  $V_{cell}$  were compared to the thickness of the amorphous cap calculated from measured data by means of Eq. (3.5). From Fig. 3.6, a good agreement between data and model is apparent. The highest value of the amorphous cap thickness obtained with the considered values of  $V_{cell}$  is 45 nm, which is slightly higher than half the GST layer thickness.

Finally, for each considered partial-RESET pulse amplitude, the normalized standard deviation of  $R_{GST}$  calculated from experimental data and  $e_{R_{GST}}$  as given by Eq. (3.11) were compared. As shown in Fig. 3.7, very good agreement is observed also in this case.

## 3.2 Dynamic effects in partial-RESET programming

---

In this Section, the previously described analytical model is extended to the dynamical case by including the effects of different time durations of the partial-RESET pulses.

To investigate the dynamic effect in partial-RESET programming, the single-pulse (SP) programming curve of a single memory cell was measured by considering different pulse durations.

To this end, the sequence of program and read pulse depicted in Fig. 3.8 was used. First, the memory cell was programmed to the full-SET state by means of a staircase-down (SCD) initializing sequence and, then, a single partial-RESET voltage pulse having predetermined values of amplitude ( $V_{RST}$ ) and duration ( $t_{pulse}$ ) was applied. Readout was performed after each partial-RESET pulse ( $V_{read} = 700mV$ ). In Fig. 3.9,  $V_{cell}$  is the programming voltage across the PCM cell ( $V_{cell} = V_{RST} - V_{GS,Y_0}$ , where  $V_{GS,Y_0}$  is the gate-to-source voltage of  $Y_0$ ). The above sequence was repeated with different values of  $V_{RST}$  and  $t_{pulse}$ , thus obtaining the programming curves in Fig. 3.9. A significant dependence of the obtained cell resistance over the pulse duration is observed. In particular, the slope of the programming curves increases with the pulse duration. The overall RESET dynamics is apparent

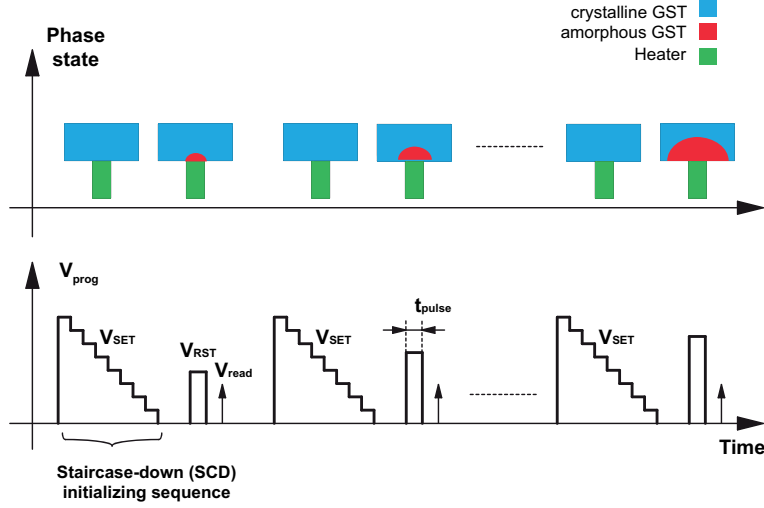


Figure 3.8: Sequence of program and read pulses used in single-pulse (SP) partial-RESET programming of PCM cells.

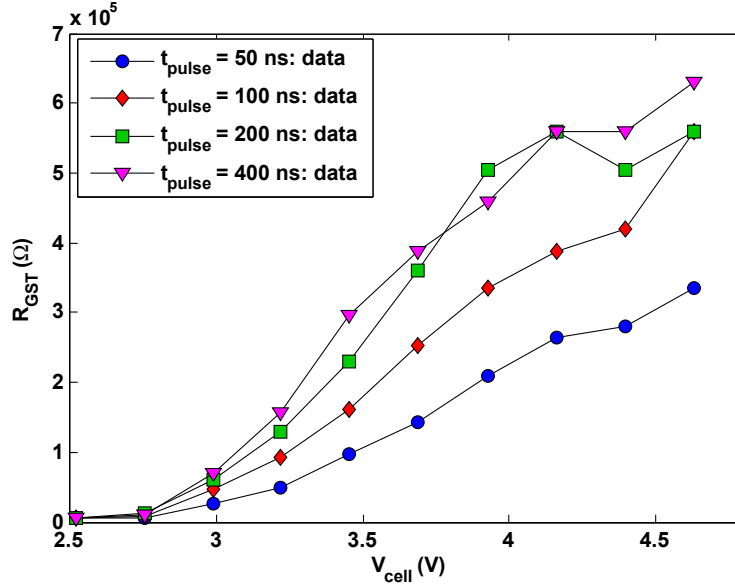


Figure 3.9: Experimental single-pulse programming curves obtained by means of the procedure shown in Fig. 3.8.

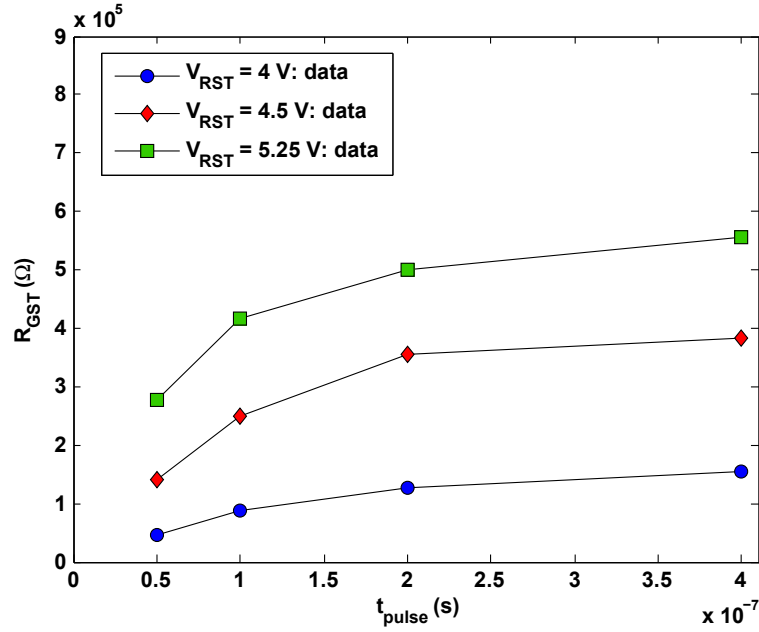


Figure 3.10: Measurements of the RESET process dynamics in single-pulse partial-RESET programming.

in Fig. 3.10, where the GST resistance obtained with the SP programming procedure for different values of  $V_{\text{RST}}$  is plotted against the pulse duration.

As highlighted in Fig. 3.11(a), the minimum programming voltage ( $V_{\text{cell,min}}$ ) required to appreciably increase the cell resistance decreases with increasing pulse duration. This difference is more evident when considering low values of  $t_{\text{pulse}}$  (50 ns and 100 ns).

In order to reproduce this effect, the temperature dynamics inside the GST layer was included in the model. To this end, it was assumed to a first approximation that the temperature dynamics inside the GST layer is independent from the distance from the heater-GST contact (this approximation is supported by finite-element simulations of the memory cell [71]). The transient temperature  $T(t)$  at the heater-GST interface is modeled, to a first order approximation, by an exponential function:

$$T(t) = (T_{\text{max}} - T_0) \cdot \left(1 - e^{-\frac{t}{\tau_T}}\right) + T_0, \quad (3.13)$$

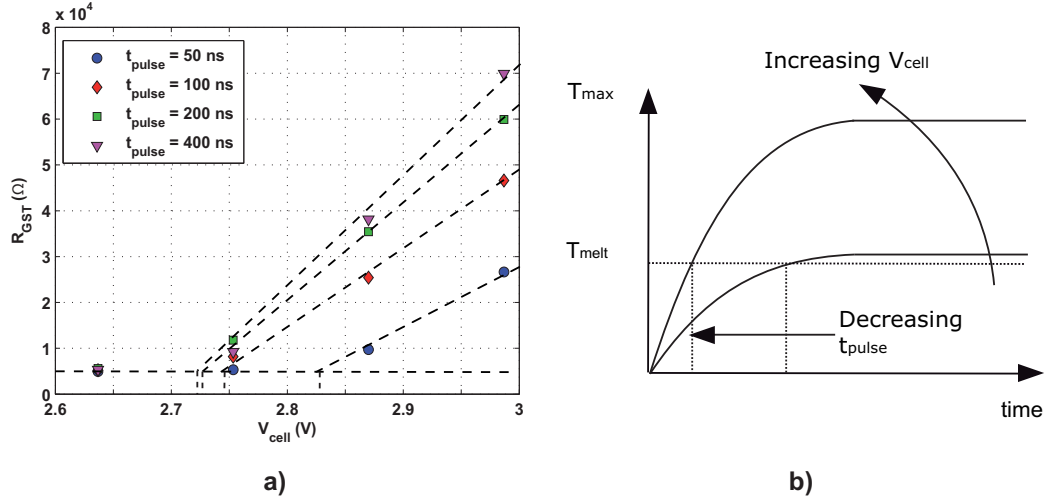


Figure 3.11: Detail of the SP programming curves showing the dependence of  $V_{cell,min}$  upon the pulse duration (a); schematic picture of the effect of the temperature dynamics on amorphization (b).

where  $\tau_T$  is the time constant for the temperature dynamics inside the GST layer. The time constant  $\tau_T$  takes the effects of both the purely electrical and the purely thermal dynamics into account. Since

$$T_{max} = \frac{R_{th} \cdot V_{cell}^2}{R_h} + T_0, \quad (3.14)$$

Equation (3.13) can be written as

$$T(t) = \frac{R_{th} \cdot V_{cell}^2}{R_h} \cdot (1 - e^{-\frac{t}{\tau_T}}) + T_0. \quad (3.15)$$

Then, Eqs. (3.4) and (3.5) can still be used to calculate the GST resistance as a function of time, provided that  $T_{max}$  is substituted by  $T(t)$  of Eq. 3.15. As schematically shown in Fig. 3.11(b), the effects of temperature dynamics are more evident when low-amplitude partial-RESET pulses are applied to the cell. The temperature dynamics inside the GST layer calls for a trade-off between pulse amplitude and pulse duration in partial-RESET



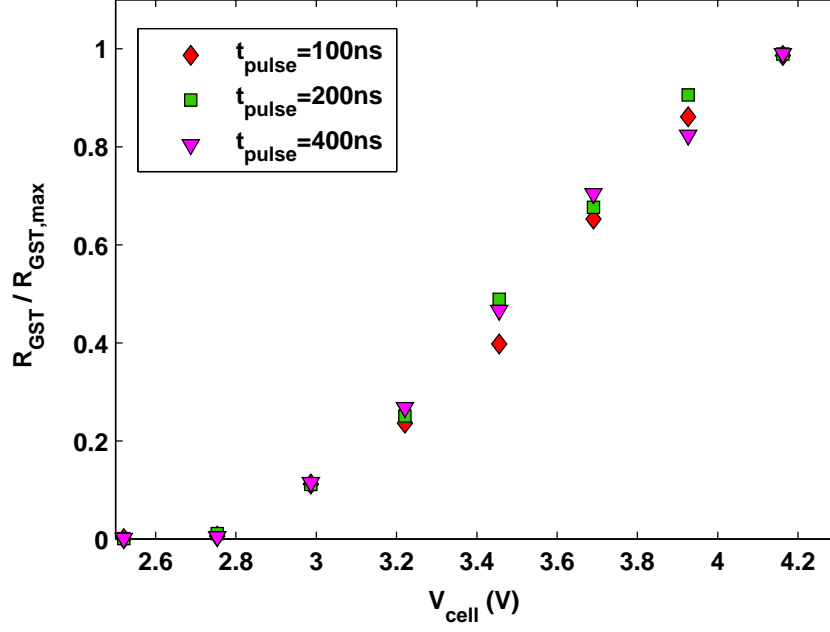


Figure 3.12: Single-pulse programming curves obtained by means of the programming procedure shown in Fig. 3.8. The GST resistance in each curve is normalized with respect to the corresponding resistance value obtained with  $V_{\text{cell}} \simeq 4.2\text{ V}$ .

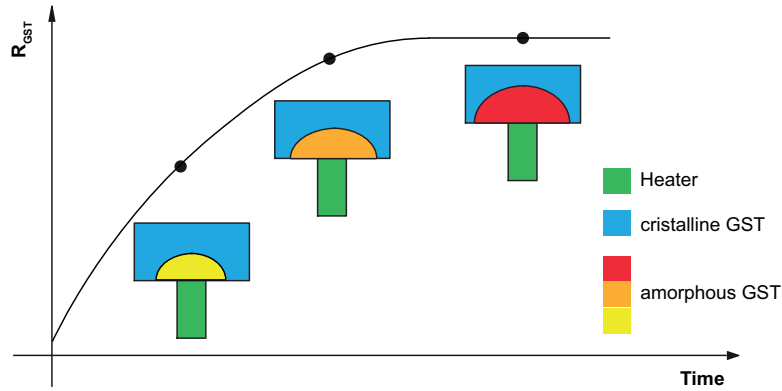


Figure 3.13: Modeling of the effect of the partial-RESET pulse duration on the amorphous cap thickness and the amorphous GST resistivity.

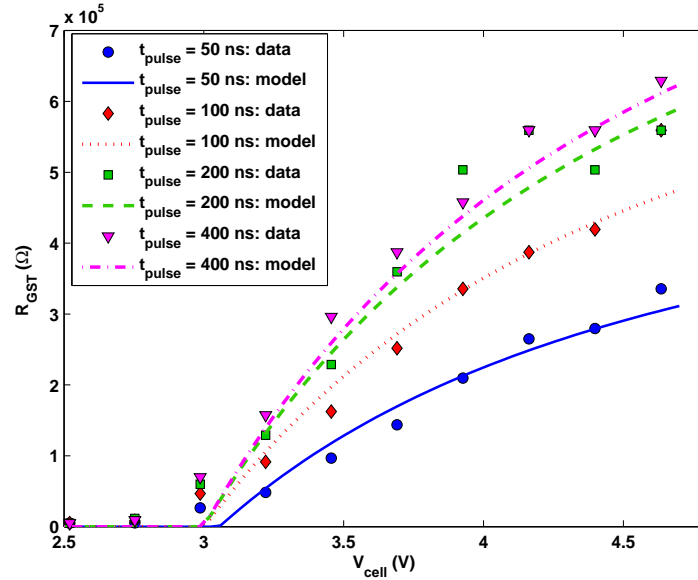


Figure 3.14: Single-pulse partial-RESET programming curves obtained by means of the procedure shown in Fig. 3.8: experimental data (dots) and model (lines).

programming, since a lower voltage is needed to reach the melting temperature when the pulse duration is high, as shown in Fig. 3.11(b). The effects of temperature dynamics become negligible when  $t_{pulse} \gg \tau_T$  ( $\tau_T$  was estimated to be about a dozen nanoseconds by electro-thermal simulations of the PCM cell).

However, from the observed RESET dynamics in Fig. 3.10, transient effects are non negligible also for long  $t_{pulse}$  values. In order to investigate the presence of further resistance dynamics mechanisms, the SP programming curves obtained with relatively long pulses (so as to make temperature dynamics negligible) were normalized with respect to the corresponding resistance value obtained with  $V_{cell} \simeq 4.2$  V. As shown in Fig. 3.12, the obtained curves are substantially superimposed (only the curves with negligible difference in  $V_{RST,min}$  are shown), meaning that they differ by only a scaling factor which is proportional to the GST resistance.

Since the GST resistance is approximately proportional to the amorphous GST resistivity, this phenomenon was modeled as a dynamical effect associ-

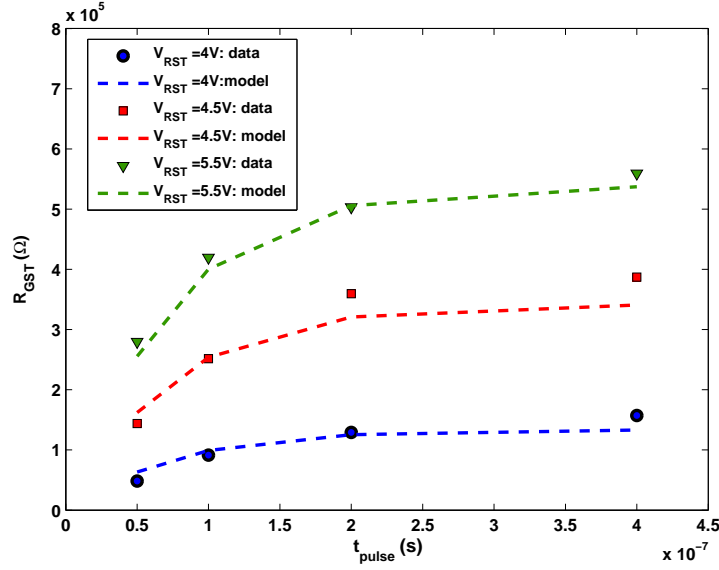


Figure 3.15: RESET process dynamics in single-pulse partial-RESET programming: experimental data (dots) and model (dashed lines).

ated to the amorphous GST resistivity, which was modified as follows

$$\rho_{A,eff}(t) = (\rho_A - \rho_C) \cdot (1 - e^{-\frac{t}{\tau_A}}) + \rho_C, \quad (3.16)$$

where  $\rho_{A,eff}$  is the effective resistivity of the programmed amorphous GST,  $\rho_A$  is the resistivity of the fully-amorphous GST,  $\rho_C$  is the resistivity of GST in the crystalline form, and  $\tau_A$  is the time constant for the amorphization process that was fit from SP experimental data. Figure 3.13 schematically depicts the two dynamics mechanisms in partial-RESET programming, namely the fast temperature dynamics that determines an increase of the amorphous cap thickness and the observed slow dynamics that was modeled as the increase of the effective amorphous resistivity  $\rho_{A,eff}$  with time.

Then, Eq. (3.6) can be extended to the dynamic case by means of Eqs. (3.15) and (3.16), as follows:

$$R_{GST} = \frac{\rho_{A,eff}(t) \cdot d}{A} \left( 1 - \frac{T_{melt} - T_0}{T(t) - T_0} \right). \quad (3.17)$$

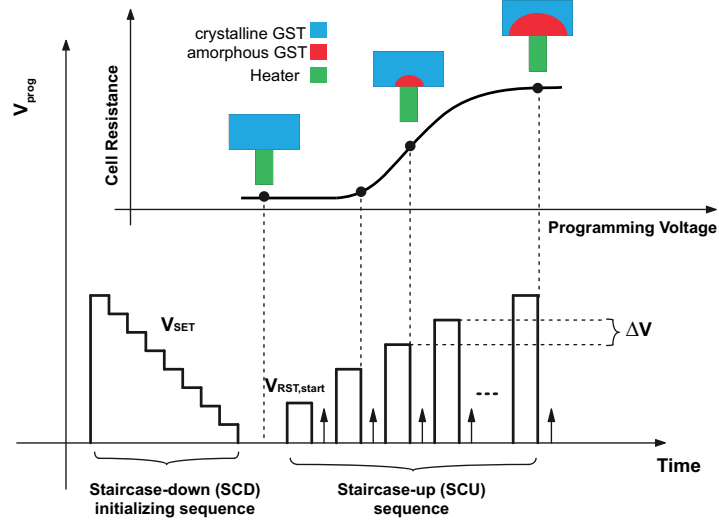


Figure 3.16: Sequence of program and read pulses used in SCU partial-RESET programming of PCM cells.

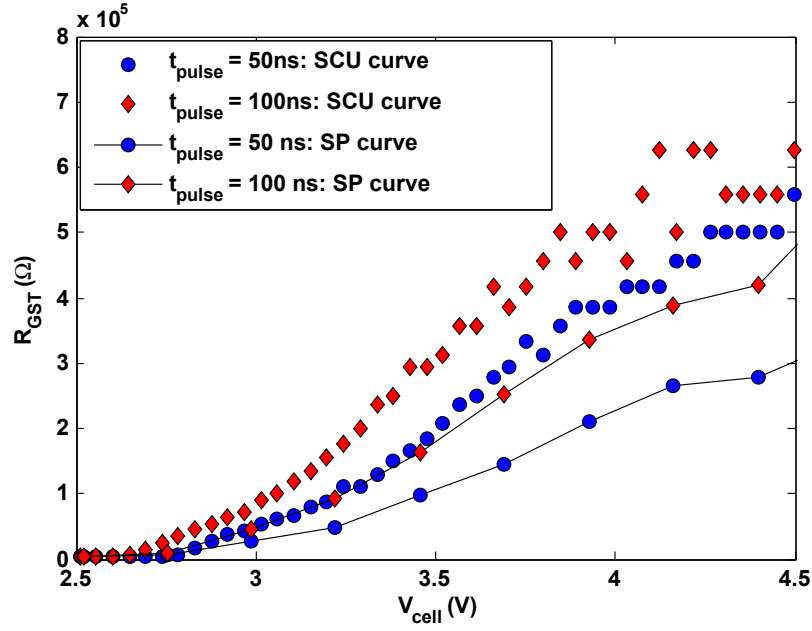


Figure 3.17: SCU programming curves obtained by means of the procedure shown in Fig. 3.16 compared to the corresponding SP programming curves.

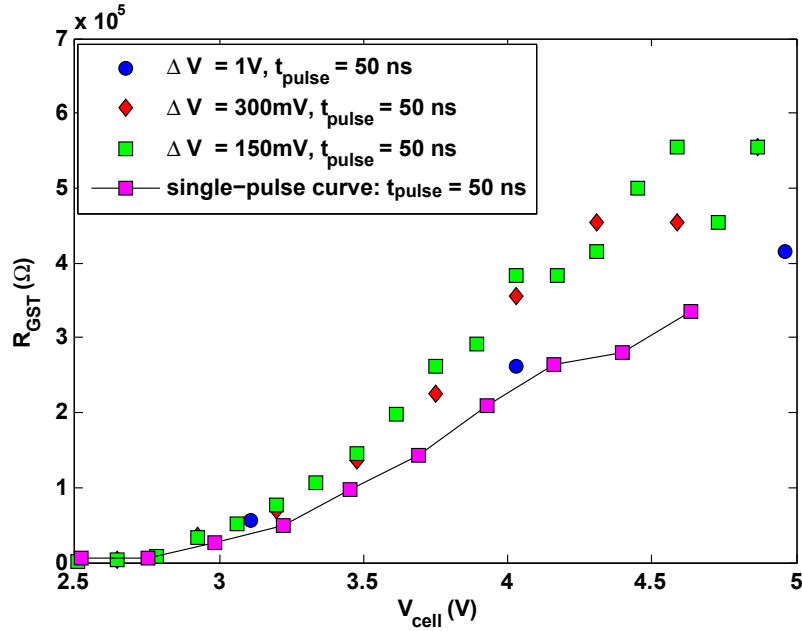


Figure 3.18: SCU programming curves obtained with different values of  $\Delta V$  and  $t_{\text{pulse}} = 50 \text{ ns}$  compared to the SP curve obtained with the same pulse duration.

### 3.2.1 Experimental validation

The values of the parameters used in simulations are summarized in Table 3.1. The proposed model is able to well reproduce the experimental SP programming curves for different values of  $t_{\text{pulse}}$  and the RESET dynamics as shown in Figs. 3.14 and 3.15.

The above described dynamic model was also validated by means of additional measurements on the same PCM cell. In particular, the partial-RESET staircase-up (SCU) programming sequence shown in Fig. 3.16 was

Table 3.1: Simulation parameters

Parameter	Value	Parameter	Value
$\rho_A$	20 $m\Omega \cdot m$	$\rho_C$	0.1 $m\Omega \cdot m$
$\tau_A$	70 ns	$\tau_T$	15 ns
$R_h$	5 k $\Omega$	$R_{th}$	320 k $^{\circ}C/W$

considered. In SCU programming, as explained in Chapter 2, the cell is first brought to the SET state by means of a staircase-down (SCD) initializing sequence and, then, a staircase-up sequence of voltage pulses, each followed by a read pulse, is applied. The SCU curves obtained with different values of  $t_{pulse}$  (the voltage increment  $\Delta V$  between two adjacent programming pulses was set to 25 mV) are shown in Fig. 3.17. The SCU programming curves are steeper than the corresponding (i.e., obtained with the same pulse duration) SP curves, due to the fact that in SCU programming each partial-RESET pulse is applied to a partially amorphized cell. This behavior is also evident when the voltage step  $\Delta V$  between adjacent pulses is increased, as shown in Fig. 3.18.

The developed dynamic model was used to simulate the SCU programming curve. To this end, the resistivity of the amorphous chalcogenide at the beginning of the  $(i+1)$ -th pulse was calculated as the resistivity of the amorphous chalcogenide at the end of the  $i$ -th pulse ( $\rho_{A,1} = \rho_C$ ), as follows:

$$\rho_{A,i+1}(t) = (\rho_A - \rho_{A,i})(1 - e^{-\frac{t}{\tau_A}}) + \rho_{A,i}. \quad (3.18)$$

Furthermore, the temperature transient,  $T(t)$ , was calculated assuming room temperature at the beginning of each pulse. The dynamic model was able to well reproduce the SCU curves obtained with different values of  $t_{pulse}$ , as shown in Fig. 3.19. The slight disagreement between model and data that can be noticed for low-voltage RESET pulses is ascribed to the effects of self-heating inside the GST layer. Although self-heating is not implemented in the model, it may be taken into account by adding its contribution to the temperature  $T_{max}$ .

As depicted in Fig. 3.20, a good agreement between model and data is also apparent in the case of SCU programming curves obtained with different values of  $\Delta V$ , ranging from 150 mV to 1 V. In particular, the model adequately reproduces the dependence of the slope of the SCU programming curves on the value of  $\Delta V$ , demonstrating good prediction capabilities.

The model may be fruitfully employed to choose programming parameters in order to optimize partial-RESET algorithms for multilevel storage.

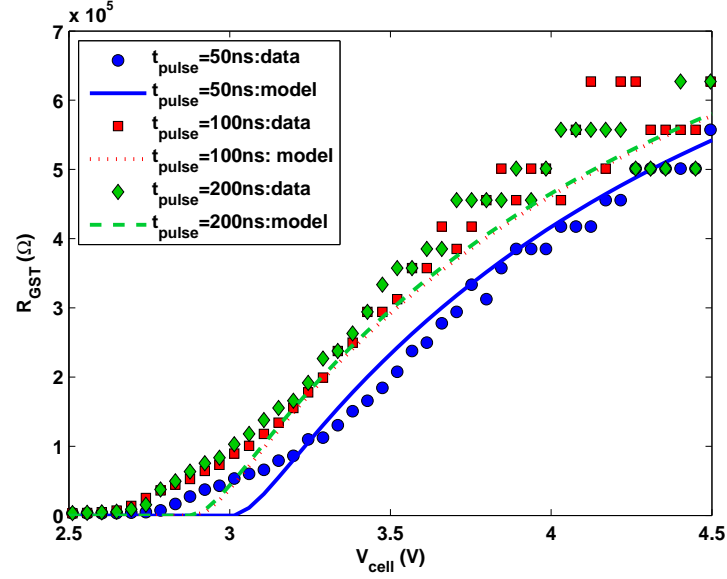


Figure 3.19: SCU programming curve obtained by means of the procedure shown in Fig. 3.16: experimental data (dots) and model in Eq. (3.17) (dashed lines).

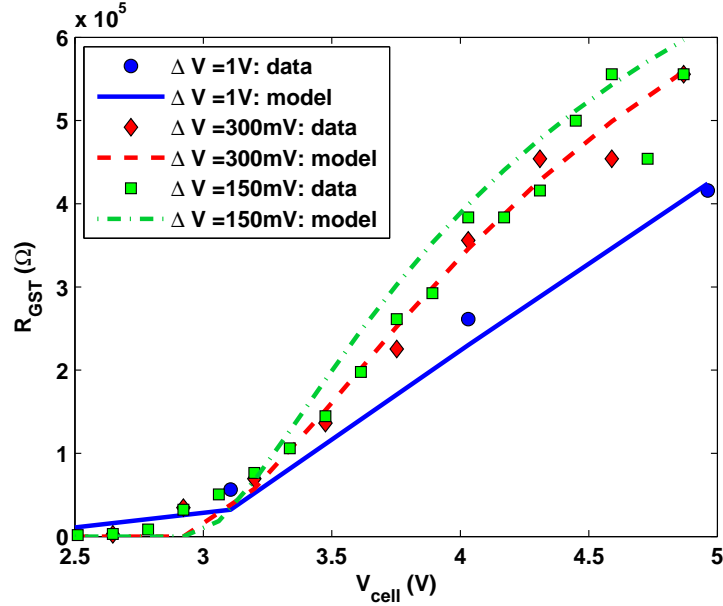


Figure 3.20: SCU programming curves obtained with different values of  $\Delta V$  and  $t_{pulse} = 50\text{ ns}$ : experimental data (dots) and model in Eq. (3.17) (lines).

# 4

## Programmed resistance stability

Multi-level programming in Phase Change Memories (PCMs) requires adequate understanding of the phenomena which affect the stability of the programmed resistance levels.

The programmed resistance changes with time due to two physical phenomena: the crystallization of the amorphous GST [72, 73] and the drift of the amorphous GST resistivity [57, 58], which decreases and increases, respectively, the cell resistance. In multi-level storage, where the cell may be programmed to any among  $n > 2$  different resistance levels, both the above phenomena affect data retention since they may cause problems in distinguishing two adjacent resistance levels of a PCM cell. As pointed out in Chapter 2, multilevel states can be programmed in two main ways: partial-RESET and partial-SET programming.

For the considered  $\mu$ trench architecture [51], the partial-RESET programming approach gives substantially rise to a series-type phase configuration, where the two phases (the amorphous and the crystalline one) are placed in series with respect to the current flow, the amorphous phase forming a cap above the heater. In this case, the chalcogenide resistance basically depends on the thickness of the amorphous cap [74]. On the other hand, partial-SET programming gives rise to the formation of a conductive path inside the amorphous cap [75]. The drift phenomenon is generally ascribed to the amorphous chalcogenide material and, thus, it is influenced by the distribution of the amorphous phase inside the active region. In this Chapter, the drift of a full-SET state is also measured, showing that a very slow drift dynamics is present in the polycrystalline phase obtained by means of electrical pulses.



The crystallization process depends on the thermal history of the amorphous chalcogenide, and may thus be affected by programming conditions.

In this Chapter, an experimental analysis of the intermediate resistance stability is carried out on a statistical population of cells so as to attenuate the effects of the intrinsic resistance noise and fabrication process spreads. First, the drift dynamics on an array of PCM cells programmed to different intermediate resistance states by means of a partial-RESET and a partial-SET programming procedure [49] is analyzed. Then, the stability of partial-SET states obtained by means of single-pulse programming is investigated considering the impact of the characteristics of the applied pulse (i.e., duration and amplitude).

## 4.1 Low-field resistance drift

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Low-field resistance drift has been ascribed to different phenomenon comprising mechanical relaxation effects [57, 76] and trap density evolution over time [77, 78], or a combination of them. The drift phenomenon is not a problem for data retention in bilevel storage, where it contributes to increase the resistance difference between the full-SET and the full-RESET states, thus improving the read margins.

On the other hand, drift is a key issue for data retention in multilevel storage. In fact, it causes a shift and a broadening of the programmed resistance distributions, thus posing severe constraints on the accuracy of readout circuitry and on the maximum storing capacity or, equivalently, on the maximum number of intermediate levels that can be allocated inside the available window. To improve reliability, some drift compensation or cancelation techniques have been proposed in the literature [52, 59, 60]. Moreover, level spacing can be optimized to ensure an adequate distance between adjacent distributions [79].

### 4.1.1 Partial-RESET states

The experimental analysis was carried out on a statistical population of cells (1K-cell sub-array), in order to attenuate the effects of the unavoidable resistance noise and the technological spreads that heavily affect measurements.

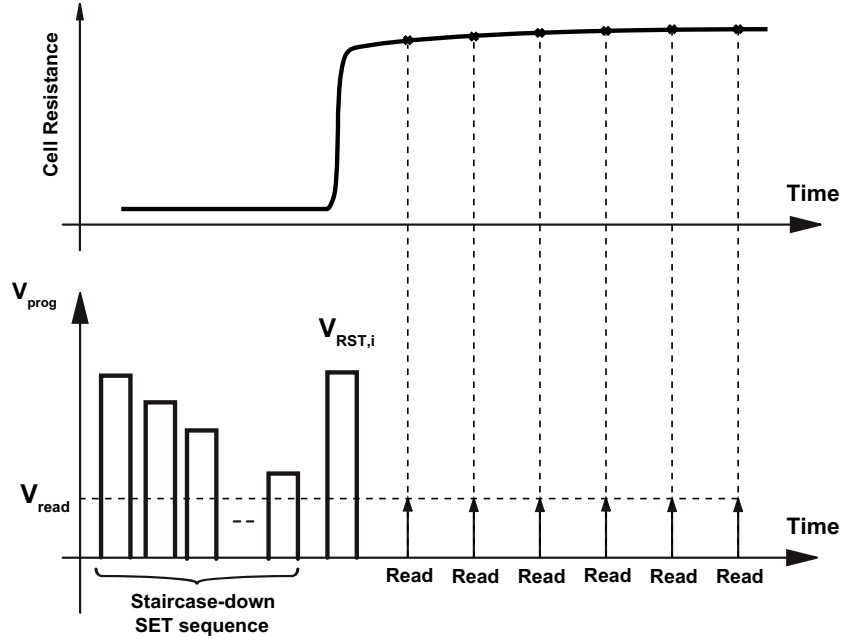


Figure 4.1: Programming sequence used to characterize the GST resistance as a function of the applied partial-RESET voltage.

Each cell of the sub-array was programmed into its minimum resistance state through a full-SET operation (see Fig. 4.15) and, then, a single partial-RESET pulse with a duration of 100 ns and amplitude  $V_{RST,1}$  was applied. After this programming pulse, the resistance of each cell was measured by properly biasing the gate of the MOS transistor  $Y_0$  with a stable read voltage ( $V_{read} = 700$  mV) and by sensing the current flowing through the PCM cells.

The read operation was repeated at fixed time steps for the required measurement time interval (about 30 minutes). Once the drift dynamics was obtained for the programming pulse of amplitude  $V_{RST,1}$ , the sub-array underwent a further full-SET operation and, then, was programmed with a partial-RESET voltage pulse of amplitude  $V_{RST,2} = V_{RST,1} + \Delta V$ ,  $\Delta V$  being a suitable increase of the programming voltage. The voltage applied to the word-line is such that the ON resistance of the MOS transistor  $M_{SEL}$  is negligible when compared to the heater resistance. The procedure continued until the whole available resistance window was measured. By applying the

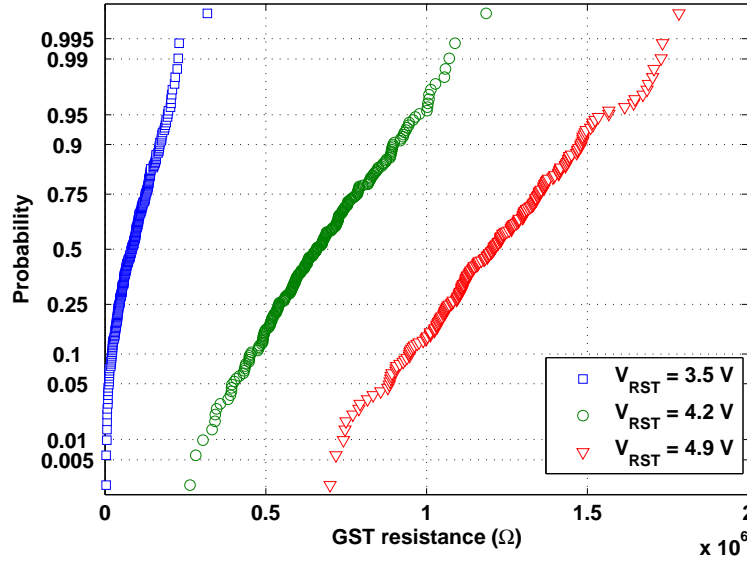


Figure 4.2: Gaussian distribution curves of the GST resistance obtained after applying RESET pulses having different amplitudes to cells initially programmed in a full-SET state. The high variability is essentially due to the spread of the cell parameters over the considered array.

above sequence, a wide resistance window ranging from few  $k\Omega$  to about  $2 M\Omega$  was obtained.

In the following, the measured GST resistance  $R_{GST}$ , obtained by subtracting the heater contribution from the measured cell resistance  $R_{cell}$ , is considered. For the sake of clarity, the obtained distribution for three different values of  $V_{RST}$  are shown in Fig. 4.2. It can be noticed that a given value of resistance can be obtained with different pulse amplitudes due to the spread of memory device parameters over the array.

In partial-RESET programming, a series-type configuration is obtained inside the GST layer for the considered cell architecture. Hence, the GST resistance essentially depends on the thickness of the amorphous cap above the heater. In order to analyze the dependence of the drift dynamics on the initial low-field resistance  $R_{GST}$ , the resistance window was split into 12 bins and a classification of the collected data was performed by grouping together

the cells having initial resistance belonging to the same bin. Then, the mean drift dynamics was calculated for each cluster of PCM cells. Every measure was performed at room temperature. The obtained results are in agreement with the well known power-law dependence of the low-field amorphous-state resistance over time [57, 58]:

$$\frac{R_{GST}(t)}{R_0} = \left( \frac{t}{t_0} \right)^\nu, \quad (4.1)$$

where  $R_0$  is a reference GST resistance,  $t_0$  is a normalizing constant, and  $\nu$  is referred to as the drift dynamics exponent. The main contribution to the resistance drift is ascribed to an increase of the amorphous-GST resistivity  $\rho_A$  which has, therefore, the same power dependence upon time as given by Eq. (4.1).

The mean drift exponent  $\nu$  calculated for each initial resistance bin strongly depends on the initial resistance of the cells (i.e., the resistance of the first measurement), as shown in Fig. 4.4. A comparison of the drift dynamics of two cells programmed to two RESET states having initial resistance different by an order of magnitude is shown in Fig. 4.3. The drift exponent ranges from less than 0.01 to about 0.07, the minimum value being achieved with a GST resistance slightly higher than that of the fully crystalline GST layer. In particular, when considering two different resistance levels  $R_{GST,1}$  and  $R_{GST,2}$ , the following relation is obtained

$$\nu_1 = \nu_2 \cdot \ln \left( \frac{R_{GST,2}}{R_{GST,1}} \right). \quad (4.2)$$

The drift exponent increases logarithmically with the low-field GST resistance up to a saturation value (about 0.07), which is reached for a GST resistance of about 300  $k\Omega$ . From then on, a further increase of the GST resistance does not significantly affect the value of  $\nu$ .

By neglecting, to a first order, the effects of the irregular shape of the amorphous cap, the resistance of the GST for the considered cell architecture can be considered linearly dependent on the thickness of the amorphous cap that is obtained after the partial-RESET operation. This cap experiences a compression due to the presence of the surrounding crystalline chalcogenide.

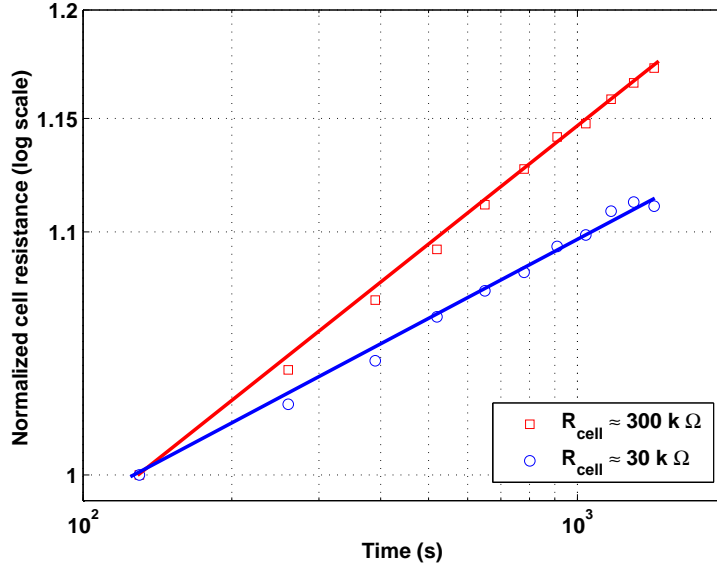


Figure 4.3: Comparison of the drift dynamics of two clusters of PCM cells having a different initial mean resistance. The mean resistance of each cluster is normalized with respect to the mean resistance of the first measurement.

In addition, the density of the amorphous phase,  $\delta_A$ , is lower than the density of the crystalline phase,  $\delta_C$ . This difference is about 6.8% for GST [80]. The stress originated inside the GST layer due to the partial-RESET operation, is redistributed between the crystalline and the amorphous GST so as to minimize the mechanical energy of the system. Although an accurate estimation of the residual stress on the amorphous GST is a difficult task due to the complex shape of the structure, a rough estimate can be obtained by considering a monodimensional model of the GST layer, and assuming that the thickness of the GST layer is independent of stress conditions. This approximation is supported by the fact that the GST layer is surrounded by rigid materials such as *TiN* and *W* [81]. So, the thicker the amorphous cap, the thinner the remaining crystalline GST. Since the stiffness coefficient of a GST layer is inversely proportional to its thickness, as the thickness of the amorphous GST increases, its stiffness ( $k_A$ ) decreases, whereas the stiffness of the crystalline GST ( $k_C$ ) increases. If  $x_{A0}$  and  $x_{C0}$  are the thickness of

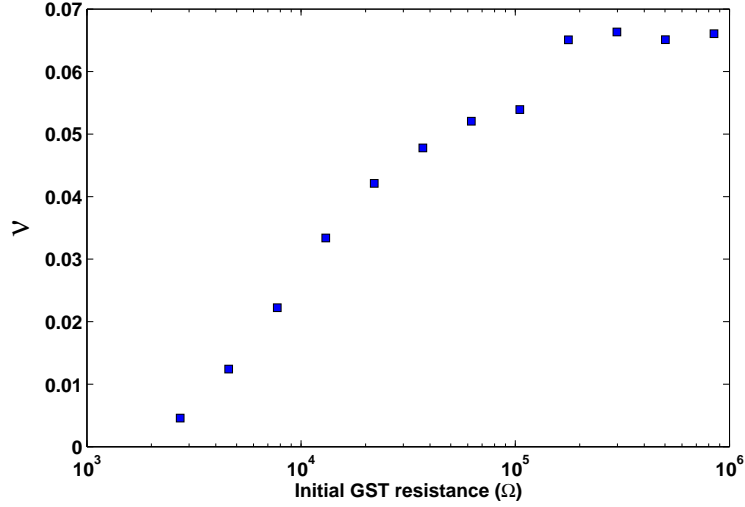


Figure 4.4: Dependence of the exponent  $\nu$  of the low-field amorphous GST resistance drift on the initial GST resistance.

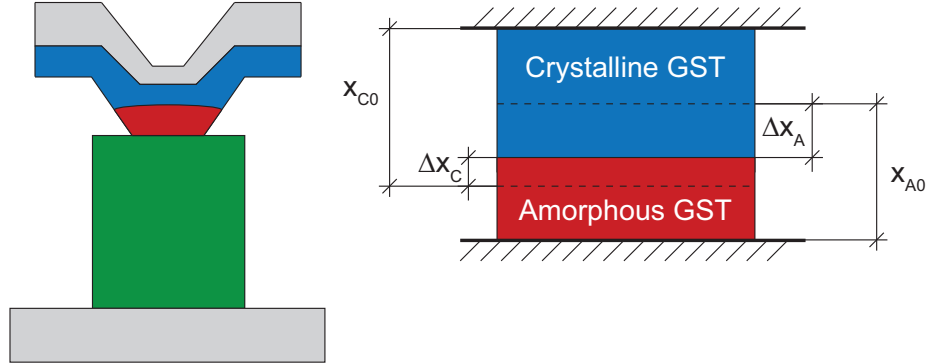


Figure 4.5: Definition of the mechanical variables  $x_{A0}$ ,  $x_{C0}$ ,  $x_{CA}$ ,  $\Delta x_A$  and  $\Delta x_C$  (simplified monodimensional geometry)

the amorphous layer and the crystalline layer, respectively, when no external forces are applied, the stiffness coefficients of the two layers can be expressed as  $k_A = \frac{E_A A}{x_{A0}}$  and  $k_C = \frac{E_C A}{x_{C0}}$ , where  $E_A$  and  $E_C$  are the Young's modulus of amorphous and crystalline GST, and  $A$  is the cross-sectional area of the layers. At equilibrium, holds the following:

$$k_A \Delta x_A = k_C \Delta x_C, \quad (4.3)$$

where  $\Delta x_A$  and  $\Delta x_C$  are the deformations of the amorphous and the crystalline GST, respectively. The sum  $\Delta x_0 = \Delta x_A + \Delta x_C$  is the thickness of the initially crystalline GST which undergoes phase transition, multiplied by the factor  $(\delta_C/\delta_A - 1)$ . In other words,  $\Delta x_0$  is the thickness of the partially amorphous GST layer when no external force is applied. So,  $\Delta x_0$  increases with the degree of amorphization. The strain  $\frac{\Delta x_A}{x_{A0}}$  is proportional to the thickness of the amorphous cap after the RESET operation. Via simple hand calculations, it is possible to obtain:

$$\frac{\Delta x_A}{x_{A0}} = A \cdot \frac{x_{A0}}{x_{A0} - B}, \quad (4.4)$$

where  $A = \frac{E_C}{E_A} \left(1 - \frac{\delta_C}{\delta_A}\right)$  and  $B = \frac{\delta_C}{\delta_A} d$  depend on the thickness of the GST layer, on the Young's modulus, and on the density of amorphous and crystalline GST. Equation (4.4) shows that the pressure inside the amorphous cap increases with the degree of amorphization, which is in agreement with the above measurements. Moreover, when scaling  $x_{A0}$  and  $d$  by the same amount, it turns out that  $\frac{\Delta x_A}{x_{A0}}$  remains unchanged. This was experimentally demonstrated by means of drift measurements carried out on fully-RESET cells having a different chalcogenide layer thickness [57]. In addition, the dependence of drift on hydrostatic pressure has recently been found to be responsible for different drift dynamics in  $Ge_2Te_2Sb_5$  nanowires [82]. From the above considerations, a reduction of resistance drift may be achieved by optimizing the cell geometry and the surrounding materials so as to decrease the hydrostatic pressure inside the amorphized GST.

#### 4.1.2 Partial-SET states

To measure the drift dynamics of partial-SET states, a sub-array consisting of 10K PCM cells was considered. All measurements were performed at room temperature. Following the operating sequence shown in Fig. 4.6b, each cell of the sub-array was first programmed to its minimum-resistance state through a full-SET operation ( $V_{SET,in}$  was chosen so as to avoid history effects on the GST alloy). Then, each cell of the sub-array was programmed to the full-RESET state by means of a 100-ns RESET pulse with an amplitude

$V_{RST} = 4.8 \text{ V}$  (applied to the gate of  $Y_0$ ) and the RESET resistance of each cell was measured. Finally, a single 200-ns voltage partial-SET pulse of amplitude  $V_{SET,i}$  was applied to obtain a partial-SET state. The programming voltage values were chosen so as to widen the obtained resistance window ( $V_{SET,i} = 1.75 \text{ V} + \Delta V \cdot i$ ,  $\Delta V = 0.25 \text{ V}$ ,  $i = 1 \div 4$ ). The used programming pulse amplitudes are higher than the threshold voltage of the cells in the RESET state. Then, the power delivered to the cell roughly depends on the resistance of the cell in switching conditions, which is roughly the same for every cell, regardless of its initial low-field resistance value. After the partial-SET pulse, the resistance of each cell belonging to the sub-array was read by biasing the gate of  $Y_0$  with a stable read voltage ( $V_{G,read} = 700 \text{ mV}$ ) and sensing the current flowing through the PCM cell. The read operation was repeated at predetermined time steps for a time interval of about 30 minutes, like in partial-RESET drift characterization.

In order to investigate the stability of the full-SET state, a conventional staircase-down programming algorithm [53] was applied to each cell of the array, and the read current was measured under the same conditions used for partial-SET drift measurements.

In the following, the low-field resistance of the GST active volume,  $R_{GST}$ , will be considered.  $R_{GST}$  is obtained by subtracting the heater contribution and the estimated resistance of the crystalline phase above the active region from the measured cell resistance.

In order to study the dependence of the drift dynamics on the programmed  $R_{GST}$  (i.e., on the resistance value obtained with the first resistance measurement, which was carried out 130 s after the programming operation due to our experimental setup), the resistance window was split into 12 bins and the cells having initial resistance belonging to the same bin were grouped together. Then, the mean drift dynamics of each cluster of PCM cells was calculated.

In particular, the relative increase of  $R_{GST}$  during a given time interval ( $\Delta t = 30 \text{ minutes}$ ) with respect to the first resistance measurements was calculated from the experimental data. Fig. 4.7 shows the comparison of the relative increases of the GST resistance as a function of the programmed  $R_{GST}$  for the partial-SET states obtained with the above experimental pro-



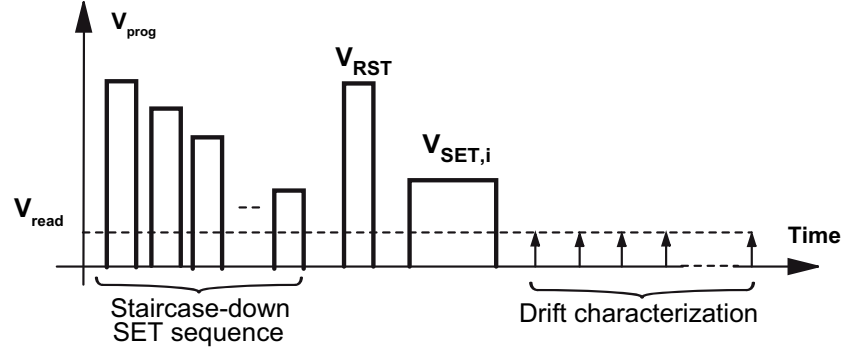


Figure 4.6: Operating sequence used to characterize the GST resistance drift of partial-SET states.

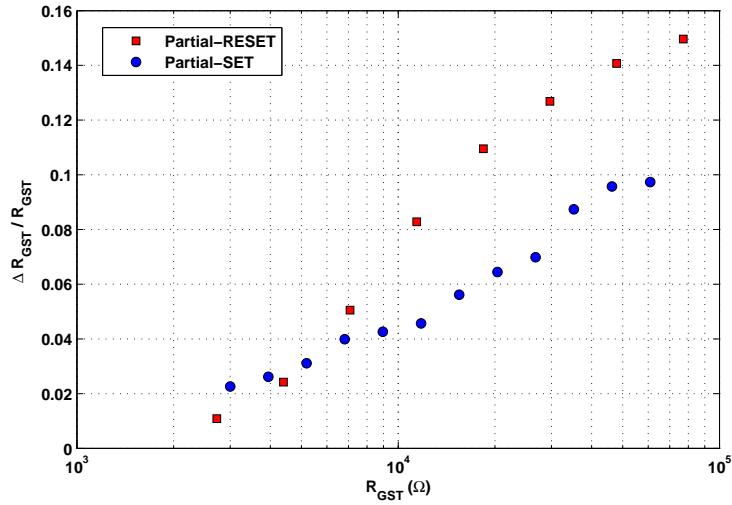


Figure 4.7: Relative variation of the GST resistance ( $\frac{\Delta R_{GST}}{R_{GST}}$ ) after 30 minutes from the first measurement (which was carried out 130 s after the programming pulse): partial-RESET states (square) and partial-SET states (circles).

cedure and the partial-RESET states studied in the previous Section [74]. It can be noticed that  $\frac{\Delta R_{GST}}{R_{GST}}$  increases with  $R_{GST}$  in both cases, starting from a minimum value of about 0.02, which is observed for cells programmed to a state having slightly higher resistance than the full-SET state.

To explain this behavior, the phase configuration obtained inside the active area with partial-SET and partial-RESET programming has to be considered. As pointed out in the literature [75], in partial-SET programming a conductive path is dagged inside the amorphous volume obtained after the RESET operation. Since quite low resistance values are considered, the path can be assumed to be complete (differently from the case of partial-SET states having high resistance [66]), thus giving essentially rise to a parallel-type phase configuration inside the active region.

Then, the active GST resistance can be expressed as the parallel of the amorphous-phase resistance  $R_A$  and the crystalline-phase resistance  $R_C$ :

$$R_{GST} = R_C || R_A = \frac{R_A R_C}{R_A + R_C}. \quad (4.5)$$

Both  $R_A$  and  $R_C$  depend on the thickness,  $z_a$ , of the amorphous cap obtained after the RESET operation and the cross section  $A_C$  of the conductive filament obtained after the partial-SET pulse.  $R_{GST}$  can be written as a function of these parameters as follows:

$$R_{GST} = \frac{\rho_C \rho_A z_a}{A \rho_C + A_C (\rho_A - \rho_C)}, \quad (4.6)$$

where  $A$  is the GST-heater contact area and  $\rho_A$  ( $\rho_C$ ) is the resistivity of amorphous (crystalline) GST. The value of  $z_a$  obtained with the considered RESET pulse amplitude  $V_{RST}$  can be estimated to be in the order of 30 nm [70], thus allowing to estimate  $A_C$  from every value of  $R_{GST}$  and, then, to determine the contribution of  $R_C$  and  $R_A$  to the GST resistance.

The drift of  $R_A$  can be modeled as the increase of the electrical resistivity of amorphous GST from its initial value  $\rho_A$  to  $\alpha \rho_A$ ,  $\alpha > 1$ , during  $\Delta t$ . Then, it turns out that

$$\frac{\Delta R_{GST}}{R_{GST}} = \frac{\alpha(R_C + R_A)}{\alpha R_A + R_C} - 1. \quad (4.7)$$

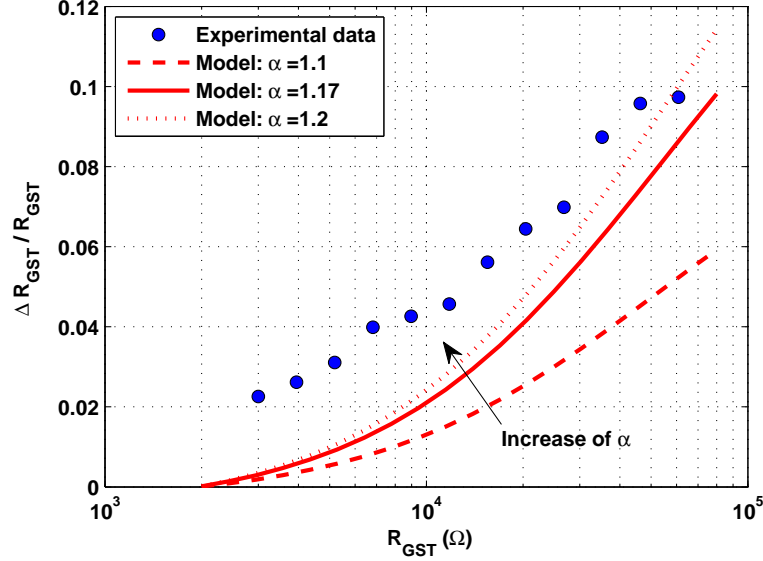


Figure 4.8: Relative variation of the GST resistance ( $\frac{\Delta R_{GST}}{R_{GST}}$ ) in partial-SET programmed cells after 30 minutes from the first measurement: comparison between experimental data and values calculated with Eq. (4.7) for different values of  $\alpha$ .

The value of  $\alpha$  was set according to the drift dynamics of the RESET state obtained with the considered  $V_{RST}$ . By choosing the value of  $\alpha$  corresponding to the initial RESET resistance of our cells [70],  $\alpha = 1.17$ , Eq. (4.7) underestimates the experimental data. This disagreement cannot be ascribed to the used value of  $\alpha$ , as can be noticed from Fig. 4.8, which shows that the curve corresponding to the experimental data is intrinsically different from the curves obtained by means of Eq. 4.7.

To determine if the conductive filament is responsible for such a disagreement, its contribution to the drift dynamics has to be separately determined. To address this item, the drift dynamics of the full-SET state was measured, assuming that its conduction properties are similar to those of the conductive filament of partial-SET states. The full-SET state was obtained with an SCD procedure ( $V_{SET,start} = 5$  V,  $V_{SET,stop} = 1$  V,  $\Delta V = 25$  mV, and  $t_{pulse} = 100$  ns). The obtained results are shown in Fig. 4.9. It can be observed a slight

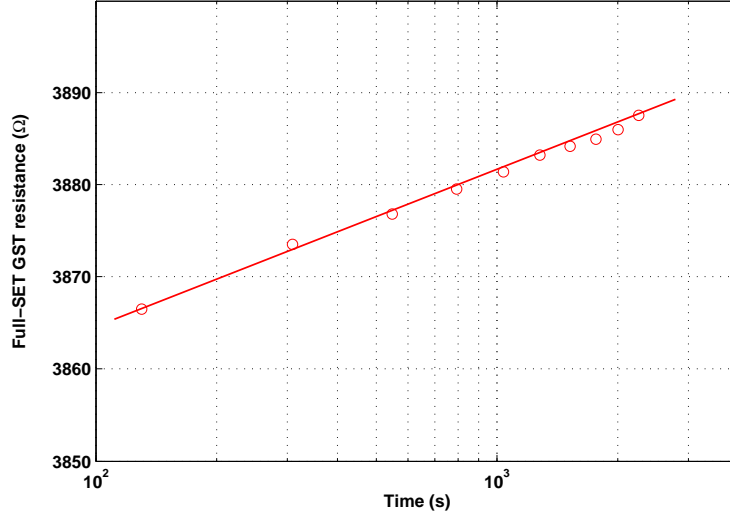


Figure 4.9: Log-log plot of the experimental results of the GST-layer full-SET resistance drift over time.

increase of the full-SET resistance over time, which corresponds to a relative increase of the GST layer resistance of about 0.005 during the considered  $\Delta t$ . This value is in good agreement with data presented in the literature [83] and may be ascribed to the presence of a residual fraction of amorphous material after the full-SET programming operation.

Similarly, a drift contribution of the conductive path may contribute to low-field resistance drift in partial-SET states. This contribution can be modeled as an increase of the equivalent resistivity of the conductive filament from its initial value  $\rho_C$  to  $\beta\rho_C$ ,  $\beta > 1$ , during  $\Delta t$ , which leads to the following expression:

$$\frac{\Delta R_{GST}}{R_{GST}} = \frac{\alpha(R_C + R_A)}{\frac{\alpha}{\beta}R_A + R_C} - 1. \quad (4.8)$$

The faster the drift dynamics, the higher  $\frac{\Delta R_{GST}}{R_{GST}}$ . According to the calculated fitting, the equivalent resistivity of the percolation phase increases by a factor  $\beta \simeq 1.02$  from the first to the last resistance measurement. This

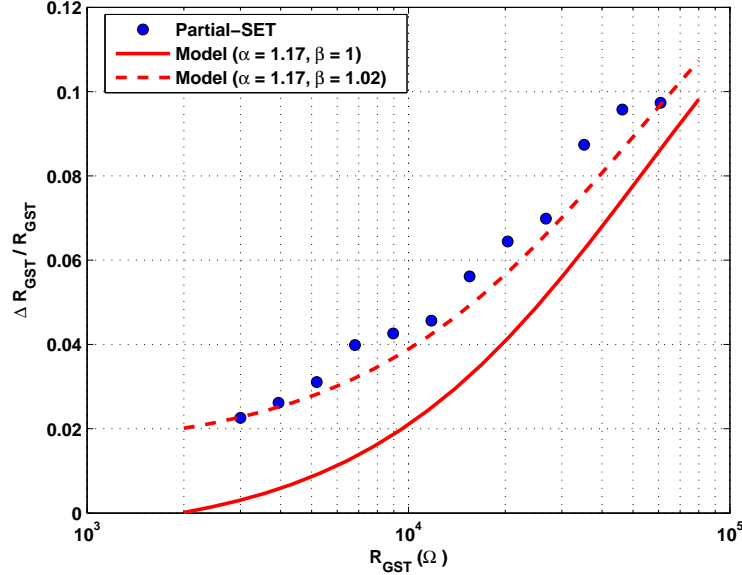


Figure 4.10: Relative variation of the GST resistance ( $\frac{\Delta R_{GST}}{R_{GST}}$ ) in partial-SET programmed cells after 30 minutes from the first measurement: comparison between experimental data and Eq. 4.8.

value is higher than that obtained in the full-SET case, which is ascribed to the presence of a higher fraction of residual amorphous phase inside the conductive path resulting from the different programming conditions (only one pulse is applied for drift characterization in partial-SET states while a staircase-down sequence of pulses is applied to obtain the full-SET state).

The developed model and the experimental data are compared in Fig. 4.10. A very good agreement is observed when the drift phenomenon of the percolation path is taken into account.

## 4.2 Crystallization in partial-SET states

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The aim of this Section is to contribute to the development of data retention optimized partial-SET programming algorithms for multilevel storage in PCMs. In partial-RESET programming, each pulse produces an amorphous phase state of the chalcogenide material, thus suggesting that the considered

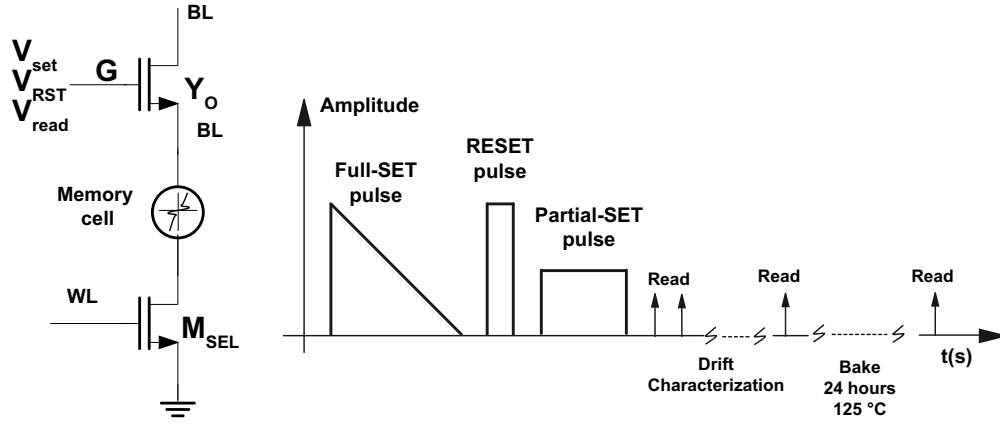


Figure 4.11: (a) Simplified schematic of the circuit used to program and read the memory cells in the used experimental device and (b) experimental procedure.

programming operation does not facilitate crystallization process. On the other hand, in partial-SET programming, each pulse determines a significant thermal stress on the initially amorphous chalcogenide, suggesting that the programming operation itself may have a relevant effect on data retention properties. In this respect, in this Section the stability of intermediate states obtained by means of the partial-SET programming technique is addressed by analyzing the effects of the width and the amplitude of the programming pulses on the degradation of intermediate programmed resistance levels over time. The average behavior of an array of PCM cells was studied, showing that data retention properties degrade as the programming pulse amplitude and/or time duration increase.

#### 4.2.1 Experimental procedure and drift correction

The experimental procedure used to study crystallization in partial-SET states consists in the following sequential steps (Fig. 4.11) applied to a sub-array of 2048 cells. First, a full-SET operation was carried out, followed by a full-RESET 100-ns voltage pulse (5.2 V). Then, the considered cells were programmed by means of a single partial-SET current pulse having predetermined amplitude and time duration values. After programming, the cell current was read every 3 minutes over a time interval of about 30 minutes

( $t_{drift}$ ) to characterize the drift dynamics. Then, the PCM device was baked for 24 hours at 125 °C and, finally, the cell current was measured again. The cell conductance was calculated from the cell current and, then, the contributions of the heater and the crystalline GST above the active volume were removed in order to consider only the active GST conductance.

It is worth to point out that, due to the stochastic nature of crystallization, the same partial-SET programming pulse may give rise to different values of the cell conductance, so that by applying the same pulse to a cell array, the behavior of a fairly large set of intermediate states can be investigated.

In order to remove drift effects from the results of the above measurements, the drift dynamics was modeled with the power-law dependence over time that holds in the cases of full-RESET and partial-RESET states [74]. Thus, the drift exponent  $\nu$  was estimated from the data collected with the readout sequence in Fig. 4.11, by using the following equation for the GST conductance  $G_{GST}$ :

$$G_{GST}(t) = G_{GST,0} \left( \frac{t}{t_0} \right)^{-\nu}, \quad (4.9)$$

where  $t$  is time and  $G_{GST,0}$  is the conductance measured at the reference time  $t_0$ , in our case 130 s after the programming operation. A basic assumption is that crystallization effects are negligible at room temperature in a time interval of 30 minutes. The calculated drift coefficient is plotted in Fig. 4.12 as a function of  $G_{GST,0}$ . In order to estimate the drift contribution to the GST conductance shift during bake, the equivalent drift time at room temperature  $T_0$  which leads to the same conductance drift of the bake operation was calculated according to the following equation [83]:

$$t_{eq} = \tau^{(1 - \frac{T_{bake}}{T_0})} t_{bake}^{\frac{T_{bake}}{T_0}}, \quad (4.10)$$

where  $\tau$  is the atomic time ( $10^{-13}$ s). The highest contribution of the drift to the resistance variation is obtained at the beginning of the bake period. During this period, the crystallization process is slow due to the presence

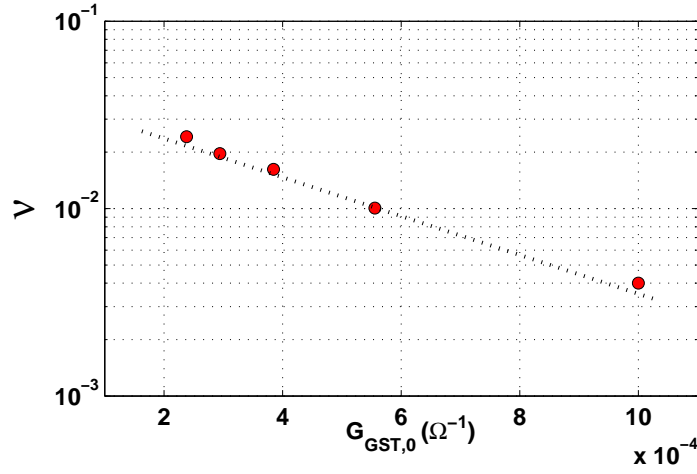


Figure 4.12: Extrapolated drift exponent,  $\nu$ , of the programmed GST conductance before the bake operation as a function of the GST conductance,  $G_{GST,0}$ , measured at reference time  $t_0$ .

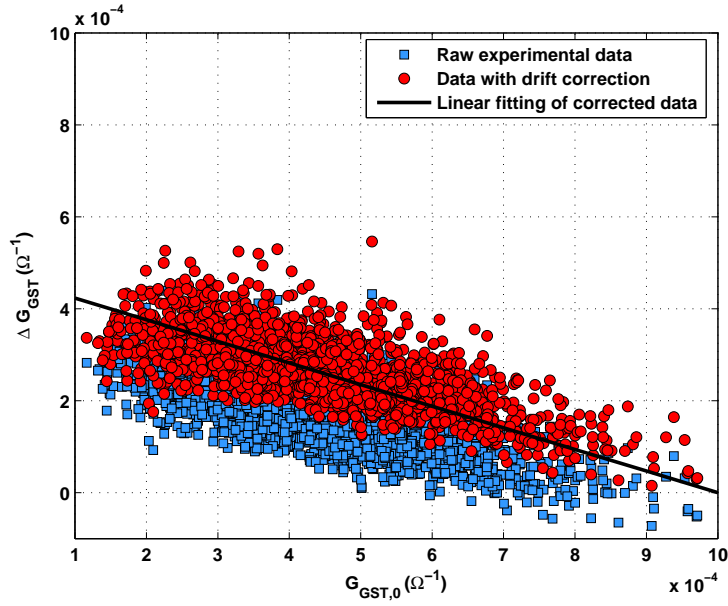


Figure 4.13: Variation of the GST conductance due to bake as a function of the programmed GST conductance: raw experimental data (circles) and data with drift correction (squares). Cells are programmed with a single current pulse having a time duration of  $1\mu s$  and an amplitude of  $350\mu A$ .



of only few initial nuclei that grow in size. The crystallization process is gradually sped up by the formation of new nuclei during bake. For this reason, the drift contribution was estimated by assuming a constant  $\nu$  during bake to a first order approximation.

By using the obtained values of  $\nu$  and  $t_{eq}$ , it was possible to calculate the effect of drift on the GST conductance during measurements:

$$\frac{\Delta G_{bake,drift}}{G_{GST,prebake}} = \left(\frac{t_{eq}}{t_{prebake}}\right)^{-\nu} - 1, \quad (4.11)$$

where  $G_{GST,prebake}$  is the GST conductance measured before the bake operation (i.e., at  $t_{prebake}$ ).

The above characterization enabled to evaluate the drift contribution and compensate for its effects in the experimental data by subtracting  $\Delta G_{bake,drift}$  from the GST conductance variation calculated from raw experimental data. The comparison between raw experimental data and data corrected for drift contribution is shown in Fig. 4.13 as a function of  $G_{GST,0}$ . It can be noticed that  $G_{GST,0}$  is equivalent to the corresponding drift-corrected value of GST conductance measured before bake, since the crystallization is negligible during drift measurements. Only data with drift correction will be considered in the following discussion, in order to analyze the crystallization contribution to the GST conductance variation during bake.

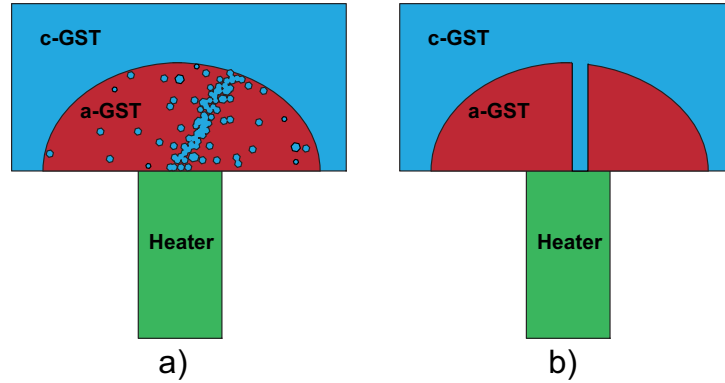


Figure 4.14: Schematic cross-section of a partially SET PCM cell: (a) random-nucleation effect on the phase configuration and (b) purely parallel phase configuration.

#### 4.2.2 Stability of partial-SET states

In order to investigate the physical phenomena that are responsible for the stability of the programmed partial-SET states, the phase distribution achieved after a partial-SET pulse has to be considered. Partial-SET programming gives substantially rise to a parallel phase configuration, in which a conductive path shunts the surrounding amorphous phase [62, 63, 64, 65]. Some evidence of incomplete filament formation in partial-SET states has also been provided in the literature [66], but concerning resistance states having high resistance (i.e., close to the full-RESET state resistance), whereas relatively low resistance states are considered in this study.

The qualitative representation of the phase configuration obtained after a partial-SET pulse is shown in Fig. 4.14(a). Since the maximum temperature inside the GST alloy during programming is achieved in proximity of the conducting filament, this zone shows the highest nucleation probability during the partial-SET pulse. For the sake of simplicity, the phase configuration in Fig. 4.14(a) can be approximated with an equivalent (i.e., having the same GST conductance) ideal parallel phase configuration, as shown in Fig. 4.14(b). Since the ideal configuration is purely parallel, the GST conductance can be expressed as:

$$G_{GST,0} = G_A + G_C = \frac{\sigma_A(A - A_C)}{L} + \frac{\sigma_C A_C}{L}, \quad (4.12)$$

where  $\sigma_A$  and  $\sigma_C$  are the conductivities of the amorphous and the crystalline GST, respectively,  $A$  is the GST-heater contact area,  $A_C$  is the equivalent cross-section of the conductive current path, and  $L$  is the equivalent thickness of the initially amorphous GST volume.

Consider now an increase in the equivalent cross-section of the crystalline path due to crystallization during bake. The GST conductance after bake can be written as

$$G'_{GST} = \frac{\sigma_A(A - A_C)(1 - \gamma) + \sigma_C(A_C + \gamma(A - A_C))}{L}, \quad (4.13)$$

where  $\gamma$  is the fraction of the amorphous volume that crystallizes during bake, thus adding a contribution  $\Delta A_C = \gamma(A - A_C)$  to the cross-section of the crystalline path.

It is worth noticing that, in principle, also the activation energy of electrical conduction in the intermediate states may be responsible for a variation of the GST conductance during bake. The activation energy of the overall GST conductance changes during bake due to the change in the contribution of amorphous and crystalline phases (with their respective activation energies) to GST conductance. However, in the partial-SET case, since the phase configuration is parallel, the crystalline phase dominates the GST conductance (this is not true, for instance, in partial-RESET states [56]). Then, it is actually the activation energy  $E_c$  of the crystalline phase conductivity that gives the major contribution to the activation energy of the overall GST conductance. Since  $E_c$  is very small, any possible change of its value due to bake may be neglected, allowing us to ascribe the substantial GST conductance variation to the sole change of the conductive path size.

From Eqs. (4.12) and (4.13), the GST conductance variation due to crystallization turns out to be

$$\Delta G_{GST} = G'_{GST} - G_{GST,0} = \gamma(G_{GST,max} - G_{GST,0}), \quad (4.14)$$

where  $G_{GST,max}$  is defined as  $\frac{\sigma_C A}{L}$  and can be estimated from the GST conductance in the full-SET state (in our case,  $G_{GST,max} \simeq 1 \text{ m}\Omega^{-1}$ ). From Eq. (4.14), it can be noticed that the dependence of  $\Delta G_{GST}$  on the programmed conductance  $G_{GST,0}$  is linear, as is also evident from the experimental data in Fig. 4.13.

Since, from above, the impact of the programming operation on data retention can be synthesized by means of parameter  $\gamma$ , an experimental analysis was carried out to evaluate the dependence of this parameter on the time duration and the amplitude of partial-SET programming pulses. As is apparent from the experimental results in Fig. 4.15, the value of  $\gamma$  decreases with decreasing time duration of the applied 350  $\mu\text{A}$  partial-SET pulse, from about 0.47 when  $t_{pulse} = 1 \text{ }\mu\text{s}$  to about 0.35 when  $t_{pulse} = 200 \text{ ns}$ . Similar considerations can be drawn by comparing the retention of cells programmed with current pulses having different amplitudes and the same time duration, as shown in Fig. 4.16. In this case, for any given value of active GST conductance, the retention properties improve as the amplitude of the programming pulse decreases. In particular, coefficient  $\gamma$  decreases from 0.47 when considering a 1  $\mu\text{s}$  partial-SET pulse with an amplitude of 350  $\mu\text{A}$  to about 0.27

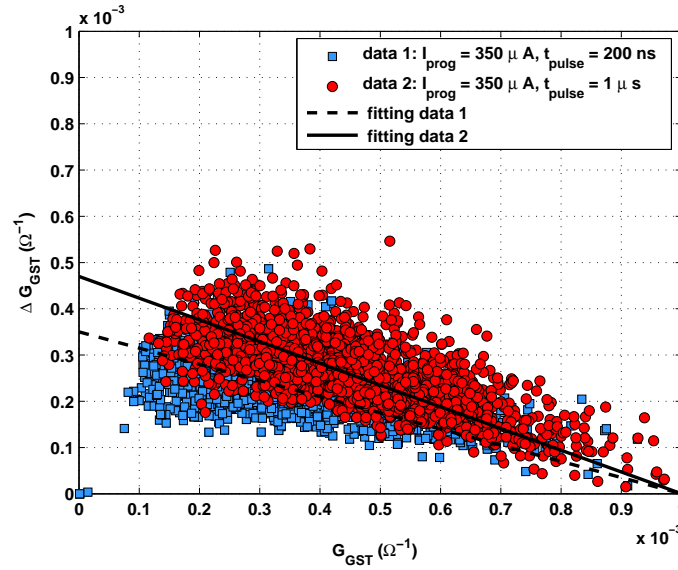


Figure 4.15: Measured retention of cells programmed with current pulses having different time durations and the same amplitude as a function of the GST conductance  $G_{GST,0}$ .

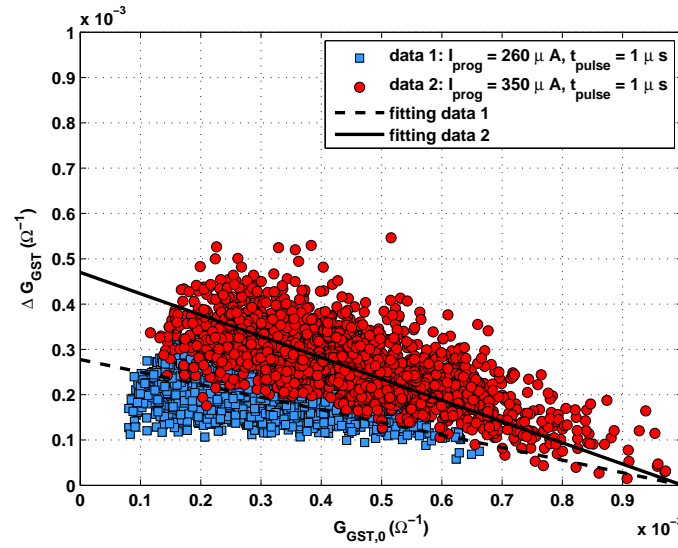


Figure 4.16: Measured retention of cells programmed with current pulses having different amplitudes and the same time duration as a function of the GST conductance  $G_{GST,0}$ .

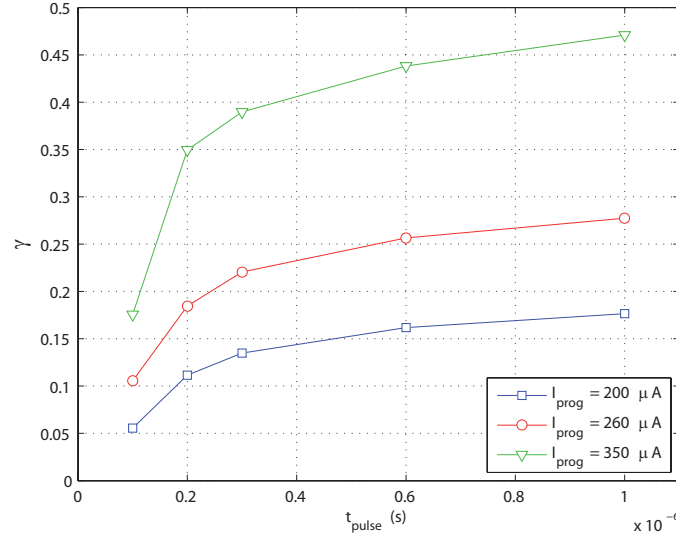


Figure 4.17: Dependence of crystallization coefficient  $\gamma$  calculated from experimental data upon pulse duration for different values of programming current  $I_{\text{prog}}$ .

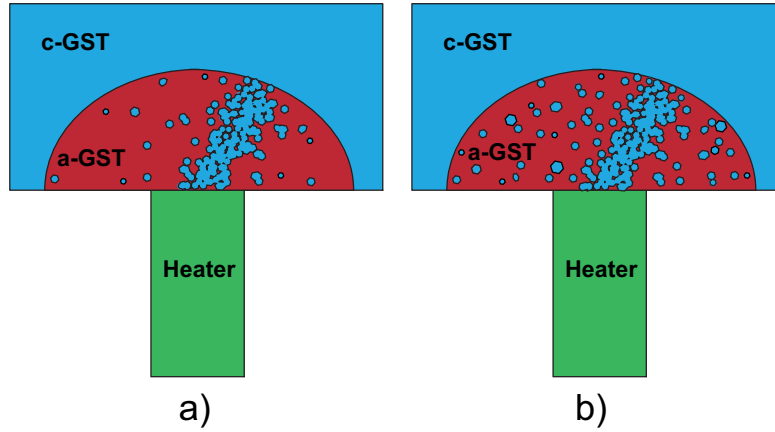


Figure 4.18: Two phase configurations that correspond to the same value of GST conductance but are obtained with different partial-SET pulses, namely: with a low-amplitude current pulse (a) and with a high-amplitude current pulse (b).

when applying a 1  $\mu\text{s}$  partial-SET pulse with an amplitude of 260  $\mu\text{A}$ . In summary, the data retention properties of cells having the same programmed GST conductance appear to be as an average worse in the case of cells programmed with a longer and/or higher partial-SET pulse, as shown in Fig. 4.17 for different values of pulse duration and programming current.

The above behavior is ascribed to the different programming thermal stress on the residual amorphous phase when pulses having different energy are applied. To explain this point, consider the two different partial-SET phase configurations in Fig. 4.18, which correspond to the same value of GST conductance but are obtained with different pulse amplitudes. As pointed out above, this case may occur since nucleation inside the amorphous GST is a random process. However, the programming thermal stress on the residual amorphous phase increases with the pulse amplitude, thus determining, as an average, a higher density of crystallites inside the amorphous GST and a higher average crystallite size. This difference affects the phase evolution during bake, which results in different data retention properties. Practical algorithms for multilevel programming consist in a sequence of pulses, typically a staircase-up sequence [84], each one contributing to the total thermal stress on the residual amorphous phase. As a guideline to improve data retention, the parameters of such sequence must be chosen so as to minimize the energy delivered to the memory cell, while still maintaining programming accuracy of the desired levels.

# 5

## Scaling of programming current and read window

In PCMs, the programming power and the read window depend on the electrical properties of the cell materials as well as on the architecture and the size of the memory cell. In this Chapter, the dependence of program and read windows on key geometrical cell parameters is investigated, with the aim to assess the impact of technology scaling on memory cell performance. To this end, the electrical and thermal resistances of the PCM cell have been expressed as a function of the geometrical parameters of the device, and used in the analytical model of partial-RESET programming of the PCM cell proposed in Chapter 3. In the following, the static model of the RESET operation is considered for simplicity.

### 5.1 Programming operation

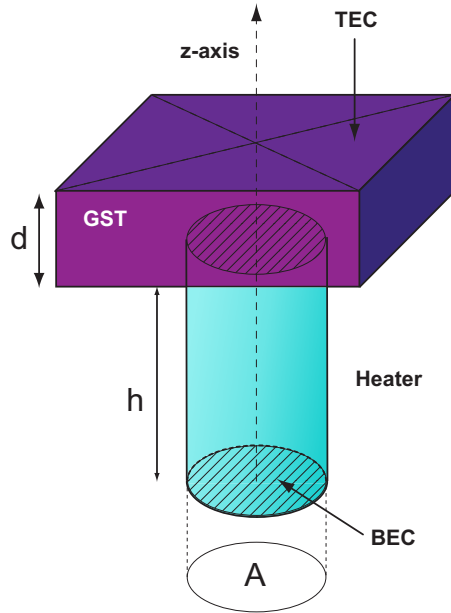
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First, the impact of technology scaling on the programming window is analyzed, focusing the attention on the programming power. The maximum programming power is required by the RESET operation, where the highest temperatures are needed so as to melt the active GST volume. The programming current will be considered in the following analysis, since it affects the capability to program more cells in parallel and, thus, the maximum programming throughput that can be achieved in a PCM chip. The minimum current value required to melt a portion of the active GST layer is referred to

as the melting current,  $I_{melt}$ . In other words,  $I_{melt}$  is the current that makes the temperature at the GST-heater interface reach the melting point of the GST alloy.

When the current flowing through the memory cell during a write operation is higher than  $I_{melt}$ , the obtained RESET resistance increases with the current pulse amplitude. In fact, the maximum temperature inside the cell increases with the pulse amplitude, thus leading to a larger melted region and, hence, the amorphization of a larger GST volume.

To analyze the effects of technology scaling on PCM cells, a parameter which allows a proper comparison of cells having different dimensions must be introduced. To this end, the full-RESET state was defined as the state obtained when the maximum temperature inside the PCM cell during programming reaches a predetermined value  $T_{RST,max}$ . This temperature  $T_{RST,max}$  is achieved with a current pulse of amplitude  $I_{RST,max}$ . Due to the different values of their electrical and thermal resistances, different cells require different pulse amplitudes (i.e., different values of  $I_{RST,max}$ ) to reach



*Figure 5.1: Structure of the lance heater PCM cell. TEC and BEC are the top and the bottom electrode contact, respectively.*



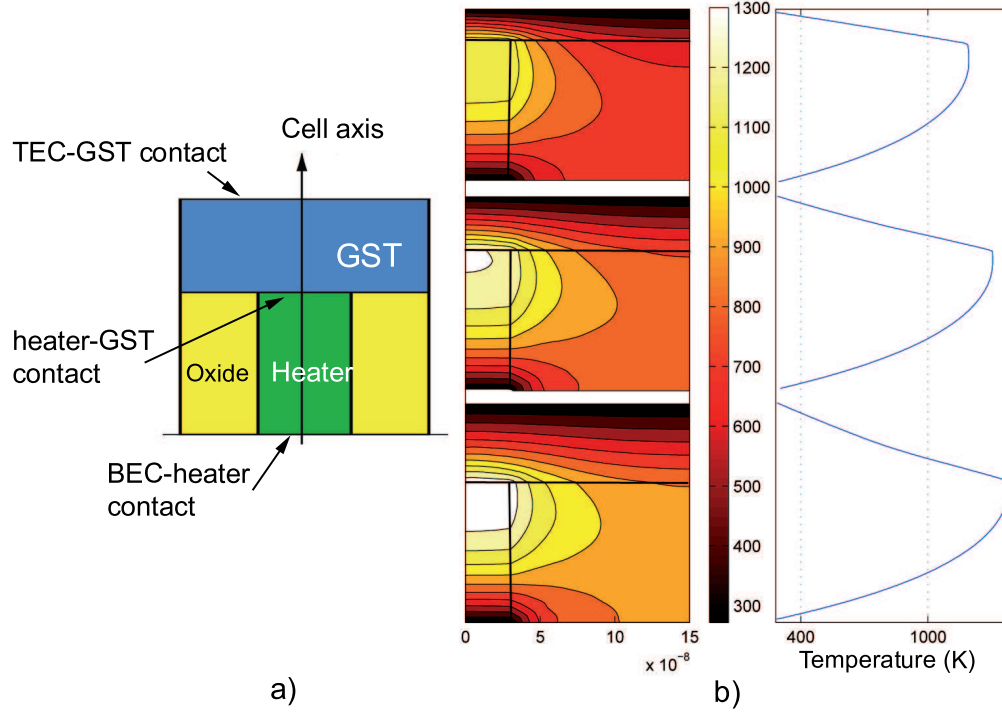


Figure 5.2: Cell structure (a) and simulated temperature maps inside a lance heater PCM cell with different values of GST layer thickness (b):  $d_1 = 40$  nm,  $d_2 = 70$  nm, and  $d_3 = 100$  nm. Notice that the temperature profile is almost linear inside the GST layer. The maps were obtained by means of our 3D finite-element model [71].

$T_{RST,max}$ . In any case,  $I_{RST,max}$  is directly related to the melting current  $I_{melt}$  (typically,  $I_{RST,max}$  is about 50% higher than  $I_{melt}$ ), which can thus be considered as the key parameter in the following analysis.

The temperature reached inside a lance heater cell of given sizes can be estimated by means of the approximated electro-thermal model presented in Chapter 3. In general, the temperature increase in the active GST volume is due to the Joule effect related to the current flow both through the heater (heater heating) and through the GST layer itself (GST self-heating). Nevertheless, GST self-heating can be neglected when considering high-amplitude RESET pulses. In fact, under these conditions, the resistance of the GST

layer (both in the crystalline and in the amorphous state) is negligible with respect to the heater resistance due to high-field effects (indeed, the PCM cell is operated in the ON region). In this case, we can thus estimate the temperature profile inside the PCM cell by considering only the Joule power generated inside the heater. We assume, for simplicity, a cylindrical geometry of the heater and calculate the temperature along the  $z$ -axis (Fig. 5.2(a)).

The power generated in a volume  $A\delta z$  located at a distance  $z$  from the BEC contact is equal to  $\delta Q = \frac{I^2 \rho_h}{A} \delta z$ , where  $I$  is the current flowing through the cell and  $\rho_h$  is the electrical resistivity of the heater material. The power amount  $\delta Q$  contributes to the temperature increase  $\Delta T$  at the heater-GST interface with a term  $\delta T$  given by

$$\delta T = [(R_{th,GST} + R_u(z)) \| R_d(z)] \frac{R_{th,GST}}{R_{th,GST} + R_u(z)} \delta Q, \quad (5.1)$$

where  $R_u(z) = \frac{h-z}{\kappa_h A}$  and  $R_d(z) = \frac{z}{\kappa_h A}$  ( $\kappa_h$  being the thermal conductivity of the heater material) are the heater thermal resistances from the coordinate  $z$  to the GST-heater contact and to the BEC contact, respectively, and  $R_{th,GST}$  is the equivalent thermal resistance of the GST layer.

By integrating Eq. (5.1) along the  $z$ -axis from the BEC contact ( $z = 0$ ) to the GST-heater contact ( $z = h$ ), we obtain the temperature  $T$  at the interface:

$$\begin{aligned} T &= \frac{I^2 \rho_h h}{A} \cdot \frac{R_{th,GST} R_{th,h}}{2(R_{th,GST} + R_{th,h})} + T_0, \\ &= I^2 R_h \frac{1}{2} (R_{th,GST} \| R_{th,h}) + T_0. \end{aligned} \quad (5.2)$$

In the above equations,  $T_0$  is room temperature,  $R_h = \frac{\rho_h h}{A}$  is the electrical resistance of the heater, and  $R_{th,h}$  is the thermal resistance of the heater, which can be expressed as  $\frac{h}{\kappa_h A}$ .

In order to estimate the dependence of  $R_{th,GST}$  on the geometrical dimensions of the memory cell, we simulated the temperature profile along the  $z$ -axis inside the GST layer with a previously proposed 3D model [71]. Fig. 5.2(b) shows the obtained results for different values of the GST layer thickness. It can be noticed that the temperature decreases almost linearly inside the GST layer with increasing distance from the GST-heater contact.

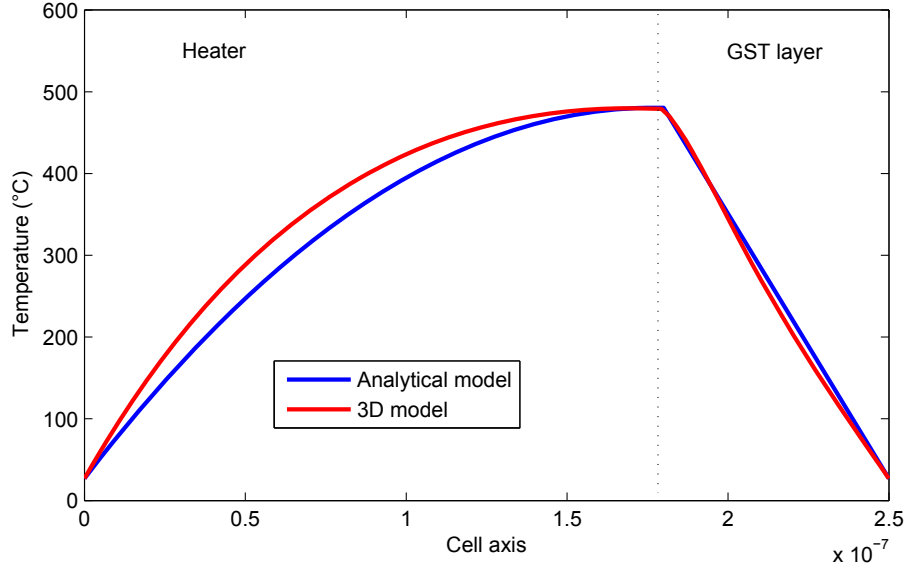


Figure 5.3: Comparison of the thermal profile along the cell axis obtained by means of the analytical model and the 3D finite-element model [71].

The accuracy of the linear approximation increases as the ratio between the GST layer thickness and the heater radius decreases. Since this behavior suggests that heat flow inside the GST is substantially directed along the  $z$ -axis, a reasonable approximation for the thermal resistance of the GST layer is  $R_{th,GST} \simeq \frac{d}{\kappa_{GST}A}$ , where  $\kappa_{GST}$  is the thermal conductivity of the GST material.

The temperature profile obtained by means of Eq. (5.2) is compared with 3D finite-element simulation in Fig. 5.3, showing good agreement, especially inside the GST layer. The slight disagreement inside the heater is ascribed to the heat flow in the material that surrounds the heater. To take this contribution into account, the value of  $\kappa_h$  used in the compact model was set higher than the actual physical value.

From Eq. (5.2), by taking the expression of  $R_{th,h}$  and  $R_{th,GST}$  into account, we calculate the value of the current  $I_{melt}$  at which the melting tem-

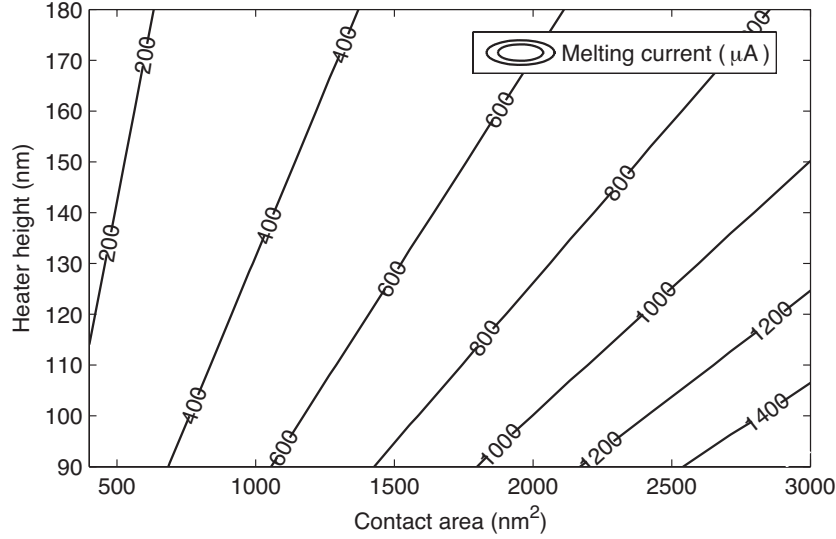


Figure 5.4: Map of the melting current  $I_{melt}$  as a function of the GST-heater contact area and the heater height (the GST layer thickness was set to 70 nm).

perature  $T_{melt}$  is achieved at the heater-GST interface:

$$\begin{aligned}
 I_{melt} &= \sqrt{2 \cdot \frac{(T_{melt} - T_0)}{\rho_h k_h} \frac{(R_{th,GST} + R_{th,h})}{R_{th,GST} R_{th,h}^2}}, \\
 &= \frac{A}{h} \sqrt{2 \cdot \frac{(T_{melt} - T_0)}{\rho_h} \left( \kappa_h + \kappa_{GST} \frac{h}{d} \right)}. \quad (5.3)
 \end{aligned}$$

By substituting, in Eq. (5.3), the values of the electrical and thermal parameters summarized in Tab. 5.1, we obtained the results shown in Fig. 5.4. As can be seen from Eq. (5.3), the melting current depends on  $\frac{h}{d}$  and the heater dimensional ratio  $\frac{A}{h}$ . In particular, since  $\kappa_{GST}$  is typically much smaller than  $\kappa_h$ ,  $I_{melt}$  can be approximated as:

$$I_{melt} \simeq \frac{A}{h} \sqrt{2 \cdot (T_m - T_0) \frac{\kappa_h}{\rho_h}}. \quad (5.4)$$

Due to fabrication process constraints, heater geometries with a high aspect ratio may not be easily manufacturable. Several fabrication solutions

have been proposed to overcome lithographic limits and, thus, realize heater structures with minimized contact area [25, 38] and, hence, lower values of  $I_{melt}$ . Heater geometries having a high aspect ratio will be considered with the purpose of investigating scaling perspectives, even though they may require advanced fabrication techniques.

When all linear dimensions are scaled by a factor  $\epsilon < 1$  (isotropic scaling), the reduction of  $I_{melt}$  turns out to be proportional to  $\epsilon$  while, in the case of planar dimensions scaling (shrinking),  $I_{melt}$  decreases as  $\epsilon^2$ . The reduction of the heater height ideally leads to a linear increase of  $I_{melt}$  due to the decrease of the Joule power and the heater thermal resistance. On the contrary, the reduction of the contact area only by the given factor, that is the shrinking approach, leads to a proportional decrease of the melting current, due to the increase of both Joule power and the thermal resistance of the cell by the same factor.

## 5.2 Read operation

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The available read window in a PCM device depends on the minimum (SET) and the maximum (RESET) values of the cell resistance. To get an estimation of the effects of technology scaling over the read window, an analytical expression of the GST layer resistance in the full-RESET and the full-SET state has to be calculated. When programming the cell into its full-RESET state, the GST layer undergoes crystalline to amorphous phase transition in the region where the temperature exceeds the melting point. As pointed out above, we can approximate the thermal profile inside the GST along the  $z$ -axis with a straight line. Under this assumption, the thickness  $z_{a,max}$  of

Table 5.1: Electrical and Thermal Properties of Cell Materials

Heater thermal conductivity	$\kappa_h$	$36 \frac{W}{m^{\circ}C}$
GST thermal conductivity	$\kappa_{GST}$	$0.5 \frac{W}{m^{\circ}C}$
Heater electrical resistivity	$\rho_h$	$30 \mu \Omega \cdot m$
Cryst. GST electrical resist.	$\rho_C$	$0.1 m \Omega \cdot m$
Amorph. GST electrical resist.	$\rho_A$	$10 m \Omega \cdot m$

the amorphous cap obtained by applying a full-RESET pulse to the cell can be expressed as:

$$z_{a,max} = d \frac{(T_{RST,max} - T_{melt})}{T_{RST,max} - T_0}. \quad (5.5)$$

Thus, the thickness of the amorphous cap obtained by means of the RESET operation is a fraction  $f = \frac{(T_{RST,max} - T_{melt})}{T_{RST,max} - T_0}$  of the GST layer thickness [50].  $z_{a,max}$  determines the value of the GST resistance in the full-RESET state and, thus, the lower edge of the read current window. Since the temperature gradient during the RESET operation is much higher along the  $z$ -axis than along the other two directions, the ratio between the thickness and the width of the amorphous cap is quite low, which allows us to estimate the cell resistance in the full-RESET state as

$$R_{RST} \simeq \rho_A \frac{fd}{A}, \quad (5.6)$$

where  $\rho_A$  is the amorphous GST resistivity and the heater resistance  $R_h$  has been neglected since it is much lower than the resistance of the GST layer after the full-RESET pulse.

Let us now estimate the cell resistance in the full-SET state. By neglecting the current spread inside the crystalline GST, we can write:

$$R_{SET} = \frac{\rho_C d + \rho_h h}{A} \quad (5.7)$$

where  $\rho_C$  is the resistivity of crystalline GST and  $\rho_h$  is the resistivity of the heater material.

When considering the current sensing approach, the SET (RESET) read current  $I_{read,SET}$  ( $I_{read,RST}$ ) can be expressed as

$$I_{read,SET} = \frac{V_{read}}{R_{SET}}, \quad (5.8)$$

$$I_{read,RST} = \frac{V_{read}}{R_{RST}}, \quad (5.9)$$

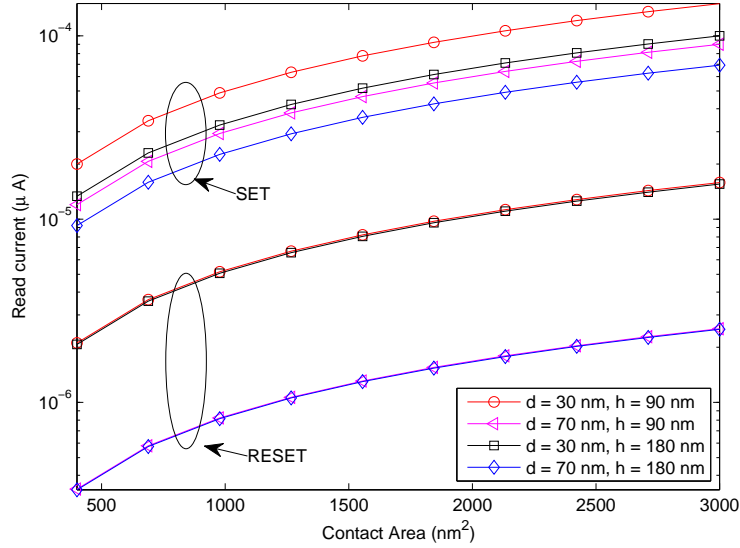


Figure 5.5: Constant voltage approach: read current as a function of the contact area  $A$  for different values of GST layer thickness  $d$  and heater height  $h$ . The read voltage is assumed to be 0.3 V.

where  $V_{read}$  is the value of the read voltage across the storage element. In order to avoid unintended programming during readout,  $V_{read}$  must be low enough to prevent electronic switching of the amorphous chalcogenide (if any). From above, the read current window is affected by both the value of  $V_{read}$  and the geometrical scaling strategy.

Two possible read approaches may be implemented: constant voltage readout, where  $V_{read}$  is kept constant despite the geometrical scaling, and constant field readout, where the electrical field inside the GST is maintained constant while the geometry is scaled.

When  $V_{read}$  is kept constant, the electrical field  $E_{read}$  inside the amorphous GST during readout increases as the amorphous cap size is scaled down ( $E_{read} \approx \frac{V_{read}}{f \cdot d}$ ). In this case, in order to calculate the read current, the exponential dependence of the amorphous GST resistivity on the electrical field [85, 52] must be taken into account. For a given PCM cell in the RESET

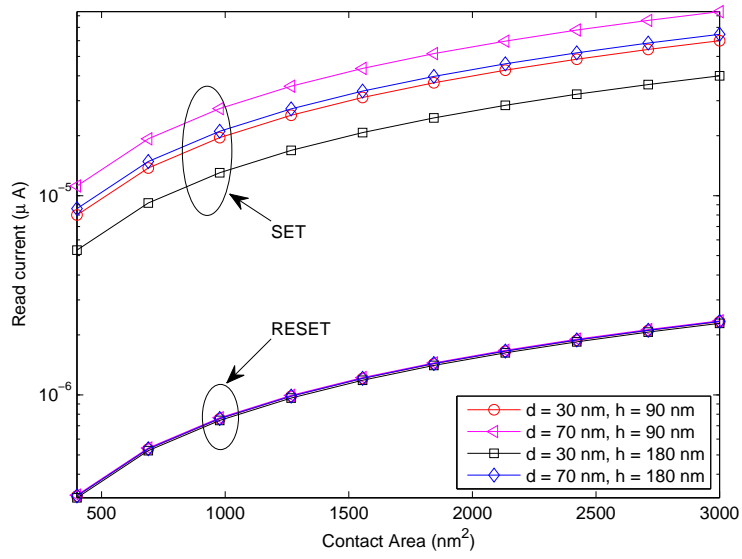


Figure 5.6: Constant field approach: read current as a function of the contact area  $A$  for different values of GST layer thickness  $d$  and heater height  $h$ . The read voltage is assumed to be proportional to the thickness of the GST layer ( $V_{\text{read}} = 0.3 \text{ V}$  @  $d = 70 \text{ nm}$ ).



state, neglecting the heater resistance, we have

$$R_{RST} \propto \exp\left(-\frac{E_{read}}{E_{ref}}\right), \quad (5.10)$$

where  $E_{ref}$  is the electrical field which activates the amorphous GST resistivity. The value of  $V_{read}$  must be chosen so as to ensure that, for any considered cell size, the PCM device is operated in the read region (OFF zone) and the electrical field is kept below the critical switching field. In this respect, we chose  $V_{read} \simeq 0.3$  V and calculated the cell resistance and the read current for both the SET and the RESET state.  $E_{ref}$  was set to 30 M V/m [86].

It can be noticed from the simulation results in Fig. 5.5, that the constant voltage approach leads to a significant increase of the minimum read current (RESET state), mainly due to the dependence of the amorphous GST resistivity on the electrical field. Moreover, the SET read current increases as the thickness of the GST layer and/or the heater height decrease, due to the reduction of the SET cell resistance. According to Eqs. (5.6) and (5.7), the heater height has a significant impact over the read current only when the cell is in its SET state.

The above results hold for constant voltage readout. Several studies [86, 19] show that the threshold voltage  $V_{th}$  of an amorphous GST volume decreases linearly with its thickness which, in our case, is a fraction of the GST layer thickness. Then,  $V_{read}$  can be chosen to be proportional to  $d$ , so as to keep the electrical field inside the amorphous GST during readout ( $E_{read} \simeq \frac{V_{read}}{f \cdot d}$ ) roughly constant and lower than the critical value for threshold switching. This approach is referred to as constant field readout in the following.

When considering constant field scaling, the current read window scales as shown in Fig. 5.6. The read voltage was set to 0.3 V for  $d = 70$  nm. The RESET read current is substantially independent of  $d$  and  $h$ , since the read voltage and the cell resistance roughly scale by the same factor. As opposed to the previous approach, in constant field scaling the SET read current decreases with decreasing  $d$ . In fact,  $R_{SET}$  is less sensitive than  $V_{read}$  with respect to  $d$  due to the non negligible contribution of the heater resistance. The dependence of  $I_{read}$  on the contact area is qualitatively the

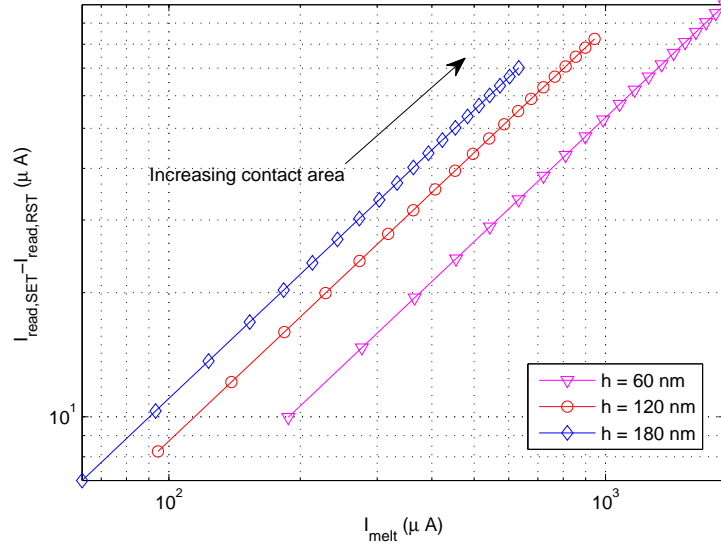


Figure 5.7: Constant field approach: width of the read window as a function of the melting current for different values of geometrical parameters. The thickness of the GST layer was set to 70 nm.

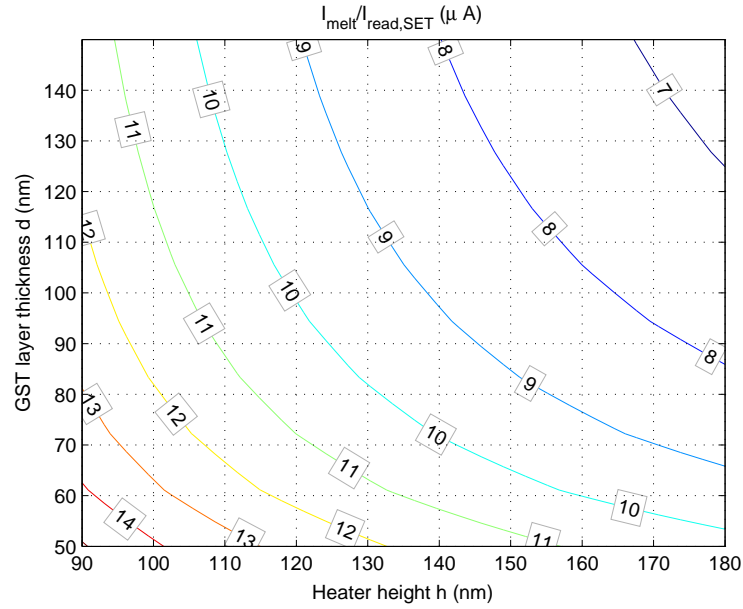


Figure 5.8: Constant field approach: ratio between the melting current and the SET read current as a function of the contact area,  $A$ , and the heater height,  $h$ .

same as in the constant voltage case. In both approaches, the read window becomes narrower with decreasing contact area. As a consequence, higher accuracy of sensing circuits is required in order to correctly read the memory cell contents.

As can be seen from Fig. 5.7, the width of the read window decreases with decreasing melting current. It is worth to point out that the melting current must be reduced to achieve low power operation. In addition, the reduction of both the maximum read current and the melting current is beneficial from the viewpoint of the thermal disturb during readout. In fact, when considering the constant field approach, from Eqs. (5.3) and (5.7), the ratio between the melting current and the maximum read current (i.e., the read current of the cell in the SET state) can be expressed as

$$r \simeq \left( \frac{\rho_C}{E_{read}h} + \frac{\rho_h}{E_{read}d} \right) \sqrt{2\kappa_h \frac{T_{melt} - T_0}{\rho_h}}. \quad (5.11)$$

Unlike the melting current,  $r$  is ideally independent of the contact area. Furthermore, as shown in Fig. 5.8,  $r$  increases with decreasing values of  $d$  and  $h$ , which implies a reduction of thermal disturbs during the PCM cell read operation.

# Conclusions

This Thesis is devoted to the characterization and modeling of Phase Change Memory (PCM) cells with  $\mu$ Trench architecture realized in 180-nm technology, with emphasis on multilevel programming.

Chapter 1 has described the properties of PCMs with respect to other innovative non-volatile memory technologies and introduced the working principles of a PCM cell.

In Chapter 2, partial-RESET and partial-SET programming have been investigated at both the single-cell and the array level, with the aim to evaluate their performance from the viewpoint of multilevel storage. Four levels have been successfully placed inside the available window, choosing an optimized spacing strategy according to the characteristics of the chosen programming approach. In particular, for the considered  $\mu$ trench cell architecture, high resistance levels are easier to place when using partial-RESET programming, while the partial-SET approach enables low resistance levels to be programmed with good accuracy.

Chapter 3 has been devoted to the modeling of partial-RESET operation, with the aim to understand the dynamic effects of the amorphization process.

In Chapter 4, the stability of the programmed intermediate levels has been studied, considering both low-field resistance drift phenomenon and crystallization. In particular, the drift phenomenon turns out to be slower in partial-SET states than in partial-RESET states for a given programmed value of cell resistance, which has been ascribed to the different phase configurations obtained inside the active GST volume with the two programming strategies. The crystallization process has been investigated in partial-SET states as a function of the program pulse parameters, showing that resistance stability is improved when the cell is programmed by means of low-amplitude or short-duration pulses.

Finally, in Chapter 5, the effects of cell geometry scaling on the programming current and read windows have been analyzed starting from the simplified analytical model of the cell behavior proposed in Chapter 3. In  $\mu$ Trench cells, the RESET current can be reduced by increasing the heater height or decreasing contact area between heater and GST. However, also the read current window narrows with decreasing contact area between the heater

and the GST, thus arising a performance trade-off between the programming and the read operation. Two scaling approaches for the read voltage have been considered: constant read voltage and constant field scaling. In the former approach, the read voltage is kept constant when scaling down the cell size, thus determining a significant narrowing of the read current window when the thickness of the GST layer is reduced. In the latter approach, the read voltage is decreased proportionally to the thickness of the GST layer, thus keeping the electrical field constant inside the amorphous phase, which enables the read window to be widened with respect to the previous case.

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