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XXII Ciclo

Insights Into the Design of mm-Wave CMOS Receivers for Gb/s Applications

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Tesi di Dottorato di

Stefano Bozzola

to mum and dad

to Marco

"..finchè u matin cresciä da puèilu rechèugge

frè di ganeuffeni e dè figge,

bacan d'a corda marsa d'aegua e de sä,

che a ne liga e a ne porta 'nte 'na creuza de mä."

Fabrizio de Andrè

Creuza de mä

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Contents

Introduction **1**

1 Introduction to Millimeter Waves **7**

1.1 What's Millimeter Wave 7

1.1.1 ITRS and CMOS Evolution 10

1.2 Why Millimeter Waves 11

1.2.1 Applications 12

1.3 Wireless HDMI Proposal 15

1.3.1 Operating Band Frquencies 17

1.3.2 Modulation and Bit Rate 19

1.3.3 Error Vector Magnitude 21

1.3.4 Phase Noise 22

1.3.5 Receiver Sensitivity 24

2 Circuit Design **25**

2.1 MOS Transistor at mm-Wave 26
2.1.1 Maximum Oscillation Frequency 26
2.1.2 Minimum Frequency for Unconditional Stability 27
2.1.3 Maximum Available Gain 28
2.1.4 Maximum Stable Gain 29
2.1.5 Mason's Unilater Function 29
2.2 Transistor Design at mm-Wave 31
2.2.1 Gate Resistance 32
2.2.2 f_{max} Optimization 35
2.2.3 Gain Optimization 38
2.2.4 Cascode Topology 39
2.2.5 Inductively Degenerated Topology 43

3 MOS Validation 45
3.1 Pad and De-embedding Structures 47
3.2 NMOS Cascode Stages 48
3.3 Common Source Stage 53

4 Frequency Generation 57
4.1 54 GHz VCO 58
4.1.1 Inversion Mode MOS Varactor 59
4.1.2 VCO Design 64
4.1.3 Measurement Results 67
4.2 Frequency Dividers 73

4.2.1 Miller's Dividers 76
4.2.2 Injection Locked Dividers 79

5 Receiver Front-End 87

5.1 Direct Conversion 88
5.2 Sliding IF 89
5.2.1 Receiver Chain 91
5.2.2 Frequency Generation 97
5.2.3 Measurement Results 100
5.2.4 Conclusions 105
5.3 Wideband Sliding IF 108
5.3.1 Receiver Chain 109
5.3.2 Frequency Generation 113
5.3.3 Measurement Results 114
5.3.4 Conclusions 118

List of Figures 120

List of Tables 127

Bibliography 133

Introduction

CMOS scaling is providing ultra-fast devices, attractive for signal processing at Ka band, mm-wave and even in the THz gap [1] [2]. Several commercial applications, from high data rate wireless LANs to automotive cruise control, from remote sensing to medical imaging, would get momentum from a low cost implementation technology.

Building blocks and front-ends already achieve acceptable performances in the 60 GHz to 100 GHz range, even adopting relatively old technologies such as 130 nm CMOS, but the path toward commercialization requires more robust, lower power solutions. Benefit from node scaling is expected. In particular, power savings in the front-end high frequency blocks, due to the increased maximum oscillation frequency f_{max} and maximum available gain, and in the voltage controlled oscillator (VCO) and dividers, due to improved variable capacitor quality factor (Q) and reduced capacitive para-

sitics.

Industry interest is presently focused to high data rate applications such as high definition uncompressed video down-streaming leveraging the 7 GHz unlicensed bandwidth around 60 GHz. The push is toward compact low power solutions where selection of the processing architecture is a key factor. In 2008 the ECMA and WirelessHD groups published a standard proposal for a 60 GHz PHY for High Definition uncompressed video wireless transmission (WHDMI) up to 4 Gb/s [3].

This Ph.D work focuses on the study of millimeter waves applications and the best solutions to realize a fully integrated CMOS receiver for such high definition video down-streaming applications, considering architectures and building blocks.

This project started in 2005 in cooperation with "Studio di Microlettronica" (STMicroelectronics). Since there were little experience at that time regarding transistor modeling and design at such high frequencies, I have done a careful analysis on transistor topologies and their behavior at millimeter wave frequencies to understand the maximum gain achieving at 60 GHz and so the best gain solution. I have also studied the impact of the layout on the transistor performances and a test-chip with different devices has been integrated and measured. Measurements, done in cooperation with Berkeley Wireless Research Center (BWRC, Berkeley, CA, USA) and Prof. Ali M.

Niknejad, shown a good agreement with simulations, validating the transistor modeling used.

Once validated the models used, building blocks, like LNAs, VCOs and dividers, feasibility has been investigated. I have been involved mainly into studying and designing Voltage Controlled Oscillators (VCOs). The main effort has been done to achieve large tuning range and low phase noise while maintaining reasonably low the power consumption since, at that moment, state of art VCOs showed good performance in phase noise, but small tuning ranges, insufficient to cover the 7 GHz bandwidth described before or vice versa. A careful analysis on varactors and their factor of merit (Q) was then necessary , since at such high frequencies they are the main responsible for overall Q degradation. Then I designed and integrated a VCO operating at 54 GHz. Measurements show state of art performances both in tuning range (more than 12%) *and* phase noise (-118 dBc/Hz at 10 MHz offset).

Later on, once integrated and measured the main building blocks, an accurate analysis on the architecture to better realize a mm-wave front-end has been performed. Advantages and disadvantages of the main architectures, like Direct Conversion, Superheterodyne, Sliding IF, have been investigated considering performances, layout complexity and power consumption . A *sliding IF* architecture approach has

been selected. It consists in a first down-conversion to 1/3 of the received frequency, followed by a quadrature down-conversion to baseband. The operating frequencies of the two local oscillators (LOs) used are then one the half of the other one. In this case, compared to a classical Superheterodyne double conversion, it is possible to generate the two LOs using just one VCO working at 1/3 (or 2/3 GHz) of the received frequency, and obtain the other one just multiplying (or dividing) by two the first one, making necessary just on Phased Locked Loop (PLL).

Both versions have been realized. A narrow band front-end using a 20 GHz quadrature VCO and a multiplier and a wide band front-end with a 40 GHz differential VCO and two dividers to generate a better quadrature have been integrated and measured.

The first version presents a narrow band LNA and RF mixer, while the IF mixer is relatively broadband. The VCO I designed presents a special cross coupled topology in order to extract the second harmonic content directly from the 20 GHz quadrature VCO itself, avoiding an explicit multiplier. Measurements show a peak gain of about 28 dB at 64 GHz, with a tuning range of more than 12% and a phase noise of -115 dBc/Hz at 10 MHz offset. The main problems of this front-end were the narrow band and the quite critical quadrature. The latter, infact, is provided mainly by a first harmonic coupling on I and Q VCOs. This means that increasing the

quadrature accuracy can limit the overall phase noise performances.

To solve this problems, a wide band front-end has been designed and integrated. In this case the LO is generated by a 40 GHz differential VCO, while I and Q 20 GHz quadrature signals are provided more robustly by two injection locked dividers. The wide band LNA, moreover, is obtained by capacitively coupled inter-stage resonators for maximum gain-bandwidth product. For the wide band RF mixer, furthermore, I investigated and used a wide band resonating load consisting in a wide band filter based on transforming coupling. Measured overall performances of this fully integrated CMOS receiver shows 35.5 dB peak gain with a 13 GHz -3dB bandwidth around 61 GHz, 5.6 dB minimum noise figure and $<$ 6 dB in the entire bandwidth, -115 dBc/Hz at 10 MHz offset from 60 GHz phase noise and 12.6% frequency tuning range, drawing only 75 mA from 1 V supply (using a 65 nm CMOS technology by STMicroelectronics). These results fully satisfy the stringent requirements of the ECMA standard proposal regarding both the gain (and noise) and the frequency generation.

This work is then organized as follow:

In **Chapter 1** a general overview on millimeter wave frequencies and applications is given. A more detailed discussion regarding the ECMA standard proposal in provided.

In **Chapter 2** the key features regarding the circuit design at mm-wave frequency are discussed. The principal parameters to evaluate active devices performances at very high frequency are described and transistor design strategies are evaluated. A test-chip of active devices with different topologies is then described

In **Chapter 3** MOS modeling evaluation is described. Measurements from the test-chip described in the previous chapter are reported and compared with simulation.

In **Chapter 4** the issue of the frequency generation at millimeter wave frequencies is faced considering its most critical blocks: the VCO and the dividers. In this framework, we investigate the design of VCOs for mm-wave applications in 65 nm CMOS. In particular, an inversion mode Metal-Oxide-Semiconductor structure (I-MOS) is employed to realize the voltage controlled variable capacitor [4]. The the best approach regarding frequency dividers is then investigated.

In **Chapter 5** the receiver architecture is studied. Sliding IF architecture is introduced and described and the two different fully integrated receiver front-end using this kind of architecture previously described are reported and measured (narrow band and wide band).

Chapter 1

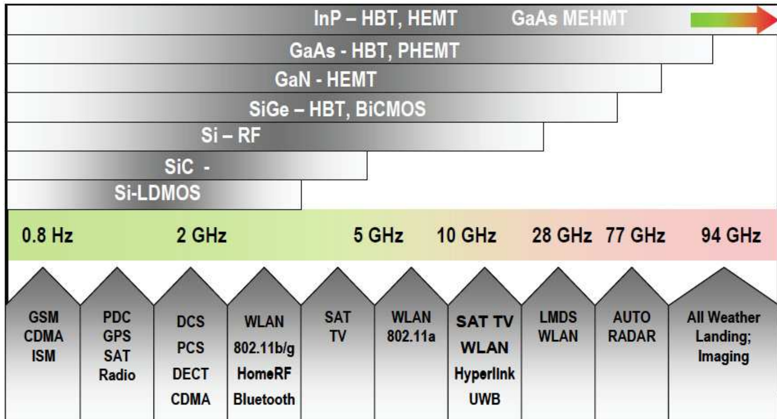
Introduction to Millimeter Waves

1.1 What's Millimeter Wave

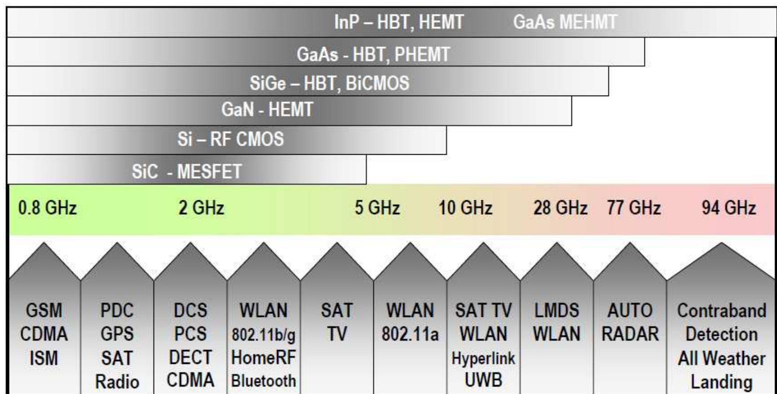
Millimeter waves (mmW) are electromagnetical waves that propagate with a wavelength in the order of millimeters. Millimeter wave spectrum generally includes frequencies higher than 30 GHz. Those frequencies have been historically used just for military and satellite applications due to the very high costs involved in the technology required.

Unlike most of the lower frequencies spectra, where silicon based

technologies dominate, there are a number of distinct semiconductor and device technologies which compete for this applications marketplace and most of them are usually quite expensive for mass production. Currently, devices and integrated circuits are manufactured on four different substrate materials [5]: GalliumArsenide (GaAs), Indium Phosphide (InP), Silicon Carbide (SiC) and Silicon (Si).
However, a commercial interest in millimeter wave spectrum and applications has grown steadily over the past decade. Compound III-V semiconductors have traditionally dominated this spectrum over the past several decades. However, today, with the drive to low-cost high-volume applications such as auto radar, along with scaling to sub-100 nm dimensions, the group IV semiconductors Silicon (Si) and Silicon-Germanium (SiGe) are rapidly moving up to mmW frequencies.
Fig. 1.1(a) illustrates the 2007 *International Technology Roadmap for Semiconductors* (ITRS) wireless communication application spectrum. Compared to the 2005 one (Fig. 1.1(b)), all the technologies have moved to higher frequencies and the boundary between the group IV semiconductors Si and SiGe and the III-V semiconductor GaAs has been moving to higher frequencies too. This means that Si-based technologies in the last few years have become usable for mmW applications too.



(a) 2007



(b) 2005

Figure 1.1: International Technology Roadmap for Semiconductors

ITRS foresees that in future years, Si-based technologies will prevail for high volume, cost sensitive markets in the millimeter wave range, while they will be unlikely to replace III-Vs in applications where either high power, gain, or ultra low noise is required.

1.1.1 ITRS and CMOS Evolution

Millimeter waves applications, as depicted in the previous paragraph, require high gain at such high frequencies together with very low achievable noise figure and power consumption. This means that whatever kind of technology is used, it has to guarantee an high enough maximum working frequency (f_{max}), and the possibility to realize passives with good performances (i.e. low losses). This usually implies to have technologies with high resistive substrate, and a metal stack with low resistivity as well.

Device Technology—RF CMOS	-								
CMOS NFET [1 HP CMOS lag 2 yrs]	-								
V_{dd}: Power Supply Voltage (V)	1.1			1			0.95	0.9	0.9
EOT: Equivalent Oxide Thickness (Å) [13]	12	11		9	7.5	6.5	5.5	5	6
L_g: Physical L_{gate} for High Performance logic (nm)	32	28	25	22	20	18	16	14	13
Peak F_t (GHz)	280	320	360	400	440	490	550	630	670
Peak F_{max} (GHz)	340	390	440	510	560	630	710	820	880
NF_{min} (dB) at 24GHz	2	1.8	1.6	1.4	1.3	1.2	1.1	1	0.9
NF_{min} (dB) at 60GHz	5.1	4.5	4.0	3.6	3.3	3.0	2.7	2.4	2.3

Figure 1.2: RF CMOS ITRS

Historically, pure CMOS technology was very poor in this. By the way, Fig. 1.2 shows the expected CMOS roadmap for future years [5]. It shows that the continuous scaling down of the gate length implies an high enough increase in the peak f_{max} due mainly to a capacitive and resistive parasitics reduction. Starting from 90 nm CMOS, f_{max} higher than 150 GHz are achievable, making this technology usable for application in the range of 60 GHz. Future CMOS evolution, from 45 nm on, shows peak maximum frequencies even higher (e.g 340 GHz for 32 nm gate length), similar to other more expensive technologies, and high enough to be utilized for hundreds of GHz applications like medical imaging.

1.2 Why Millimeter Waves

In the past, millimeter wave frequency range has been used only for military or special medical applications. Therefore the spectrum between 20 GHz and few hundreds of GHz was mainly unlicensed and free, and not crowded as other lower frequency ranges as the GSM/UMTS/WLAN ones. This, and the fast increasing demand for very large bandwidth and higher and higher bit rate wireless applications makes those frequency very valuable.
Moreover, moving to higher frequencies reduces the form factor of

the required antennas as antenna dimensions are inversely proportional to carrier frequency. Therefore, given a fixed area, a single antenna can be replaced by antenna arrays to enhance the gain and the directivity.

1.2.1 Applications

During the last decade a lot of applications have been proposed and investigated for this spectrum.

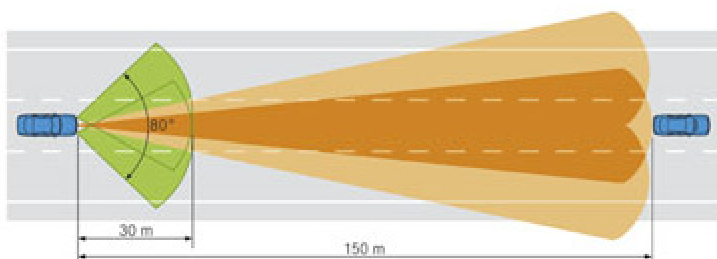


Figure 1.3: Vehicule radar example

In 2002, in order to prevent road accidents due to human errors using *collision warning systems* and automatic vehicle interventions, the FCC committee introduced 7 GHz unlicensed bandwidth around 24 GHz spectrum exclusively for vehicular radar systems (Fig. 1.3).

Considering that the main specifications for such systems are the scanning angle and the capability of precisely determining an object's location and tracking it, a very large signal bandwidth together with a very short wavelength become fundamental.

Figure 1.4: WPAN example

In 2003 the IEEE 802.15.3 working group for Wireless Personal Area Network (WPAN) began investigating the use of 7 GHz of unlicensed spectrum around 60 GHz as an alternate physical layer (PHY) to enable very high speed Internet access, streaming content downloads and wireless data bus for cable replacement (Fig 1.4)[6], targeting a data rate greater than 2 Gb/s. Moreover the peak of oxygen absorption at 60 GHz (Fig 1.5), while eventually precluding communications over distances greater than few kilometers, is very helpful for short-range WPAN (e.g for domestic uses).

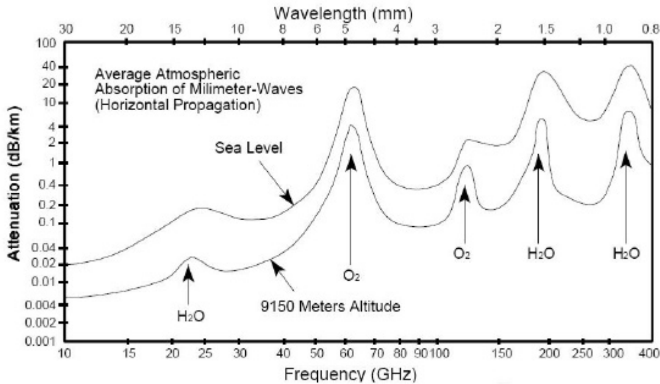


Figure 1.5: Air attenuation

In 2008 the ECMA and WirelessHD groups, developed a standard proposal for a 60 GHz PHY for High Definition uncompressed video wireless transmission (WHDMI) up to 4 Gb/s or compressed 5.1 surround sound audio with 1.5 Mb/s [5].

In the same years a lot of other wide bandwidth applications have been proposed. The 94 GHz spectrum, for example, has been chosen for weapons detection and imaging application (Fig 1.6). Moreover long term projections [5] show a promise for many applications in the areas of medical imaging, spectroscopy and security, in the spectrum from 100 to 1000 GHz.

Figure 1.6: Weapons detection

1.3 Wireless HDMI Proposal

As depicted in the previous section, in 2003 a wide unlicensed bandwidth of 7 GHz was allocated around 60 GHz.

Fig 1.7 shows how these frequencies were allocated all over the world. It can be seen that the allocated frequencies were almost the same everywhere, making future systems possibly compatible everywhere. This was possible because historically those frequencies were almost unused, apart for military and medical applications.
Moreover the high oxygen absorption in this range made it very valuable for indoor short range applications, such as audio and video

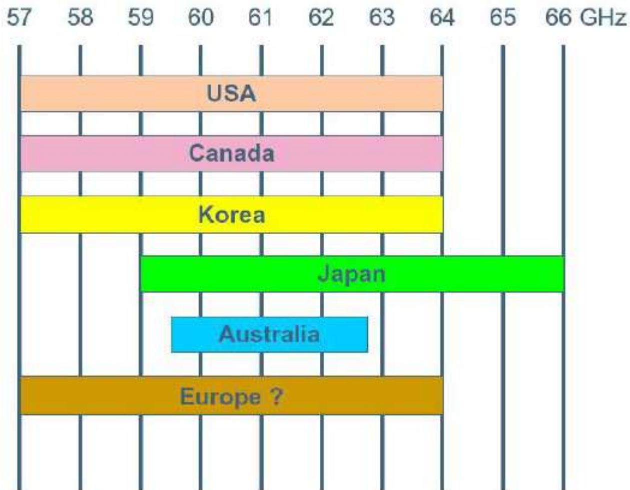


Figure 1.7: World 60 GHz band allocations

downstreaming.
This opened the possibility to realize wireless communication systems with data rates up to several Gb/s and replace systems that up to now were only wire based.

The standard proposal by ECMA and Wireless HD defines a 60 GHz PHY and HDMI PAL for short-range unlicensed communications providing high rate wireless personal area network (including point-to-point), transport for both bulk data transfer and multimedia streaming, addressing usages and applications such as high definition

(uncompressed/lighly compressed) AV streaming, access point wireless docking station and short range sync-to-go [5].
The standard defines three device type, all coexisting and interoperating with each other.

Device Type A offers video streaming and WPAN application in 10 meter range anche it si considered the 'high end - high performance' device.

Device Type B offers video and data applications over shorter range (1-3 meters) point to point. It is considered the 'economy' devices and trade off range and performances in favour of low cost implementation and low power consumption.

Device Type C is positioned to support data only applications at less then 1 meter range. It is considered a 'bottom end' device providing simplest implementation, lowest cost and lowest consumption.

1.3.1 Operating Band Frquencies

This PHY operates in the 57 to 66 GHz frequency band as shown in Fig. 1.8.

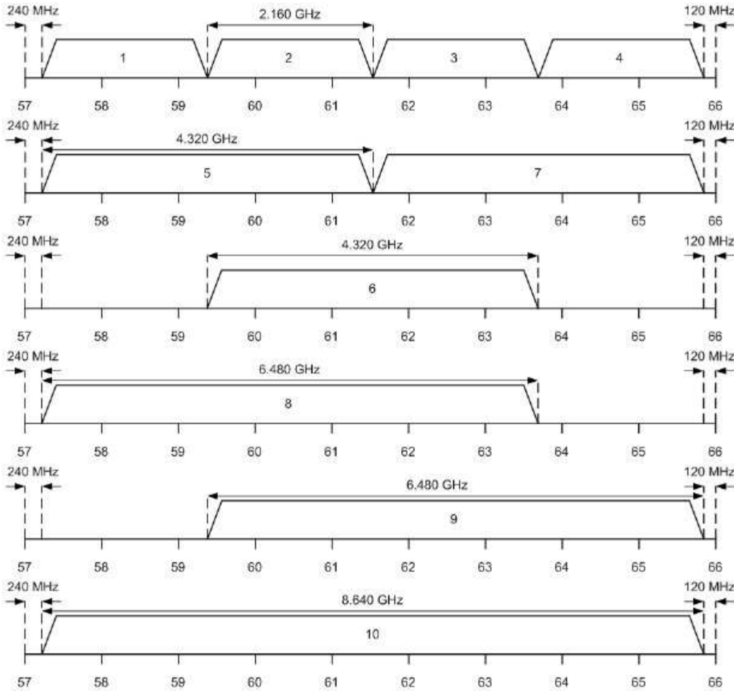


Figure 1.8: Channels numbering

Four frequency channels are defined and used by the all three types, with a frequency separation for these channels of 2.16 GHz. However, as shown in Fig. 1.8 the standard supports bonding of two or three adjacent channel to achieve higher data rates, or the same data rates while using smaller but more efficient constellations. Channel definitions and carriers are reported in Fig. 1.9.

BAND_ID (n_b)	Channel Bonding	Lower Frequency (GHz)	Centre Frequency (GHz)	Upper Frequency (GHz)
1	No	57.240	58.320	59.400
2	No	59.400	60.480	61.560
3	No	61.560	62.640	63.720
4	No	63.720	64.800	65.880
5	Yes (1 & 2)	57.240	59.400	61.560
6	Yes (2 & 3)	59.400	61.560	63.720
7	Yes (3 & 4)	61.560	63.720	65.880
8	Yes (1, 2, & 3)	57.240	60.480	63.720
9	Yes (2, 3, & 4)	59.400	62.640	65.880
10	Yes (1, 2, 3, & 4)	57.240	61.560	65.880

Figure 1.9: Band allocation

1.3.2 Modulation and Bit Rate

The standard proposal provides two possible transmission and reception modes:

- Single Carrier Block Transmission (SCBT)
- Ortogonal Frequency Division Multiplexing (OFDM)

In this work only the OFDM has been considered. There are 3 main operation mode (named A14, A15, A16 in [5]), without channel bonding, depending on the maximum bit rate.
The first two of them work respectively up to 1 and 2 Gb/s with a QPSK modulation, while the third one works up to 4 Gb/s while using a 16QAM modulation scheme.

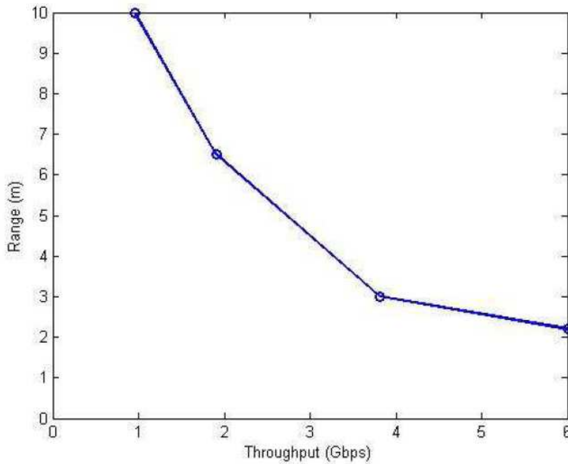


Figure 1.10: Range versus Data Throughput

Fig. 1.10 shows the variation of the maximum transmission range increasing the data throughput.

1.3.3 Error Vector Magnitude

Increasing the data rate of a system increases the probability of receiving a wrong symbol (for a given modulation). The error between the measured symbol and the ideal one is called Error Vector, as depicted in Fig. 1.11 and it is usually characterized by its magnitude (EVM).

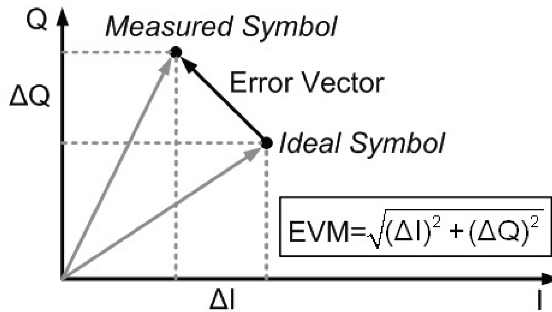


Figure 1.11: Error Vector Magnitude

It can be seen as a sort of noise superimposed to the ideal symbol, so it is naturally affected by all the sources of the receiver that generate imperfections, such as thermal noise, phase noise, I/Q errors and non-linearities of amplifiers.

This means that considering a given Bit Error Rate, higher data rates will demand more stringent EVM as illustrated in Fig. 1.12.

The picture shows the ECMA standard requirements for the EVM from 1 to 4 Gb/s data rate given a bit error rate of 4e-11. It is possible to see that a minimum EVM of about -11 dBm is required for maximum data rate.

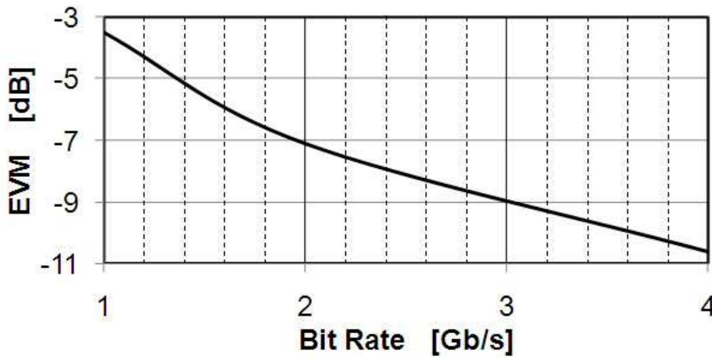


Figure 1.12: EVM versus Bit Rate

1.3.4 Phase Noise

As shown before, Phase Noise (L(f)) is a primary source of EVM degradation.
As illustrated in Eq. 1.1,

$$EVM_{PN} \simeq \sqrt{2\int (L(f)df} \tag{1.1}$$

this degradation is proportional to the square root of the phase noise integral over the wanted bandwidth (Fig. 1.13).

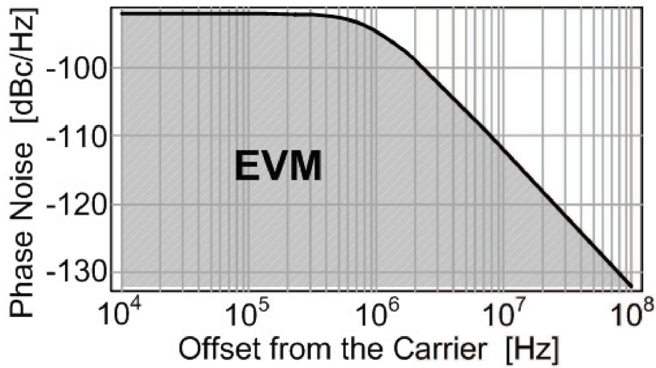


Figure 1.13: EVM due to Phase Noise

Fig. 1.14 shows the relation between the EVM degradation and the required Phase Noise at 10 MHz offset, considering a 1-MHz PLL bandwidth.
It can be seen that considering other transceiver imperfections, a phase noise of -115 dBc/Hz at 10Mhz offset is recommended for a 60 GHz carrier.

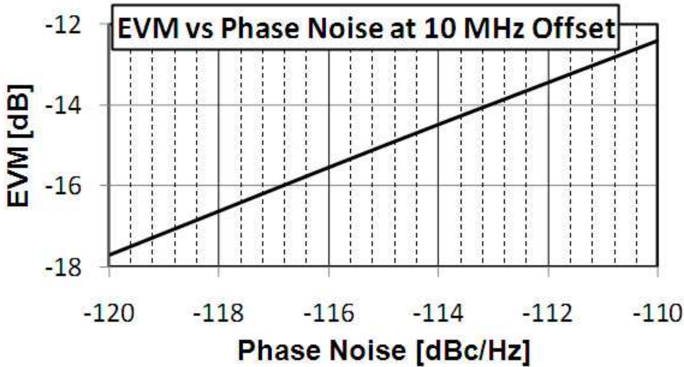


Figure 1.14: EVM degradation versus Phase Noise at 1 MHz PLL bandwidth

1.3.5 Receiver Sensitivity

Because of the losses by the oxygen absorption and the high data rates required, receiver sensitivities are very stringent for this frequencies. They vary with the modulation and the data throughput:

- -60 dBm at 1 Gb/s bit rate
- -50 dBm at 2 Gb/s bit rate
- -50 dBm at 4 Gb/s bit rate

Chapter 2

Circuit Design

Implementing circuits operating near the frequency limits of a given technology requires careful optimization at all levels: device, circuit and system architecture [6].
At a transistor level, a clear understanding of the fundamental limitations of CMOS transistors is necessary to design and layout an optimal device for operation at mm-wave frequencies.
For passives a careful analysis of design methodologies is necessary considering the substrate limitations of a CMOS pure bulk technology.
Moreover at 60 GHz the signal wavelength on silicon is about 2.4mm.
This mean the the circuits can be eventually considered to be lumped,

only if the layout is very compact. This, also, means that at such high frequencies non only capacitive parasitics must be taken into account but also and the inductive ones.

2.1 MOS Transistor at mm-Wave

In order to understand the fundamental limitations of CMOS transistors at such high frequencies, there are some particular parameters that are not usually used at lower frequencies, but are often used in the microwave world. In particular those parameter are the maximum frequency of oscillation (f_{max}), the minimum frequency over which the device is unconditionally stable (f_{crit}), the maximum stable gain (MSG), the maximum available gain (MAG) and the Mason's unilateral function (U)[7].

2.1.1 Maximum Oscillation Frequency

For baseband and digital circuits, the dominant parasitics limiting the performance of CMOS transistors are the capacitors. For this reason the main way to determine the maximum transistor speed for such applications is the f_t, defined as Eq. 2.1:

$$f_t = \frac{g_m}{C_{gs}} \tag{2.1}$$

where g_m is the transconductance gain of the transistor and C_{gs} is the main capacitive contribution of the transistor. This drives the process engineer to optimize technology for highest f_t.

While reducing parasitic capacitors helps high-frequency performances, at mm-wave frequencies resistive losses due to transistor and layout parasitics pay an increasingly important role since they dissipate power that cannot be restored. For this reason at mm-wave it is better to use a different parameter called f_{max} which represents the maximum frequency at which the device remains active. It is determined not only by sizing and bias conditions, but it is also highly dependent on resistive losses due to transistor and layout parasitics.

2.1.2 Minimum Frequency for Unconditional Stability

There are three operation regions for active devices:

- Instable region
- Conditionally stable region
- Unconditionally stable region

In the first one the device starts oscillating for whatever input and output loading conditions. In the second one the device stability is assured only for determined input and output loading impedances, while in the last one the device is unconditionally stable regardless the input and output loading impedances. The operation region depends mainly on the gain of the considered devices and its unilateral behavior.
The frequency over which the device becomes unconditionally stable is called f_{crit}.

2.1.3 Maximum Available Gain

If the device is operating in the unconditionally stable region a Maximum Available Gain (MAG) is defined (Eq. 2.2). MAG is the maximum power gain a device can achieve considering the input and the output matched.

$$MAG = |\frac{S_{21}}{S_{12}}|(K - \sqrt{K^2 - 1}) \tag{2.2}$$

S_{21} and S_{12} are part of the S-parameters of the device and K is the stability parameter (Eq. 2.3).

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{12}|} \tag{2.3}$$

where $Delta$ is defined as (Eq. 2.4):

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{2.4}$$

The parameter $|S_{21}/S_{12}|$ is called Ḟigure of Meritḟor the transistor.
Moreover, the frequency at which the MAG is equal to 0 dB is exactly the f_{max} of the device and determines the frequency at which the device itself ends to be active and begins to work as a passive one.

2.1.4 Maximum Stable Gain

If the device is operating below f_{crit}, and so in the conditionally stable region, a Maximum Stable Gain (MSG) is defined.
It is defined as the maximum available gain when $K = 1$ (Eq. 2.5):

$$MSG = |\frac{S_{21}}{S_{12}}| \tag{2.5}$$

2.1.5 Mason's Unilater Function

Mason's Unilater Function, U is often used as a metric for a two-port device. It represents the maximum power gain that the device can deliver if a lossless reciprocal embedding to unilaterize the device

itself is used [7]. U is also a good metric for characterizing a three terminal device with a common terminal such as a transistor.
It is defined as Eq. 2.6:

$$U = \frac{|k_{21} - k_{12}|^2}{4(\Re(k_{11})\Re(k_{22}) + \Re(k_{12})\Re(k_{21}))} \tag{2.6}$$

where k_{ij} are the two-port Y or Z parameters.
U is invariant to the common terminal, so a common-gate amplifier has the same U as a common-source one. If $U > 0\ dB$ the device is active. If $U < 0\ dB$ the device is passive. The frequency at which $U = 0\ dB$ is the same at which $MAG = 0\ dB$ and it is the f_{max} of the device.

As a comparison all this device gains are plotted in Fig. 2.1. MSG is plotted for low frequencies where $K < 0\ dB$. At breakpoint, K becomes $> 0\ dB$ and the device is unconditionally stable and thus MAG is plotted. Note that the U curve is always larger than MAG but both curves cross 0 dB together. At this point the device becomes passive.

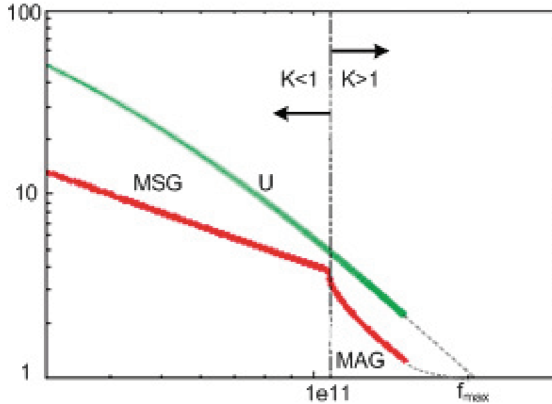


Figure 2.1: MSG, MAG and U function for an active device

2.2 Transistor Design at mm-Wave

The parameters described in the previous section are very important because they give an idea of the potential of a technology. Moreover they depend not only on technology parameters, but they are also very layout dependent. So it becomes very important the way transistors are designed end laid out in order to maximize the working frequency (f_{max}) and the available gain.

Theoretically f_{max} is independent of the numbers of fingers of a multifinger transistor, as long as the device dimensions are much smaller than a wavelength [6]. Therefore it is sufficient to be concerned only

with the optimal layout for a single finger of a multifinger transistor. As mentioned before f_{max} is mainly limited by resistive losses of the transistor itself and the main contributors are the gate resistance (R_G), the source/drain resistances (R_S, R_D), and the resistive substrate network.

2.2.1 Gate Resistance

Gate resistance is the main resistive contributor in MOS transistor using polysilicon gates. It has three main resistance contributions.

The first one is given by the ohmic gate resistance (R_{ohmic}). In modern CMOS technology gates are realized with heavily doped polysilicon, whose conductivity is in the order of few ohm/square. This gives an ohmic gate resistance between the gate contact and the effective gate at the channel interface, and considering the distributed nature of the charge in the channel can be modeled as in Eq. 2.7 when the gate is contacted on both sides [8], [9]:

$$R_{ohmic} \simeq \frac{1}{12}\frac{W}{L}R_{poly\square} \tag{2.7}$$

where W is the total width, L is the gate length and $R_{poly\square}$ is the sheet resistance of polysilicon gate.

The second term of the total resistance comes from the gate contacts themselves (R_{gcont}). Since contact lateral dimensions are scaling down with the lithography, higher contact resistance is expected (Eq. 2.8):

$$R_{gcont} = \frac{R_{cont}}{N_{cont}} \tag{2.8}$$

where N_{cont} is the number of contacts in parallel. This resistance can be considered in series with the total gate capacitance, given by the channel and the overlap ones.

The latter part of the total resistance seen from the gate comes from *Non Quasi Static* (NQS) effects [9] and it is associated only with the channel capacitance. In the quasi static model normally used to derive MOSFET equation in books and simulators, the channel charge, both depletion and inversion, is assumed to be in equilibrium with the gate capacitance at every time. This hypothesis directly leads to the representation of the gate capacitance with no series resistance. However in a real MOS transistor the channel responds to the gate voltage variation in a finite amount of time, resulting in a finite time constant (hence a finite resistance and a finite Q) to a gate voltage variation. This delay can be modeled with a bias-dependent

gate resistance, as proposed by [8] that can be modeled as Eq. 2.9

$$R_{NQS} = \frac{1}{12}\frac{L}{W}R_{NQS\square} \qquad (2.9)$$

In the case of a transistor in triode mode and in strong inversion it can be modeled as Eq. 2.10:

$$R_{NQS} = \frac{1}{12}\frac{V_{ds}}{I_{ds}} \qquad (2.10)$$

In the case of $V_{ds} = 0$, being R_{on} the so called ON resistance at $V_{ds} = 0$ it becomes Eq. 2.11:

$$R_{NQS} = \frac{1}{12}R_{on} \qquad (2.11)$$

It is quite clear that the global gate resistance is a function of the gate length (L), width (W) and the number of fingers (N_F) used to layout the device. As first approximation it can be assumed that for a fixed width, the finger length is proportional to $1/N_F$ while the number of contact is proportional to N_F. Considering the total width of a MOS transistor as $W = N_F W_F$, where W_F is the finger width, the NQS resistance is mainly proportional to $L/(W/N_F) = N_F \cdot L/W$, hence for N_F finger in parallel to L/W. This means that this resistance, differently from the previous one, does not depend on the

layout for fixed W and L.

The total resistance seen from the gate is therefore (Eq. 2.13):

$$R_G = R_{ohmic} + R_{gcont} + R_{NQS} \tag{2.12}$$

$$R_G \simeq \frac{1}{N_F}\left(\frac{1}{12}R_{poly\square}\frac{W_F}{L} + \frac{R_{cont}}{N_{cont}N_F}\right) + \frac{1}{12}R_{NQS\square}\frac{L}{W} \tag{2.13}$$

and is a function of N_F, W_F and L (assuming a fixed W). It can be seen that assuming a fixed total W, R_G decreases increasing the number of fingers as soon as the latter term is not dominant. Given the technology parameters an optimum value for L can be found in order to minimize the total resistance. Anyway, minimizing the resistance *must not* be confuse with maximizing the quality factor of a transistor. Infact in order to increase the Q of a transistor itself, the product $C_G \cdot R_G$ must be minimized (where C_G is the total gate capacitance). So, considering that in inversion region C_G is mainly proportional to L, a minimum L is required.

2.2.2 f_{max} Optimization

Usually in CMOS technology gate resistance cannot be neglected with respect to source/drain resistances and the substrate one. How-

ever, by using narrow finger widths, the effect of the gate resistance can be made small compared to the other parasitic resistors. Moreover, using narrow fingers, the substrate contacts can be placed very close to the device minimizing substrate losses [6].

W_F $[\mu m]$	I_{ds}/W_{tot} $[mA/\mu m]$	f_t $[GHz]$	f_{max} $[GHz]$
5	70	127	71
3.33	70	127	97
2.5	70	127	117
2	70	127	132
1.25	70	127	159
1	70	127	168
0.5	70	127	179

Table 2.1: f_t and f_{max} for a $W_{tot} = 20\mu m$ common source NMOS

This means that reducing the finger width of a transistor, the maximum operating frequency (f_{max}) of the transistor will increase significantly. Table 2.1 shows the f_{max} and f_t for a 20 μm total width transistor with minimum channel length at fixed current density varying the finger width.

It can be noticed that, while the f_t is invariant considering a finger width variation (for a fixed current density), f_{max} depends

strongly to this variation, and can be much larger or smaller than f_t itself. Thus, for an optimal layout for mm-wave applications CMOS transistors have to be designed using a lot of very narrow fingers.

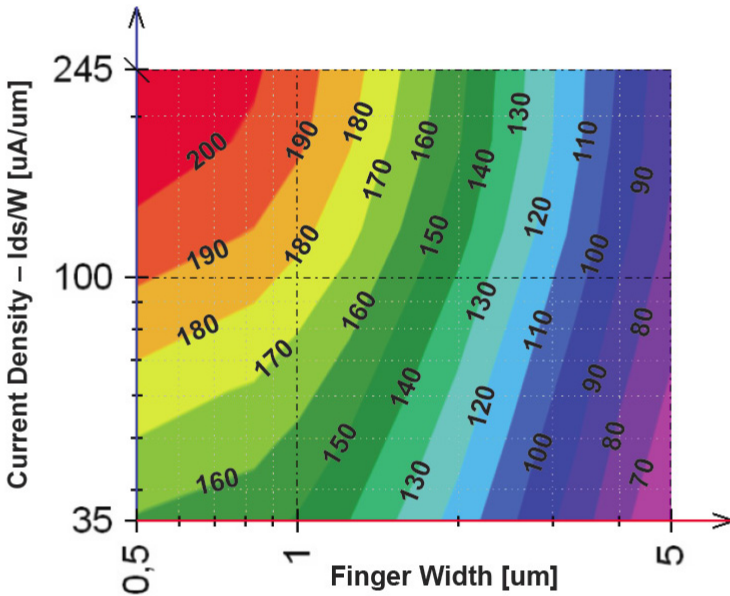


Figure 2.2: f_{max} versus W_F and current density for $W_{tot} = 20\mu m$

Fig. 2.2 shows simulated f_{max} for a common source 65nm N-channel MOS (NMOS) transistor with minimum channel length as a function of the finger width and bias current density. Varying the current density it is possible to reach f_{max} of about 200 GHz.

Furthermore, it can be noticed that the f_{max} increase is linear with the finger width, but tends to saturate for W_F values lower than $1\mu m$. Infact, as explained before, there is a limit after which the gate resistance becomes negligible with respect to all the other resistive parasitics, making the f_{max} almost invariable to further reduction of the finger width itself.

2.2.3 Gain Optimization

As for the gain, a direct and obvious consequence of the f_{max} variation due to different finger width values is the variation of the gain itself. The gain improves reducing the finger width. By the way, this causes also a variation in frequency of the stability factor K (§ 1.1.3) and f_{crit}.

As shown in Fig. 2.3, infact, reducing the finger width determines an increase in the intrinsic gain of the device but makes it potentially more unstable. Decreasing the finger width infact increases the frequency at which the device becomes unconditionally stable.

From Fig. 2.3 it is possible to notice that in order to have significant gain at 60 GHz for a common source device a finger width of $1\mu m$ or less is recommended.

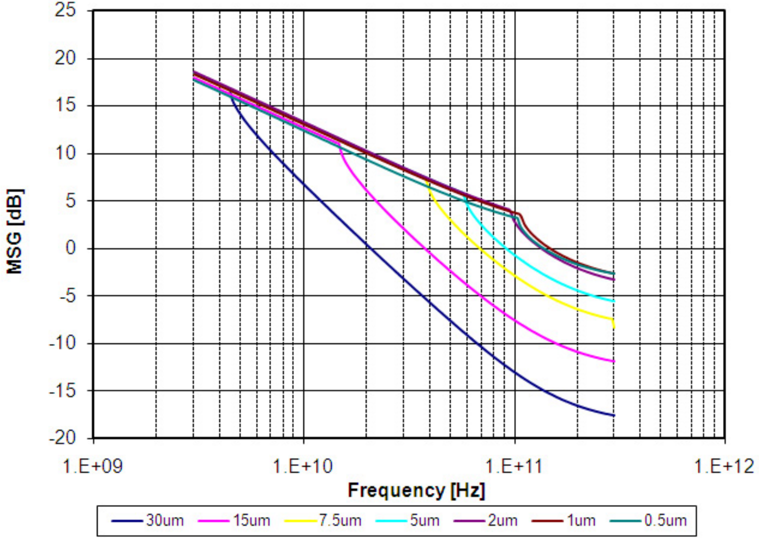


Figure 2.3: Power Gain vs Finger Width (Total Width $30\mu m$)

Moreover from the zoom in Fig. 2.4 it can be noticed, that reducing the finger width more than $1\mu m$ is not necessarily a good solution because the device seems to become more unstable again.

2.2.4 Cascode Topology

Intuitively, more a device is unilateral more it is unconditionally stable over a wider range of frequency. Moreover because of the

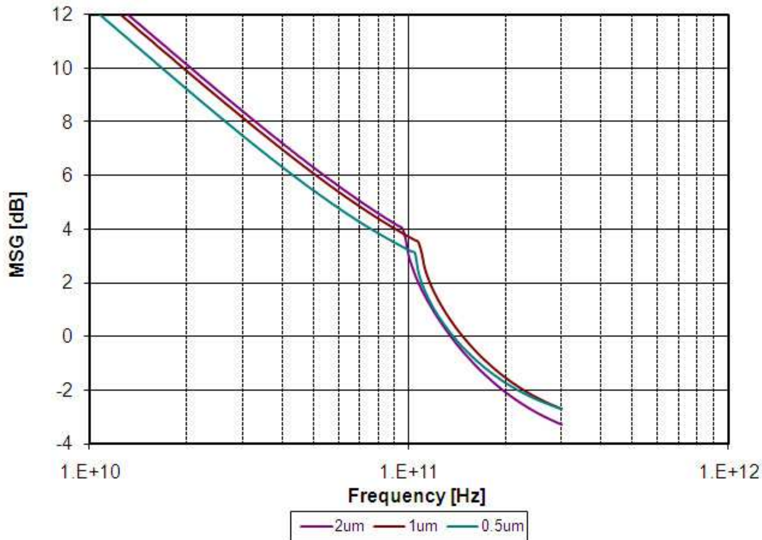


Figure 2.4: Power Gain vs Finger Width (Total Width 30μm) - Zoom

better stability of the device itself even the maximum stable gain obtainable in the conditionally stable region increases. A good solution to make a common source device more unilateral is to cascode it with a common gate stage (cascode topology).

As shown in Fig. 2.5 the MSG increase considerably in the cascode topology, and even if the device becomes unconditionally stable at a lower frequency with respect to the common source one, the

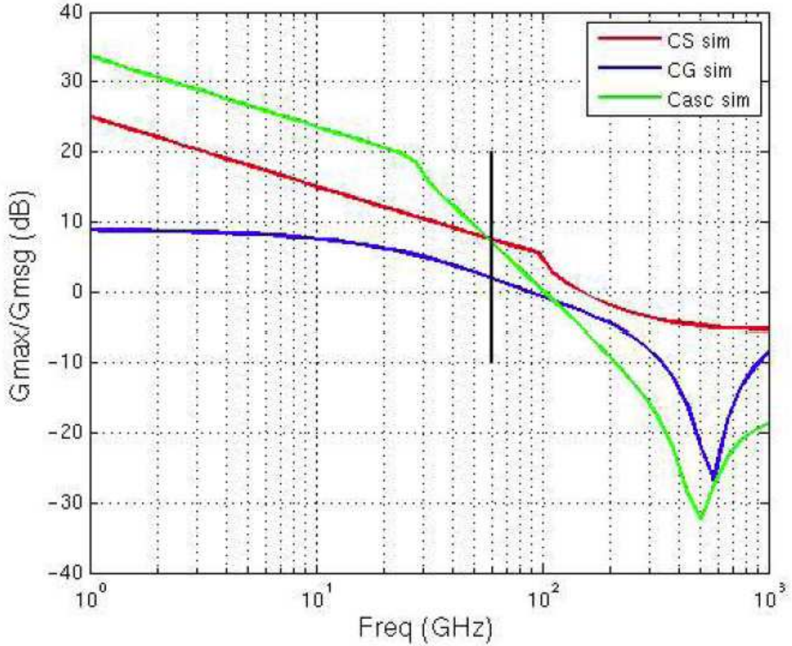


Figure 2.5: Cascode vs Common Source (CS) and Common Gate (CG)

gain at 60 GHz remains almost the same. For this reason it could be a good solution to use cascode topologies because they achieve almost the same performance of common source stages, but being unconditionally stable.

In order to minimize the parasitic capacitances a *Shared Junc-*

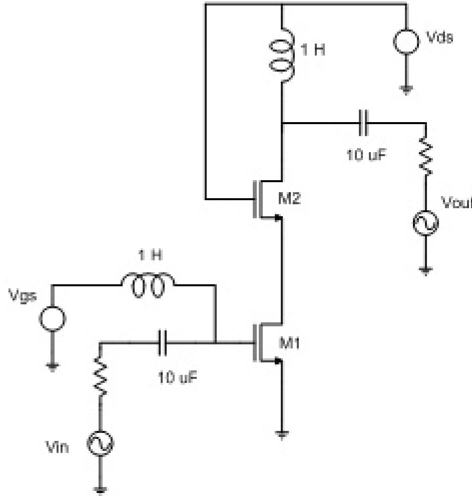


Figure 2.6: Shared Junction cascode schematic

tion layout has been investigated. Referring to Fig. 2.6 the *Shared Junction* consists in the removal of the metallization of the shared diffusions between the drain of transistor M1 and the source of transistor M2. In this way it is possible to reduce the shared diffusion sizes to the minimum allowed by the Design Rule Manual (DRM) reducing the diffusion intrinsic capacitance.

Fig. 2.7 shows the *Shared Junction* basic layout.

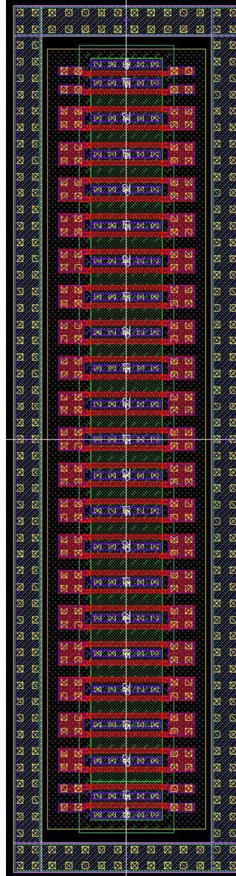


Figure 2.7: Shared Junction basic layout

2.2.5 Inductively Degenerated Topology

According to transfer function of the circuit, the transconductance gain of the degenerated stage is lower then the common source

one, because of the lower Q given by the higher real part. On the other end, a noiseless input real part allows for noise figure lower than 3 dB. However it must be observed that, while at RF frequencies the maximum available gain is high and few dB of gain losses due to the degeneration can be tolerated, this does not apply to millimeter wave frequencies, where every fraction of dB must be carefully considered. Moreover the inductance needed for the degeneration at these frequencies is in the order of some tens of pH and therefore not easily controllable and extremely sensitive to parasitic.

Chapter 3

MOS Validation

In order to validate the theory expressed in the previous chapter and to validate CMOS technology for such high frequencies a test chip has been integrated using a 65 nm CMOS technology. Main objective of this test chip was not to produce new circuits but to develop the basic components (active and passives) and design skills needed for the design at 60 GHz. In this thesis only the active devices will be considered. The devices integrated in the test chip are mainly pad and de-embedding structure, common source, common gate, cascode and inductively degenerated topology MOS trasistors. Moreover 9 different cascode NMOS transistors have been integrated with different width and finger number, while the common source topology

has been investigated regarding both N-channel and P-channel MOS. Fig. 3.1 shows a snapshot of the test-chip layout.

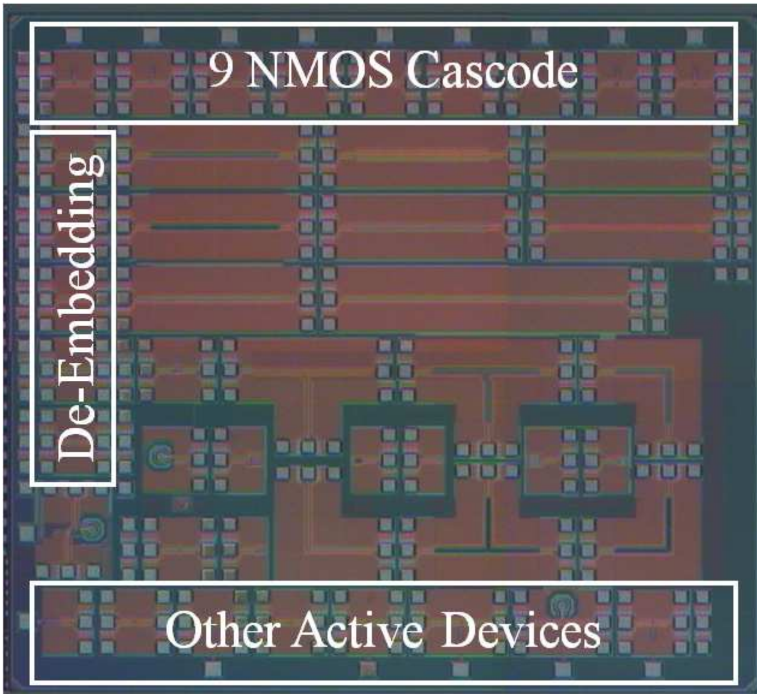


Figure 3.1: Test Chip Photomicrograph

3.1 Pad and De-embedding Structures

To allow Ground-Signal-Ground (GSG) probing, custom GSG pad have been designed. Access line from the pad to the 50 Ohm transmission line has been designed to provide a 50 Ohm impedance path to the signal from the probe to the device under test (DUT). Pad top view is shown in Fig. 3.2 To reduce the parasitic capacitance of the signal pad, only the two top metal layers have been used.

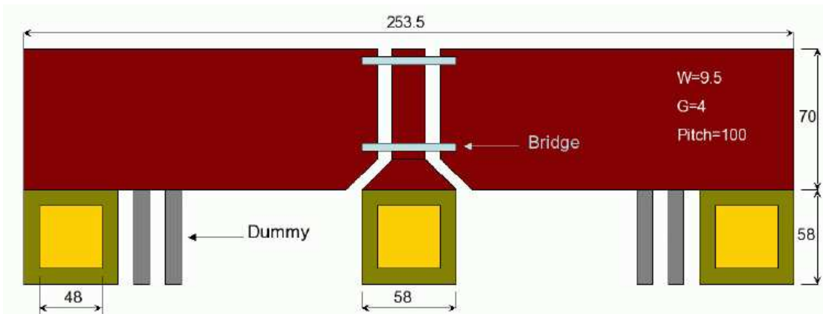


Figure 3.2: GSG Pad - Top View

To allow pad and access line de-embedding a completed set of pad structures providing short, open and thru needed to estimate the scattering parameters of the pads and access lines themselves. Three main de-embedding methods have been used and compared to better characterize the pads:

- Thru
- Open/Short
- Cascade Open/Short/Thru

3.2 NMOS Cascode Stages

Nine different cascode devices have been integrated in the test chip using the *Shared Junction* layout described in the previous chapter. The schematic used is the same as in Fig. 2.6, where transistors M1 and M2 have the same dimensions. Table 3.1 shows the sizes of the 9 different cascode stages.

W_{tot} $[\mu m]$	L $[\mu m]$	$\sharp$ $Fingers$	$Finger\ Width$ $[\mu m]$
10	0.06	20/10/5	0.5/1/2
20	0.06	20/10/5	0.5/1/2
40	0.06	20/10/5	0.5/1/2

Table 3.1: *Shared Junction* MOS sizes

A big effort has been done to optimize the layout of the cascode devices in order to minimize eventual feedback parasitic capacitances to make the device unconditionally stable over a wider frequency range. Figure 3.3 shows the degradation of the power gain frequency

due to parasitic feedback capacitances.

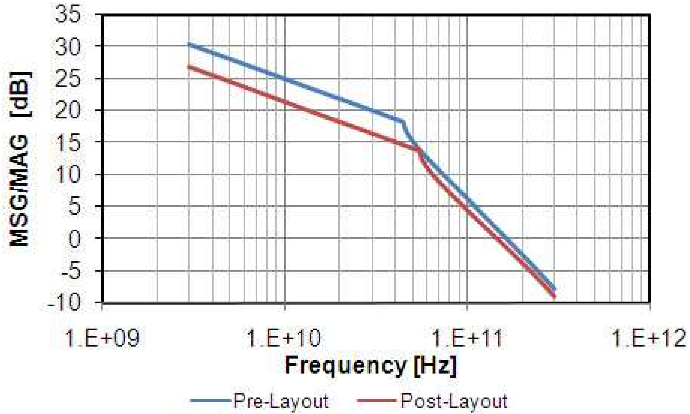


Figure 3.3: MSG/MAG degratation due to layout parasitics

Another important aspect is to maintain fixed the gate voltage of the cascaded transistor, otherwise it will cause a bandwidth degradation. For this reason it is fundamental to capacitively filter that node. Furthermore, in order to avoid oscillations due to this filtering capacitances and inductive parasitic (most likely at high frequency) a resistor is needed. So the schematic and the layout used to bias the gate of cascode device are shown in Fig. 3.4. Fig. 3.5 shows the complete layout of one of the shared junction device.

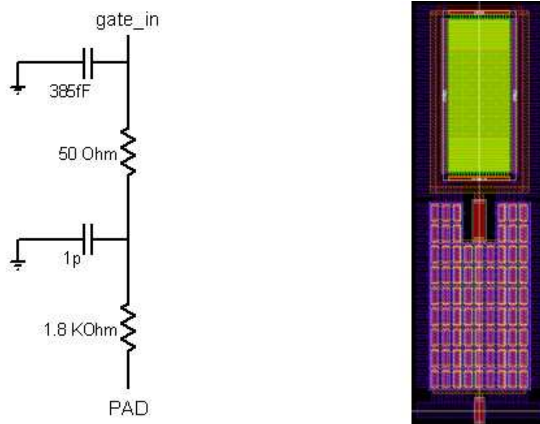


Figure 3.4: Gate Bias

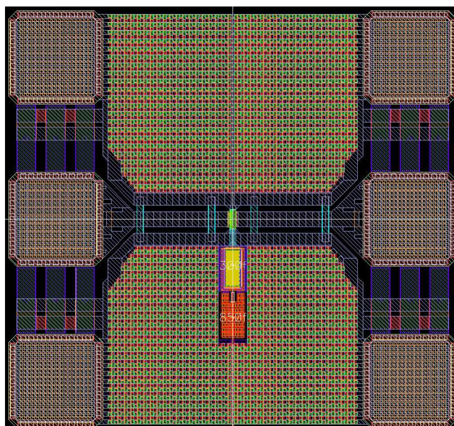


Figure 3.5: Shared Junction Cascode Top Level

Those 9 cascode devices have been measured and characterized. They were probed using Cascade 60 GHz probes and a 65 GHz VNA to measure device S-parameters. Fig. 3.6 shows power gain results for the 20μm total width cascode using a finger width of 1μm.

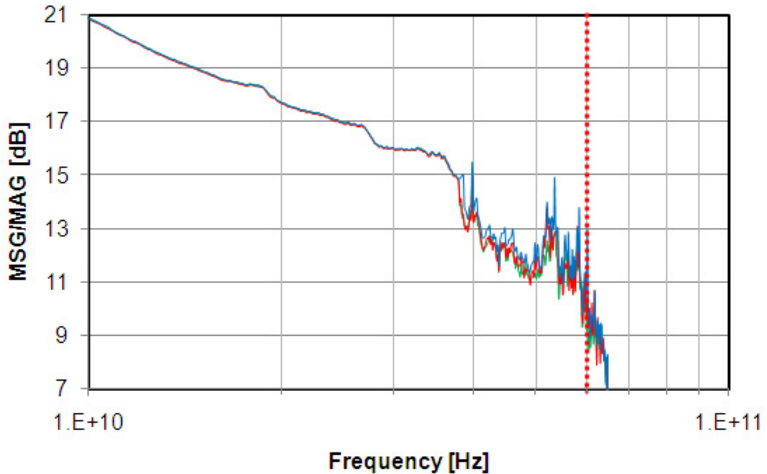


Figure 3.6: Measured MSG/MAG for $W_{tot} = 20\mu m$ and $W_F = 1\mu m$

Due to instruments limitation, measurements are quite noisy at very high frequency, but extrapolating the curve from 40 GHz a measured unconditionally stable power gain (MAG) of about 9 dB has been measured. This is pretty close to the simulations shown previously in Fig. 3.3. The picture shows quite well also the transition

from the conditionally stable region and the unconditionally stable one.

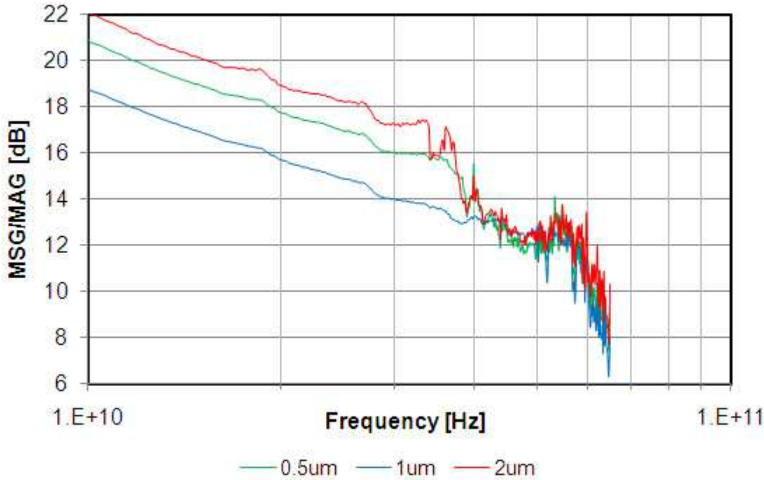


Figure 3.7: Measured MSG/MAG for $W_{tot} = 20\mu m$ and different W_F

Fig. 3.7, moreover, compares the measurements results obtained using the same total width of $20\mu m$ but changing the finger width. The picture shows measurements for finger width of $0.5, 1$ and $2\mu m$. It can be noticed the difference in stability between a W_F of 1 or 2 μm, while there is no big difference between 0.5 and 1. That is why has been preferred to choose $1\mu m$ as the best trade off.

Finally Fig. 3.8 shows different results for different biasing of the input transistor. The best performance has been obtained using a V_{gs} of about 0.8 V.

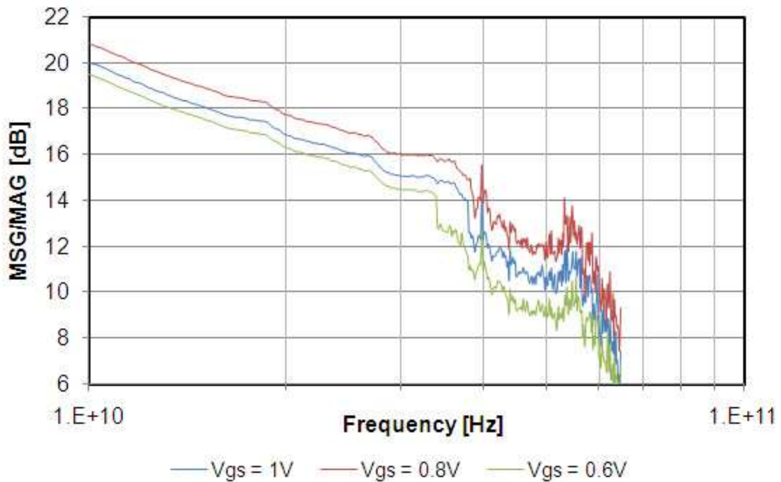


Figure 3.8: Measured MSG/MAG for $W_{tot} = 20\mu m$ and $W_F = 1\mu m$ for different bias

3.3 Common Source Stage

As described previously, common source structures have been investigated, both N-channel and P-channel MOS. A fixed size of

$20\mu m/0.065\mu m$ with 20 fingers has been used. A bias of $V_{gs} = 0.8V$, $V_{ds} = 1.2V$ (negative for PMOS) has been chosen in order to maximize the transconductance. A current density of $0.33mA/\mu m$ is achieved.

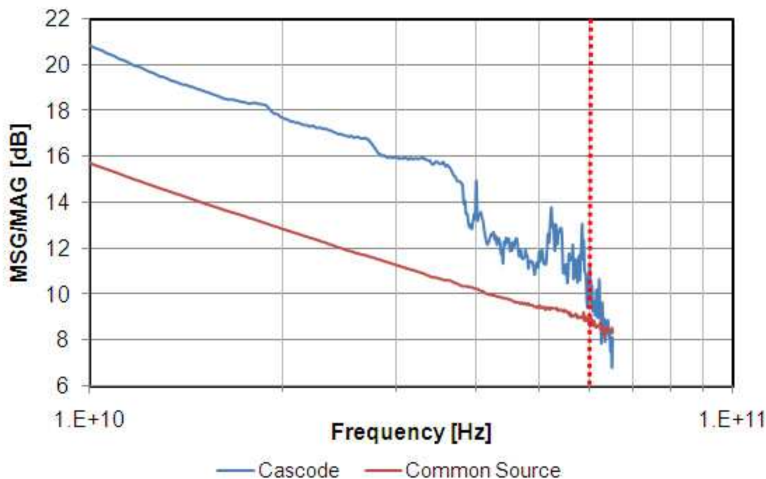


Figure 3.9: Measured MSG/MAG for $W_{tot} = 20\mu m$ and $W_F = 1\mu m$ for different bias

To minimize the gate resistance, short gate fingers have been used, contacted on both sides with a double row of contacts. According to simulations, further finger width reduction does not have great benefit on the f_{max} of the transistor, while increases the average length of the routing reducing the available space for contacts

on source and drain diffusions. Fig. 3.9 shows the measured result compared to the equivalent cascode structure. It can be noted that the common source structure is more conditionally stable than the cascode one as predicted by the simulations, while the power gain at 60 GHz is more or less similar (about 9 dB). This is in very strong agreement with the simulations depicted in Fig. 2.5 and recommends to use cascode structure instead of common source, because they present the same power gain but the first one is unconditionally stable.

Chapter 4

Frequency Generation

Frequency generation is one of the most critical point at millimeter wave. As described in Chapter 1, frequency requirements for application at 60 GHz are very stringent. A very large tuning range is needed together with a low phase noise, while keeping the power consumption low.
For this reason the first step is to understand the real potential of CMOS bulk technology regarding frequency generation at such high frequencies. In particular considering a Phase Locked Loop (PLL) the most critical block are the Voltage Controlled Oscillator (VCO) and the Dividers. These blocks are the only two in a PLL that are required to work at maximum frequency.

This chapter will describe firstly the design and the realization of a 54 GHz VCO in 65 nm CMOS technology. Then it will investigate the best solution to realize dividers at millimeter wave.

4.1 54 GHz VCO

Over the past five years, the maximum operating frequency of VCOs fabricated in silicon technology has almost quadrupled from 25.9 to 117.2 GHz [10]. Push-push VCOs using the second harmonic operating at 63 to 131 GHz [ref KKO] have also been demonstrated. However, among these, the bulk CMOS fundamental VCOs operating around or above 50 GHz usually show poor phase noise, limited frequency range or large power consumption [10].
Moreover, benefit from node scaling is expected due to the increase of the f_{max} of the devices and to the improved variable capacitor quality factor (Q) and the reduced capacitive parasitics. At such high frequencies, infact, while the Q of the inductors slightly increases, the Q of varactors and capacitors in general decreases a lot, making the latter the biggest responsible for Q degradation at millimeter wave.
For this reason the design of VCOs for mm-wave applications in 65 nm CMOS has been investigated. In particular, an Inversion Mode

Metal-Oxide-Semiconductor structure (I-MOS) is employed to realize the voltage controlled variable capacitor [1]. In a N-MOS VCO topology, infact, it allows exploiting the complete Capacitance-Voltage (C-V) characteristic (compared to Accumulation Mode varactors (A-MOS) [4].

4.1.1 Inversion Mode MOS Varactor

The cross-section of an Inversion Mode N-MOS variable capacitor is shown in Fig. 4.1

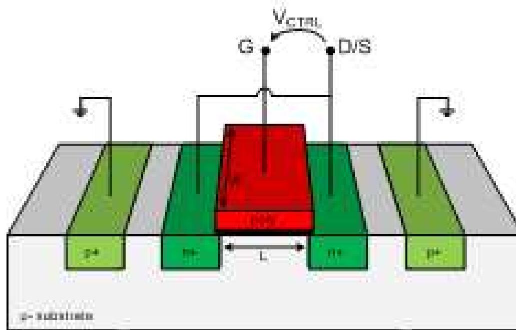


Figure 4.1: Cross-section of an Inversion Mode N-MOS variable capacitor

A Metal-Oxide-Semiconductor structure is opened on the p substrate, with two $n+$ diffusions providing the minority carriers when

the surface layer is inverted. The contacts (D/S) to the $n+$ diffusions are tied together and the capacitor is controlled by the voltage applied between Gate (G) and D/S (V_{CTRL})[11].

The inversion mode variable capacitor, realized as a transistor with shorted Drain and Source, is first available in newly developed processes. On the contrary, Silicon Foundries tend to develop the accumulation mode varactor only later on. Both the alternatives benefit from device scaling.

Moreover, as it will be shown, an I-MOS VCO, employing N-MOS cross-coupled pairs, allows full exploitation of the C-V varactor characteristic while both controlling terminals are kept within the voltage range allowed by the technology. For these reasons an I-MOS varactor has been employed in this work, even though the A-MOS alternative, in the same technology, is attractive, eventually showing a better tuning range - Q trade off [4].

The operation of the I-MOS varactor is as follows. Let us assume the gate voltage is at the maximum available voltage, i.e. the supply voltage Vdd, while the S/D terminal is used as control terminal (V_{tune}) and the bulk is grounded. As it will be clearer in the next section, this is the actual varactor operating condition. When V_{CTRL} equals Vdd, the channel is strongly inverted and the capacitance is mainly the oxide capacitance $C_{ox} \cdot W \cdot L$.

Increasing the control voltage toward Vdd determines a threshold

increase, due to the body effect, together with a reduction of the overdrive voltage and the channel charge tends to vanish. When the control voltage reaches $Vdd - Vth$ the channel inversion charge is roughly zero and the region under the gate oxide is depleted. The capacitance seen from the gate is hence given by the series of the gate oxide and the depletion oxide capacitances, the latter being smaller than the former. Note that, because the gate-bulk voltage is always positive, this configuration does not allow the device to operate in accumulation mode, resulting in a strictly monotonic C-V characteristic.

However, this simple model does not take into account the overlap capacitance that, in modern CMOS technologies, is not a negligible fraction of the oxide capacitance. For minimum length devices, the overlap capacitance is greater that the depletion one and represents the minimum varactor capacitance.

As depicted before, the main limit of tank Q at mm-wave frequencies is the varactor Q. For this reason, maximizing varactor Q is key. In inversion, the surface layer presents a resistance proportional to R_{on}, i.e. the device small signal triode resistance (§ 2.2.1).

Because R_{on} is directly proportional to the channel length L, the quality factor increases as $1/L^2$, highlighting the remarkable quality factor increase when selecting minimum length devices. The finite conductivity of the poly-silicon gate determines a further series re-

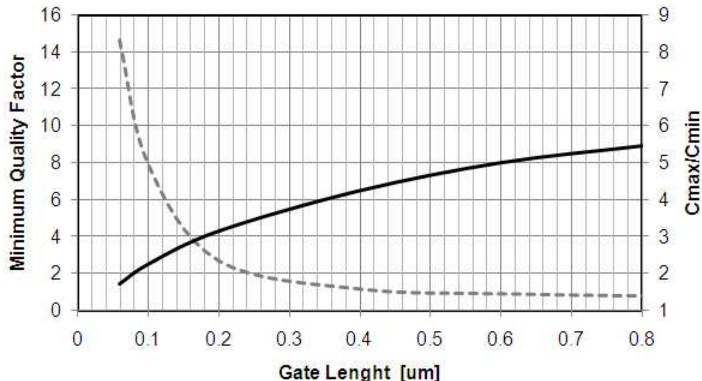


Figure 4.2: Minimum Q (dotted line) and C_{max}/C_{min} ratio as a function of gate length at 60 GHz

sistive component. Usually the device is made up of several small width fingers laid out in parallel, in order to reduce the gate resistance. On the other end, the fixed parasitics increase with reducing finger width, thus reducing the achievable tuning range. $W_F = 1\mu m$ has been chosen as a compromise, eve though with this choice the gate resistance is estimated the main resistive component, actually limiting the achievable Q.

Fig. 4.2 shows the simulated minimum Q and C_{max}/C_{min} ratio of varactors of $W_{tot} = 20\mu m$ with varying gate lengths at 60 GHz. The minimum Q decreases a lot with an increase in the gate length,

while the tuning ratio increases. It can be noted that in order to achieve a Q high enough at 60 GHz, minimum length is required. At such L the C_{max}/C_{min} ratio results to be about 1.8, enough by the way for the requirements of the standard proposal about tuning range. Moreover, since it is impossible to increase the length of the devices, a vary careful layout has to be done in order to reduce as much as possible capacitive parasitics.

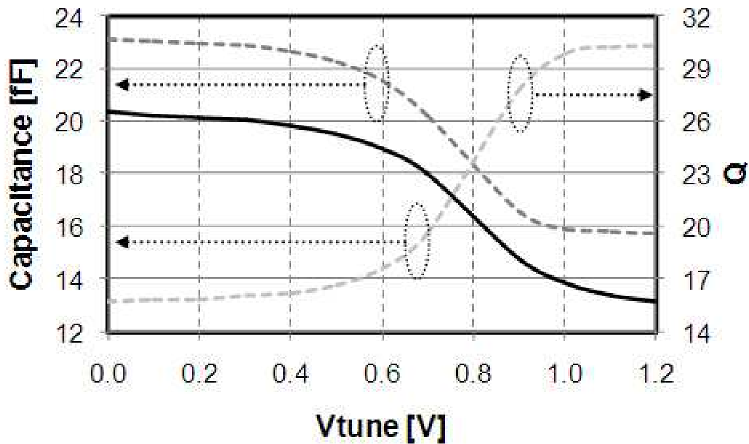


Figure 4.3: Measured C-V characteristic (continuous line) and simulated C-V and Q (dotted lines)

A stand alone version of the varactor component has been inte-

grated for characterization. Fig. 4.3 shows the simulated and measured C-V characteristic, for a varactor structure, with 15 finger of 1μm width and minimum length. The slight difference between measured and simulated capacitance is attributed to the limited resolution of the de-embedding procedure. The minimum capacitance value is 13.5 fF, maximum 20.4 fF, resulting in a tuning range of about 21%. The quality factor is simulated only because a direct measurement does not provide results accurate enough.

4.1.2 VCO Design

A N-MOS cross-couple pair VCO topology has been then investigated and integrated. The schematic is reported in Fig. 4.4.

In order to maximize the frequency tuning range, the tank capacitance should be maximized for given oscillation frequency. On the other end, a proportional smaller inductance does penalize the oscillation amplitude, for given biasing current, and as a consequence the phase noise.

The fixed total tank capacitance comprises inductor, cross-coupled pair and buffer parasitics plus minimum varactor capacitance. The actual choice of varactor range, and as a consequence varactor size, requires few design iterations. Because transistor plus inductor parasitics are in the order of 40 fF, a varactor capacitance range of 70

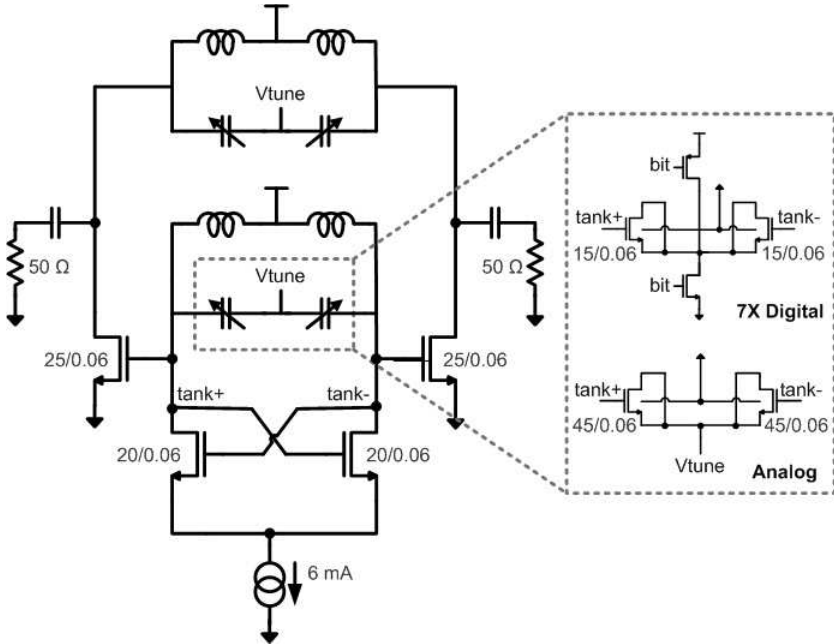


Figure 4.4: VCO and buffer schematic. The in-let shows the varactors architecture

fF to 105 fF has been selected, determining a 70 pH inductance for a 60 GHz oscillation frequency. A remarkable frequency tuning range in excess of 10% is expected, while a current of few mA allows an oscillation amplitude around 650 mV (0-peak) differential and a state of art phase noise figure of merit, due to the tank high quality factor.

Because the I-MOS C-V characteristic is steep, the varactor is

made up of 7 device units in parallel, digitally controlled by 3 bit lines and 1 device unit for analog control, as show in the in-set of Fig. 4.4.

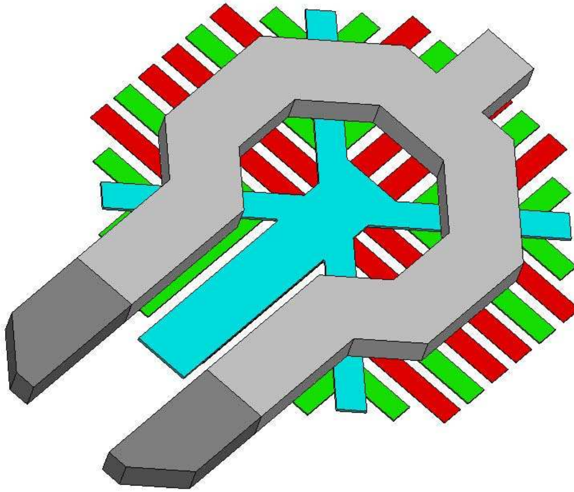


Figure 4.5: 70 pH inductor

The combination of digital and analog tuning results in a lower VCO gain, for the same covered frequency range, with benefit to supply noise rejection and minimization of AM to PM noise conversion.

The inductor has been laid out as a differential octagonal one turn inductor with a center tap (Fig. 4.5). The metal width is 12μm and the total length, including the metal taper to the varactor (that have to be considered at such high frequency), is 218 μm. Simulations,

performed by means of Agilent Momentum©, provide Q of about 15 at 60 GHz (Fig. 4.6).

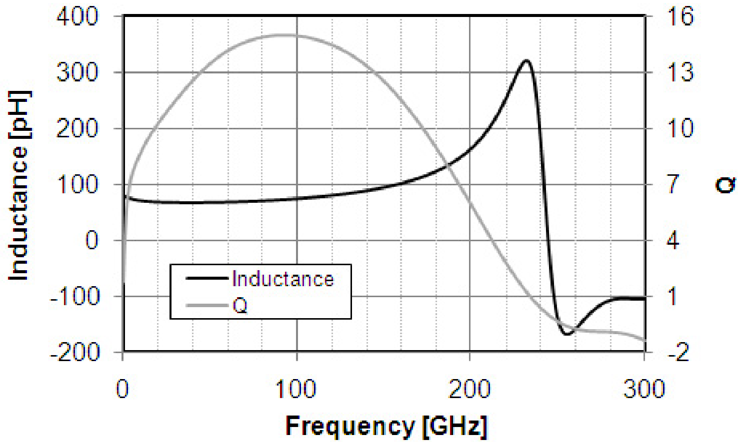


Figure 4.6: 70 pH inductor

Fig. 4.7 shows the complete layout of the VCO.

4.1.3 Measurement Results

The VCO of Fig. 4.4 has been implemented using a 65 nm CMOS process from STMicroelectronics. Output buffers, employing a resonant load network, identical to the tank network for optimum matching, are integrated to drive the instrument low impedance. The chip occupies 475 X 485 μm^2 including bond pads. Despite the VCO

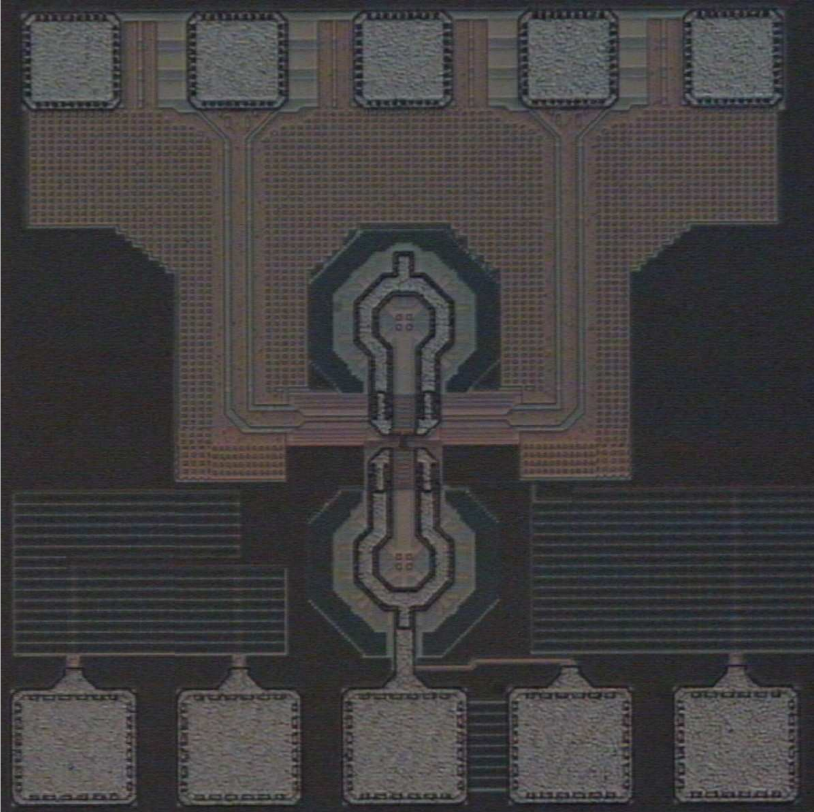


Figure 4.7: 54 GHz VCO Photomicrograph

has been designed to be measured differentially with Ground Signal Ground Signal Ground (GSGSG) probes, it has been measured single ended on-wafer using Cascade Infinity GSG RF probes with 100 μm

pitch operating up to 67 GHz. A Rohde & Schwarz FSU Spectrum Analyzer up to 67 GHz has been used.

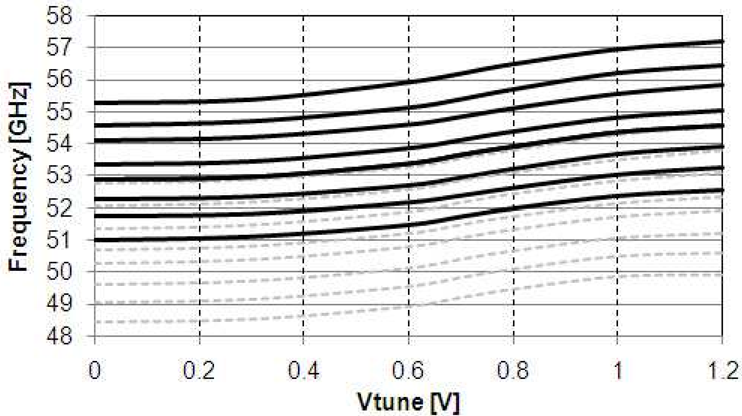


Figure 4.8: Measured (continuous line) and simulated (dotted lines) oscillation frequency vs control voltage

Fig. 4.8 shows the measured oscillation frequency versus control voltage. The frequency range covers 51 GHz to 57.2 GHz, i.e. 11.5% around the 54 GHz center frequency. The center frequency differs from the target of 60 GHz because no post-layout simulations, including inductor S-parameter description from Momentum©, were done before chip submission because of limits in our CAD set-up.

However, simulations done later on show a good agreement with measurements, as shown in Fig. 4.8.

Measurements to determine the current for oscillation start-up versus control voltage have been performed to estimate the actual tank Q. Fig. 4.9 shows the results.

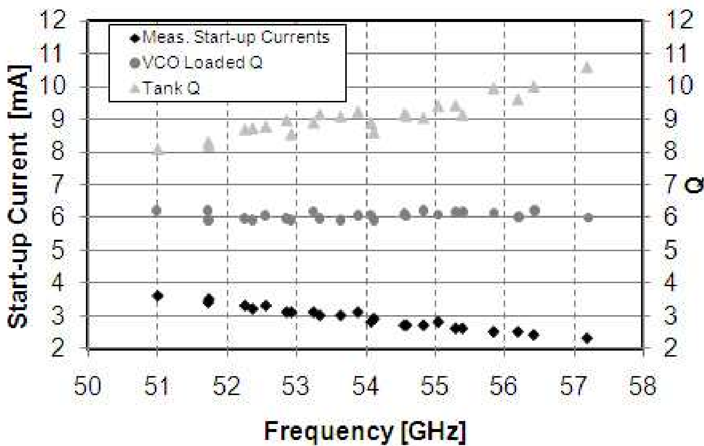


Figure 4.9: Measured start-up currents and Q vs frequency

The loaded quality factor, obtained from simulations as the tank loaded Q causing oscillation at the measured current is rather flat because both cross-coupled and buffer devices limit tank Q when the I-MOS is in depletion. This is more evident from tank Q curve, where the effect of loading devices is de-embedded. Moreover, the tank Q is in good agreement with varactor Q simulation of Fig. 4.3 considering the simulated inductor Q is around 15, as shown in Fig. 4.6.

Phase noise (PN) measurements have been performed at a nominal current of 6 mA, while supply voltage is set to 1.2 V.

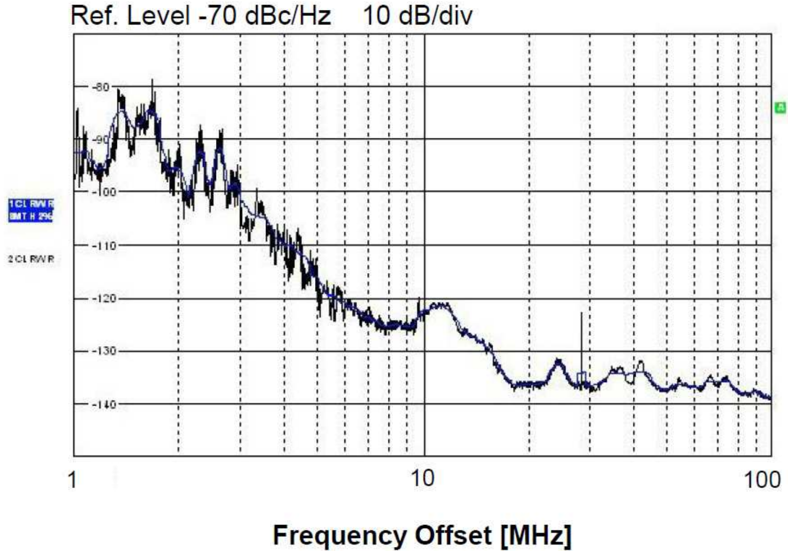


Figure 4.10: Measured Phase Noise at the lowest frequency (51 GHz)

Fig. 4.10 shows the measured phase noise when the oscillation frequency is minimum, i.e. 51 GHz. Beyond 20 MHz offset, the noise level is determined by instrument noise floor and the curve flattens. On the contrary, for offsets lower than few MHz the measured value it is not reliable because the VCO phase noise has been measured in free running mode. At 10 MHz offset the minimum phase noise

is -122 dBc/Hz, resulting in a noise FOM of -187.6 dBc/Hz and a FOM_T of -188.7 dBc/Hz. FOM and FOM_T are defined as in Eq. 4.1 and Eq. 4.2 [12].

$$FOM = PN - 20\ log(\frac{f_{osc}}{\Delta f}) + 10\ log(\frac{P_{diss}}{1mW}) \tag{4.1}$$

$$FOM_T = PN - 20\ log(\frac{f_{osc}}{\Delta f} \cdot \frac{FTR}{10}) + 10\ log(\frac{P_{diss}}{1mW}) \tag{4.2}$$

where Δf is the frequency offset from the carrier (f_{osc}) and FTR is the Frequency Tuning Range.

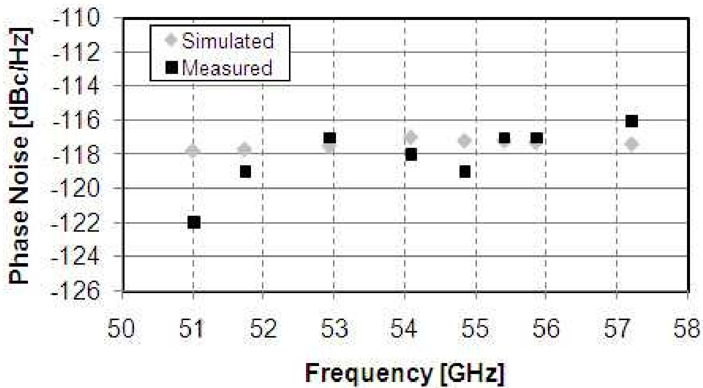


Figure 4.11: Measured and simulated Phase Noise at 10 MHz offset vs frequency

Phase noise measurements have been performed at various frequency. The detected values at 10 MHz offset are reported in Fig. 4.11 and compared to simulations.

Table 4.1 reports a comparison with the state of art oscillators and VCOs in the same frequency range (at the date the VCO was fabricated). The proposed solution shows the best noise FOM *and* tuning range among VCOs employing lumped tank [13], based on a standing wave oscillator, has a wider tuning range but 3 times the area.

This work proves that ultra scaled nodes, together with a careful design (varactor in particular), provide frequency references for mm-wave application, with high spectral purity, low area and robust, i.e. adjustable against spread due to process variations.

4.2 Frequency Dividers

There are many different topologies in order to implement frequency dividers. But not everyone is suitable for millimeter wave application [14]. The principal topologies are:

- Static Source-Coupled Logic (SCL) divider
- Dynamic CMOS divider

Section	This Work	[12]	[10]	[13]
Technology [nm]	CMOS 65	CMOS 65 SOI	CMOS 130	CMOS 180
Technique	MOS - VAR	MOS - VAR	MOS - VAR	Standing Wave
Central Frequency [GHz]	54	70.2	56.5	40
Tuning Range [%]	11.5	9.55	9.8	20
PN @ 10 MHz [dBc/Hz]	-118	-106.4	-108	-100.2 @ 1MHz
Power [mW]	7.2 @ 1.2V	5.4 @ 1.2V	9.8 @ 1.5V	27 @ 1.5V
FOM [dBc/Hz]	-184	-175.7	-175	-177.9
FOM_T [dBc/Hz]	-185.2	-175.3	-174.5	-183.9
Area (with pads) [mm^2]	0.23	N.A.	0.24	0.625

Table 4.1: VCOs State of Art

- True Single Phase Clock (TSPC) divider
- Miller divider
- Injection-Locked Frequency (ILFD) divider
- PLL-Based divider

The first three categories, based on flip-flop digital logic, cannot work at very high frequencies. In particular, TSPC dividers cannot work at frequencies higher than 10 - 12 GHz, while SCL ones can go up to 20 - 24 GHz (for 65 nm CMOS technology). Miller's dividers and ILFDs are, on the contrary, suitable for mm-wave applications, but they present a higher power consumption and a lower locking bandwidth. The basic idea, then, is to implement the first dividing block of a mm-wave PLL dividing chain as ILFDs or Miller's dividers (because they need to work at maximum speed) while realizing the rest of the chain with SCL, dynamic CMOS or TSPC dividers.

A *static SCL* divider is based on a digital flip-flop based logic. The divide by two operation is obtained by connecting two D latches, the master and the slave. The clock frequency is divided by two connecting the inverted outputs of the slave latch to the master ones. The maximum operating frequency of such a divider is technology dependent, and is determined by the pole generated by the output capacitance of the pre-amplifier and the resistance loading the first

stage itself. There is so a trade off between the bandwidth and the gain of the pre-amplifier limiting the frequency performances of this kind of divider. Operating frequencies of 20 - 24 GHz can be obtained with a current consumption of few mA.

TSPC dividers are based on a domino dynamic logic, while using only one clock phase (classic dynamic CMOS dividers require two clock phases). The principal benefit of a TSPC divider is the power efficiency (few hundreds of μA) but as for the dynamic CMOS dividers they suffer from capacitive loads and so they are limited to 10-20 GHz of input frequency. However, they can be used for the last block of the dividing chain because their power consumption is negligible with respect to the rest or the circuit.

4.2.1 Miller's Dividers

This topology has been introduced in 1939 by Miller. As shown in Fig. 4.12 it is based on a feedback that multiplies together the output and the input frequencies. The signal so generated is then filtered. Under certain conditions of phase and amplitude, the only spectral component self-sustained is at $\omega_{in}/2$.

In Fig. 4.13 is shown the schematic that realizes this kind of

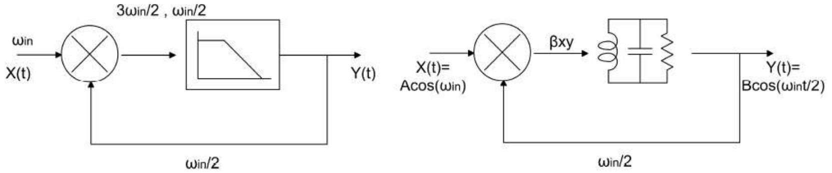


Figure 4.12: Miller's divide by two block diagram with lowpass and bandpass filter

divider. [15] describes that in order to let the oscillation start at half of the input frequency, the amplitude A of the input sinusoid must respect the condition in Eq. 4.3 [15]:

$$A \geq \frac{2}{\beta}\sqrt{1+(\frac{Q\Delta\omega}{\omega_n})^2} \tag{4.3}$$

where β is the conversion gain of the mixer, Q the factor of merit of the RLC filter and ω_n the central frequency of the tank itself.

Moreover, the locking-range for this kind of divider is (Eq. 4.4)[15]:

$$\Delta\omega \approx \frac{\omega_n}{Q}(\frac{2}{\pi}g_m R) \tag{4.4}$$

where g_m is the transconductance of the differential pair with sources grounded and R is the parallel resistance of the tank.

The Miller's divider, that is similar to the injection locked dividers, presents a very good locking range. At low frequencies simulations show that it works pretty well, but, at millimeter wave fre-

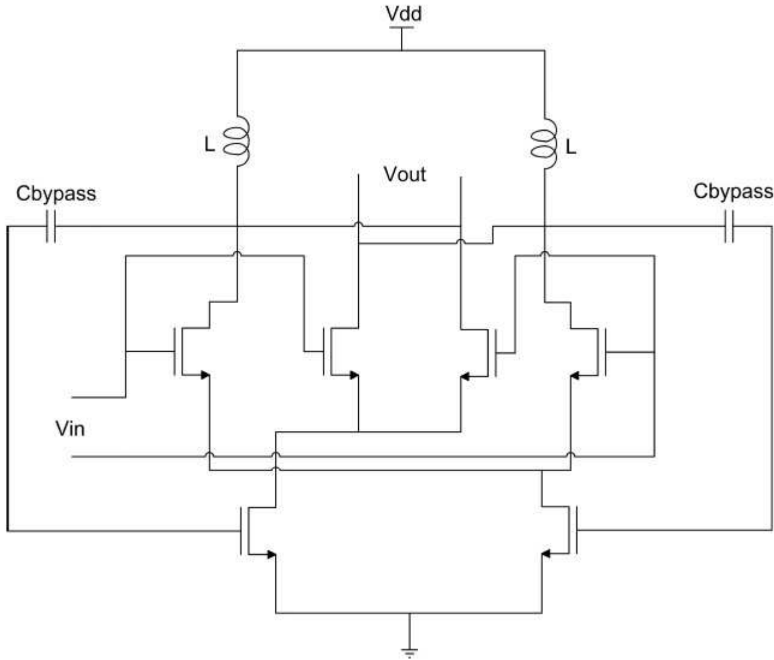


Figure 4.13: Miller's divide by two block schematic

quencies it has some limits. Increasing the input frequency, the loop gain decreases because of the pole generated by the parasitic capacitance of the drain of the differential pair with sources grounded. This node is not resonated out, so as a consequence, at 60 GHz the oscillation at $\omega_{in}/2$ is no more self-sustained, making this kind of divider not very suitable for millimeter wave applications.

4.2.2 Injection Locked Dividers

Consider now the Injection Locked divider (ILFD). The schematic of a classic ILFD is reported in Fig. 4.14.

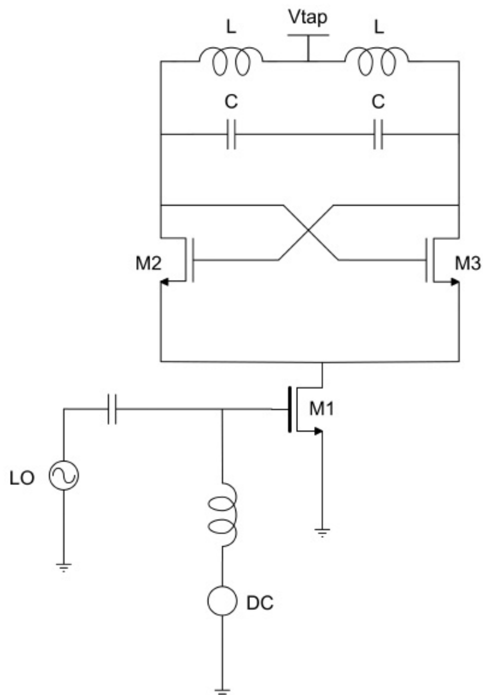


Figure 4.14: Injection Locked divide by two schematic

In this case the signal is injected into the gate of the current generator that bias the LC oscillator. The LC tank resonates at half of the input injected frequency. For this kind of divider the locking range is set to (Eq. 4.5) [16]:

$$\Delta\omega \approx \frac{2\omega_0}{3Q}\eta \tag{4.5}$$

where ω_0 is the carrier, and η is the ratio between the injected current and the dc current. It can be noted that the locking-range is then directly proportional to the injection efficiency and inversely proportional to the factor of merit. As a consequence at mm-wave frequency it is very important to resonate out the parasitic at the source of the cross-coupled pairs in order to enhance the current injection.

Moreover, the oscillation amplitude in the locking bandwidth is given by (Eq. 4.6) [16]:

$$V_0 = Z_0\frac{4}{\pi}I_{DC}[1 + \frac{\eta}{3}cos(2\phi)] \tag{4.6}$$

where ϕ is the phase shift between the input and the output signal.

This kind of injection locked divider, although working at very high frequency, presents low performance in locking range because of the poor injection efficiency. Moreover simulations [14] show that this kind of ILFD is not able to cover the bandwidth required by 60

GHz applications.

For this reason a new solution has been investigated [14]. It is illustrated in Fig. 4.15. In this case the signal is directly injected into the tank using both a P-MOS and an N-MOS [17]. Although it is not strictly symmetrical, in this way it is possible to drive the divider differentially.

An accurate mathematical analysis of this circuit [14] determined that in this case the locking-range is given by (Eq. 4.7):

$$\Delta\omega \approx \frac{\beta V_{in}}{4C} \tag{4.7}$$

where β for a MOS transistor is defined as (Eq. 4.8):

$$\beta = \mu \, C_{ox} \frac{W}{L} \tag{4.8}$$

and C is the total capacitance of the tank (including the injecting transistors).

It can be noted that the locking bandwidth is no more explicitly dependent on the Q of the tank (as it was in the previous one). Moreover the locking range is inversely proportional to the total tank capacitance. As a consequence reducing as much as possible the capacitive tank (an so increasing the inductance value) it is possible to maximize the locking-range itself.

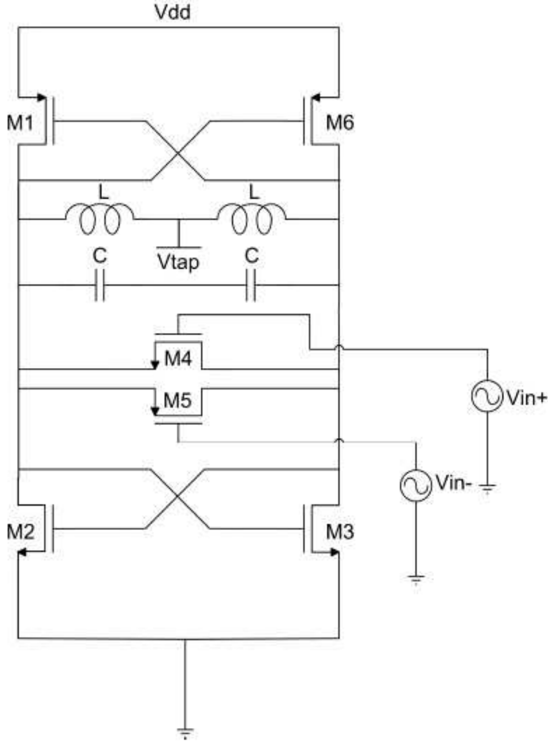


Figure 4.15: Injection Locked divide by two schematic with direct injection on the tank

Furthermore, the peak output oscillation amplitude is given by (Eq. 4.9)[14]:

$$V_{out} \propto \sqrt{I_{DC}} \tag{4.9}$$

This means that the output amplitude mainly depends on the squared root of the bias current.

Moreover, two more main aspects have to be considered and studied in an injection locked divider. The first one concerns the sensi-

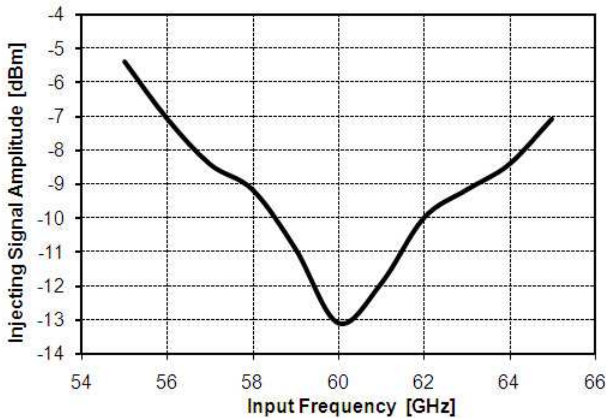


Figure 4.16: Sensitivity of a Direct Injected ILFD

tivity of the ILFD that means the minimum input signal amplitude needed to lock the ILFD itself. This sets the minimum output amplitude of the VCO driving the divider, that at millimeter wave frequencies can be critical. Fig. 4.16 shows the sensitivity required for a p-n ILFD. It can be noted that to correctly lock the divider across the entire bandwidth of [3] an input amplitude $<$ -5 dBm is required.

This is a reasonable value for VCOs operating at millimeter wave, making the sensitivity not particularly critical.

The second one regards the divider output signal amplitude across the locking bandwidth. As shown in Fig. 4.17 near the limits of the locking area, the output signal amplitude decreases a lot, making the divider itself unable to drive properly the following stages (PFDs or Mixers, depending on the applications). This sets an *effective* locking range that is smaller than the total one achievable, and that is mainly determined by the minimum input amplitude required by the following stages.

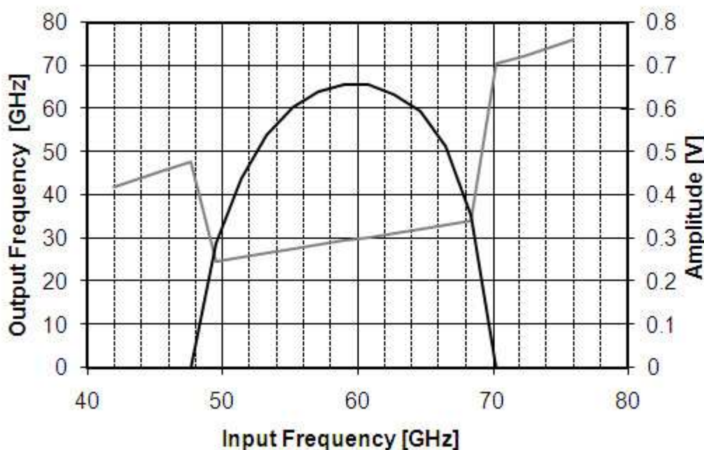


Figure 4.17: ILFD locking range and output signal amplitude

Post-layout simulations show that this kind of divider can obtain a locking range higher than 25% around 60 GHz while consuming about 6 mW at 1.2 V supply (for a 65 nm CMOS technology) and considering a minimum ILFD output amplitude of 400 mV (0-peak, differential) as already shown in Fig. 4.17.

This means that this kind of divider, compared to the other topologies, is pretty suitable for millimeter wave applications because it is able to cover the entire bandwidth of the W-HDMI standard proposal [14] while keeping the power consumption low.

Chapter 5

Receiver Front-End

In the previous chapters the possibility of using bulk CMOS technology to realize both gain stages and frequency generation blocks has been demonstrated.

In order to fulfil the stringent requirements about the Wireless HDMI applications described in Chapter 1, a careful analysis leading to the choice of the best architecture to realize a complete integrated receiver front-end is necessary.

The main aspects that have to be considered are performances, power consumption and layout feasibility.

5.1 Direct Conversion

The easier architecture is the *direct conversion.* As shown in Fig. 5.1, it downconverts the 60 GHz signal directly to baseband using only a couple of I and Q mixers. The frequency generation is then made using only one Phase Locked Loop (PLL), and then a VCO, working at 60 GHz.

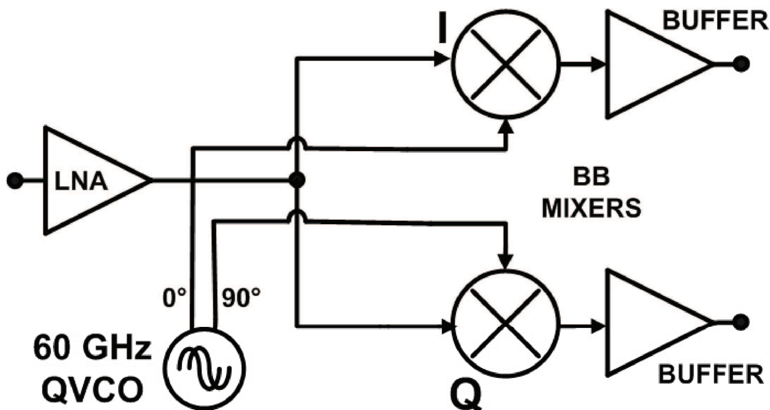


Figure 5.1: Direct Conversion Block Diagram

Unfortunately, this kind of architecture needs to generate the desired tuning range and quadrature directly at 60 GHz, making prohibitive the power consumption requirements to ensure low enough phase noise. State of art 60 GHz PLL, infact, reports a phase noise

of about -95 dBc/Hz at 10 MHz offset [18], almost 20 dB higher than the requirements expressed in § 1.3.4.

Moreover, because the VCO is working at 60 GHz, and considering (as discussed in the previous chapter) that SCL dividers work only up to 20 GHz, two stages of Injection Locked divider are needed in order to close the PLL. This means 2 more inductors to be laid out, as the ILFD has a resonant load. This, together with the 4 inductors needed for the frequency generation (I and Q VCOs and relative resonant buffers), means that a total of 6 inductors has to be laid out just considering the frequency generation. This makes the layout very complicated.

5.2 Sliding IF

In order to avoid these problems, a *Sliding IF* conversion architecture has been investigated. As shown in Fig. 5.2 it is based on a first down-conversion to 1/3 the received frequency, followed by a quadrature down-conversion to DC. In particular, a quadrature oscillator around 20 GHz provides I and Q signals for second step conversion while a second harmonic is extracted and amplified in order to drive the RF mixer. Therefore, although the double conversion, only 1 PLL is needed operating at 20 GHz. This relaxes a lot the power

consumption requirements to achieve the wanted phase noise, tuning range and quadrature.

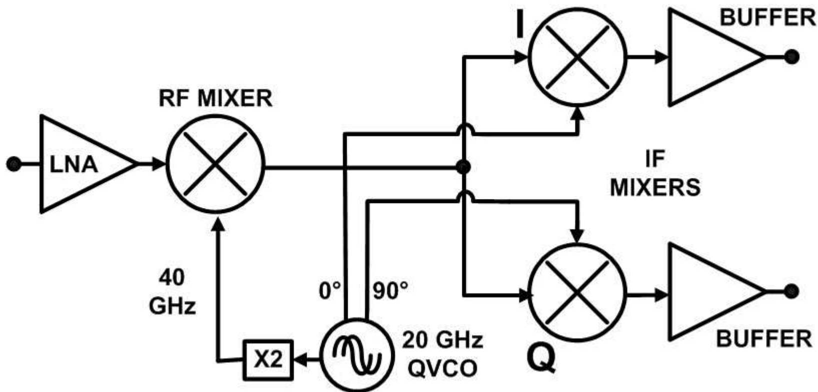


Figure 5.2: Sliding IF Conversion Block Diagram

As a consequence, no Injection-Locked dividers are required. This means that in this case only 5 inductors are needed. One for the differential RF mixer and 4 for the frequency generation (as it will be shown later).

The proposed sliding IF solution employs a 20 GHz quadrature VCO, meeting the required phase noise with 12.5% tuning range and a limited power consumption of 36 mW.

5.2.1 Receiver Chain

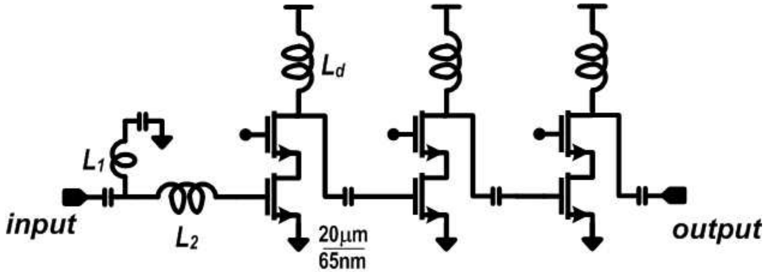


Figure 5.3: Simplified schematic of the LNA

The Low Noise Amplifier (LNA) (shown in details in Fig. 5.3) adopts three stages to achieve 16 dB gain, enough to suppress noise of the following processing blocks. Each stage uses a cascode structure. As described in §2.2.4, common source and common gate devices have equal size allowing a *shared junction* inter-digitized layout to minimize stray capacitance at the common node, responsible for gain and noise degradation. Devices are biased at an optimum current density of 225 μA/μm for maximum f_t.

The network made of L_1 and L_2 matches the input to 50 Ω, while there is no 50 Ω interstage matching, but inductive loads (L_d) resonate out device parasitics in each stage for maximum gain. The last stage, furthermore, directly drives the transconductor of the first mixer.

Transmission lines (T-lines), as well as spirals, are viable to implement inductors at millimeter waves. While the latter allow a more compact layout, we opted for T-lines making the design faster and more reliable, due to the accurate model both for forward and return current signal path. In the LNA, infact, this problem becomes very important due to the single ended topology of the circuit itself.

Once decided to bias all transistors at their optimum current density, the final sizes of the transistors themselves were chosen according to noise analysis.

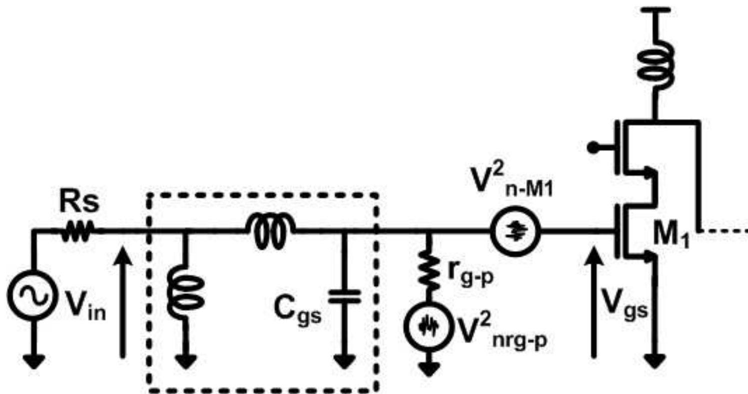


Figure 5.4: Simplified schematic of the first stage of the LNA

Consider first the input stage, schematically represented in Fig. 5.4. As in all receiver a 50 Ω input matching is required. The gate resistance, here represented as its parallel equivalent r_{g-p}, is so trans-

formed to 50 Ω by the matching network and sets a lower bound to the noise figure of 3 dB.

Then the second main contributor to the noise figure is the noise of transistor M_1. Due to the matching network gain ,A_M (Eq. 5.1):

$$A_M = \frac{V_{gs}}{V_{in}} = \sqrt{\frac{r_{g-p}}{R_S}} \tag{5.1}$$

the input referred noise power spectral density due to M1 channel thermal noise results (Eq. 5.3):

$$V^2_{n-in,M1} = \frac{4kT\gamma}{g_{m1}} \frac{1}{A^2_M} = \frac{4kT\gamma}{g_{m1}} \frac{R_s}{r_{g-p}} \tag{5.2}$$

At optimum current density, and once fixed the finger width of the transistors, that means once fixed the resistance of the single gate, g_m and the total gate resistance exhibit opposite dependance on the total device width, making the input stage ultimately independent of the device dimensions. This holds true even when considering a lossy matching network, although the overall noise figure increases.

Considering the second stage, shown in Fig. 5.5, the input referred noise from this stage is derived as (Eq. **??**):

$$V^2_{n-in,M2} = \frac{4kT\gamma}{g_{m2}} \frac{1}{A^2_M \cdot g^2_{m1} \cdot R^2_p} \tag{5.3}$$

where R_p is the total parallel resistance loading the first stage at resonance. The first stage voltage gain develops on an LC load, where

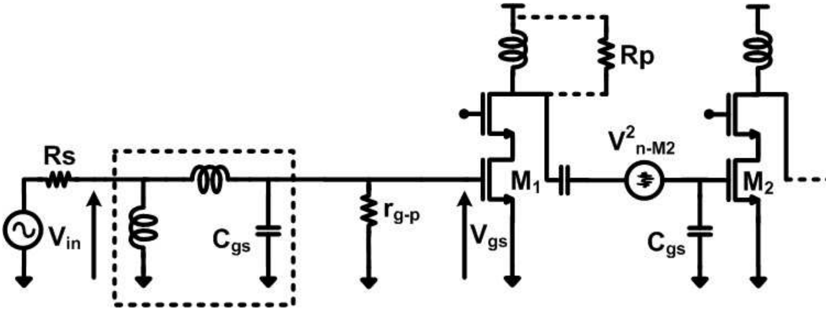


Figure 5.5: Simplified schematic of the second stage of the LNA

the second stage input capacitance is the dominant fraction, thus reducing with W. As a consequence, the inductance and parallel resistance increase, and so does the first stage voltage gain. Equivalent input noise voltage of the second stage, so, improves reducing its width. The minimum value is set by fixed parasitics, mainly due to interconnections.

In order, then, to save current in the first stage, while reducing the noise contribution of the second one, we have selected a relatively small gate width of 20 μm in both stages. The third stage is finally introduced to achieve the targeted 16 dB gain and it is designed following the same rationale.

The RF mixer, shown in Fig. 5.6, presents a double balanced Gilbert Cell topology to assure best LO suppression. The RF trans-

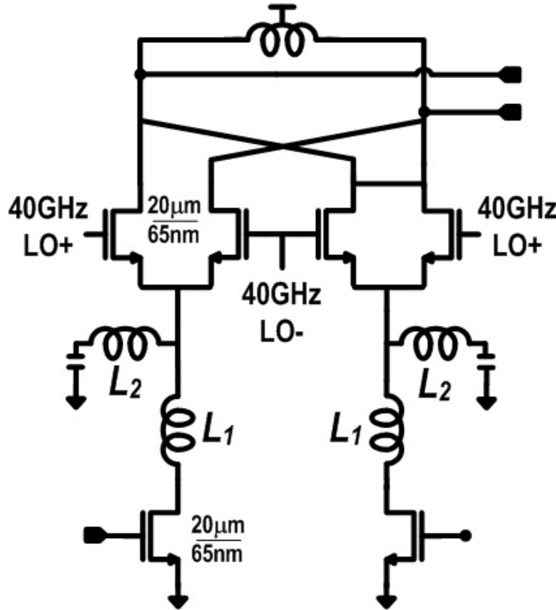


Figure 5.6: Simplified schematic of the RF mixer

conductor is driven single ended because of the single ended topology of the LNA. A spiral inductor, resonating out device parasitics, loads the RF mixer. Despite the relatively high frequency, we opted for a spiral instead of a transmission line because the signal at the mixer output is differential, making current returns modeling less critical.

On the contrary, L_1 and L_2, used single ended, have been implemented using transmission lines. Those two inductors do not just resonate out capacitive parasitics at the drains of the transconduct-

ances, but are used to match the switching pairs input impedance with the transconductor output impedance, providing almost 3 dB current gain boost.

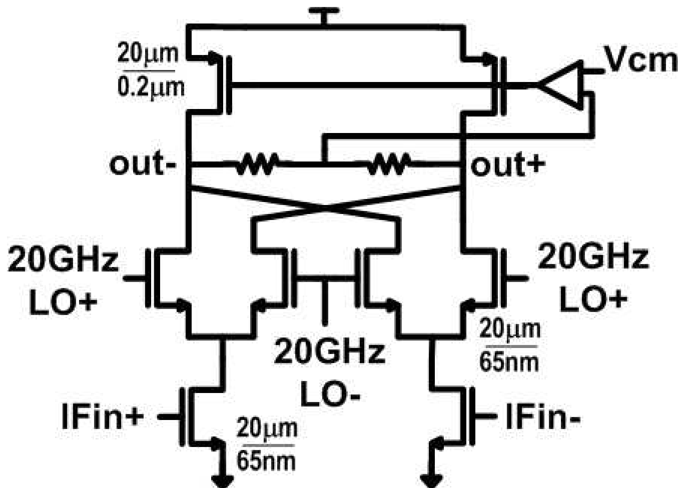


Figure 5.7: Simplified schematic of the IF mixers

IF quadrature mixers, as shown in Fig. 5.7, present also a double balanced Gilbert Cell topology. They use a differential active load to maximize output resistance for given voltage room. P-MOS current sources, controlled by means of a common-mode feedback, bias the mixer. Open drain differential pairs buffers cascading the receiver are used to drive measurement instruments.

5.2.2 Frequency Generation

Quadrature signals driving the IF mixers are generated by means of two P-N LC oscillators, coupled via cross-connected transistor $M_1 - M_4$, as shown in Fig. 5.8 (first harmonic coupling) [19].

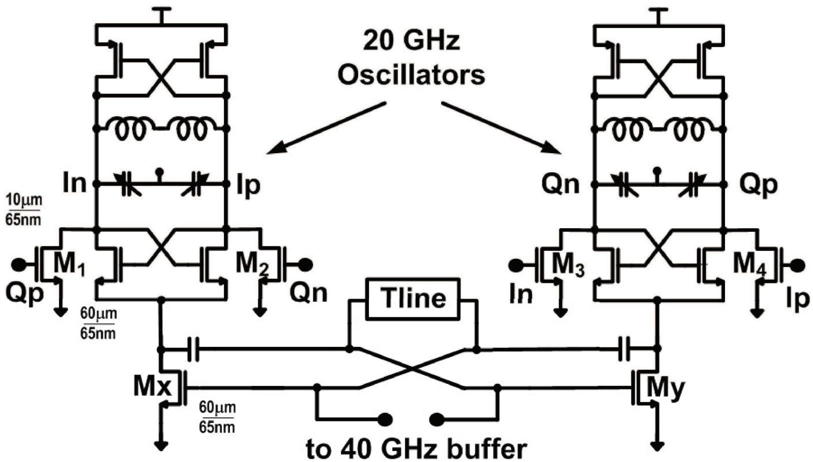


Figure 5.8: Simplified schematic of the VCO

Like in any differential oscillator, the common sources of the fully differential active pairs have a second harmonic content. Moreover, they have opposite phases because the oscillators run in quadrature [20]. This differential second harmonic content is then reinforced by the loop built around M_x and M_y. After further amplification

through pseudo-differential stages (not shown in Fig. 5.8), the extracted signal at twice the frequency drives the RF mixer.

Capacitive parasitic at common sources nodes are resonated out by an inductor reinforcing the 40 GHz current injected into M_x and M_y. In the final layout because of limited space to place all the inductors required, the latter one has been laid out as a transmission line around the inductor of the 40 GHz pseudo differential buffer.

Each oscillator uses P-N transconductors so that the output common mode voltage (around Vdd/2) allows DC coupling to the IF mixers.

The estimated total fixed capacitive parasitic at tank nodes is about 160 fF. Targeting a frequency tuning range of 13% results in a varactor with 130 fF maximum capacitance and 40 fF minimum capacitance, together with 255 pH inductance for a 20 GHz oscillation frequency.

In order to obtain the desired tuning range while keeping relatively small the VCO gain, two capacitor banks have been implemented (Fig. 5.9).

The first one is for fine tuning and is made by N-MOS in n-well varactors (A-MOS). In this case A-MOS varactors have been preferred to I-MOS ones because the common mode of the oscillators is set to Vdd/2. Using A-MOS it is possible to explore the entire tuning characteristic with a control voltage (V_{tune}) in the 0 V to

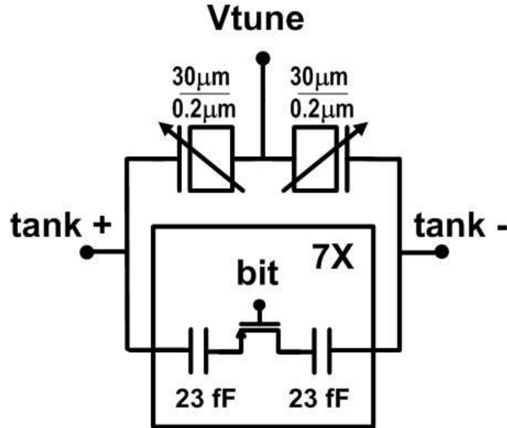


Figure 5.9: VCO capacitive tank

Vdd range, while it is not possible with I-MOS. As shown in Fig. 5.9, non minimum length has been chosen to increase the tuning range (expected in the order of 12%), as discussed in §4.1.1. This is possible because at 20 GHz varactors minimum Q is still higher than 10 even with non minimum length (Fig. 5.10).

The second bank is for coarse tuning. It is made of 7 blocks of digitally switched MOM capacitors, using 3 bit lines. Switched MOM capacitors have been preferred to switched A-MOS varactors because of their better Q at 20 GHz.

The tank inductor has been laid out as a differential octagonal one turn shielded inductor. The metal width is 10 μm and the total

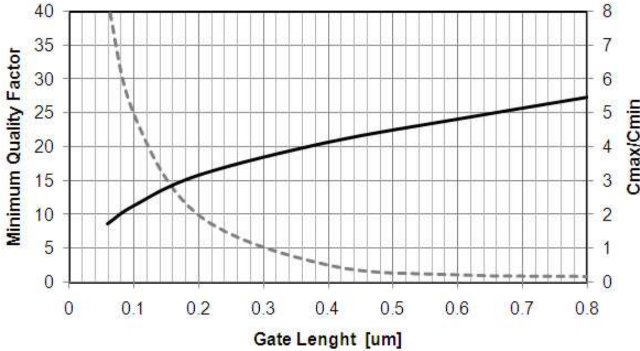


Figure 5.10: Minimum Q (dotted) and Cmax/Cmin ratio at 20 GHz

length, including the metal taper to the varactors, is 500 μm. Simulations, performed by means of Agilent Momentum, provide Q of about 23 at 20 GHz.

5.2.3 Measurement Results

Fabricated prototypes, with chip photomicrograph shown in Fig. 5.11 have been probed for characterization.

The chip draws about 53 mA from 1.5 V supply, including biasing. Measured S_{11}, gain and noise figure have been compared with simulations in Fig. 5.12. Simulations and measurements are very close. By the way, peak gain frequency is slightly higher than simulated

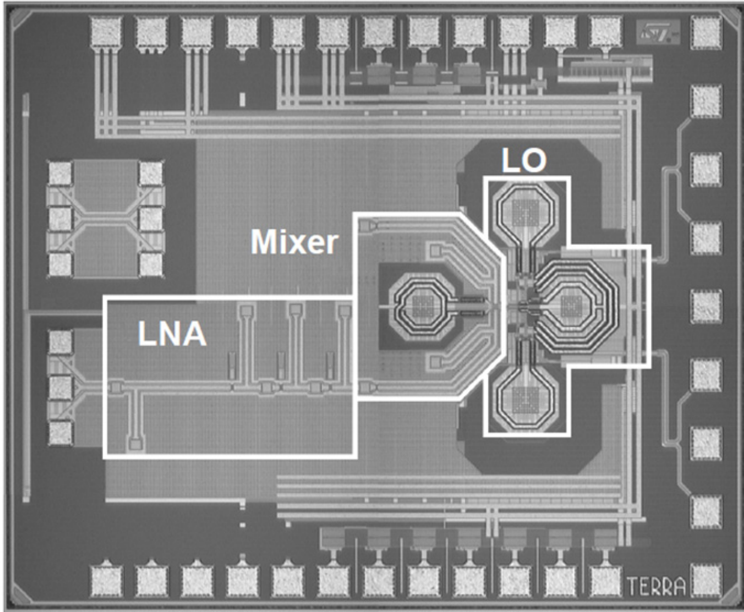


Figure 5.11: Die photomicrograph (2.15 mm^2 area)

(around 1 GHz) and this is mainly attributed to an overestimation of mixer parasitics. Also the measured peak gain magnitude is 3 dB different from the simulated one and this depends mainly on inaccuracies in the MOS modeling. But, considering the 3 stages LNA, it results as a reasonable error of less than 1 dB per stage.

The measured peak gain is 28 dB, while the -3 dB bandwidth (RF bandwidth) is about 5 GHz. The minimum noise figure is about 9

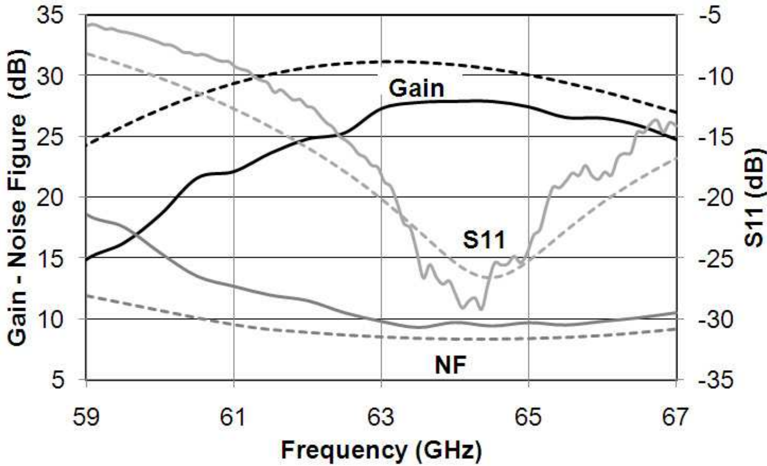


Figure 5.12: Measured (continuous line) and simulated (dotted line) Gain, S_{11} and Noise Figure

dB. Measured image rejection ratio is $>$ 60 dB while the input 1-dB compression point is about -26 dBm as shown in Fig. 5.13.

The frequency tuning range of the VCO, going from 59 GHz to 67 GHz, is about 12.5% covering an RF bandwidth of 8 GHz around 63 GHz. The I/Q mismatch is less then 5 degrees.

The received signal experiences two frequency translations. As shown in Fig. 5.14, the phase noise of an equivalent local oscillator running at received frequency has been measured down-converting an input tone (provided by an Agilent mm-wave source) to 100 MHz. The Agilent source provides a signal much purer than the on chip

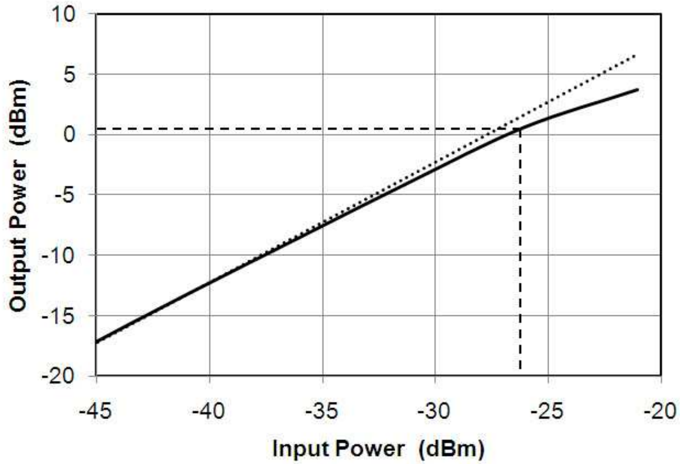


Figure 5.13: Measured 1-dB Compression Point

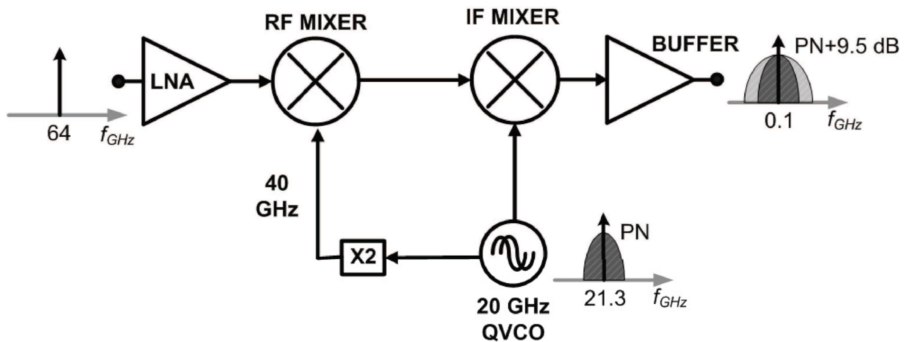


Figure 5.14: Phase Noise measurement setup

VCO signals, thus the output measured phase noise is only determined by the on chip VCO itself. Phase noise, thus determined by the VCO, is -115 dBc/Hz at 10 MHz offset at an equivalent carrier frequency of 64 GHz. Fig. 5.15 shows the measured output spectrum.

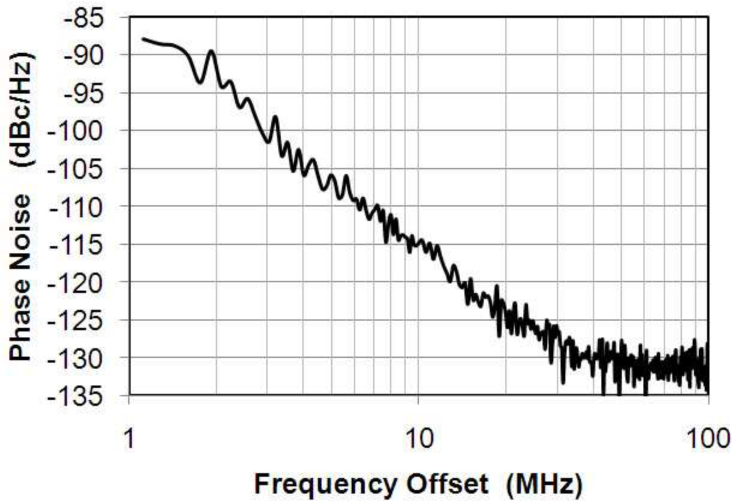


Figure 5.15: Measured Phase Noise

The noise spectra of the two LO's are fully correlated (being generated by the same VCO), meaning the 20 GHz QVCO phase noise estimate is 9.5 dB lower, i.e -124 dBc/Hz at 10 MHz offset, in good agreement with simulated results. Table 5.1 summarize the obtained results.

Parameter	Value
Voltage Gain	28 dB
Noise Figure	9 dB
RF bandwidth	5 GHz
Input 1-dB CP	-26 dBm
Image Rejection Ratio	$>$ 60 dB
Tuning Range	12.5%
I/Q Mismatch	$< 5°$
LO Phase Noise 10 MHz Offset	-115 dBc/Hz (64 GHz)
Total Power Consumption	80 mW
LO Power Consumption	36 mW
Supply Voltage	1.5 V
Active Chip Area	~ 0.5 mm^2
Technology	$<$ 65 nm CMOS

Table 5.1: Result Summary

5.2.4 Conclusions

A fully integrated mm-wave receiver based on a Sliding IF architecture has been investigated and integrated. Table 5.2 shows a comparison between this work and the state of art.

	This Work	JSSC09 [1]	JSSC08 [21]
Voltage Gain [dB]	28	22	30
Noise Figure [dB]	9	5.7	7.1
RF bandwidth [GHz]	5	4.5	N.A.
Tuning Range [%]	12.5	ext tuning	16.6
LO Phase Noise [dBc/Hz]	64 GHz	60 GHz	50 GHz
1 MHz Offset	-87	-84	-85
10 MHz Offset	-115	N.A.	N.A.
LO Current (no bias) [mA]	20	3.3	38
Total Current (no bias) [mA]	45	30	62
Supply Voltage [V]	1.5	1.2	1.2
Technology [nm]	65 CMOS	90 CMOS	90 CMOS

Table 5.2: Result Summary

This table demonstrates that the goal of realizing a 60 GHz receiver respecting the strict requirements of [3] regarding the frequency generation (discussed in Chapter 1) has been fully achieved while consuming half the current with respect to state of the art. The noise figure, although in spec, is still a little higher but this is due mainly to the choice of using low leakage digital transistors that were the only available at the time the design was done.

Moreover the RF bandwidth it is still not enough to cover the entire bandwidth of the standard proposal discussed in Chapter 1 [3]. The main limit to this are the narrow band LNA and the RF Mixer, the it is actually the real bottleneck. In the next chapter a new receiving front-end with wideband LNA and RF mixer will be described.

5.3 Wideband Sliding IF

As described in the previous paragraph a Sliding IF architecture is very valuable because it relax the requirements of the frequency synthesizer. By the way the front end presented in the previous chapter can suffer few disadvantages. Firstly the RF bandwidth covered by the LNA must be higher than 12 GHz to respect the standard proposal described in Chapter 1 [3]. Moreover, the carriers proposed by the standard itself are from about 58 GHz to 65 GHz. Considering the 2 GHz bandwidth for each channel (around every carrier), this means that the RF mixer must have a -3 dB bandwidth higher than 5 GHz (must be as flat as possible between 18 GHz and 23 GHz). Finally the frequency generation proposed previously can suffer of I/Q unbalance for a given phase noise required. Quadrature signals, infact, are generated through first harmonic coupling. So as described in [19], to reduce the I/Q error a stronger coupling is necessary, affecting a lot the phase noise performance.

For this reasons a new wideband front-end has been designed and fabricated (Fig. 5.16). In this case high performance transistors have been used to enhance gain and noise figure performances.

The new front-end introduces capacitively coupled inter-stage resonators in the LNA for maximum gain-bandwidth product, a VCO operating at 40 GHz and derives I and Q IF driving signals from

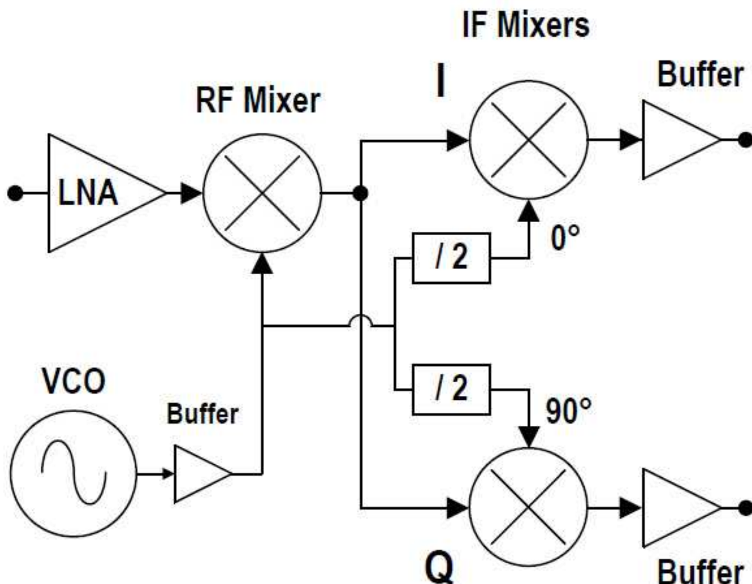


Figure 5.16: Wide-Band Front-End block diagram

the RF reference by means of wide-band infection locked frequency dividers by two (describe in § 4.2.4).
This permits again to reduce the operating frequency of the VCO and so of an eventual PLL, and to generate more accurate I/Q phases.

5.3.1 Receiver Chain

The circuit diagram of the RF front-end is reported in Fig. 5.17.

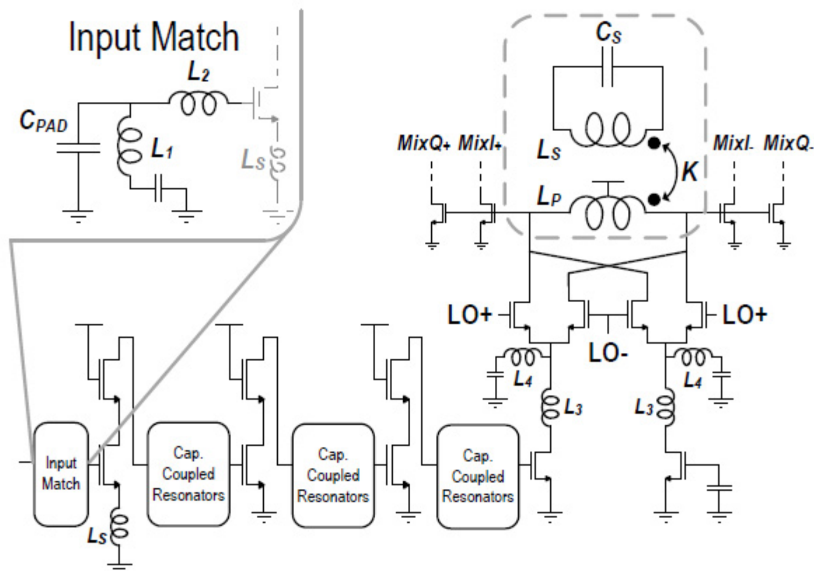


Figure 5.17: Wide-Band LNA and RF mixer

The LNA adopts three amplifying stages to achieve about 26 dB gain and employs capacitively coupled inter-stage matching (Fig. 5.18) designed for about 14 GHz RF bandwidth with about 1 dB ripple. A low gain mode can be selected by reducing the biasing current of transconductor devices in each stage.

Device sizes in each stage has been chosen according to the same noise analysis done in § 5.2.1.

As in the previous design, the RF mixer consists in a double

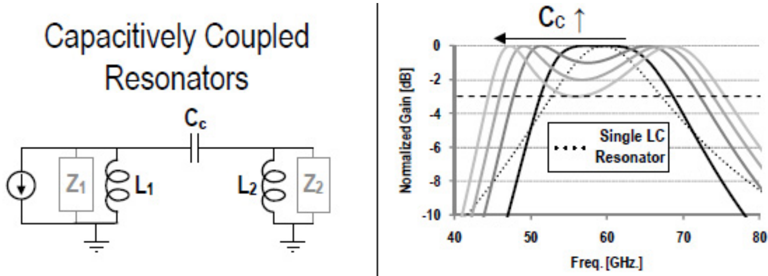


Figure 5.18: Gain-Bandwidth enhancement

balanced Gilbert Cell driven single ended by the LNA (Fig. 5.17). Again a current gain boost is realized by inductor L_3 and L_4 which match transconductor and switching pair impedance.

Furthermore, in order to enhance the bandwidth of the mixer itself, instead of adding low Q varactors to tune the resonating load, a wide band filter based on transforming coupling has been realized using the IF interstage network shown in Fig. 5.17, comprised of the RF mixer load and the IF mixers input.

The inductance of the primary winding resonates out all device parasitic at IF center frequency while the secondary resonates at the same frequency with an explicit MOM capacitor. The mutual inductance between the two windings is the responsible of a little split of the two resonance, enlarging the mixer bandwidth. Optimum performance in terms of bandwidth and ripple are achieved with mild coupling [22].

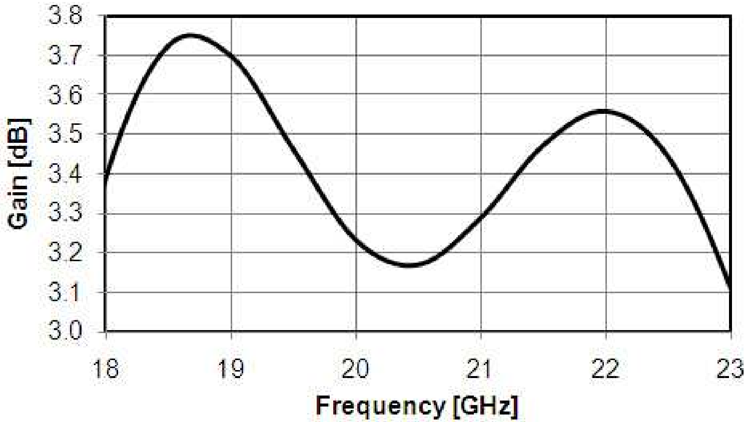


Figure 5.19: Simulated RF Mixer Gain

As the alignment (excluding the mutual inductance) of the frequency resonance is very important to obtain a flat response while adding the mutual contribution, the MOM capacitor loading the secondary winding has been divided in three blocks digitally switched. This also permit to obtain almost 1 dB gain boost on each side of the required bandwidth. Fig. 5.19 shows the simulated gain of the RF mixer in typical conditions.

Capacitive coupling, adopted in the LNA inter-stages, was also viable leading to even better gain-bandwidth performances but we opted for this alternative for the following reasons:

- parallel inductor to resonate out separate parasitic capacitors

would require inductances > 1 nH occupying a large area and complicating device layout

- at IF stage gain is less critical allowing maximum bandwidth as main target
- the mixer has a differential topology

5.3.2 Frequency Generation

The on-chip reference is tuned at 2/3 the received frequency for signal down-conversion to a sliding intermediate frequency. With respect to a conventional super-heterodyne architecture, the required tuning range is reduced because the reference fractional bandwidth equals the received fractional bandwidth. At the same time, the lower frequency favors reducing phase noise for given consumption. As reported in Fig. 5.16 the LO is composed by a 40 GHz differential VCO followed by two wide-band injection locking dividers to generate the 20 GHz I/Q signals. These two signals are the buffered and used to drive the IF mixers.

The VCO is a classic LC-VCO with cross-coupled N-MOS differential pair and a P-MOS current generator on the inductor center tap (Fig. 5.20).The P-MOS current generator has been used instead of an N-MOS one to obtain better performance on phase noise, and to make the output voltage not higher than Vdd. The tank capacitor

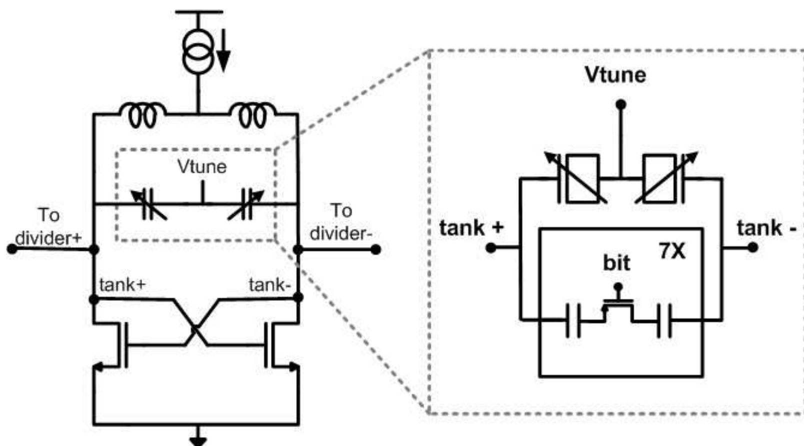


Figure 5.20: 40 GHz VCO schematic

comprises MOM switched devices for coarse tuning with N-MOS in n-well varactors for fine tuning, in order to maximize capacitor (and resonance) quality factor. The inductor value is about 70 pH.

This 40 GHz differential signal is then used to drive the RF mixer and two injecion locked divider by two providing I and Q signals. The VCO locks the divider by signal injection in parallel to the tank (as already illustrated in Fig. 4.15[17].

5.3.3 Measurement Results

The chip has been fabricated using a 65 nm GP CMOS technology by STMicroelectronics, and the micrograph is shown in Fig. 5.21. A

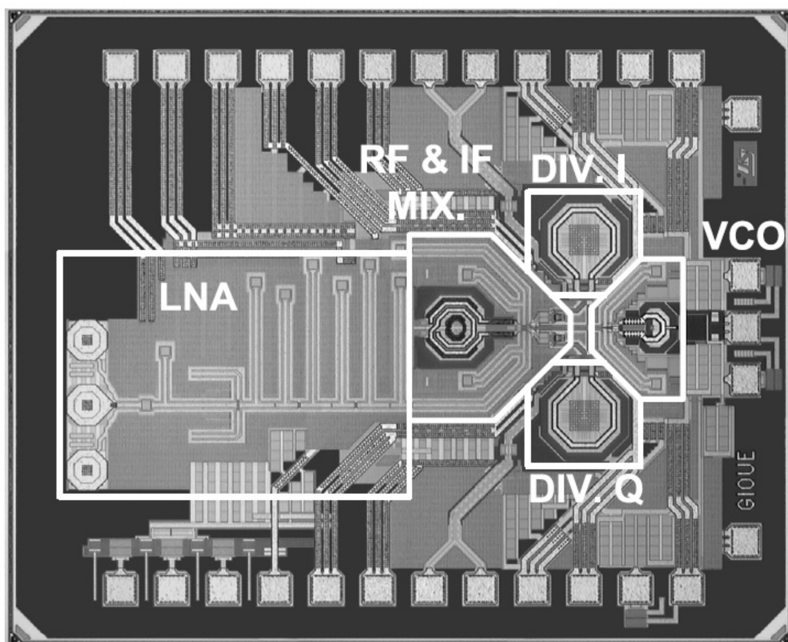


Figure 5.21: Chip Photomicrograph

second version, not integrating the on-chip VCO and where the reference is externally provided through a wide-band integrated balun, is also available. Dies were probed for characterization. Fig. 5.22 shows measured gain and noise figure versus RF frequency for the two versions. Peak gain is 35.5 dB and the RF bandwidth is higher the 13 GHz, with external reference. In-band gain ripple is < 2 dB.

The fully integrated version achieves the same peak gain while the

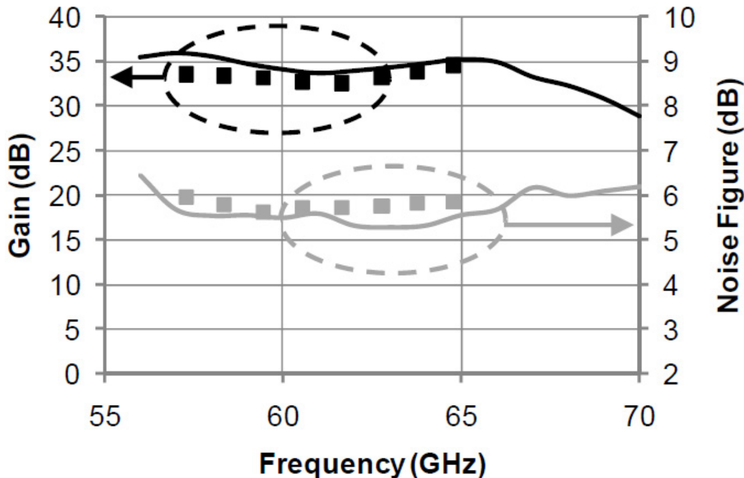


Figure 5.22: Measured gain and noise figure: external LO (continuous line) and on chip VCO (dots)

explored bandwidth is limited by the on-chip VCO frequency range of 12.6%. An under-estimation of tank parasitics lead to a slight down-shift of 2.7 GHz of the oscillator center frequency. Measurements were performed inserting a small metal plate in close proximity to the VCO tank with the effect of reducing the inductance and shifting the frequency upwards [23]. Fig. 5.23, moreover shows the gain variation of the chain versus the RF mixer MOM switching.

The receiver proves to be highly sensitive in the whole bandwidth, with NF always better than 6 dB in the VCO frequency range and an

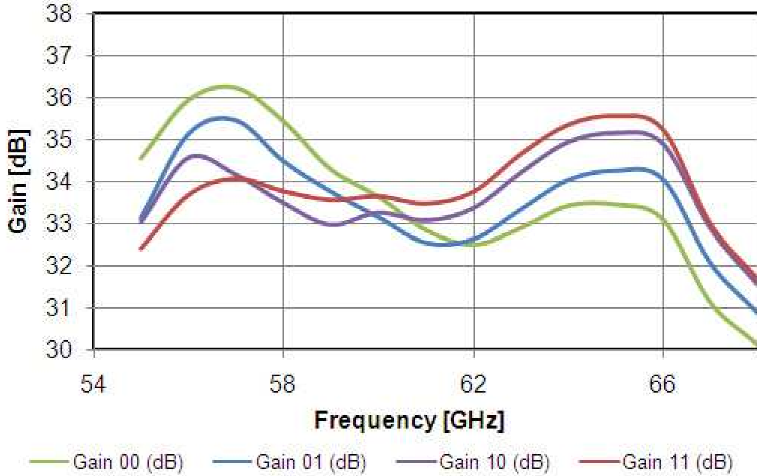


Figure 5.23: Measured gain varying MOM in the RF Mixer load

absolute minimum of 5.6 dB. The measured 1-dB compression point (in low gain mode, about 14 dB) is -21 dBm. Furthermore, a large image rejection ratio of better then 80 dB has been measured.

As in the previous Sliding IF front-end, the received frequency experiences two frequency translations. The phase noise of an equivalent local oscillator running at received frequency has been derived down-converting a pure input tone to 200 MHz (as already described in § 5.2.3). The phase noise thus determined by the VCO, is -115 dBc/HZ at 10 MHz offset at an equivalent carrier frequency of 60 GHz, as shown in Fig. 5.24.

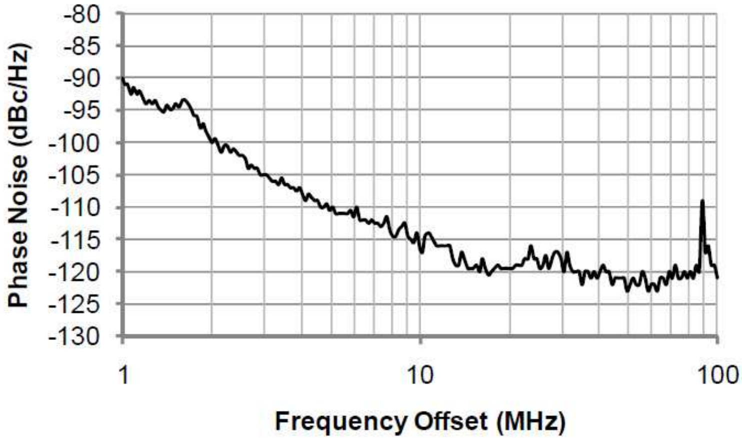


Figure 5.24: Measured Phase Noise

5.3.4 Conclusions

Table 5.3 provides a summary of this work performances and a comparison versus the state of art.

A wideband front end, able to cover the stringent requirements of [3] for both frequency generation and wideband gain, has been integrated and demonstrated using a bulk CMOS technology.

	This Work	[24]	[25]	[26]
Voltage Gain [dB]	35.5	30	22	14.7
Noise Figure [dB]	5.6-6.5	7.1-9.8	5.7-7.1	5.6-7.2
RF bandwidth [GHz]	13	N.A.	4	10
Image Rejection [dB]	80	N.A.	N.A.	N.A.
Tuning Range [%]	12.6	16.6	ext LO	ext LO
LO Phase Noise [dBc/Hz]	60 GHz	50 GHz	60 GHz	N.A.
1 MHz Offset	-90	-85	-84	N.A.
10 MHz Offset	-115	N.A.	N.A.	N.A.
Input 1-dB CP) [dBm]	-21	-29.9 (High gain)	-27.5	-22
Power [mW]	75	65	36	151
Supply Voltage [V]	1	1.2	1.2	1.2
Technology [nm]	65 CMOS	90 CMOS	90 CMOS	65 CMOS

Table 5.3: Result Summary

List of Figures

1.1 International Technology Roadmap for Semiconductors 9
1.2 RF CMOS ITRS 10
1.3 Vehicule radar example 12
1.4 WPAN example 13
1.5 Air attenuation 14
1.6 Weapons detection 15
1.7 World 60 GHz band allocations 16
1.8 Channels numbering 18
1.9 Band allocation 19
1.10 Range versus Data Throughput 20
1.11 Error Vector Magnitude 21
1.12 EVM versus Bit Rate 22
1.13 EVM due to Phase Noise 23

1.14 EVM degradation versus Phase Noise at 1 MHz PLL bandwidth 24

2.1 MSG, MAG and U function for an active device 31
2.2 f_{max} versus W_F and current density for $W_{tot} = 20\mu m$ 37
2.3 Power Gain vs Finger Width (Total Width $30\mu m$) . . 39
2.4 Power Gain vs Finger Width (Total Width $30\mu m$) - Zoom 40
2.5 Cascode vs Common Source (CS) and Common Gate (CG) 41
2.6 Shared Junction cascode schematic 42
2.7 Shared Junction basic layout 43

3.1 Test Chip Photomicrograph 46
3.2 GSG Pad - Top View 47
3.3 MSG/MAG degratation due to layout parasitics . . . 49
3.4 Gate Bias 50
3.5 Shared Junction Cascode Top Level 50
3.6 Measured MSG/MAG for $W_{tot} = 20\mu m$ and $W_F = 1\mu m$ 51
3.7 Measured MSG/MAG for $W_{tot} = 20\mu m$ and different W_F 52
3.8 Measured MSG/MAG for $W_{tot} = 20\mu m$ and $W_F = 1\mu m$ for different bias 53

3.9 Measured MSG/MAG for $W_{tot} = 20\mu m$ and $W_F = 1\mu m$ for different bias 54

4.1 Cross-section of an Inversion Mode N-MOS variable capacitor 59
4.2 Minimum Q (dotted line) and C_{max}/C_{min} ratio as a function of gate length at 60 GHz 62
4.3 Measured C-V characteristic (continuous line) and simulated C-V and Q (dotted lines) 63
4.4 VCO and buffer schematic. The in-let shows the varactors architecture 65
4.5 70 pH inductor 66
4.6 70 pH inductor 67
4.7 54 GHz VCO Photomicrograph 68
4.8 Measured (continuous line) and simulated (dotted lines) oscillation frequency vs control voltage 69
4.9 Measured start-up currents and Q vs frequency 70
4.10 Measured Phase Noise at the lowest frequency (51 GHz) 71
4.11 Measured and simulated Phase Noise at 10 MHz offset vs frequency 72
4.12 Miller's divide by two block diagram with lowpass and bandpass filter 77
4.13 Miller's divide by two block schematic 78
4.14 Injection Locked divide by two schematic 79

4.15 Injection Locked divide by two schematic with direct injection on the tank 82
4.16 Sensitivity of a Direct Injected ILFD 83
4.17 ILFD locking range and output signal amplitude . . . 84

5.1 Direct Conversion Block Diagram 88
5.2 Sliding IF Conversion Block Diagram 90
5.3 Simplified schematic of the LNA 91
5.4 Simplified schematic of the first stage of the LNA . . . 92
5.5 Simplified schematic of the second stage of the LNA . 94
5.6 Simplified schematic of the RF mixer 95
5.7 Simplified schematic of the IF mixers 96
5.8 Simplified schematic of the VCO 97
5.9 VCO capacitive tank 99
5.10 Minimum Q (dotted) and Cmax/Cmin ratio at 20 GHz 100
5.11 Die photomicrograph (2.15 mm^2 area) 101
5.12 Measured (continuous line) and simulated (dotted line) Gain, S_{11} and Noise Figure 102
5.13 Measured 1-dB Compression Point 103
5.14 Phase Noise measurement setup 103
5.15 Measured Phase Noise 104
5.16 Wide-Band Front-End block diagram 109
5.17 Wide-Band LNA and RF mixer 110
5.18 Gain-Bandwidth enhancement 111

5.19 Simulated RF Mixer Gain 112
5.20 40 GHz VCO schematic 114
5.21 Chip Photomicrograph 115
5.22 Measured gain and noise figure: external LO (continuous line) and on chip VCO (dots) 116
5.23 Measured gain varying MOM in the RF Mixer load . . 117
5.24 Measured Phase Noise 118

List of Tables

2.1 f_t and f_{max} for a $W_{tot} = 20\mu m$ common source NMOS 36

3.1 *Shared Junction* MOS sizes 48

4.1 VCOs State of Art 74

5.1 Result Summary 105
5.2 Result Summary 106
5.3 Result Summary 119

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