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High Voltage Integrated Class-B Amplifier for Ultra-Sound Transducers in BCD-SOI Technology

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Introduction

The ability to peer into the human body is an essential diagnostic tool in medicine and is one of the key issues in health care. Our population is aging globally; for example, over 20% of the population in Japan is already over 65 years old. Older people require many more imaging investigations than do younger ones. Cancer and heart disease are the number-one killers, approaching 40% of all deaths. Improved image quality becomes essential for effective diagnostics in these cases. Shorter examination times, shift to outpatient testing, and noninvasive imaging are rapidly needed. The challenges to contain health-care costs are enormous, and technology solutions are needed to address them.

There are four major imaging modalities. Their effective signal positions on the electromagnetic spectrum vary from megahertz (MHz) for ultrasound, through gigahertz (GHz) for magnetic resonance imaging (MRI), to 1018 Hz for X-ray/computed tomography (CT) [1]. Ultrasound is a simple, non invasive and accessible imaging technique that allows the evaluation of musculoskeletal system in real time, with the advantages of examining the joints in a dynamic way. The technique is based on the principle of analyzing the echo from a transmitting sound wave. The sound waves are created by applying a

transmit voltage to the transducer element, which generates a related acoustic pressure. Most commonly, the transducer is made of piezoelectric material that deforms when an electrical field is applied and conversely generates an electrical voltage when it is mechanically deformed.

The design of the front-end electronics (transmitter and receiver) is complicated by the high electrical impedance of the transducer elements. This is particularly emphasized by the use of very small elements since the Transducer electrical impedance is inverse proportional to the element area. The high impedance requires rather high transmit voltages of several hundred volts to achieve the desired output acoustic pressure. The generation of the high voltage transmit waveform has historically been a challenging part in the system design and remains so today.

Most commercially available ultrasound systems have a limited number of transducer elements inside the ultrasound probe. There is usually a one to one correspondence between each element and the system channel located inside the console. This limits the maximum number of channels to few hundreds organized in rows. In application where 3D objects moving fast have to be imaged, such as cardiology, it is believed the row of elements should be replaced by a matrix. But electronics must be moved from the console into the probe – handle. Application specific integrated circuits consuming low power become key components of the system. Considerable advancement in the functions of ultra-sound systems is presently underway. The renewed interest is determined by a potential increase in device volumes, with low cost ultra-sound devices recently hitting the market, and by the ever increasing rates when data are transferred from the array to the electronics in reception

[3, 2]. Integration and advanced electronics, e.g. including micro-electro-mechanical systems, are playing a key role [4].

In this work, we address the design of transducer's drivers which need to be capable of high output powers up to the MHz range. Pulsers are usually adopted because of the high efficiency and simplicity [5, 6]. Arbitrary waveform generators are nonetheless very attractive enabling apodization profiles with high resolution, beams with low harmonic content and instantaneous changes in transmit energy between pulses [7, 8]. But their use is today rather limited because of the high manufacturing costs, power dissipation and space constraints.

In view of an increased level of integration, the availability of a BCD technology, capable of watts level driving at high frequency, encourages investigation of linear amplifiers. Advantages in terms of reliability, space and cost would derive. Furthermore, low distortion allows employing the amplifier in harmonic imaging where higher harmonic echoes (usually the second) of the fundamental transmitted frequency, either generated by reflection from micro-bubbles or on propagation, are selectively detected and used for imaging [9]. As a consequence, the harmonics of the transmitted signal need to be suppressed as much as possible and the received signal is derived solely from the non-linear behavior of the body. Today, low HD_2 in second harmonic imaging is achieved by out-of-phase transmission techniques where an off-chip transformer balances positive and negative pulses [10, 11]. A low distortion linear amplifier would allow getting rid of this expensive off-chip component plus enabling beam-forming with high contrast.

This work is then organized as follow:

- **Chapter 1** covers the general principles involved in forming ultrasonic images and discuss ultrasound system blocks. The principal parameters to evaluate ultrasound system performances are described. A Comparison between linear driver and pulser is presented and the advantages of first solution are evaluated.

- **Chapter 2** gives an overview of BCD technologies, capable of integrating Bipolar, CMOS and DMOS devices. This makes possible to build high-voltage circuits that are cointegrated with high-quality control logic and high-speed, low-noise, and low-power analog circuitry. These processes are ideally suited for implementing high-voltage circuits required in ultrasound systems.

- **Chapter 3** described the design of a fully integrated solution of linear amplifier suitable for ultrasound systems. The proposed amplifier, closed in a feedback loop, uses a high g_m low-voltage transconductor driving a high voltage trans-impedance stage operating in class-B. Device parameters vary with signal amplitude making circuit analysis involved. Techniques to analyze large signal frequency response, distortion and stability are proposed in this chapter leading to useful design insights.

- **Chapter 4** shows experimental results obtained with realized prototypes. The adopted technology is BCD6-SOI of STMicroelectronics. Experiments show that amplifier performances are adequate for the ultrasound application.

Chapter 1

Electronics for Medical Ultrasound

Medical ultrasound, which has never been a very static field, is undergoing particularly interesting and exciting changes today. The most dramatic of these changes involves extensive miniaturization from a large scanner to a laptop, tablet computer, or handheld device. Surprisingly, much of this reduction has been accomplished without significant loss in performance. In fact, additional capabilities such as real-time 3D imaging have become available as part of this miniaturization process. As often happens, a dramatic change such as the one just described introduces many unexpected benefits. Foremost among these is a migration of the ultrasonic imager from its traditional home in radiology and cardiology departments to the hands of specialists. One can even envision migration to the hands of the primary care physician. A key driver behind these changes is a continued reduction in power and size of electronic devices due to Moore's Law. Medical ultrasound

is an ideal target for miniaturization and further integration, since the spatial requirements of the physical sensor array are particularly small, especially when compared to the room-sized gantries required for computed tomography (CT), magnetic resonance imaging (MRI), positron emission tomography (PET), and related fields. Ultrasound transducer arrays being used today are layered structures a fewmillimeters thick with contact surfaces on the order of a few centimeters by about 1cm. The remainder of the system is largely comprised of processing electronics that are highly amenable to miniaturization. Therefore, as opposed to other imaging modalities, ultrasound stands to benefit greatly from current and future trends in electronic miniaturization. This chapter gives the technical background needed to appreciate the processes just described.

1.1 Ultrasound Imaging Principles

Ultrasound machines form images of biological tissue by transmitting focused beams of sound waves into the body and then listening for the reflected sound waves to determine the structure of the tissue being imaged.

This process is illustrated in Fig. 1.1: A handheld probe containing an array of transducer elements is applied to the body. The ultrasound machine creates a focused beam of sound using the array of transducer elements whose outputs are phased relative to each other. The sound waves are created by applying a transmit voltage to the transducer elements, which generates a related acoustic pressure at the face of the transducer. Sound waves propagate out from the face of the transducer and add constructively at a point

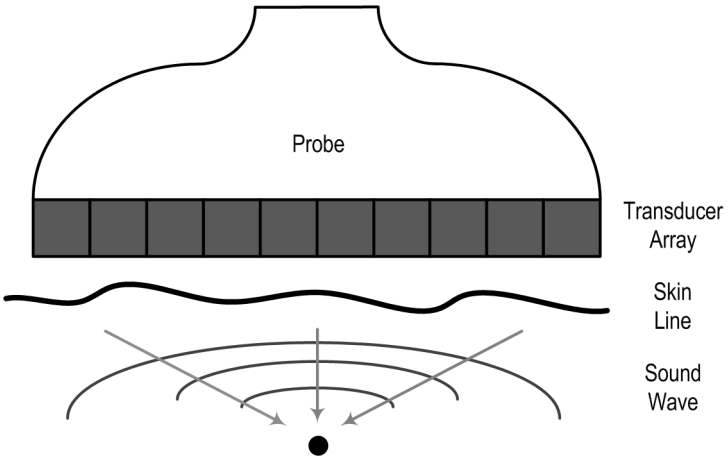

Figure 1.1: Schematic of the imaging process.

distant from the plane of the transducer inside the body.

Depending on the acoustic impedance of the tissue along the path of the acoustic beam, a proportionate level of sound is reflected and travels back to the face of the transducer. The received echoes are phased relative to one another and added up in order to preferentially focus the attention of the system along the line of sight of the receive beam.

Unlike other medical imaging devices, ultrasound images reflections that arise from changes in acoustic impedance as sound waves travel from tissue of one type to another. One important consequence of this is that structures which are oblique to the path of the ultrasound beam are often weakly imaged [12]. In addition, strong reflectors will tend to shadow deeper structures by preventing sound waves from reaching them. Another source of information is backscatter from small reflectors which give tissues such as liver a speckle-like structure.

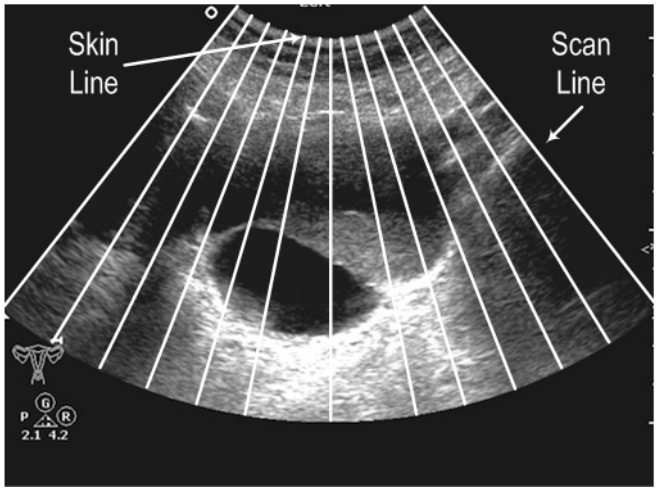

Figure 1.2: Image showing scan lines.

1.1.1 Scanning

Imaging using ultrasound consists of building up a 2D or 3D representation of the subject using multiple scan-lines that are acquired adjacent to each other within the body. This is illustrated in Fig. 1.2, where a number of individual scan lines (white lines) are highlighted. While they are shown separated in the figure, in reality they are contiguous and build up the image. The transducer transmits ultrasound into the body, echoes representing tissue structure are received, and these echoes are then processed and displayed by the ultrasound machine.

Figure 1.3 shows the progression in the development of probe architectures. The first ultrasound probes consisted of a single element that was manually moved along the patient in order to generate an image (Fig. 1.3a).

Today, the majority of ultrasound products use electronically scanned probes. These can be further divided into linear scan and sector scan types. In linearly scanned probes, the beam is translated horizontally along the

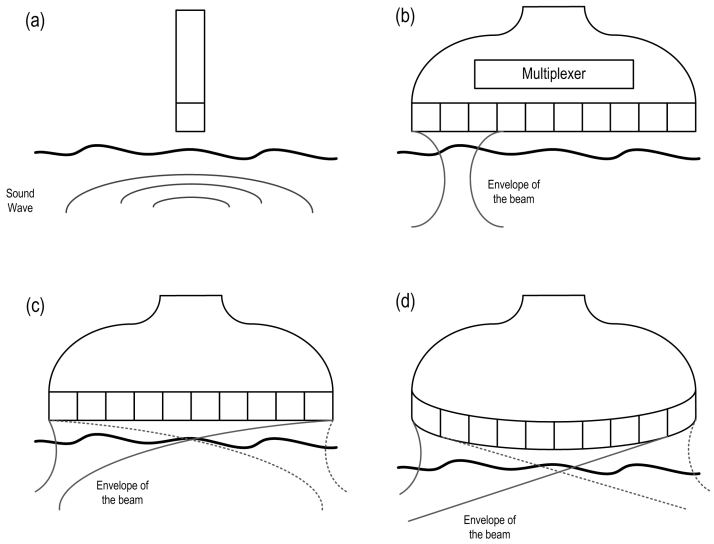

Figure 1.3: Ultrasound scanning probe types. (a) Manual scan with single element. (b) Electronically scanned1D linear array. (c) Electronically scanned 1D phased array showing two different steering directions (A and B). (d) Electronically scanned 1D curved array.

face of the transducer also known as the aperture (Fig. 1.3b). Translation is accomplished by successively selecting different groups of transducers electronically. In sector scan probes (also called phased array probes), the beam is scanned radially with the transducer probe as the pivot for the fan beam (Fig. 1.3c). Radial scanning is done by relative phasing of channel delays in order to steer the beam. The group of elements that are active at any given time is known as the active aperture. Finally, curved array probes are linear probes that implement sector scanning due to their geometry (Fig. 1.3d).

The choice of probe type is dependent on the requirements for access to the tissue being imaged as well as the nature of the structures themselves. For example, in cases where large structures (such as a fetal head) need to be imaged from a small aperture, a curved or phased array probe might be

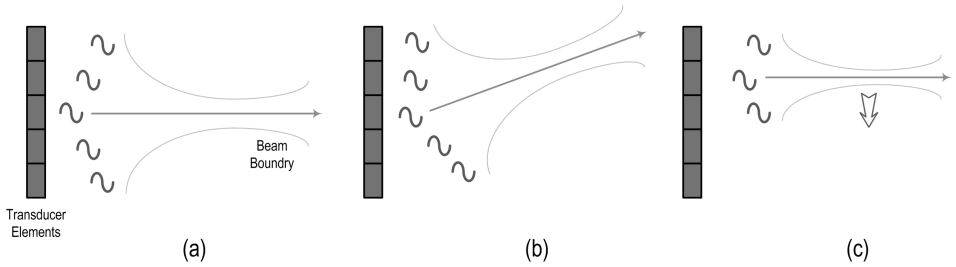

Figure 1.4: Beam formation. (a) Focused beam. (b) Focusing and steering. (c) Aperture translation.

used. In cases where access is not as much of an issue, but large imaging area near the probe is required (such as for carotid artery imaging), linear probes would be used.

1.1.2 Beam Formation

Beam formation can be divided into the simultaneous operations of focusing and steering [13]. In addition, certain systems use multiplexing to accomplish aperture translation. Focusing is accomplished by time delay of the transmit channels such that the acoustic waves add constructively at the focal point as shown in Fig. 1.4a. Steering refers to changing the beam angle while the aperture remains fixed in space. Steering is accomplished by delaying the transmit channels so that the focal point is moved at an angle relative to the normal center of the active aperture. This is shown in Fig. 1.4b, where the beam is steered to a focal point. Note that in this case both focusing and steering are used.

Translation of the aperture is accomplished by successively switching in different groups of transducer elements to accomplish a linear scan of the active beam across the face of the array as shown in Fig. 1.4c. Steering and

linear scanning can be combined, as is the case with spatial compounding [14].

Time delay of the transmit signals is accomplished in the system beamforming electronics by shifting the transmit control signals relative to each other in time so that the resulting acoustic waves are transmitted with the required phase delay. The extent of phase delay required on each channel is calculated in real-time by the beamforming electronics based on the required instantaneous location of the focused ultrasound beam for the given scan.

Beam formation is also done during reception in a similar fashion as on transmit. In this case it can be thought of as focusing the attention of the receive electronics such that only echoes originating at the focal point achieve the maximum antenna gain at the particular instant. The beam-forming configurations can be different on transmit and receive to independently optimize the transmit and receive beams. The beamwidth at the focus can be approximated by Eq. 1.1 [15].

$$bw = \lambda(f\#) \tag{1.1}$$

The f# (or f-number) is a measure of the degree of focusing and is defined as [16]

$$f\# = \frac{focus}{D} \tag{1.2}$$

where focus refers to the location of the axial focus, and D is the aperture size.

1.1.3 Transmit/Receive Cycle

Ultrasound machines build images one line at a time by multiple successive transmit and receive cycles. Each of these cycles forms an ultrasound beam in a particular direction to acquire the respective line. This process is illustrated in Fig. 1.5a.

A diagram of the ultrasound transmit/receive cycle is shown in Fig. 1.5b. The cycle as shown is known as a B-mode cycle and is the most commonly used cycle today.

The transmit cycle is repeated each time that a new line is to be acquired. Typically between 50 and 400 lines are acquired where each one takes approximately 100–300 ms. The pulse repetition frequency (PRF) depends on the application. For example, cardiology requires PRF rates as high as 10 kHz while abdominal imaging is typically done at 3 to 4 kHz PRF rates.

The cycle begins with reconfiguration of the electronics including any beamspecific control data for the mux switches and the pulsers. Reconfiguration is generally avoided during the receive cycle in order to prevent any digital noise from coupling into the receivers and causing image artifacts. Therefore, given a fixed frame rate set by the expectations of the user, the time for reconfiguration takes away from the available receive time. This reduces the penetration capability of the system and is therefore undesirable. For this reason, reconfiguration must be made as short as possible (typically less than $10\mu s$).

Next, the transmit cycle begins during which all active pulsers in the array are fired each according to its assigned phase delay. The cycle ends

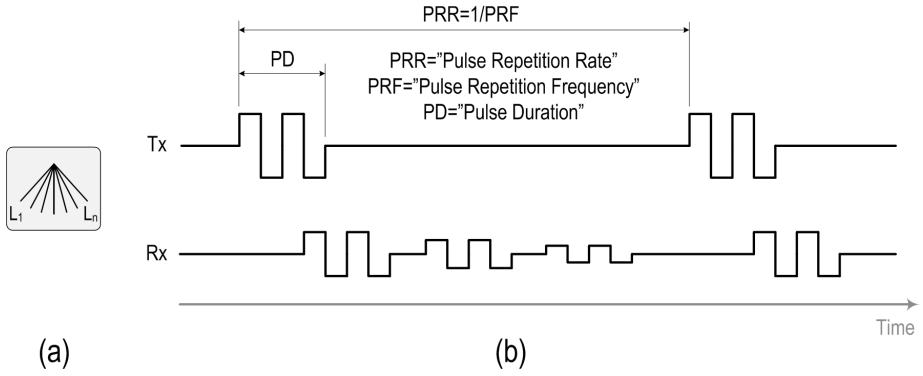

Figure 1.5: Ultrasound beam acquisition. (a) Successive lines used to build up the image. (b) Transmit/receive cycle in terms of the voltage as seen at the transducer.

after the last pulse has completed its transmission.

Immediately following the transmit cycle, the receive cycle begins and lasts until all of the echoes have returned from deep within the body. As shown in Fig. 1.6, a graph of the receive cycle has the important property that depth in the body is linearly related to increasing time along the x-axis. This can best be understood as follows: Immediately after the first transmit pulses occur, echoes begin to come in from tissue in the body. In fact, the transmit pulses first hit the skin line, then hit the tissue immediately underneath the skin, then the tissue following that, and so on, until they have propagated on through, very deep into the body. At each point the tissue being stimulated by transmit pulses returns an echo. These echoes, in turn, propagate back through the tissue to the transducer array where they are then converted into electrical energy for the receive signal. With the assumption of a constant speed of sound, one can convert the time interval between echos to distance in tissue as shown in Fig. 1.6.

Another important property of Fig. 1.6 is the log magnitude signal at-

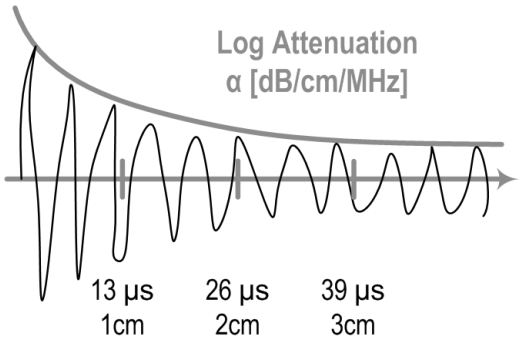

Figure 1.6: Signal level attenuation with depth in the body. Note that the return signal frequency is shown much lower than in reality for illustration.

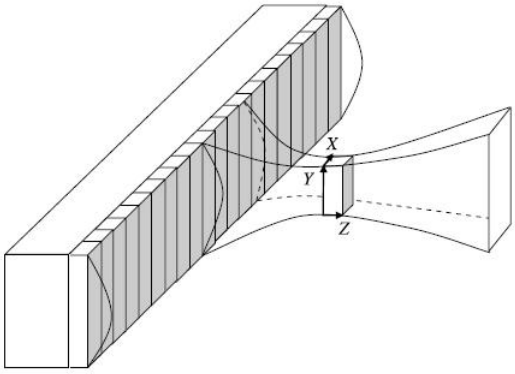

Figure 1.7: Illustration of ultrasound beam generated using a linear ID array showing elevational (Y), axial (Z) and (X) azimuthal resolutions at the beam focus. The array is focussed in elevation using a fixed focus lens.

tenuation that echoes experience when traveling through tissue in the body. Echoes that return sooner are coming from structures that are close to the transducer and therefore experience much less attenuation than echoes that return later. This attenuation must be corrected for in order to display a useful image with uniform grayscale levels at all pixels.

1.1.4 Image Quality Performance Parameters

Image quality in ultrasound images is directly affected by a number of parameters that are discussed below.

- ***Reflection:*** losses can be incurred when the acoustic wave propagates from one tissue type to another. This is, in general, not an issue because waves propagate between layers of soft tissue in which water is a major constituent; however, two types of reflectors do transmit the majority of sound back. These are gas in the lungs and gastrointestinal tract and bone. Therefore when imaging through these tissues, partial or complete occlusion of other surrounding structures may occur. Sound is also strongly reflected at the transition between the transducer and the body. In fact, direct contact is needed since the attenuation going from the body to air would be too great to be useful. Typically a special acoustic gel is used to ensure that a good acoustic coupling is maintained between the transducer probe face and the body.

- ***Absorption:*** absorption, α, is measured in $\frac{dB}{cm \cdot MHz}$, where a varies from 0.5 for fat to 2.0 for muscle [12]. Round-trip attenuation is given by 2α, so for typical tissue (fat) it is approximately 1 $\frac{dB}{cm \cdot MHz}$. The ability of a particular probe to image to a certain depth within the body is defined as penetration depth and varies significantly depending on application.

- ***Resolution:*** Spatial resolution in ultrasound imaging is determined by three interacting effects as can be seen in Fig. 1.7. Axial (or range

or longitudinal) resolution is the resolution along the direction of travel of the transmitted ultrasound beam. This resolution is limited by the length of the transmitted ultrasound pulse. Elevational and azimuthal resolutions are determined by how well the ultrasound beam can be focused in these two orthogonal directions. Probes that image finer detail do so using higher frequencies, and therefore they achieve much poorer penetration than probes that image at lower detail at lower frequencies due to absorption. In the usual nomenclature for characterization of acoustic fields, λ is the wavelength of the ultrasound signal given by

$$\lambda = \frac{c}{f} \tag{1.3}$$

where f is the frequency of the transmitted signal, and c is the speed of the sound in the medium (nominally $1540\frac{m}{s}$ for soft tissue). The beam can be broken into three distinct regions: the focal region appearing near the center of the beam, the near field, a region of poor focusing which appears close to the transducer, and the far field a region of poor focusing distant from the transducer. A strong focus is associated with a narrow beamwidth at the focus and a short depth for the focal region; operating conditions with lower f-numbers are considered more strongly focused. A good approximate expression for depth of focus (DOF) is given by Eq. 1.4 [15, 16].

$$DOF = 7\lambda(f\#)^2 \tag{1.4}$$

- ***Dynamic Range:*** Signal dynamic range is limited by the maximum transmit pressure and the minimum detectable return signal. The transmit pressure is directly related to the required pulsing voltage. The maximum transmit pressure is strictly regulated by the FDA in the United States in order to reduce the chances of adverse events such as heating of tissue. The minimum receive voltage is technology-dependent and is currently limited by the noise in the front-end preamplifier.

1.2 The Ultrasound System

The system components are discussed in this section to provide a functional understanding of the system. The starting point for this discussion is the beamformer control unit shown in Fig. 1.8, which is responsible for synchronizing the generation of the sound waves and the reflected wave measurements. The controller knows the region of interest in terms of width and depth. This region gets translated into a desired number of scan lines and a desired number of focal points per scan line. The beamformer controller begins with the first scan line and excites an array of piezoelectric transducers with a sequence of high voltage pulses via transmit amplifiers. High voltage (HV) pulsers, as shown in Fig. 1.9a, are usually adopted to drive the transducers because of the high efficiency and simplicity. Arbitrary waveform generators realized with a high voltage linear amplifier driven by a digital-to-analog converter (Fig. 1.9b) are nonetheless very attractive enabling apodization profiles with high resolution, beams with low harmonic

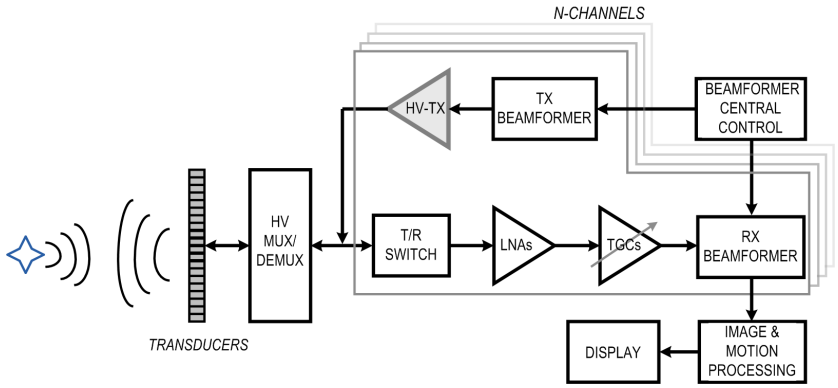

Figure 1.8: Schematic diagram of typical ultrasound imaging architecture.

content and instantaneous changes in transmit energy between pulses. Furthermore, low distortion allows employing the amplifier in harmonic imaging where higher harmonic echoes (usually the second) of the fundamental transmitted frequency, either generated by reflection from micro-bubbles or on propagation, are selectively detected and used for imaging.

The pulses go through a transmit/receive switch, which prevents the high voltage pulses from damaging the receive electronics. Note that these high voltage pulses have been properly time delayed so that the resulting sound waves can be focused along the desired scan line to produce a narrowly focused beam at the desired focal point. The beamformer controller determines which transducer elements to energize at a given time and the proper time delay value for each element to properly steer the sound waves towards the desired focal point.

As the sound waves propagate toward the desired focal point, they migrate through materials with different densities. With each change in density, the sound wave has a slight change in direction and produces a reflected sound wave. Some of the reflected sound waves propagate back to the transducer

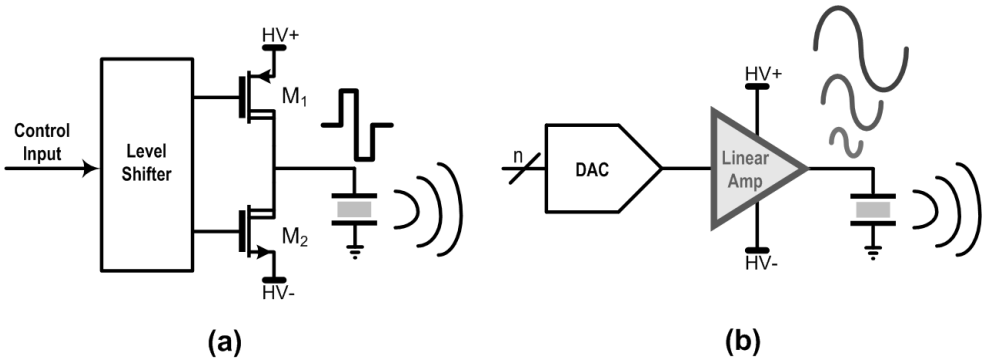

Figure 1.9: Pulser (a) and arbitrary waveform generator (AWG) (b).

and form the input to the piezoelectric elements in the transducer. The resulting low voltage signals are scaled using a time gain control amplifier (TGC) before being sampled by analog-to-digital converters (ADC). The TGC is configured so that the gain profile being applied to the received signal is a function of the sample time since the signal strength decreases with time (e.g., it has traveled through more tissue).

Once the received signals reach the Receive beamformer, the signals are scaled and appropriately delayed to permit a coherent summation of the signals. This new signal represents the beamformed signal for one or more focal points along a particular specific scan line. The beamformer operations are typically performed in application-specific integrated circuit (ASIC), field-programmable gate array (FPGA), DSP or a combination of these components. The choice of devices depends on the number of channels used in beamforming, which determines the input/output requirement as well as the processing requirement to perform digital beamforming. Once the data is beamformed, depending on the imaging modes, various processings are carried out.

Main imaging modes are reported below:

- **A-mode** (Amplitude) imaging displays the amplitude of a sampled voltage signal for a single sound wave as a function of time. This mode is considered 1D and used to measure the distance between two objects by dividing the speed of sound by half of the measured time between the peaks in the A-mode plot, which represents the two objects in question. This mode is no longer used in ultrasound systems.

- **B-mode** (Brightness) imaging is the same as A-mode, except that brightness is used to represent the amplitude of the sampled signal. B mode imaging is performed by sweeping the transmitted sound wave over the plane to produce a 2D image. Typically, multiple sets of pulses are generated to produce sound waves for each scan line, each set of pulses are intended for a unique focal point along the scan line.

- For **CW (Continuous Wave) Doppler**, a sound wave at a single frequency is continuously transmitted from one piezo-electric element and a second piezo-electric element is used to continuously record the reflected sound wave. By continuously recording the received signal, there is no aliasing in the received signal. Using this signal, the blood flow in veins can be estimated using the Doppler frequency. However, since the sensor is continuously receiving data from various depths, the velocity location cannot be determined.

- For **PW (Pulse Wave) Doppler**, several pulses are transmitted along each scan line and the Doppler frequency is estimated from the rela-

tive time between the received signals. Since pulses are used for the signaling, the velocity location can also be determined.

- For **Color Doppler**, the PW Doppler is used to create a color image that is super-imposed on top of B-mode image. A color code is used to denote the direction and magnitude of the flow. Red typically denoted flow towards the transducer and blue denotes flow away from it. A darker color usually denotes a larger magnitude while a lighter color denotes a smaller magnitude.

- **Harmonic Imaging** is a new modality where the B-mode imaging is performed on the second (or possibly other) harmonics of the imaging [3]. Due to the usual high frequency of the harmonic, these images have higher resolution than conventional imaging. However, due to higher loss, the depth of imaging is limited. Some modern ultrasound systems switch between harmonic and conventional imaging based on depth of scanning. This system imposes stringent linearity requirements on the signal chain components.

1.2.1 Harmonic Imaging

When sound propagates through the body, it is composed of a group of frequencies that defines its spectral content. If the ultrasonic wave consists of a single frequency (the fundamental frequency), then it forms a sine wave passing through tissue. Harmonic frequencies are those that occur at a multiple of the fundamental frequency. In classic physics teaching, ultrasonic energy propagates by a linear process, meaning that new frequencies cannot

be created. Attenuation may differentially affect some frequencies more than others. Therefore the spectral content may change with propagation, but frequencies absent in the original wave cannot subsequently appear. However, it has become apparent recently that there are nonlinear acoustic effects active in ultrasonography. The nonlinear effects of the interaction of ultrasound with matter (both on propagation and reflection) may create frequencies not present in the incident beam. These two ways of generating harmonic frequencies (reflection and propagation) define the very different applications of harmonic imaging in contrast and noncontrast imaging.

When ultrasound strikes contrast microbubbles, these may vibrate (and hence retransmit) at second and higher multiples of the insonifying frequency [18, 19, 20, 21, 22, 23]. Because tissue reflection generates very little of this harmonic energy, tuning the ultrasound receiver to the second harmonic frequency will preferentially display the contrast agent within the image [24, 23]. There is much more to be said about contrast harmonics, but the remainder of this review will focus on tissue harmonic imaging. Tissue harmonic imaging differs fundamentally from contrast harmonic imaging in that the harmonic frequencies are mostly generated on propagation through tissue, not on reflection from an object.

This was characterized quantitatively as long ago as 1962 by Eq. 1.5, where P_2 is the second harmonic, $\frac{B}{A}$ is nonlinear parameter of the tissue medium (5.2 for water), f is frequency of insonification, ρ is density of the tissue medium, v is acoustic velocity, p_{ac} is applied acoustic pressure, and d

is distance of propagation [25].

$$P_2 \approx \left(\frac{B}{A} + 2\right) \frac{\pi f}{2\rho v^3} \cdot d \cdot p_{ac}^2 \tag{1.5}$$

One way of understanding frequency generation is to realize that water (and tissue) is not a completely incompressible medium. Thus at the peaks of pressure, water is slightly denser than it is at the troughs of pressure. This change in density also affects how sound travels through water. Sound travels just a little faster at the peaks of waves than in the troughs. This leads to a very slight change in the shape of the wave as it propagates. At each instant in wave propagation, an infinitesimal amount of harmonics is generated.

Eq. 1.5 illustrates two aspects of harmonic generation that are critical to their utility in improving image quality:

- the growth with distance of propagation;
- the nonlinear relation between source pressure and second harmonic pressure.

The rise in harmonic frequency energy with transmission distance (shown by the linear factor d in Eq. 1.5) follows predictably from an understanding of how harmonic frequencies are generated. At the transducer surface, the ultrasound pulse is composed only of the fundamental frequencies. As soon as it propagates through tissue, however, energy builds at the second harmonic frequency. After a few centimeters of distance, enough energy has been converted from the fundamental frequency to yield a significant second harmonic frequency energy wave (Fig. 1.10). Because much of the artifact

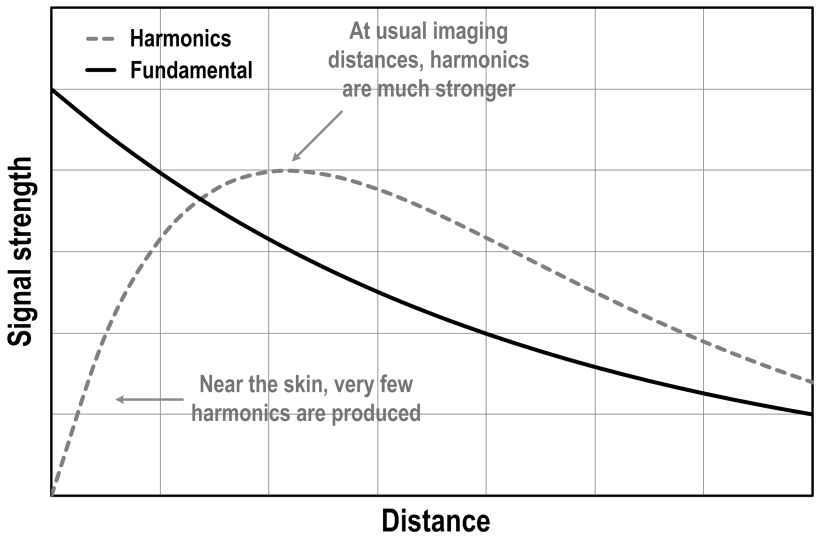

Figure 1.10: Relation between imaging distance and strength of fundamental and harmonics frequencies.

in an echocardiographic image is related to reverberations and scattering at or near the chest wall, these artifacts contain relatively little harmonic frequency energy. If imaging is confined to the harmonic range, then much of the nearfield artifacts are eliminated.

The second key aspect of harmonic imaging, the nonlinear relation between fundamental frequency energy and harmonic frequency energy, can be understood by considering again how the harmonic frequencies are generated. Harmonics are generated by the change in density of water and the changes in sound velocity through water. These are changes that occur more dramatically with higher energy waves than lower energy waves. Thus the generation of harmonics is related nonlinearly (the squared relation between P_2 and p_{ac}) to fundamental frequency energy. Fig. 1.11 illustrates such a relation whereby weak fundamental frequencies produce almost no harmonic frequency energy, whereas strong fundamental waves generate considerable

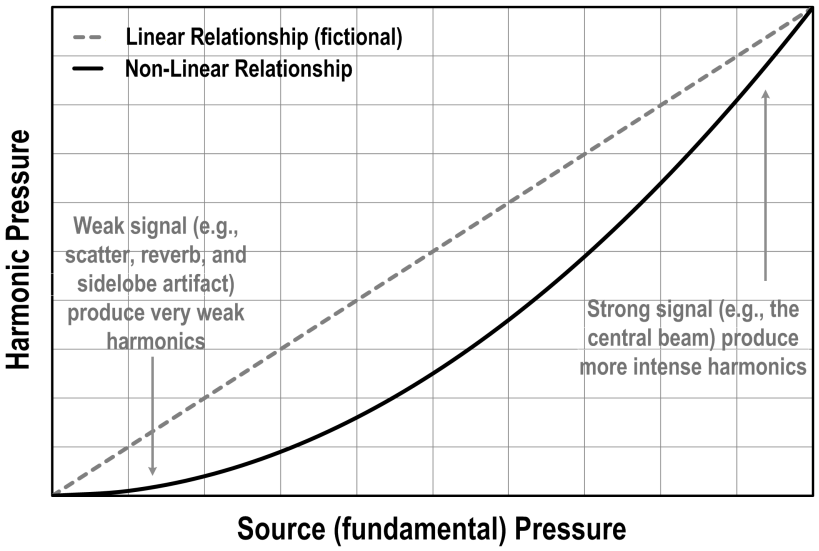

Figure 1.11: Schematic showing relation between pressure in source (fundamental) wave and pressure at harmonic frequency.

harmonic frequency energy. This is critically important because much of the artifacts in echocardiography result from aberrant propagation that is considerably weaker than the central imaging beam.

It is important to remember that even in the most extreme circumstances, the amount of harmonic frequency energy returning from tissue is much less than that returning at the fundamental frequency. Because all of the benefit of harmonic frequency energy imaging is obtained by elimination of the fundamental frequency, three critical instrumentation issues must be adhered to. First, the instrument must have wide dynamic range. With harmonic imaging, we are losing 10 to 20 dB of signal strength. To preserve the signal-to-noise ratio, it is essential that very wide dynamic range be available for imaging this relatively weak signal. Second, the transmitter must emit very little energy at the harmonic frequency. It might be thought that a 2 MHz

imaging beam would have a spectrum only at 2 MHz, but the requirements of short pulses in ultrasound currently ensures that both higher and lower frequencies are present within the transmitted signal. For example, if nine waves of a 2 MHz signal are transmitted as a square pulse (Fig. 1.12a), then the spectrum (Fig. 1.12b) shows energy as far out as 6 MHz, with considerable energy present at the desired harmonic frequency of 4 MHz. In contrast, if the transmitted pulse has a smooth onset and offset, then the frequencies are contained in a narrower band. Specifically, a gaussian-shaped pulse (like a bell curve, Fig. 1.12a) will have a gaussian-shaped spectrum that falls to zero energy at twice the fundamental frequency. Thus the short but rounded pulse contains almost no energy within the desired harmonic band (Fig. 1.12b). The final requirement is for a sharp receiver filter within the imaging chain, so that only the harmonic frequencies are passed to the demodulator. When these technical requirements are met, the improvement in image quality can be quite significant [17].

1.2.2 Apodization

Spatial weighting of the aperture is known as apodization and is analogous to time-domain weighting in signal processing. Apodization is sometimes used for transmit and receive beam formation. In this case the amplitudes of the output waveforms across the aperture are modified using a windowing function (for example, a Hamming window). This is typically implemented using multilevel pulsers or linear amplifiers. Apodization is used in order to reduce the presence of imaging artifacts caused by sidelobes of the ultrasound

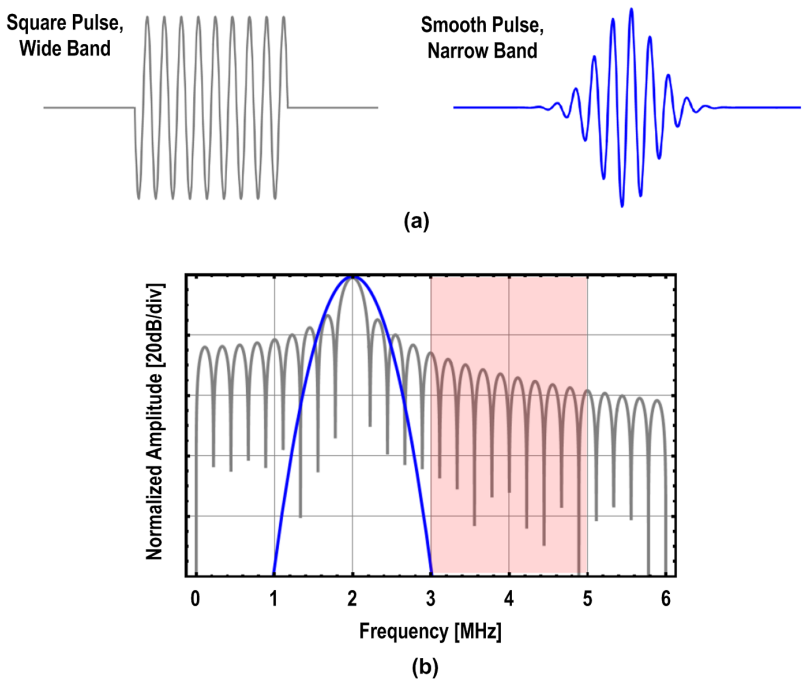

Figure 1.12: Comparison of wide band and narrow band ultrasound pulses.

beam [26]. Side lobes are smaller lobes of transmit energy on either side of the main beam which are generated naturally as part of the beam-formation process as illustrated in Fig. 1.13b. The drawback is that the main lobe becomes wider with consequent reduction in lateral resolution (Fig. 1.13a).

1.2.3 Pulsers

A standard architecture for an ultrasound pulser is shown in Fig. 1.14. The circuit uses DMOS devices in the output stage in order to implement a half-bridge to charge the transducer load capacitance up to HVP and then down to HVN. In a unipolar pulser, the signal swings between HVN and HVP, where HVN in this case is simply ground. The peak-to-peak transmit voltage is typically on the order of 300 V, and in some portable systems it could be

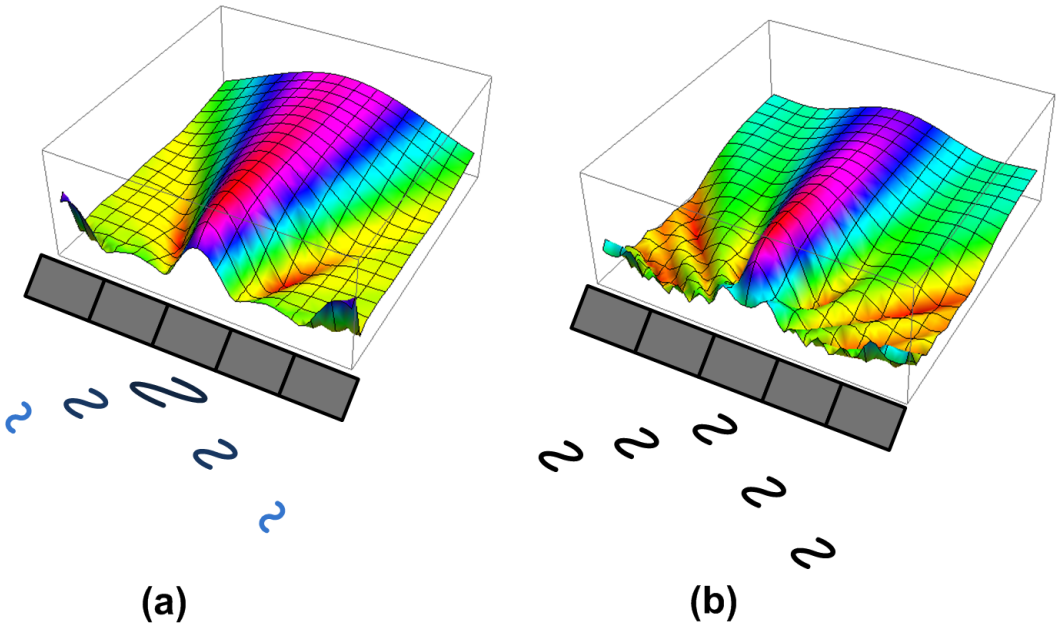

Figure 1.13: Acustic pressure with (a) and without (b) apodization.

closer to 50 V. In a trilevel (or bipolar) pulser, the output voltage swings between HVN and HVP and returns to a ground level when the cycle is completed as shown in Fig. 1.14.

Return to zero is accomplished using the clamping circuit formed by M3 and M4 in conjunction with D1 and D2. The diodes are used to prevent the clamp from turning on when the voltage swings above and below ground. This could occur if, for example, the gate of M4 was biased at ground (i.e., off state) and its drain was dropped more than 5 V below ground. Since this situation happens each time the output drops to HVN, the diode D2 is inserted to prevent M4 from turning on. In a unipolar pulser, this circuit is not needed.

Control of the output MOSFETs is accomplished using level shifters that

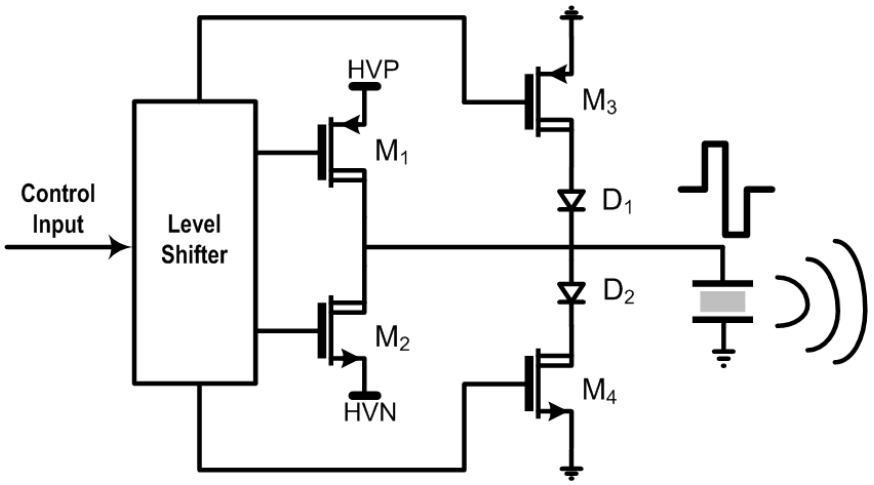

Figure 1.14: Bipolar ultrasound pulser.

take the transmit timing signals generated by a low-voltage circuit referenced around 0 V and shifts them up to the positive high-voltage HVP and down to the negative high-voltage HVN. This circuit could be composed of a resistor capacitor circuit or could also be given by a transmit latch [34] or a current mirror. The level shifter needs to be sized such that it can drive the input capacitances of the large output devices fast enough to switch the devices within the required rise time of the output waveform. This current can often be a significant power draw in itself.

The output devices are sized such that they can drive the output load fast enough to satisfy the rise-time requirements. The load can be approximated to first order as a capacitance. In the case of pulsers in the system, this capacitance consists, in large part, of the cable capacitance C_c, which typically is on the order of 100 pF or more. The transducer is modeled to first order as a capacitance C_d which can be as large as 40 pF for a linear probe.

In addition to the transducer and cable load capacitances, a significant additional parasitic capacitive load is provided by the output devices themselves. These include the drain-to-bulk capacitance C_{db} as well as the drain-to-source parasitic diode capacitance C_{ds}. Both the NMOS and PMOS devices must be accounted for. In addition, routing capacitance C_p can be important, depending on the interconnect technology used. The total load consists of each of the above-mentioned capacitances in parallel and is therefore given by Equation 1.6.

$$C_{load} = C_d + C_c + 2(C_{ds} + C_{db}) + C_p \tag{1.6}$$

The required output current for rise time, trise, is given by Equation 1.7.

$$I_{rise/fall} = \frac{C_{load}\Delta V_{out}}{\Delta t_{rise/fall}} \tag{1.7}$$

The output devices and clamp circuit will therefore be sized in order to drive this current along with some margin to account for variations in DMOS I_{ds} which may be significant.

In second harmonic imaging, the output waveform must be completely symmetric in order to avoid generation of any spurious transmitted signal power at the second harmonic frequency. Therefore, it is important that the pull-up and pull-down devices as well as the clamp be well-matched so that their rise times are as close to identical as possible. Also, in Doppler mode the requirement for very low phase noise means that jitter in the control circuitry must be minimized as much as possible.

Power dissipated by the unipolar pulser is given by

$$P = CV^2 fN \tag{1.8}$$

where C is the total load capacitance, V is the peak-peak output voltage, f is the pulse repetition frequency (PRF), and N is the number of pulses that occur during one complete transmit cycle. The square law dependence on voltage makes heat dissipation a challenging problem at high transmit voltages.

Multilevel pulsing can be used in transmit beam forming for apodization of the transmit aperture. Multilevel pulsers are also used for transmitting Gaussian-shaped pulses or chirps. Figure 1.15 shows examples of different multilevel pulse shapes that are typically used. Fig. 1.15a shows apodization on multiple parallel channels where channel 1 transmits at a peak voltage of V_1, channel 2 transmits at a peak voltage of $2V_1$, and channel 3 transmits at a peak voltage of $3V_1$. Figure 1.15b shows transmission of a shaped pulse, here a Gaussian pulse that has improved acoustic properties.

A circuit capable of implementing some of the waveforms in Fig. 1.15 is shown in Fig. 1.16. Two half-bridges are used to drive a single transducer. The first output stage is biased at HV1 while the second output stage is biased at HV2. The voltages HV1 and HV2 can be set with complete freedom by the system on each transmit cycle. The use of two output stages allows for instantaneous switching between pulsing at output voltage HV1 and pulsing at output voltage HV2. Rapidly switching between the two output stages shown in Fig. 1.16 in order to generate a color flow Doppler sequence

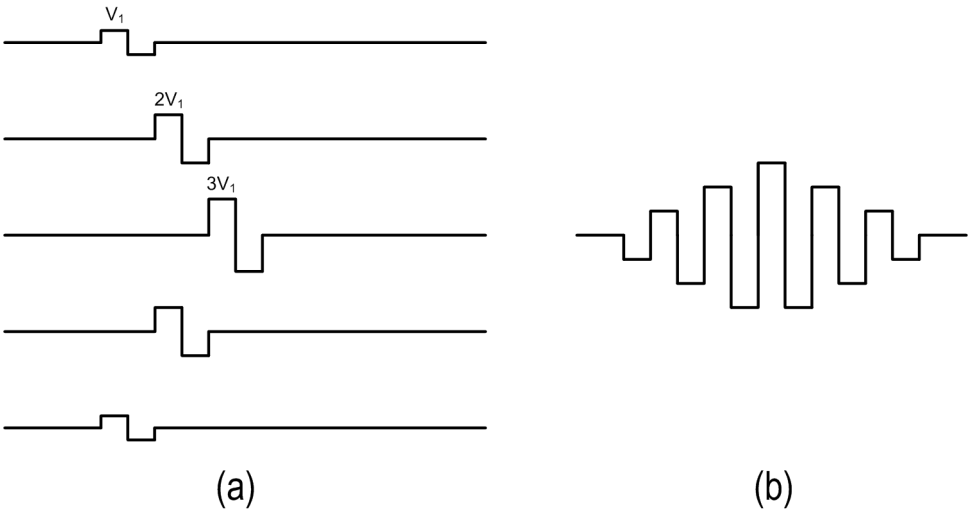

Figure 1.15: Multilevel pulser waveforms. (a) Apodization on multiple channels showing changing amplitude on different channels. (b) Example of temporal apodization on the transmit pulse in the form of a Gaussian pulse.

requires the diodes D1 and D2 which prevent the output devices in the lower-voltage transmitter from turning on while the highervoltage pulse is being transmitted.

The waveform of Fig. 1.15 can be generated using multiple channels where each channel has a different transmit voltage supplied by the system. Although these voltages can be updated on each transmit cycle to achieve the desired apodization envelope across the array, switching the supply voltages is usually undesirable due to the high power consumption on the power supplies.

1.2.4 Arbitrary Waveform Generators

In ultrasound imaging, spatial resolution increases as the transmit frequency increases, but so does the attenuation, sacrificing depth of penetration [27].

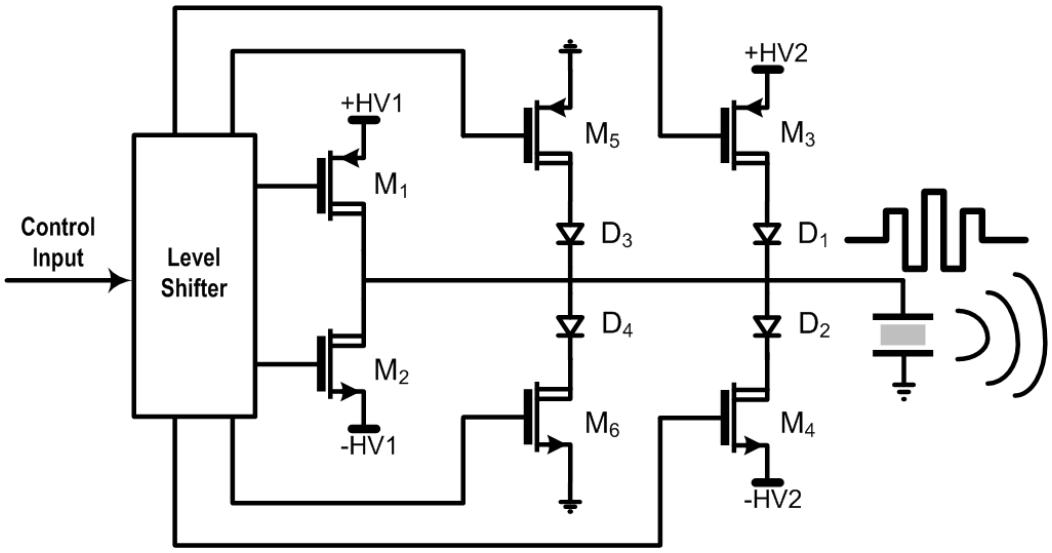

Figure 1.16: Two-level capable pulser circuit.

This drawback may be compensated by raising the excitation voltage of an ultrasonic transducer or by elongating the length of the transmit waveform. An elongated burst delivers more energy to a focal depth than does a one- or two-cycle pulse when the same transmission voltage level is applied [28].

Coded excitation that uses an elongated burst has long been known to be capable of enhancing the penetration depth of ultrasound while maintaining its spatial resolution. There are two types of coded excitation approaches: phase modulation and frequency modulation. Chiao et al. [29] compared these two methods and discussed the advantages and the disadvantages of each approach. Although systems for phase modulation transmissions are simpler to implement utilizing switching circuits [30], the levels of range side lobes are affected by phase distortion during acoustic propagation in a nonlinear media. In contrast, frequency modulations, i.e., chirp-coded excitation, result in smaller range side lobes (<40 dB) and need only single transmissions

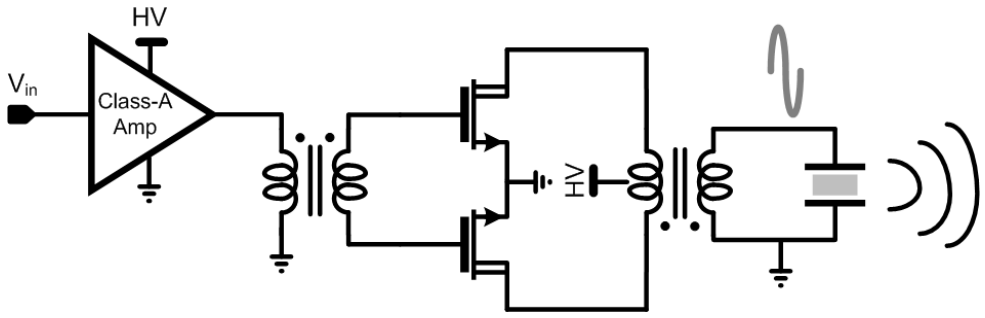

Figure 1.17: The block diagram of the linear arbitrary waveform generator.

to form one scan line.

The need for coded excitation in high-frequency ultrasound (>30 MHz) imaging is more crucial than in lower frequency ultrasound (<20 MHz), because of the attenuation at higher frequency in tissues [27].

In implementing chirp-coded excitation imaging, a functional burst generator is of paramount importance. The AWG presented in [7, 31] consists of two stages; Fig. 1.16 shows a schematic diagram of the implemented circuit. The first stage is a class-A amplifier intended to amplify an input signal with the least distortion. This stage drives a broadband signal to the second stage, adapting a custom-designed 1:1 transformer. The second stage is a class-AB amplifier. A push-pull circuit topology maximizes the amplification rate of the linear power amplifier and the final output is coupled with a center-tapped 1:1 transformer. Output stage with NMOS only and transformer allows very high symmetry in the output signal (low distortion) but this solution is not suitable for monolithic integration, due to excessive area consumption of this component. For this reason this topology is adopted only in high-end machines and not suitable for portable applications.

Another technique to improve the PA's linearity is to pre-distort the input

signal to cancel out the nonlinearity of the PA. This approach senses the output signal, calculates the distortion errors as the difference between the ideal output and the actual output, and equalizes the input waveforms to cancel the PA's nonlinearity. This technique has been widely used in RF transmitters with demonstrated effective improvement on the PA's linearity [32, 33, 34, 35]. However, the same idea has not yet been applied in ultrasound transmitter designs to improve the transmitting signal linearity.

In [36, 37] is presented a look-up table (LUT)-based digital predistortion (DPD) system for ultrasonic transmitters. The DPD scheme is implemented in the digital domain and the algorithm is divided into two stages: calibration and evaluation. During the calibration stage, the system searches for the optimal error based on the output signal using a least-mean-square (LMS) method, and stores the error in the LUT memory. In the evaluation stage, the phase of the input signal is used as the word address to access the error in the LUT. The error is added into the input to generate an equalized signal. Then, the equalized inputs are converted into analog signals through the digital-to-analog converter (DAC) and sent into the class-AB PA to cancel the PA's nonlinear characteristics (Fig. 1.18). The proposed algorithm works for both constant-amplitude sine-wave signals and amplitude-windowed signals such as Morlet wavelets.

1.3 Transducers

Since their introduction, ultrasound machines have for the most part used piezoelectric materials for transduction. The most popular material is lead

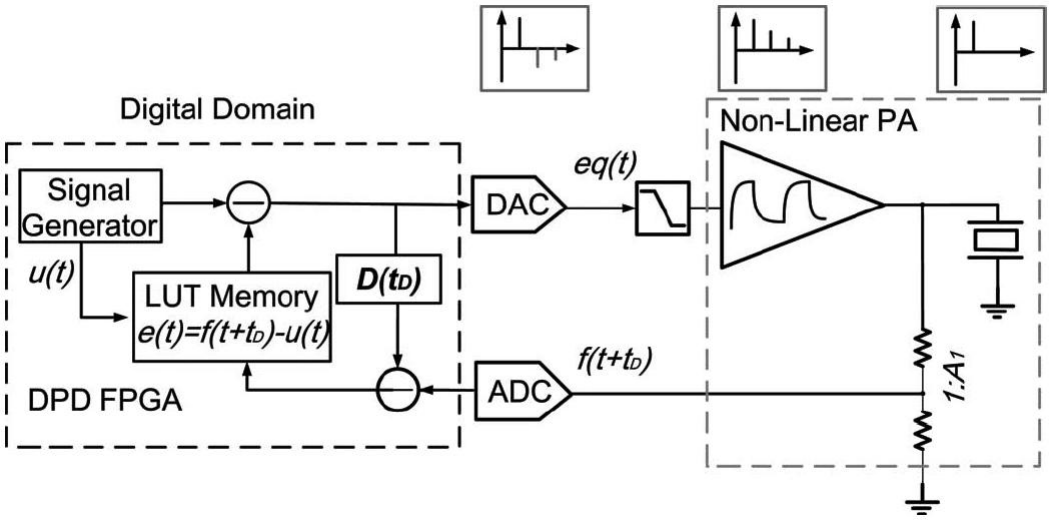

Figure 1.18: The block diagram of the digital predistortion system.

zirconate titanate, which is a ceramic that is also known as PZT. The typical PZT transducer is shown in Fig. 1.19 and consists of an acoustic–electric material (PZT) that is sandwiched between two electrodes. When a voltage is applied to the electrodes, the electric field causes the piezoelectric material to deform mechanically. Since the material is coupled to the body through matching and lens layers, acoustic energy in the form of sound waves is transferred from the transducer into the body for imaging. On receive, vibrations from the body are transferred back to the transducer, which causes the transducing material to deform mechanically. These deformations change the distance between two electrodes, thereby generating an electrical signal in response to the acoustic input. Typical values for the receive voltage range between a few microvolts rms and 100 mV rms. The acoustic lens shown in Fig. 1.19 is a material such as silicone, which can be shaped to focus the beam in elevation. An acoustic matching material is used between the piezo-

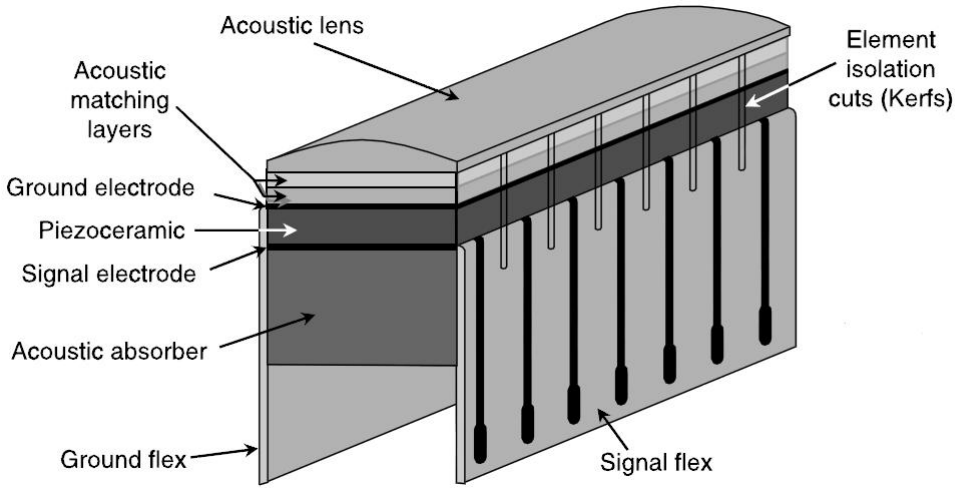

Figure 1.19: Construction of 1D linear PZT ultrasound probe array.

electric material and the lens in order to improve transfer of acoustic energy from the PZT elements into the body. The backing material is an acoustic absorber such as scatters in an absorbing matrix which damps reverberations and reduces crosstalk. Connection to the elements is typically made using a flexible circuit assembly with very fine line spacing in order to match the pitch of the elements.

1.3.1 Transducer Performance Characteristics

The dimensions of the PZT transducer determine the key performance characteristics of the device. The impulse response of the transducer is used to derive the frequency response of the device by transformation to the frequency domain. The frequency domain plot provides information on a number of important transducer performance parameters. Bandwidth can be quoted either as one-way or two-way (pulse-echo) measurements. One-way signifies

the transmit or receive bandwidth alone and two-way signifies the transmit bandwidth multiplied by the receive bandwidth. For a single transducer the one-way bandwidth is given by the -3dB frequencies while the two-way bandwidth is given by the -6dB frequencies. In second harmonic imaging, it is important to be able to image the receive signal at higher frequencies so a wider bandwidth is preferable. Fractional bandwidth is a measure of the range of frequencies over which the transducer will operate and is given by

$$FB = \frac{f_H - f_L}{f_C} \tag{1.9}$$

where f_H is the upper -3dB point, f_L is the lower -3dB point, and f_C is the center frequency.

Typical fractional bandwidth for PZT is on the order of about 70% whereas for cMUTs, it can be as high as 110%. Since higher resolution applications require higher imaging frequencies, a device with a larger fractional bandwidth has the potential to cover a broader range of applications with a single probe. Figure 1.20 shows the frequency response of a number of different transducers superimposed, including PZT and cMUT, to show how the bandwidth of these devices differs by application. cMUTs are a promising device for general imaging since they can be used to cover a broad range of imaging applications. Center frequency is the frequency at which imaging is nominally performed. Resonance frequencies are the natural modes of resonance of the transducer in conjunction with the case capacitance.

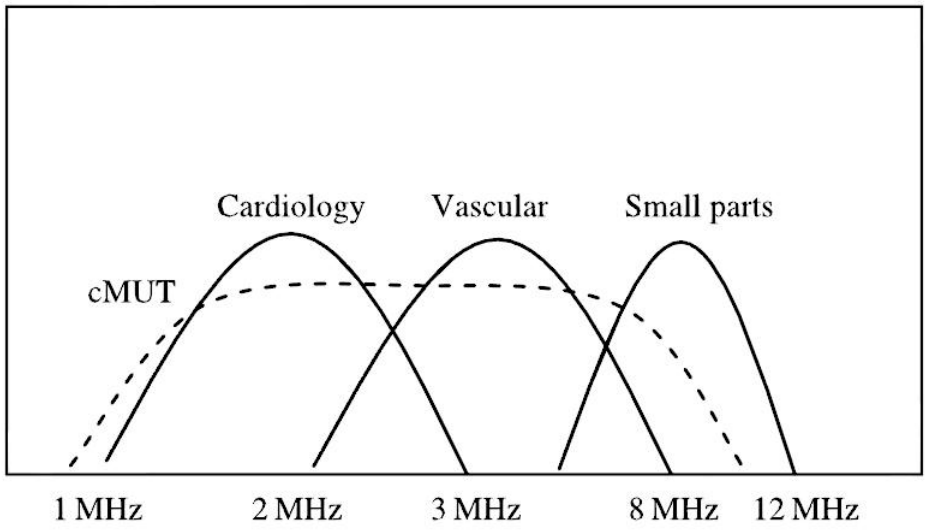

Figure 1.20: Frequency response of some currently available ultrasound probes and potential cMUT-based probes.

1.3.2 Modeling

Electrical models mimic the electrical impedance looking into the transducers from the electrical port as shown in Fig. 1.21. They may also be used to model the acoustic output for a given electrical input as represented by a voltage equivalent of the acoustic output power.

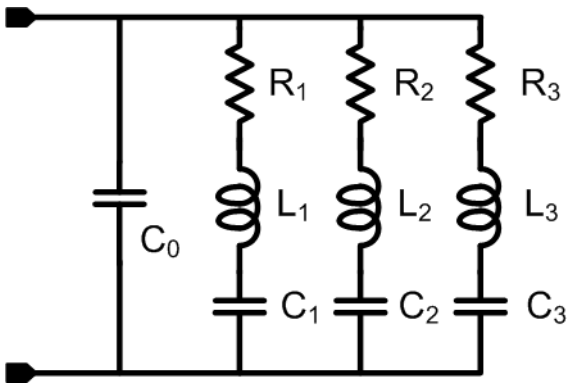

Figure 1.21: Electrical impedance model of PZT transducer.

The simplest model of a loaded transducer (neglecting electro-acoustic effects) is that of a parallel plate capacitor, C_0, which appears between two plates separated by a distance d, each with a plate area A and an insulating material (most often PZT) with dielectric constant ε_S between them. In this case, C_0 is given by Equation 1.10 [26].

$$C_0 = \varepsilon_S \frac{A}{d} \tag{1.10}$$

The capacitance C_0 is a reasonably accurate first-order approximation of the behavior of the device as a load at frequencies other than resonance and is often referred to as the bulk capacitance. A more accurate model of the transducer will take into account the resonant behavior that is due to the natural modes of operation of the device. A simple approximation of this behavior can be obtained using linear circuit components as shown in Fig. 1.21. Here the bulk capacitance C_0 also appears and can be calculated using the equation above. In addition, an RLC circuit is added to model the resonance of the transducer. Multiple RLC branches can be added to represent additional resonant modes and obtain increasingly accurate representations of the full behavior of the device. More sophisticated models of the transducer, such as the KLM model or the Mason model [38], can be used to simulate both the electrical impedance behavior of the device as well as energy transformation from the electrical to the acousto-mechanical domains and vice versa.

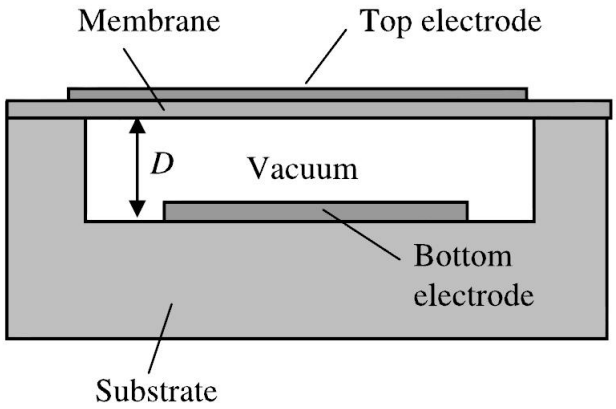

Figure 1.22: cMUT Cross section showing vibrating membrane and top electrode suspended above substrate comprising static bottom electrode.

1.3.3 Alternative Transducer Technologies

While PZT remains the gold standard material for ultrasound transducers, it has a number of features that are somewhat undesirable. The requirement to form individual elements by mechanically dicing the material makes it difficult to create large 2D arrays of very small elements for volumetric imaging. In addition, the low fractional bandwidth of PZT makes it difficult to use a single probe to cover a number of imaging applications. Also, it is difficult to fabricate PZT array elements that operate at high frequencies, which makes it unattractive for use in very high resolution applications. Lastly, the current manufacturing process for PZT makes it difficult to integrate efficiently with associated front-end electronics.

To address some of these issues, a number of groups have been working in recent years on alternative technologies. These include capacitive micromachined ultrasound transducers (cMUTs) [39, 40, 41, 42, 43] and piezoelectric micromachined ultrasound transducers (pMUTs) [44, 45].

cMUTs are micromachined devices that are manufactured using standard semiconductor processing. Figure 1.22 illustrates a cross section of a cMUT device. These operate in a fashion similar to that of the PZT except that there is no piezoelectric material. Instead, the electrodes are separated by a cavity that is typically evacuated and sealed. The distance between the electrodes, D, is on the order of a few hundred nanometers. This very small separation greatly increases the electric field across the electrodes. In addition, the electrodes themselves are composed of very thin material; typically, the top electrode covers or is comprised of a membrane that is free to vibrate. The large electric field and thin electrodes make it possible to generate sufficient electro-acoustic conversion without the requirement for a piezoelectric material. The operating frequency and output power of the devices is directly determined by the thickness of the cavity and the thickness of the suspended membrane [46]. There are currently two ways to manufacture cMUTs: surface micro-machined devices are processed in a thin layer on the surface of the wafer. They are typically manufactured by etching shallow cavities in the bulk silicon wafer and covering these with a silicon nitride membrane to form the top electrode. The bottom electrode can be formed with either a deposited metal layer or by using a highly doped silicon wafer for the substrate.

Bulk micromachined devices are processed using silicon on insulator (SOI) bonding techniques [47]. The use of SOI wafers allows the resonant cavities to be precisely defined in the active silicon layer of the first SOI wafer. The resonant membrane is formed out of the active Si layer of the second SOI wafer with the bulk section etched back to reveal the membranes.

Chapter 2

BCD Technologies

Once a specialty market, Power Integrated Circuit Technology has grown in recent years to become a major business worth more than a billion dollars. The growth rate has also become more constant, too, as the market matures and the opportunistic method of choosing applications gives way to a more systematic approach to the market.

At the same time, however, there has been a revolutionary change in the way that Power IC Technology is applied. Every system consists of a central core of processing elements isolated from the outside world by an umbrella of interface functions. The classic approach to partitioning is to divide these functions among a number of integrated circuits, each realized by a single-function technology like CMOS or bipolar. In smaller systems, however, it is necessary to combine different functions on one chip to minimize the component count. Moreover, since most systems involve some kind of interaction with actuators there is usually some sort of power element on the chip. As a result these circuits are best realized using mixed power

technologies.

While single-function technologies evolve towards finer lithographies and higher speeds, there is a corresponding evolution in mixed technologies, as more functions are included to make more versatile technologies. The trend, in fact, is towards a modular approach where basic technology steps are designed to be compatible so that additional functions can be integrated when they are needed, at the expense of a few more mask steps.

Today mixed technologies are capable of integrating CMOS macrocells as complex as microcomputer cores. They are also able to integrate non volatile memory. With this capability many small systems can now be integrated into a single chip. Eliminating external connections to dice reduces cost and increases reliability at the expense of added complexity on the die [48].

These processes are commonly used to implement display drivers and for automotive applications. They are also ideally suited for implementing high-voltage circuits required in ultrasound systems.

Ultrasound transducers are driven at high voltages in order to increase the output power, causing larger signals to be received from the body. Design of the transmit circuitry must therefore balance minimizing exposure to the patient while still transmitting enough acoustic power to yield acceptable image quality. Transmit electronics (Fig. 2.1) comprise the transmitters, multiplexers, and transmit/receive switches, all of which are implemented using BCD processes.

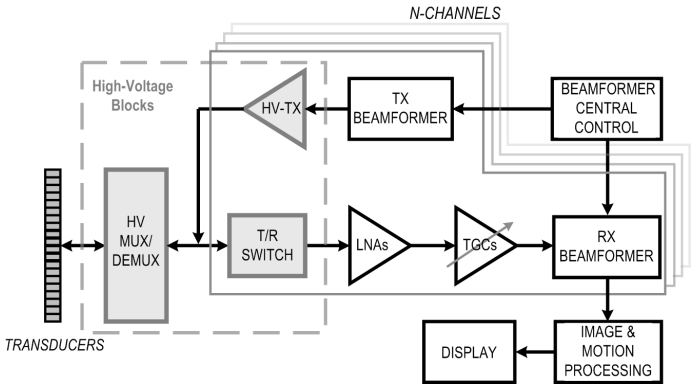

Figure 2.1: High-voltage blocks in ultrasound system.

2.1 Smart Power Technology Classification

Several different technological approaches to smart power have been explored, but all such technologies share the same basic concept of merging different structures into the same chip, tajing advantage of the similarities in processing techniques.

Smart power technologies share many characteristics and may be conveniently classified according to the isolation technique (dielectric, self or junction isolation), by the power device structure (DMOS, bipolr, IGBT or SCR) and by the position of the drain/collector contact (on the surface or the back of the die).

2.1.1 Isolation Techniques

Dielectric Isolation

Dielectric isolation allows the realisation of silicon islands completely surrounded by oxide with advantages such as the low parasitic capacitance of

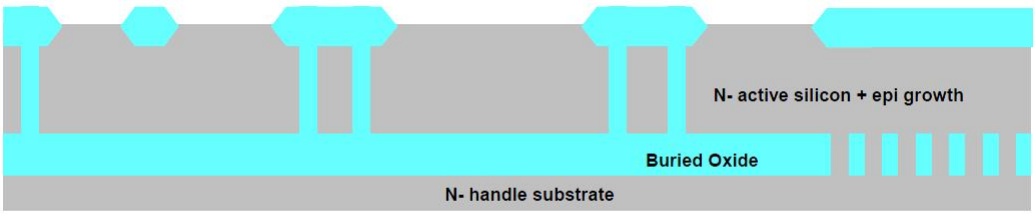

Figure 2.2: Dielectric isolation approach using narrow trenches filled with SiO_2 and polysilicon.

components to substrate, the absence of leakage current and a reduction in the size of high voltage components. However, this method requires a more complex and costly manufacturing process.

Moreover since oxide is a poor conductor of heat it limits the integration of power devices.

Today the most promising dielectric isolation approach is based on the SOI (Silicon on Insulator) substrate obtained by Silicon Direct Bonding technique with isolation plugs realised by trench etches (Fig. 2.2).

Self-Isolation

Self isolation is used when the integrated devices do not need to be completely isolated because some terminals are shared.

In this case the process is very simple and generally consists of a basic flowchart, for example CMOS and DMOS, to which a few extra steps are added to integrate additional structures. On the other side, this technique is not very flexible and is more susceptible to parasitic effects connected with biasing and supply.

Self- isolation lends itself to the integration both of high voltage and of

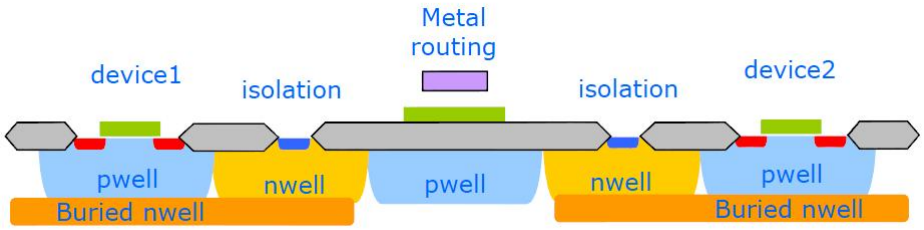

Figure 2.3: Junction isolation approach.

high current devices. In high voltage devices the most common approach is carried out with the drain/collector contact on the top of the chip. Typical applications are display drivers and PWM controllers. In high current devices the drain/collector contact i usually positioned on the rear of the chip.

Junction Isolation

With the junction-isolation technique the separation of the silicon islands where the various components are integrated is obtained through reverse-biased junction realised by diffusing P regions through the entire depth of the N-type epitaxial layer grown on a P-type substrate (Fig. 2.3). This technique is the most widely used because it offers the best compromise between cost and versatility. With various methodologies it is possible to extend the applicability of this technique to both lateral and vertical structures, high voltage and high current.

2.1.2 Integrated Power Structures

The most common power device used in a Smart Power Integrated Circuit is the DMOS transistor for the well-known advantages that it offers compared

to bipolar transistors.

Several kinds of new power devices like IGBTs, IEGTs, ESTs, MCTs, just to mntion the major ones, have been developed to compete with the performences of DMOS in high voltage and high current applications, but all these approaches are only aimed at market niches. Besides, as these are SCRs or thyristor -based structures, to overcome the problems coming from the current injection into the substrate, that can be a limiting factor to make them suitable as power elements in an integrated circuit, more recently the majority of these developmentshave been realised on SOI substrates.

Vertical & Horizontal Structures

As far as the geometry of power device integration is concerned, the positioning of the drain/collector contact on the surface or the rear of the chip is determined not only by technology but also by the needs of the application.

In a vertical structure the current flows through the device from the top to the bottom, across the substrate and the die attach area to the package itself (Fig. 2.4). This scheme, with the substrate above ground potential, is like that of discrete power devices with the addition of an isolated structure containing the control circuitry. The vertical structure allows very high current densities but there is the limitation that in one chip is only possible to integrate one power transistor, or several with the collectors or the drains shared.

In a horizontal structure the current enters and leaves the chip through the upper surface of the chip. In this case, too, an isoleted structure can be

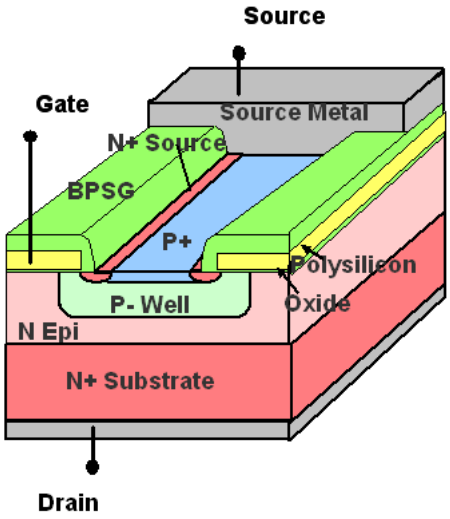

Figure 2.4: Vertical structure.

added that contains the control circuitry. This structure is derived from the adopted in standard power integrated circuits where the substrate is simply a mechanical support and a heat conductor. In the horizontal structure several variations can be distinguished on the basis of the current and voltage required.

Low Voltage High Current

Using DMOS as the power element the best structure in terms of specific ON- resistance is the lateral structure for voltage operation of few tens of volts.

High Voltage Low Current

The horizontal lateral structure that exploits the RESURF technique to reduce the surface electric field, is the most suitable for applications above

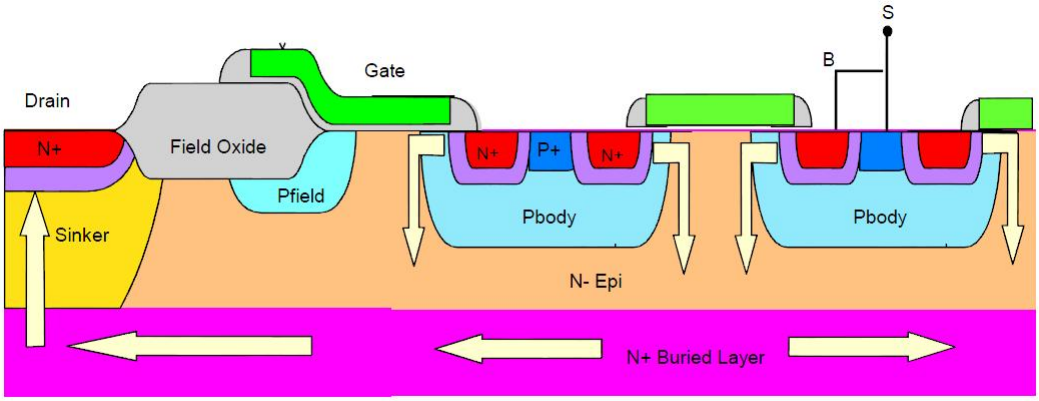

Figure 2.5: Mixed horizontal/vertical structure.

250-300V.

In the junction-isolation approach this solutions is generally limited to electrical configurations where the source floating capability is limited to few tens of volts.

This limitation can be overcome using a SOI approach.

Medium Voltage Medium Current

In mixed horizontal/vertical structures the current flow is vertical in the power device structure but the current is brought to the surface through buried layers and sinkers (Fig. 2.5). This approach allows the integration of any number of power devices connected in any way; in addition it offers medium currents and high voltages.

2.2 BCD History and Evolution

In Fig. 2.6 the genesisi and evolution of the whole BCD process family are shown.

The given dates refer to the availability of the first working silicon.

The BCD process evolution has developed not only in the voltage direction (from 16 to 700V), but also towards the reduction of the minimum lithography that is today $0.13\mu m$ in BCD-9.

In fact, another important advantage of the BCD is the dramatic increase of complexity induced in the Power ICs. This has been possible because in the BCD technology the power component is an MOS transistor where the current density depends on the geometrical ratio W/L (channel width/channel length) that can be improved simply by reducing the line width. Differently, in the power bipolar components the current density depends on the emitter area and therefore progress in microlithography does not bring any appreciable improvement in density.

With the appearance, in the early nineties, of the third generation at $1.2\mu m$ (BCD-3) where non-volatile memories (EPROM and EEPROM) are integrable too, the complexity level reached in the BCD processes has allowed to generate a new complete class of Power ICs, named "System Oriented".

This names comes from the capability of these circuits to integrate into a single monolithic solution entire systems, previously realised with more chips made with single-function technologie, like pure CMOS, bipolars and non-volatile memories.

In applications where space is limited this approach is very useful because

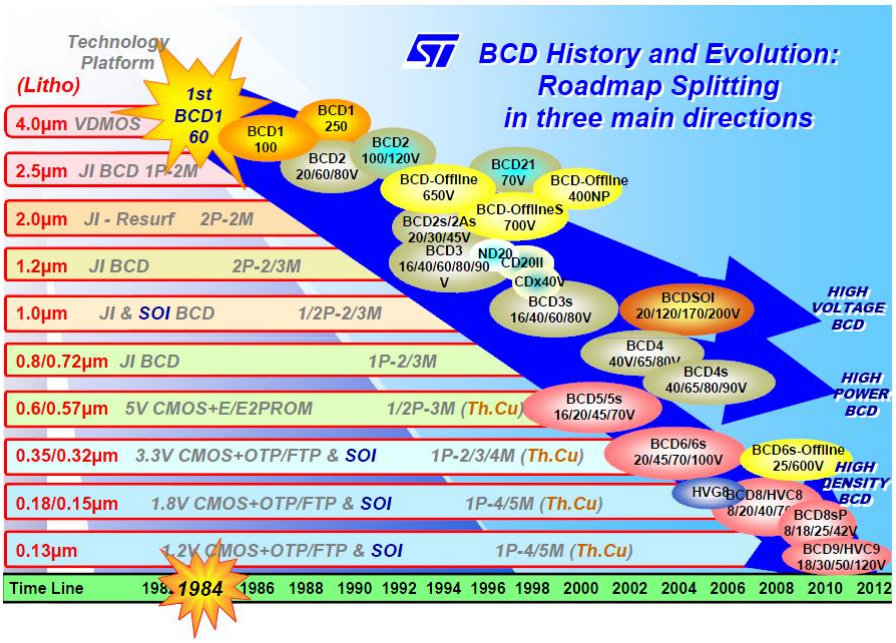

Figure 2.6: Genesis and evolution of the BCD process family.

it reduces complex systems to a minimum number of chips, just one in some cases. The trends towards portable equipment brings a need for space reduction but at the same time reduces power requirements, encouraging the move to solutions of this type.

The architecture of the third generation is based on the concept of modularity where additional process blocks for optional structures and components can be added to a basic process flow-chart without creating any disturbance. The core of the process is based on a twin-well CMOS technology used to produce micro-processos, memories, gate arrays and other logic devices.

The third generation BCD is the first real example that allows designers to take advantage of existing CMOS libraries and even to include standard micro-computer cores and EEPROM memories to realize “Software Programmable Smart Power” chips.

2.3 Process Architecture and Device Technology

In this section, the major steps involved in the BCD process construction are comprehensively listed and described to reach a complete understanding of the process architectures and of the function of each step putting them in relation with the integrable components.

In alla BCD processes the construction sequence strats from a <100> P-type substrate whose doping level is chosen in according to the maximum required voltage capability.

The key processing steps are:

- N+ buried layers Antimony or Arsenic doped are implanted to create low resistive paths for collector or drain current, to avoid punch-through limitation of floating P regions towards the P substrate and to kill the gain of parasitic PNP with P substrate acting as collector (Fig. 2.7a).

- N buried layers Phosphourous doped are added in high voltage processes both to increase the breakdown voltage of N+ buried layers versus substrate and to implement source follower capability in RESURF type high voltage devices.

- P buried layers are introduced with isolation function: a "seed" of dopant is implemented before epitaxial growth and in subsequent thermal treatments this diffuses upwards to meet a downward diffusion from the surface. This approach is followed to save silicon area. In fact, a simple diffusion of a single-junction isolating layer from the top would

require prolonged thermal treatments and consequently a larger lateral diffusion. In the RESURF approach P buried layers are introduced and dimensioned mainly to work together with the substrate in sustaining high reverse voltages.

- The N epitaxial layer grown at this step, is dimensioned to obtain the best trade-off between maximum breakdown voltage and minimum epitaxial bulk resistance contribution to ON-resistance when VDMOS is used as a power component. In BCD processes in which VDMOS is not implemented the epitaxial layer is only added to allow the formation of buried layers and the doping level is determined mostly by implemented N and P-well regions (Fig. 2.7b).

- Higly doped sinker plugs are realized by a Phosphorous deposition to contact N+ buried layer in order to bring up the current to the die surface in the vertical power devices (Fig. 2.7b).

- The junction-isolation structure is completed by the introduction of the top isolation (Fig. 2.7b).

- N-well and P-well regions are inserted when high density CMOS circuits are obtainable (Fig. 2.7c).

In this way, once obtained the platform to allocate the different integrable components, the BCD process flow continues with more specific construction steps aiming at the realization of the active part of the components and at the achievemnet of their performances.

- The active areas are defined in different ways depending on the process generation. To encounter the requests of much denser CMOS logic, the LOCOS technique has been adopted. this technique is based on the selective growth of a thick oxide (field oxide) on a silicon surface masked by a patterned silicon nitride. The nitride protects the underlying silicon from oxidizing, while allowing a thermal SiO_2 layer to grow on the exposed silicon: as a result the field oxide is semi-recessed under the starting surface. Therefore, the width of the base of the field oxide step defining the active area regions is reduced with respect to the tapered approach where this step is obtained by a prolonged wet etch.

- With the introduction of the LOCOS technique to form the component active areas in the BCD processes, it is also possible to obtain self-aligned channel stoppers on the CMOS body regions. These channel stoppers are formed by N and P-type regions, named N field and P field, implanted before the field oxide growth and are masked by the nitride left to inhibit the surface oxidation. Therefore, these layers can be positioned only under the thick oxide and never inside an active area. The result is the increase of the surface concentration of P well, N well, N epi and consequently of the parasitic threshold voltage of polysilicon gate on field oxide (Fig. 2.7d).

- The gate oxide is grown inside the active area and it is used in all the MOS components. The required CMOS transistor density of the new generation BCD process forces to reduce the gate-oxide thickness to values not compatible with the high voltage performances needed

in the vertical DMOS. Therefore there is a fisrt oxidation step used as gate-oxide growth for DMOS transistors only, while the gate-oxide growth for the CMOS components is shifted after the first polysilicon layer deposition and DMOS body diffusion step. In this case, a second polysilicon layer is also added and N+ and P+ source and drain implants are following.

- At this point optional implants can be added to the process flow to adjust the MOS threshold voltages.

- The first polysilicon gate electrode, deposited and N doped at this step, is also used as field plate, channel stopper and as an interconnection level (Fig. 2.7d).

- According to the modular approach, that is peculiar to the more advanced BCD process generations, additional steps can be inserted in the process flow before the polysilicon deposition in order to implementthe EPROM and EEPROM cells.

- Self-aligned N and P implants are performed and diffused to form the double-diffused channel regions of P-channel and N-channel DMOS transistors. The process parameters of these DMOS body implant and diffusion steps are key factor in the trade-off between the off-state breakdown and the on-state performance that must be stated in the high voltage power DMOS components. The P-body layer has a wide use as the base of NPN transistors and as P-channel MOS source and drain regions (Fig. 2.7e).

- Standard DDD (Double Doped Drain) and LDD (Light Doped Drain) implant (Fig. 2.9) and spacer formation steps (Fig. 2.8a) are carried out to build up source and drain extension regions of N-channel and P-channel MOS transistors to be used in high performance CMOS structures. In the same way, the availability of the spacer technique gives benefit in increasing the drain to source maximum voltage capability of compact Lateral DMOS (LDMOS) components.

- After N+ an P+ implants used to form source, drain and contact regions, a standard Boron Phosphorous Silicon Glass (BPSG) layer is deposited and the whole structure is provided with the conventional next contact opening step and with the first thin metal deposition (Fig. 2.8b).

- The following adopted metallization scheme strongly depends on the BCD process generation and can be distinguished in two major families: the single level, double thickness metal process and the multiple level, multiple thickness metal process. The latter has been imported in the BCD processes to make the CMOS part compatible also in the interconnection scheme with pure CMOS processes. In this way, the portability of complex logic circuits is guaranteed and the advantage of the VLSI design can be fully exploited. Anyway, this scheme has been adopted to the Smart Power IC requirements, dimensioning the last metal level thickness in order to be used in the power components (Fig. 2.8c).

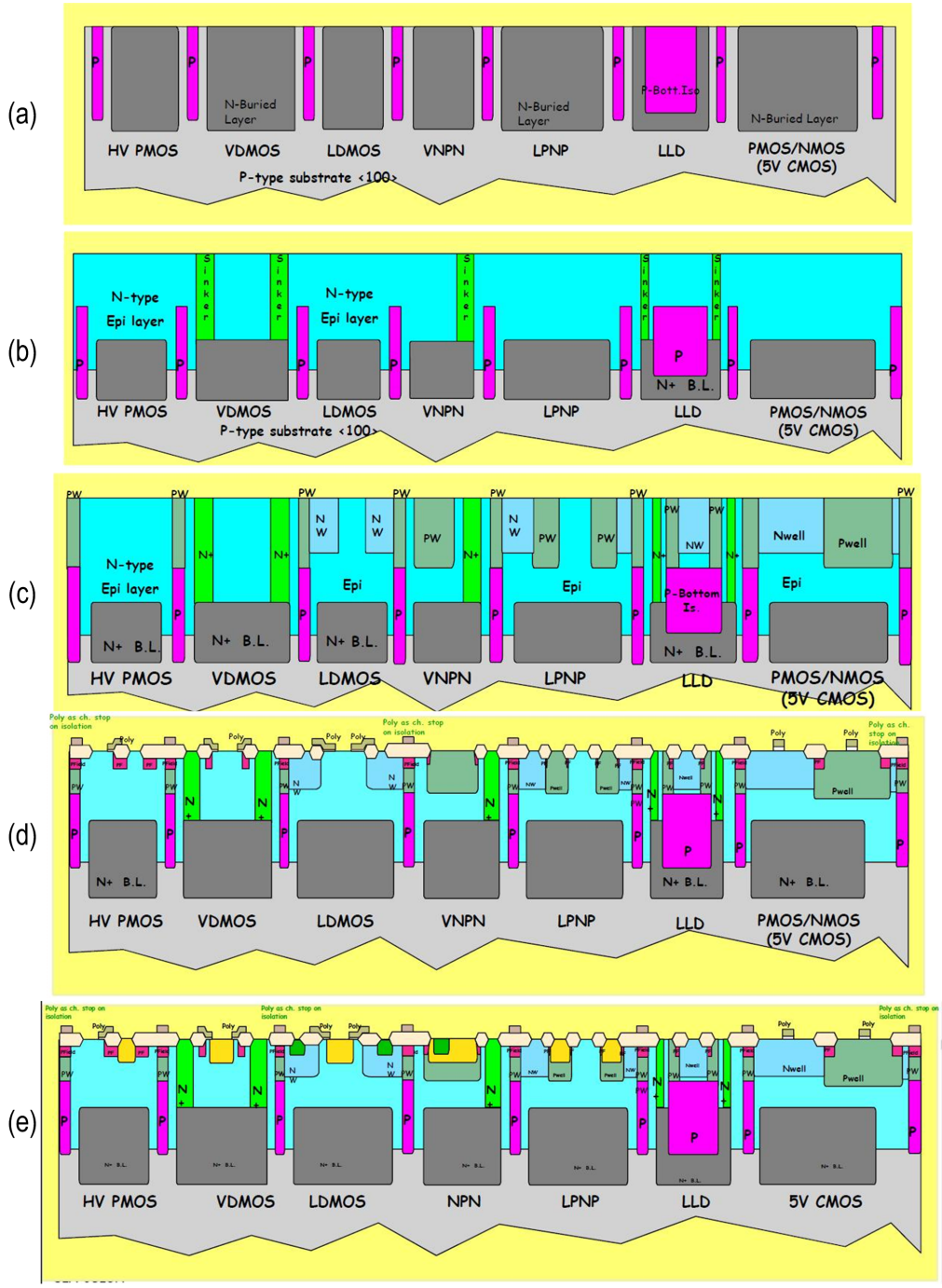

Figure 2.7: Steps involved in the BCD process (I).

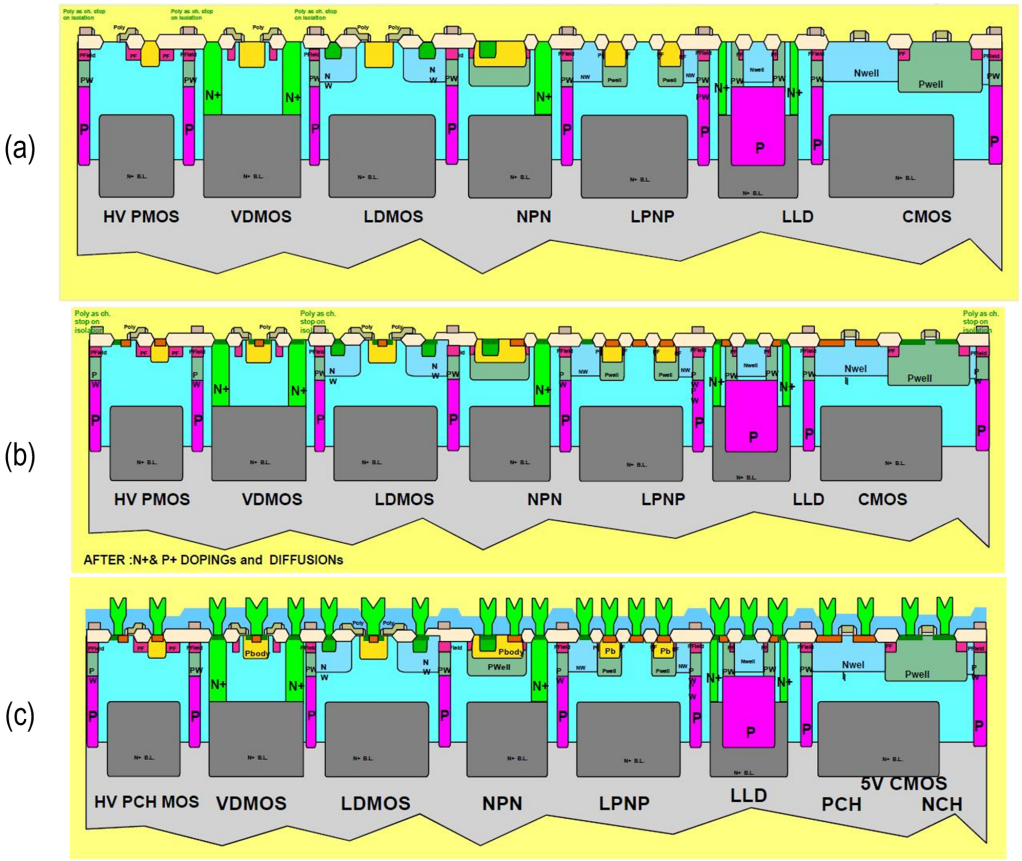

Figure 2.8: Steps involved in the BCD process (II).

2.4 High Voltage Integrable Devices

There are three different types of high-voltage devices, normally used with CMOS technology. These are Drain-Extended MOSFET [49, 50, 51, 52], Lateral double-diffused MOSFET [53, 54, 55] and Vertical double-diffused MOSFET [56, 57].

The Drain-Extended MOSFET, shown in Fig. 2.10a, is an n-channel HV transistor with long channel and non-self aligned architecture. It has a uniformed doped channel. A typical twin well CMOS process allows DEMOS transistors to be built with the n-well as the NMOS drain extension.

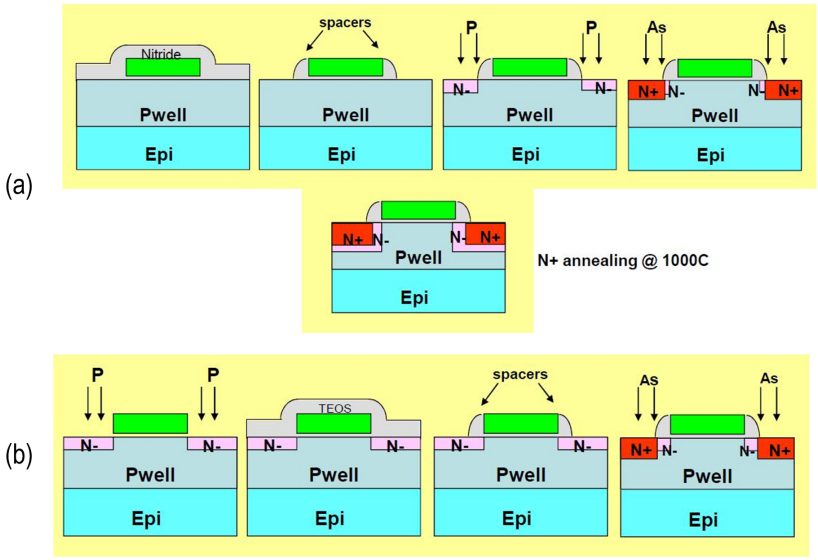

Figure 2.9: Standard DDD (a) and LDD (b) implant process.

Due to the inherent limitations of CMOS technology, DEMOS device characteristics, especially avalanche breakdown and on-resistance, are highly dependent on the n-well doping profile and surface concentration. As CMOS technology is maturing in deep-submicron lithography, other approaches were investigated in order to make available high voltage devices with improved characteristics.

The Lateral DMOS device architecture has much higher breakdown voltage than DEMOS architectures. Fig. 2.10b shows the schematic representation of N-type LDMOS device. There are many variations of LDMOS devices [53, 54, 55, 58]. The channel in the device is created using double diffused process and thus it has lateral non-uniform doping. The effective gate length is shorter than the physical length of the gate electrode. The drift region is lightly doped N-type whose length varies with increasing voltage blocking capability in the drain side. The maximum drain-source voltage, that can be

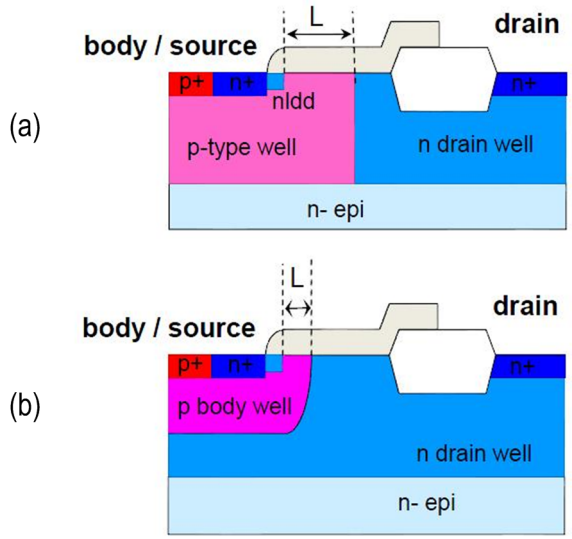

Figure 2.10: Cross-section of DEMOS (a) and LDMOS (b).

applied, is determined by the breakdown voltage of the p-n junction, which is limited by the n layer doping, thickness and field crowding at the junction edge.

The electric field in the LDMOS near the silicon surface is considerably lower than in the conventional MOS or DEMOS. However, the maximum field still remains on the surface and avalanche breakdown may occur there [59]. The surface electric field can be reduced significantly by the use of thick oxide or field plate as the maximum field is now located inside the bulk. To reduce the on-resistance in LDMOS (with field plate), the length of the field plate should be as small as possible. The effect of field plate on LDMOS characteristics e.g. breakdown voltage, quasi-saturation effect has been studied in the literature in detail [60, 61, 62, 63, 64, 65]. The on-resistance of the LDMOS can also be decreased by using the ion-implantation in the drift region [66]. The field plate also shields the gate from the drain

potential, thus minimizing the feedback (drain-to-gate) capacitance. The p-n junction and the field plate form a fairly uniform field between gate and the drain, thus giving better breakdown voltage.

The LDMOS transistors fare much better at higher frequencies compared to their vertical counterpart (VDMOS) devices.

2.5 BCD6-SOI Technology

The adopted STMicroelectronics BCD6-SOI technology has two poly and four metal layers and embeds 5V npn bipolar devices and $0.35\mu m$ CMOS transistors.

LDMOS used in the design have $1\mu m$ minimum channel length and support a maximum V_{DS} of 100V. Fig. 2.11 shows the cross-section of an N-channel LDMOS. In SOI technology (used in this design) each high-voltage device has an isolation trench: source and body of each device are shorted together internally. The bulk terminal (SUB in Fig. 2.11) is isolated from the device body by the SOI layer and is connected to the most negative voltage on the die.

Plots of I_D versus V_{DS} with V_{GS} as a parameter are shown in Fig. 2.12 for an N and P-channel LDMOS. P-channel has been sized about 2.7 times wider than N-channel to compensate holes mobility reduction.

Plots of I_D versus V_{GS} are reported in Fig. 2.13. Differentiating these characteristics can be obtained the transconductance of devices.

In particular in Fig. 2.14 are shown plots of normalized transconductance $\frac{g_m}{W}$ versus overdrive voltage $V_{OD} = V_{GS} - V_T$. N-channel exhibits a larger

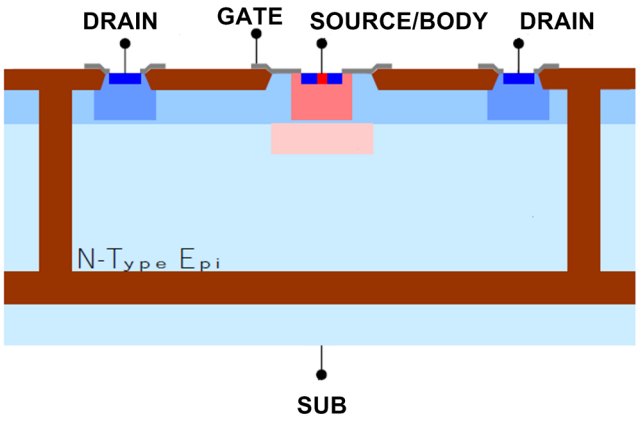

Figure 2.11: Cross-section of LDMOS in SOI technology.

normalized transconductance than P-channel LDMOS as in standard CMOS process.

Finally the cut-off frequency, defined as the frequency where the magnitude of the short-circuit, common-source current gain falls to unity, is reported in Fig. 2.15. The maximum cut-off frequencies, at the overdrive voltage of ∼2V, are 6.7GHz and 2.4GHz for N and P-channel, respectively.

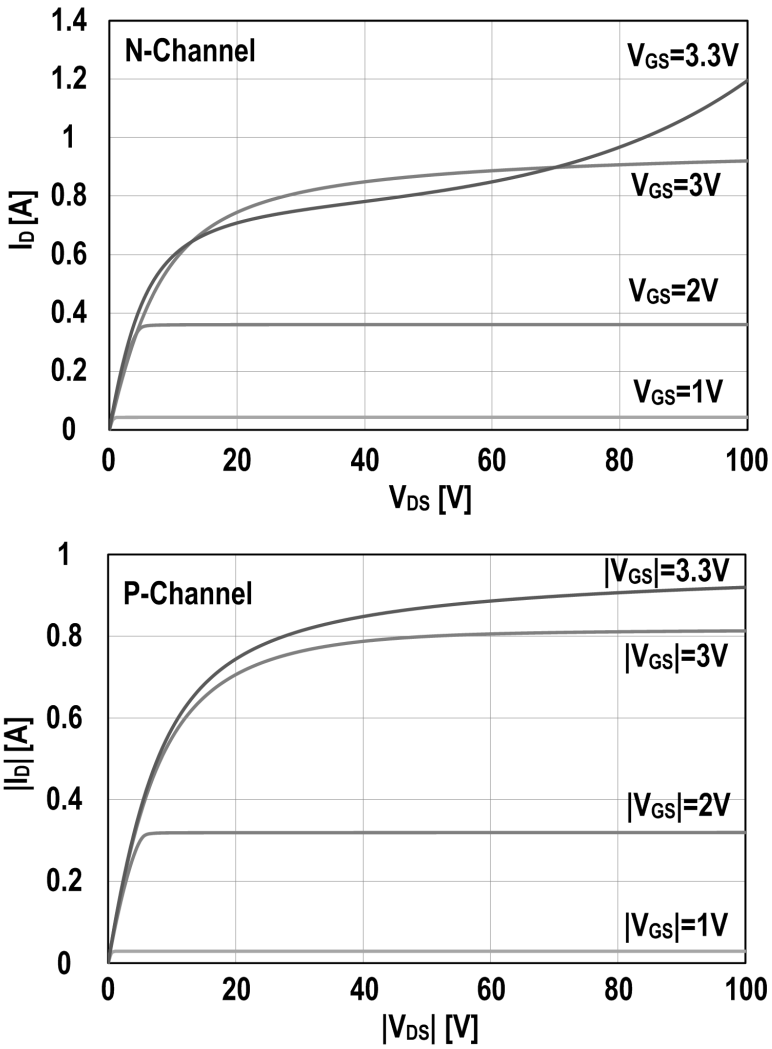

Figure 2.12: Output characteristics of LDMOS devices.

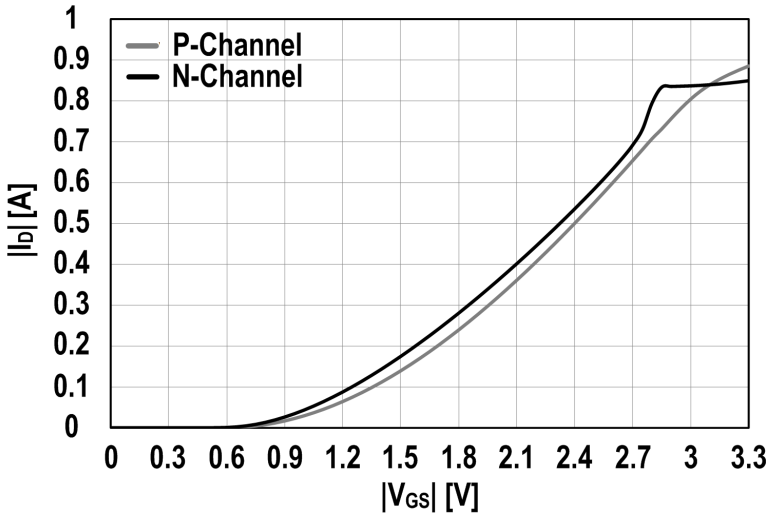

Figure 2.13: Plots of I_D versus V_{GS} of LDMOS devices.

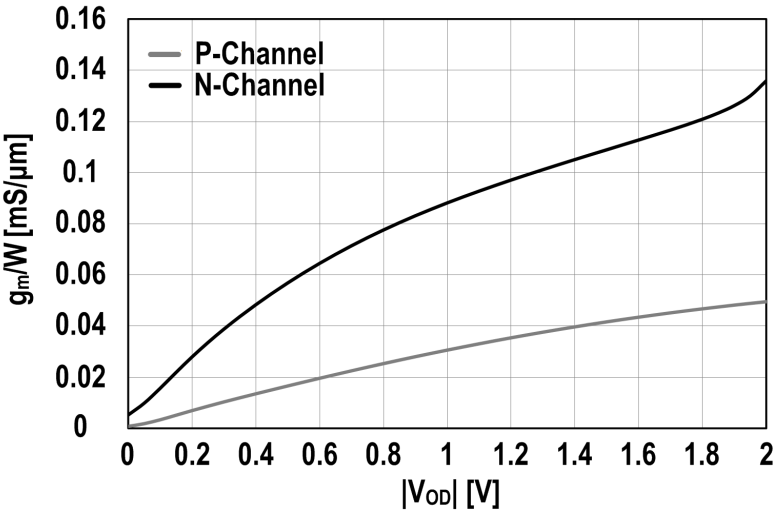

Figure 2.14: $\frac{g_m}{W}$ versus V_{OD} of N an P-channel LDMOS.

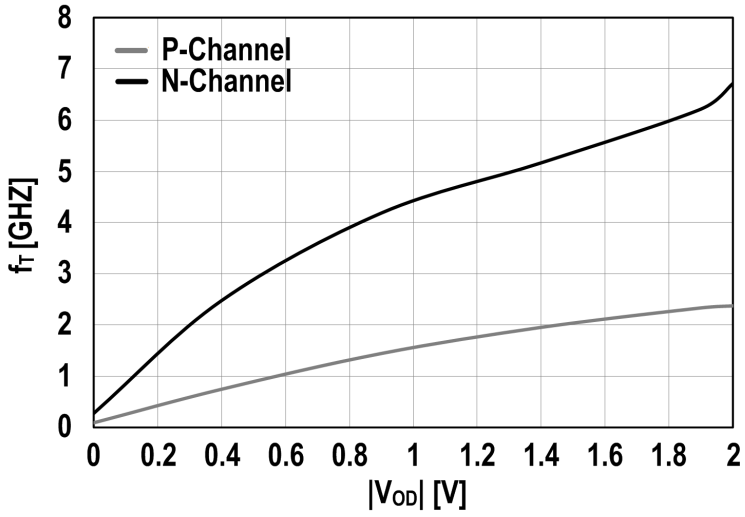

Figure 2.15: f_T versus V_{OD} of N an P-channel LDMOS.

Chapter 3

Design of an High-Voltage Amplifier for Ultra-Sound Transducers

High voltage pulsers are usually adopted to drive the transducers because of the high efficiency and simplicity. Arbitrary waveform generators realized with a high voltage linear amplifier driven by a D/A converter are nonetheless very attractive enabling apodization profiles with high resolution, beams with low harmonic content and instantaneous changes in transmit energy between pulses. Furthermore, low distortion allows employing the amplifier in harmonic imaging where higher harmonic echoes (usually the second) of the fundamental transmitted frequency, either generated by reflection from micro-bubbles or on propagation, are selectively detected and used for imaging. As a consequence, the harmonics of the transmitted signal need to be suppressed as much as possible. However arbitrary waveform generators are

presently realized with discrete components and bulky passive devices and their usage is therefore limited to high-end systems because of manufacturing costs, power dissipation and space constraints. To this extent IC technologies such as BCD, handling simultaneously high dynamic range signals at high frequency with low-voltage BiCMOS devices and multi-watt level driving through high-voltage DMOS-fets, opens up to the investigation of integrated linear amplifier topologies. From a system perspective, advantages in terms of EM interference reduction, reliability improvement, space and cost would derive.

The proposed operational amplifier, with block diagram shown in Fig. 3.1, uses a high g_m transconductor, employing thin oxide BiCMOS devices, and a trans-impedance stage using long length, high-voltage, transistors [67]. The design is aimed at maximizing the operating frequency with minimum quiescent power and harmonic distortion. In order to be attractive it should consume a maximum quiescent power in the tens of mW or even lower. Meanwhile, delivering voltage swings of 90V to ultra-sound transducers determines peak output powers as high as 20W. In order to meet these contrasting requirements, the trans-impedance stage, which is supplied at $\pm$50V, is biased in class-B.

Parameters of the trans-impedance devices vary with signal amplitude making circuit analysis involved. Large signal frequency response, distortion and stability are investigated in this paper. Describing functions are exploited to analyze the large signal frequency response [68] while stability is evaluated by considering the loop gain experienced by a small amplitude tone in presence of a large modulating signal, making the amplifier time-

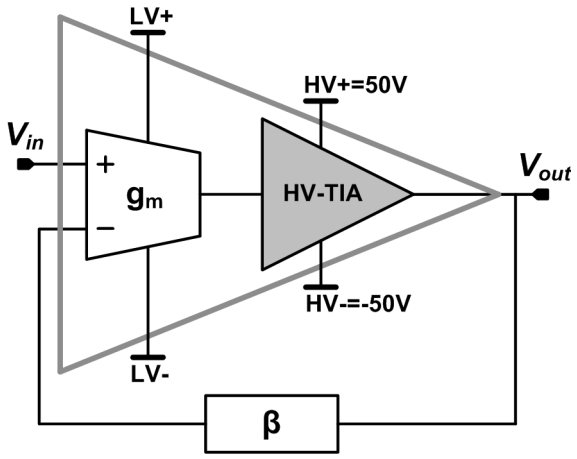

Figure 3.1: Block diagram of the proposed amplifier realizing forward gain through a low voltage supply transconductor cascaded by a high voltage supply transimpedance stage.

variant. Results are in good agreement with simulations and measurements and provide useful design insights. Prototypes of the linear amplifier have been realized in BCD6-SOI, and show the following performances: $90V_{pk-pk}$ output signals with more than 60% power efficiency, 720MHz GBW and better than -35dB HD_2 when driving a load made of a 100Ω resistor shunted with a 150pF capacitor, emulating the ultrasound transducer. The quiescent power dissipation is 37mW only.

3.1 The Operational Amplifier in BCD-SOI Technology

The adopted BCD6-SOI technology has two poly and four metal layers and embeds 5V npn bipolar devices and $0.35\mu m$ CMOS transistors with a nominal supply of 3.5V. Power DMOS-fets used in the design have $1\mu m$ minimum

channel length and support a maximum V_{DS} of 100V. The maximum cut-off frequencies, at the overdrive voltage of $\backsim$2V, are 6.7GHz and 2.4GHz for nDMOS and pDMOS, respectively. The trans-impedance stage devices operate under the maximum supply voltage of ±50V but for minimum quiescent power consumption, devices are all biased in sub-threshold (class-B). The transconductor uses the ±3V low voltage supply in order to save power consumption while using large biasing current for maximum gm. The amplifier uses two different supplies and a unity current gain buffer bridges transconductor to transimpedance stage.

The input transconductor is in class-AB, with peak output currents larger than biasing current to meet the tight slew rate requirements with limited power dissipation. The detailed schematic is reported in Fig 3.2. The input pair uses bipolar transistors for maximum $\frac{g_m}{I_b}$. The combination of pMOS and npn devices (M_1 and Q_1, M_2 and Q_2) replaces pnp, not available in this technology [69]. The drawback of this solution is the relatively low frequency of the pole at the base of $Q_{1,2}$ $f_p = \frac{1}{2\pi r_\pi C_\pi} \backsim 10MHz$, with r_π and C_π the base resistance and capacitance of $Q_{1,2}$ respectively, mandating frequency compensation to have a stable closed-loop amplifier response. After voltage to current conversion, signal currents are mirrored to the output. Cascodes M_{21}-M_{22} rise the output impedance maximizing current injection into the transimpedance stage, even at low signal levels. A transconductance gain of 60mS is achieved with a quiescent current of 4.5mA. Device dimensions and biasing currents are chosen in order to withstand a minimum supply voltage of ±2.5V and still a safe operation up to ±3.5V.

The details of the trans-impedance stage are reported in Fig. 3.3. Node A

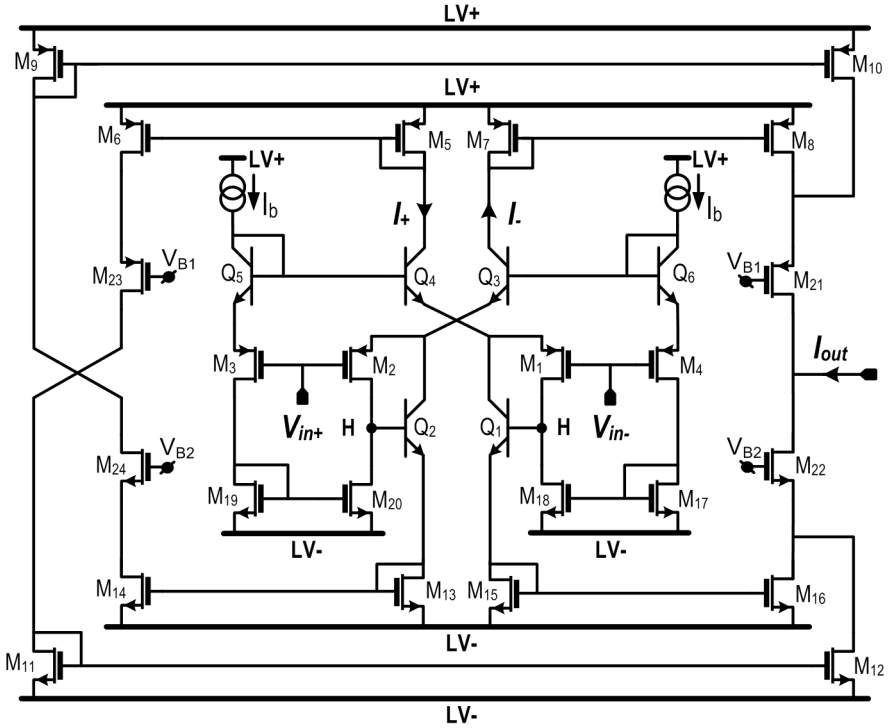

Figure 3.2: Schematic of the transconductor.

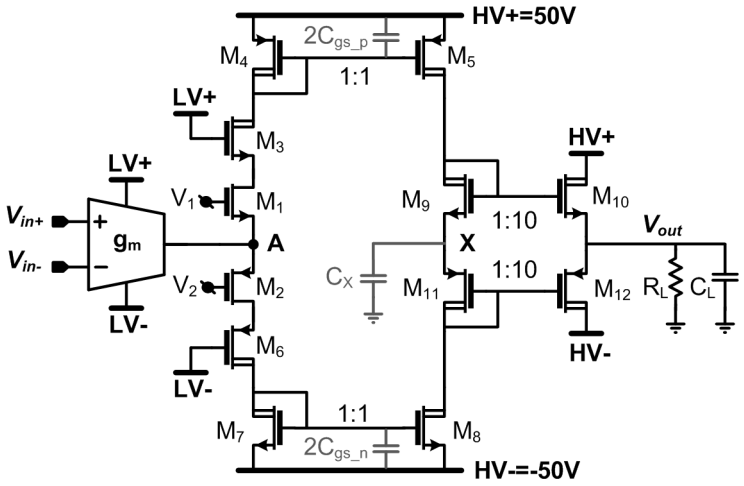

Figure 3.3: Schematic of the high-voltage trans-impedance stage.

bridges the two circuit sections: half positive and negative sinusoids of current injected from the transconductor are absorbed by common-gate devices M_1 and M_2. M_3 to M_6 shield the drain of M_1 and M_2 sustaining the large voltage drop. Transistors M_4 and M_5 (M_7 and M_8) mirror the half-sinusoid signal current with unity gain so as to develop the high voltage swing at node X. A complementary sourcefollower (M_{10} to M_{12}) drives the off-chip load making the amplifier robust against variations of the load resistor R_L and capacitor C_L. All devices are high-voltage DMOS-fets, except M_1 and M_2 which are thin-oxide devices for minimum input impedance.

The transconductor works in class-A up to relatively large input signals and the analysis of the frequency response is rather straightforward. On the contrary, the analysis of the class-B trans-impedance stage, where signals have amplitudes much larger than standing values, is challenging because mathematical tools used in linear circuits can not be automatically invoked.

3.1.1 Output Stage

The simplified schematic is reported in Fig. 3.4. Two batteries provide a level shift equal to the threshold voltage of M_{10}, M_{12} emulating the role of diode connected devices M_9, M_{11} in Fig. 3.3. The buffer is required to provide low output impedance making the overall amplifier response robust against variations of the load $Z_L(\omega)$, made by the parallel combination of 100Ω resistor and 150pF capacitor. The output transistors have to be sized wide enough to deliver the required peak output current to the load while keeping the applied voltage within safe operating limits. Considering a sinusoidal output signal up to 10MHz and 50V $V_{out-max}$ output amplitude, the maximum current flowing through the load impedance is $I_{out-max} = \frac{V_{out-max}}{|Z_L(2\pi 10MHz)|} = 700mA$. V_{GS-max}, the maximum gate-to-source voltage of M_{10}, M_{12} must not exceed 3.5V in order to assure safe operation of devices. To keep some margin against process spreads and load variations, a maximum of 3V has been assumed in the design, leading to the following dimensions for the selected devices: $(W/L)_{10} = 3.9mm/1\mu m$ and $(W/L)_{12} = 10.5mm/1\mu m$. Since devices are biased in class-B, the transistor gain is signal dependent and increases with the amplitude leading to gain and bandwidth expansion when the input level increases. In order to derive an analytical description of the frequency response, we leverage describing functions. The input-output characteristic of the devices is modeled disregarding all harmonic components in the output spectrum except the one at input signal frequency. The approach is commonly applied to the analysis of tuned RF circuits, where a sharp resonant load rejects harmonics [70, 71]. Comparison of the analytical results against

circuit simulations will show that analysis through the describing function leads to very accurate results also for broadband amplifiers, as in our case, where harmonics are not or eventually mildly attenuated. If G_M is the output stage transconductance describing function, expressions for gain A_V and -3dB bandwidth are given by:

$$A_V = \frac{G_M R_L}{1 + G_M R_L} \tag{3.1}$$

$$f_{-3dB,buff} = \frac{1}{2\pi C_L(\frac{1}{G_M}//R_L)} \approx \frac{G_M}{2\pi C_L} \tag{3.2}$$

G_M can be determined assuming a sinusoidal input signal and the output of the buffer short circuited. With M_{10} and M_{12} biased at threshold voltage ($V_{GS,Q} = V_{TH}$), the overdrive is equal to the input sinusoidal voltage, $V_{OD}(t) = V_{OD}\sin(\omega_0 t)$. Assuming square-law mosfet models, the output stage current Iout(t) is given by:

$$I_{out}(t) = \begin{cases} \frac{\beta_n}{2} V_{OD}^2 \sin^2(\omega_0 t)\ for\ 0 \leq \omega_0 t < \pi \\ \frac{\beta_n}{2} V_{OD}^2 \sin^2(\omega_0 t)\ for\ \pi \leq \omega_0 t < 2\pi \end{cases} \tag{3.3}$$

where $\beta_{n,p} = \mu_{n,p} C_{ox}(\frac{W}{L})_{n,p}$. With $\beta_n = \beta_p = \beta$, the fundamental Fourier component of the output current at ω_0 is $I_{out}\ |_{\omega_0} = \frac{4\beta V_{OD}^2 \sin(\omega_0 t)}{3\pi}$, and the expression for the transconductance follows as:

$$G_M = \frac{4\beta}{3\pi} \mid V_{OD} \mid = G_{M0} \mid V_{OD} \mid \tag{3.4}$$

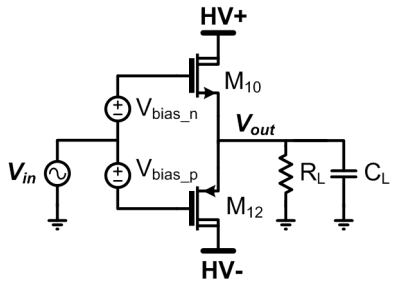

Figure 3.4: Simplified schematic of the output buffer.

revealing a direct dependence on the developed device overdrive voltage.

To gain more insight it is further convenient replacing the overdrive voltage with the output voltage signal V_{out}. By inspection of the circuit in Fig. 3.4: $V_{OD} = \frac{V_{out}}{G_{M0} V_{OD} R_L}$. Eqs. 3.1 and 3.2 can be rearranged as follows:

$$A_V(V_{out}) = 1 - \frac{1}{1 + \sqrt{G_{M0} R_L V_{out}}} \tag{3.5}$$

$$f_{-3dB,buff}(V_{out}) \approx \frac{G_{M0}}{2\pi C_L} V_{out} \tag{3.6}$$

The stage gain approaches unity for $G_{M0} V_{out} \gg \frac{1}{R_L}$ while the -3dB bandwidth expands linearly with V_{out}. The calculated low frequency gain (Eq. 3.5) is compared against the results of transient circuit simulations in Fig. 3.5 assuming the nominal load components and the device dimensions derived previously. For $V_{out} > 100mV$, calculations and simulations are in very good agreement. For $V_{out} < 100mV$ the simulated gain does not fall to zero, as predicted by Eq. 3.5, but saturates at around -6dB. In this region the amplifier has a linear behavior, i.e. the gain is flat and independent of the output voltage, due to the sub-threshold current conduction, neglected in the

analysis. This leads to a small but non-zero transconductance gain at the quiescent operating point. For the application of interest, however, output signal amplitudes larger than 1V are expected. The output stage introduces an attenuation of less than 2dB. Given the load resistance, lower attenuation could be achieved by selecting a larger G_{M0} i.e. a larger , as suggested by Eqs. 3.4 and 3.5. A larger size of the output devices would follow, at the price of an increased sub-threshold current (and power dissipation from the high voltage supply at the quiescent point) and larger buffer input capacitance. Fig. 3.6 compares the calculated and simulated -3dB bandwidth versus the output voltage. The curves are reported up to $V_{out} = 4V$ because, for larger values, devices leave the safe operating area before reaching the -3dB cut-off frequency. A very good agreement is evident for $V_{out} > 0.5V$ where the bandwidth starts expanding linearly. At lower signal levels the bandwidth does not fall to zero, but it is constant at 20MHz due to the sub-threshold device transconductance and load resistance, not considered in the model leading to Eq. 3.6. For $V_{out} > 1V$ the -3dB bandwidth of the buffer is beyond 100MHz. This value is high enough not to affect the bandwidth of the complete amplifier, as emerging from the discussion in the next subsection.

3.1.2 Trans-impedance stage

Assuming negligible output conductance of M_5 and M_8, the trans-impedance stage behaves as an integrator with the following transfer function:

$$V_{out} \approx \frac{I_{in}}{2\pi C_X} A_V \tag{3.7}$$

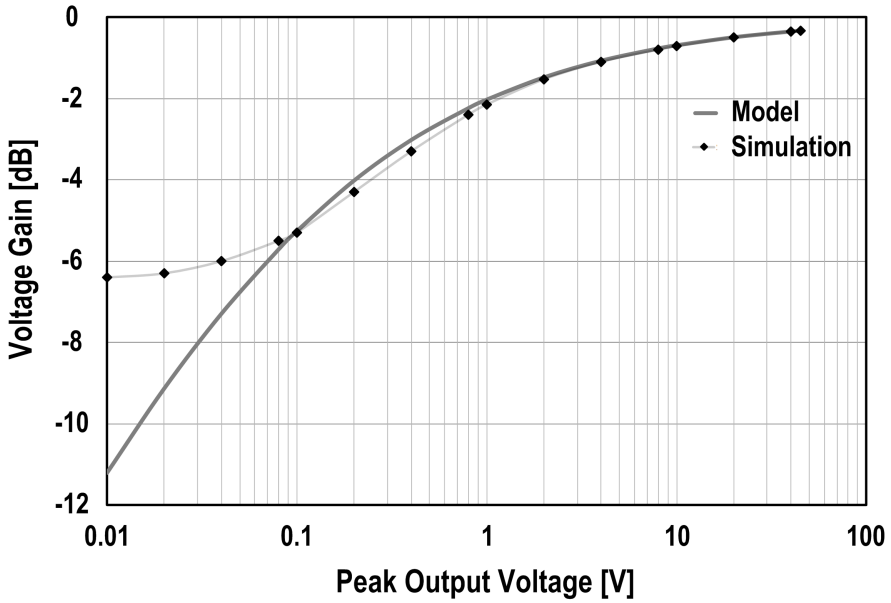

Figure 3.5: Comparison between simulated and calculated in-band gain of the output buffer.

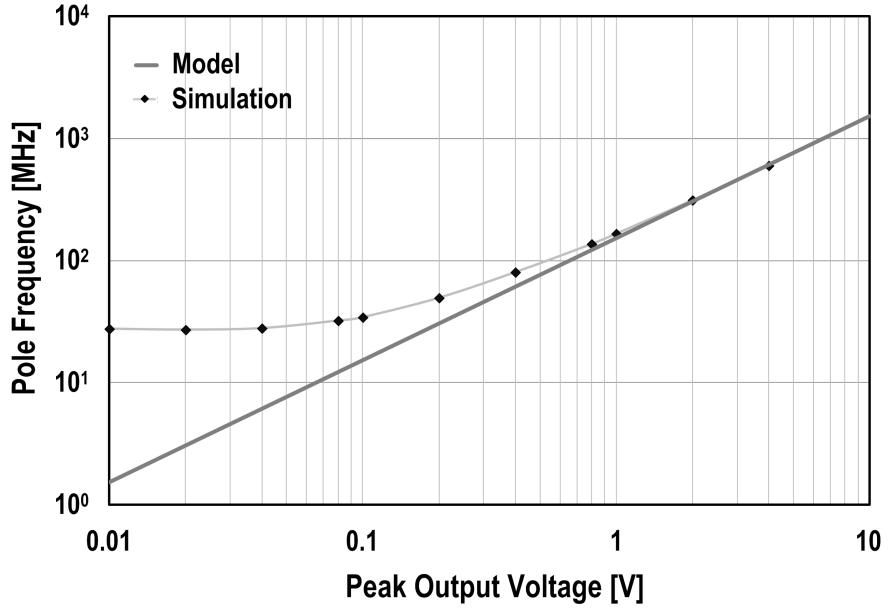

Figure 3.6: Comparison between simulated and calculated -3dB bandwidth of the buffer.

where A_V is the buffer gain, C_X is the parasitic capacitance at node X and Iin is the signal current delivered by the low-voltage transconductor. If g_m is the transconductance of the low-voltage stage, $I_{in} = g_m V_{in}$ and the gain-bandwidth product of the complete amplifier is estimated as:

$$GBW \approx \frac{g_m A_V}{2\pi C_X} \tag{3.8}$$

C_X is made of parasitics (C_p) of devices M_5, M_8, M_9, M_{11} plus the loading effect (C_{buf}) of the complementary source follower M_{10}, M_{12}. The latter changes significantly when the signal is applied because the gate to source capacitance is bootstrapped while entirely loading the node without applied signal, i.e. when devices work in sub-threshold. Referring to Fig. 3.3, the capacitance seen at buffer input is derived as:

$$C_{buf} = \frac{C_{gsN} + C_{gsP}}{1 + G_M R_L} = \frac{C_{gsN} + C_{gsP}}{1 + G_{M0} \mid V_{OD} \mid R_L} = \frac{C_{gsN} + C_{gsP}}{1 + \sqrt{G_{M0} R_L V_{out}}} \tag{3.9}$$

where C_{gsN} and C_{gsP} are the gate to source capacitance of N and P output stage devices respectively.

The higher the signal amplitude the lesser the input referred capacitance because bootstrap of C_{gs} is more effective. Fig. 3.7 shows calculated and simulated C_X versus the oscillation amplitude. A capacitance C_p of 4.2pF representing the parasitic of devices M_5, M_8, M_9, M_{11} in the high impedance node is taken into account. A very good agreement is evident and proves again that describing functions capture the effect of large signal operation very well. Transistors of the complementary current mirror are sized to the

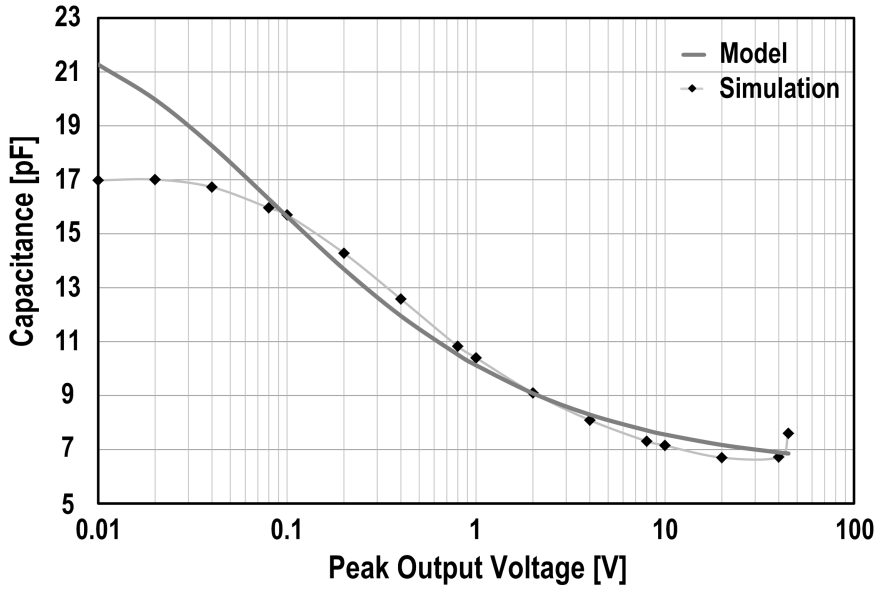

Figure 3.7: Equivalent capacitance at high impedance node versus the voltage swing.

minimum value to have V_{GS-max} of 3V when delivering the maximum current to C_X. A larger size would contribute larger parasitics on internal nodes while not providing improvements to other amplifier performances.

The target closed loop gain of the amplifier is 40dB with a -3dB bandwidth larger than 5MHz. This sets a minimum required gain-bandwidth product, $GBW > 500MHz$. From Figs. 3.5 and 3.7, the lower the output voltage amplitude, the lower the buffer gain and the larger the high impedance node capacitance. From Eq. 3.8, assuming a minimum delivered output voltage of 1V, $A_V = -2dB$ and $C_X = 10.5pF$ the minimum gm required for the low voltage transconductor to meet the required GBW is 33mS. 60mS has been selected to meet also the linearity requirements, as discussed in the next Section. Fig. 3.8 shows the simulated open loop gain versus frequency for output voltage of $1V_{0-pk}$ and $40V_{0-pk}$ assuming a transconductance stage of

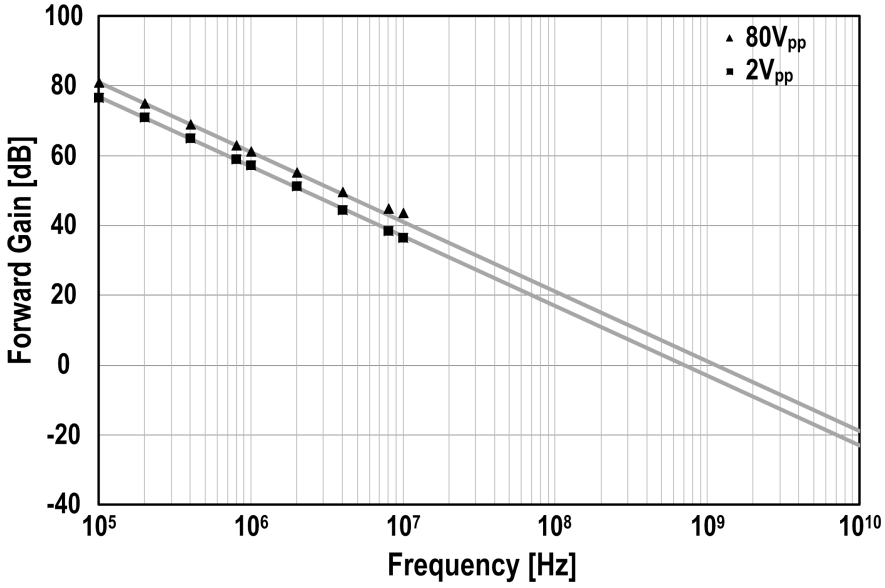

Figure 3.8: Simulated amplifier gain-bandwidth product at 2V and 80V output amplitude.

60mS with no bandwidth limitation and the complete trans-impedance stage of Fig 3.3. The extrapolated GBW are 713MHz and 1.2GHz.

The describing function can be applied to estimate the frequency location of the secondary poles introduced by the common-gate and current-mirror devices in Fig. 3.3 under large signal operation. As an example, G_M and pole frequency f_p for the pMOS diode connected device of the mirror M_4 reported in Fig. 3.3, are given by:

$$G_M = 0.2\pi\sqrt{\beta I_{in}} \; and \; f_p = 0.1\frac{\sqrt{\beta I_{in}}}{C_p} \tag{3.10}$$

where $C_p = 1.5pF$ is the parasitic capacitance to ground, roughly equal to the sum of the gate-to-source capacitances of M_4 and M_5. Assuming I_{in} of $170\mu A$, being injected into the mirror when the output voltage signal is

$1V_{0-pk}$ at 5MHz, determines G_M of 1.4mS and a pole frequency location at 148MHz. From Fig. 3.8, assuming a closed loop gain of 40dB the cut-off frequency of the loop gain is ≈7MHz i.e. well before the pole frequency of the pMOS current mirror. It can be verified that also all other poles are at least one decade beyond 7MHz, thus assuring a trans-impedance single pole low-pass closed loop shape.

3.2 Second Order Harmonic Distortion

Feedback technique provides several well-known advantages to control systems. Among the others, the improvement of linearity performance is key in electronic circuits. Provided the feedback path is linear, harmonic components generated by the amplifier are rejected by the loop [72, 73]. In the application of interest in this work, second order non-linearity is key directing the attention to any unwanted circuit asymmetry. The complementary source follower output stage, aimed at transferring the delivered signal at full swing is a possible source. The nMOS and pMOS transistors (M_{10} and M_{12}) have been accurately sized to match the static gain of the complementary source follower for positive and negative voltage excursions, as evident from Fig. 3.9 where the simulation of the static input-output characteristic is reported. HD_2 introduced by the buffer when driven by an ideal sinusoidal voltage source of $80V_{pp}$ is -90dB, constant versus frequency. On the other hand the voltage driving the buffer is developed by the signal current injected by the transconductor in the capacitor at the high impedance node X. The capacitance, as discussed in the previous sub-section, is voltage dependent and

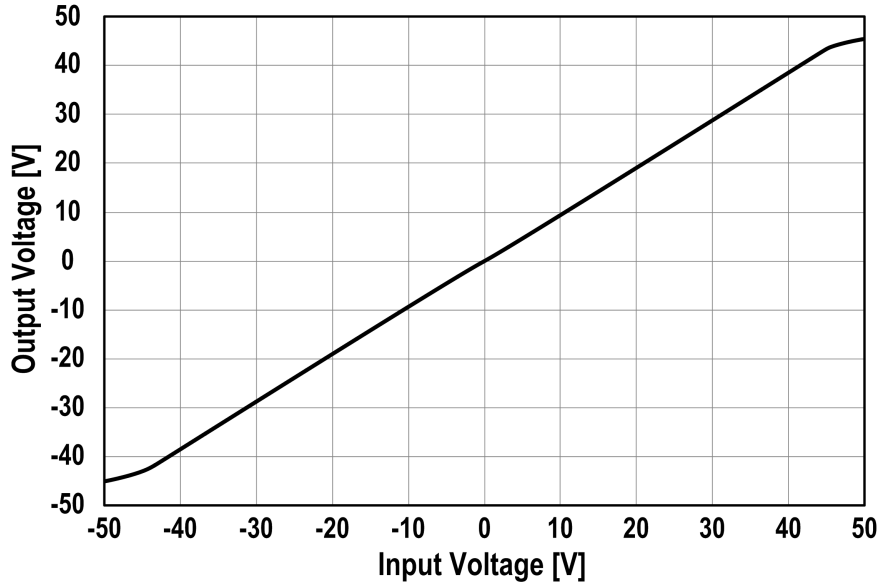

Figure 3.9: Complementary source follower static input-output characteristic.

any asymmetry, i.e. a difference between the total node capacitance during positive and negative voltage excursions leads to second-order distortion in the current-to-voltage conversion.

To gain quantitative insight, let us analyze the simplified circuit shown in Fig. 3.10a, where a transconductor injects current $I(t) = g_m V_{in} \sin(\omega_0 t)$ on a capacitor having a capacitance mismatch for positive and negative voltage swings i.e. $C(V) = C_0(1+\frac{\varepsilon}{2})\ if\ V > 0$ and $C(V) = C_0(1-\frac{\varepsilon}{2})\ if\ V < 0$. The voltage across the capacitor is solution of the differential equation $I(t) = C(V)\frac{dV(t)}{dt}$. Solution leads to the following amplitudes of the fundamental voltage component and its first harmonic: $V_{\omega_0} \approx \frac{g_m V_{in}}{\omega_0 C_0}$, $V_{2\omega_0} \approx \frac{2\varepsilon}{3\pi}\frac{g_m V_{in}}{\omega_0 C_0}$. They both decrease as $\frac{1}{\omega_0}$, while HD_2 is constant with frequency and given by:

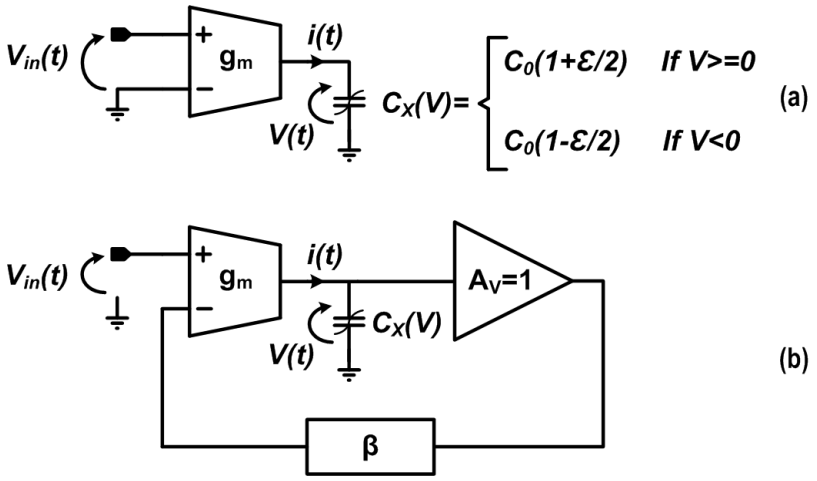

Figure 3.10: Equivalent circuits used to reproduce the second-harmonic distortion of the amplifier. Open-loop (a) and closed-loop (b).

$$HD_2 = \frac{2}{3\pi}\varepsilon \tag{3.11}$$

If we close the feedback around the transconductor driving the non-linear capacitor, as shown in Fig. 3.10b, the resulting HD_2 for a given output voltage follows [16,17]:

$$HD_2 = \frac{2}{3\pi}\frac{1}{1+G_{loop}} \tag{3.12}$$

As long as the loop gain, $Gloop = \frac{\beta g_m}{\omega_0 C_0} \gg 1$ (being β the gain of the feedback path) HD_2 rises linearly with frequency, with a slope of 20dB/dec.

In order to appreciate the validity of the analysis leading to Eqs. 3.11 and 3.12, HD_2 has been simulated for the complete amplifier. Results are reported in dots in Fig. 3.11 when delivering $80V_{pk-pk}$ output signal. Continuous line plots Eq. 3.12 with $\varepsilon = 6\%$.

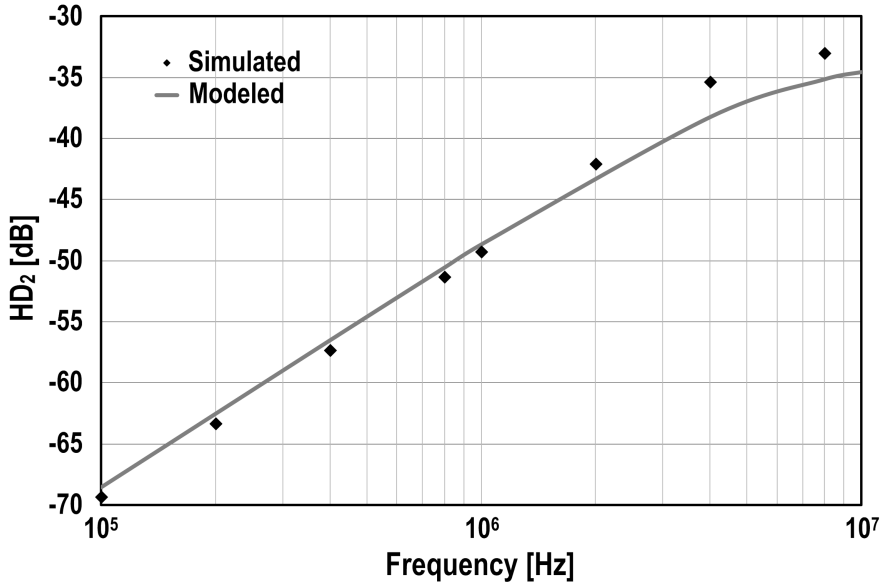

Figure 3.11: Simulated (dots) and modeled (continuous line) HD_2 versus frequency at $80V_{pk-pk}$ output voltage.

3.3 Stability

Class B operation determines signal dependent circuit parameters mandating further insight to assess closed loop stability conditions. In particular the amplifier gain-bandwidth product and secondary poles frequency vary with driving signal amplitude. Instability manifests itself as a relatively small signal superimposed to the desired output signal, as shown by the simulated transient waveform in Fig. 3.12. We can imagine a small sinusoid of amplitude v_{in} and angular frequency $\Delta\omega$ superimposed to the large driving signal at ω_0 with amplitude V_{in}. For the analysis we refer to the block diagram of the closed-loop amplifier in Fig. 3.13. To investigate stability we consider the loop gain for the small signal at $\Delta\omega$. The large input modulates device operating point of the high voltage class-B stage making the small signal loop

gain time variant, though cyclo-stationary. Fig. 3.14 shows the phase margin derived with Spectre Periodic Steady State (PSS) stability simulations [74] versus output amplitude when the amplifier delivers a large signal at 500kHz and 5MHz. The continuous curves are derived by using an ideal low-voltage transconductor with a flat frequency response, while dotted curves are with the transconductor of Fig. 3.2. Let us first consider the former case. Phase margin degrades at intermediate output voltages and low operating frequency reaching a minimum value of 25°, in this example, when the amplifier delivers $1V_{0-pk}$ at 500kHz. Stability is compromised by the secondary poles introduced by the common-gate devices and current mirrors of the trans-impedance stage of Fig. 3.3. The trans-conductance of such devices is modulated by the large signal current $I(t)$ charging and discharging the capacitor at the high impedance internal node, C_X. As shown in the next subsection, the time constant of the poles introduced by such devices for the small signal at angular frequency $\Delta\omega$ are r_0C where C is the parasitic node capacitance and $r_0 = \overline{g_m(t)^{-1}}$ is the average device resistance. The larger $I(t)$ the smaller the average value of r_0 pushing the secondary poles at higher frequency. Since $I(t)$ increases when the amplifier delivers higher output voltage at high frequency, phase margin improves. On the contrary, at very low signals levels, secondary poles move to low frequency, down to a minimum value set by the sub-threshold quiescent current drawn by the trans-impedance stage. On the other hand, at low signal levels, also the 0dB crossing frequency of the small signal loop gain moves toward lower frequencies as a result of the compression of the gain-bandwidth product of the amplifier and due to the larger attenuation of the output buffer stage and the

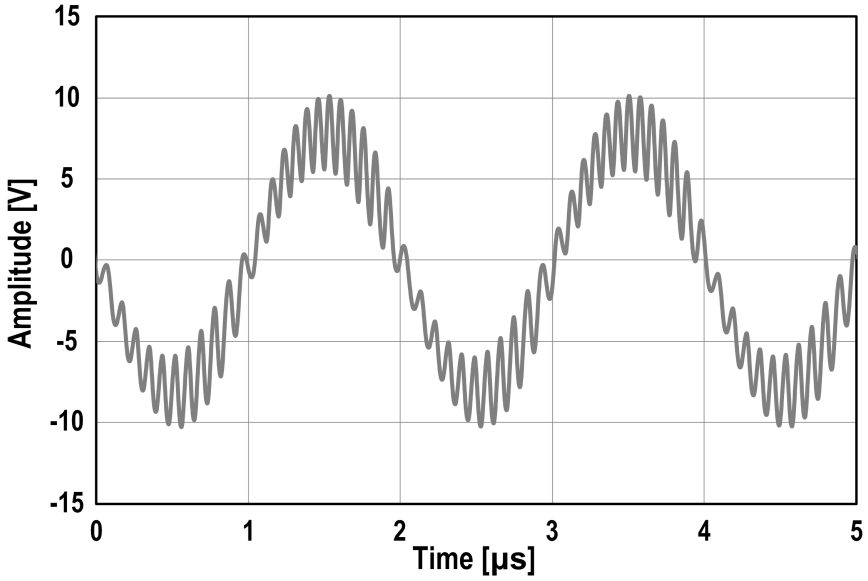

Figure 3.12: Transient output voltage showing instability.

increase of the equivalent capacitance C_X at the high impedance node. From PSS simulations, the 0dB crossing frequency of the loop gain moves from 18MHz, when the amplifier delivers the maximum swing at 5MHz, down to 1.6MHz at the quiescent operating point. The 0dB gain crossing is characterized by a single-pole 20dB/dec slope assuring a safe phase margin at low signal levels and at the quiescent point, as shown in Fig. 3.14.

The transconductor of Fig. 3.2 introduces a relatively low frequency pole ($\approx$10MHz) at the base node of $Q_{1,2}$. This pole impairs stability and, as shown by the dotted curves in Fig. 3.14, leads to a negative phase margin when the amplifier delivers intermediate voltages at low frequency. As discussed in the next chapter, the transconductor pole is compensated using lead technique through an off-chip capacitor in parallel with the feedback resistor [75].

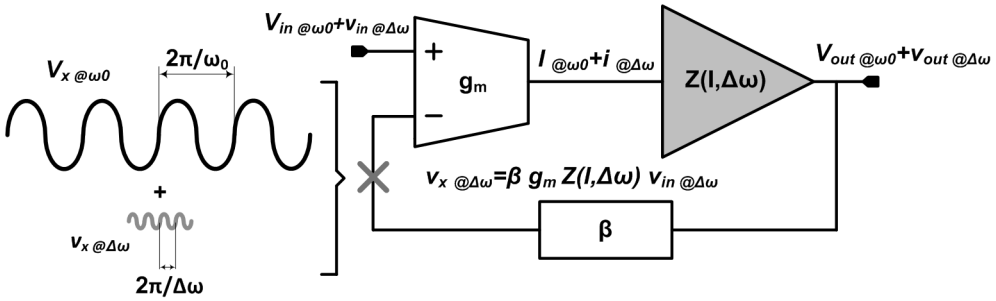

Figure 3.13: Feedback amplifier block diagram for stability analysis. Parameters of the trans-impedance stage vary depending on amplitude of the large driving signal.

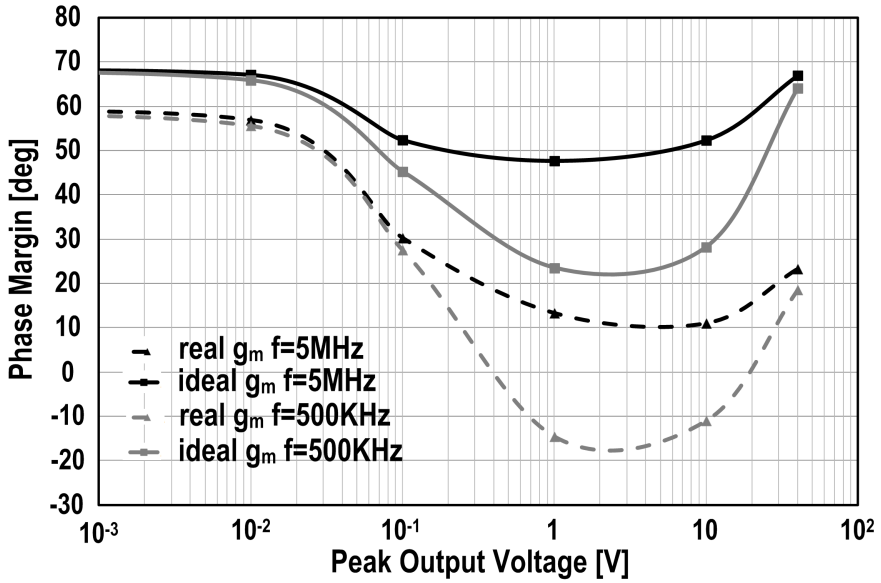

Figure 3.14: Phase margin from periodic steady-state simulations versus the large signal output swing.

3.3.1 Small signal poles calculation under periodic modulation by large signal

Let us focus on a nMOS common gate device of the transimpedance stage, shown in Fig. 3.15 and let's assume the large signal current $I(t) = I\cos(\omega_0 t)$ is at angular frequency sufficiently low to flow entirely through the transistor (i.e. the parasitic capacitance C has no effect on $I(t)$). $I(t)$ modulates the equivalent resistance at the source terminal, $r_0 = g_m(t)^{-1}$, seen by the small signal $i_{in}(t)\cos(\omega t)$. Being $I(t)$ periodic, $r(t)$ can be expressed with a Fourier series:

$$r(t) = \frac{\partial V_{GS}(t)}{\partial V(t)} = \sum_{n=0}^{\infty} r_n \cos(n\omega_0 t) \tag{3.13}$$

the small signal output current $i_{out}(t)$ is derived as:

$$i_{out}(t) = i_{in}(t) - C\frac{d[r(t)i_{out}(t)]}{dt} = I(t) - C\frac{d}{dt}\sum_{n=0}^{\infty} r_n \cos(n\omega_0 t) i_{out}(t) \tag{3.14}$$

Because we are interested in the small signal output current at the same angular frequency of $i_{in}(t)$, only the average resistance term $r_0 = \overline{r(t)}$ contributes, leading to:

$$i_{out}(t) \approx i_{in}(t) - C\frac{di_{out}(t)}{dt} \tag{3.15}$$

revealing a low pass response with time constant $r_0 C$ i.e. cut off angular frequency of $\frac{1}{r_0 C}$. A similar analysis could be carried out for pMOS common-gate and the diode connected devices of the current mirrors leading to the

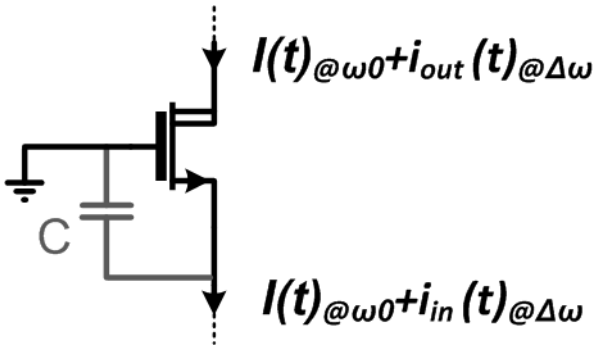

Figure 3.15: Common gate device for calculation of the small signal pole under periodic time-variant modulation by the large signal current.

same result.

Chapter 4

Experimental Results

The proposed operational amplifier has been fabricated by STMicroelectronics. Realized prototypes have been tested in standard ceramic dual-in-line packages without any heat sink. The chip photomicrograph and the block diagram of the experimental setup are shown in Fig. 4.1. The feedback network and load impedance are off-chip. The two feedback resistors set a gain of 40dB. Capacitor C_{DC} acts as a DC blocking capacitor to avoid amplification of the equivalent input offset voltage. Capacitor C_C introduces a zero in the feedback path to compensate the low frequency pole of the transconductor. The zero in the feedback network determines a pole at $\sim$8MHz in the closed-loop transfer function. The load impedance comprises a 100Ω resistor and 150pF capacitor. The input signal is provided through a National Instrument PXI-5421 16Bit 100MS/s signal source while the output is probed on a 11bit Tektronix TDS5104 oscilloscope. The high and low voltage supplies, set to $\pm$50V and $\pm$3V respectively, deliver static currents of 100A and 4.5mA leading to a quiescent power dissipation of 37mW. To avoid excessive

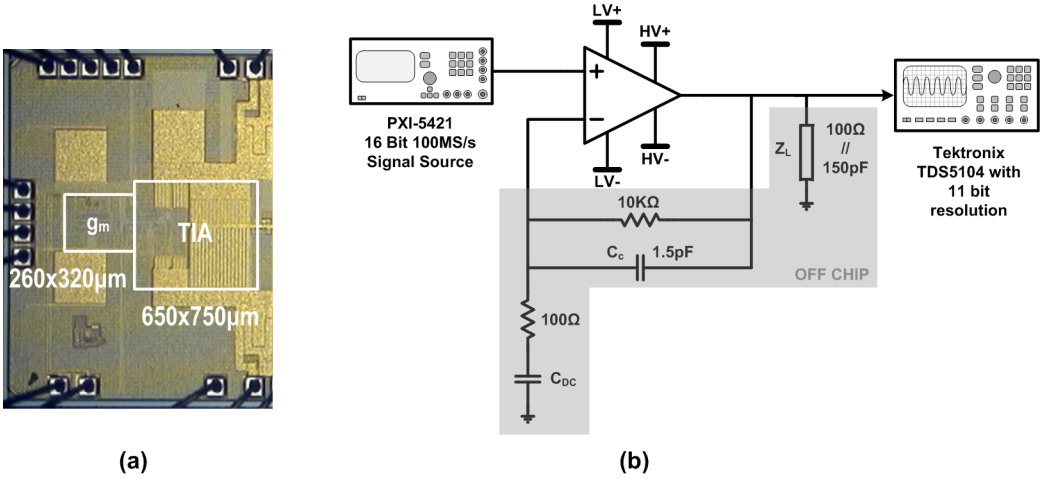

Figure 4.1: Chip photograph (a) and experimental setup (b).

selfheating, measurements of the frequency response and output power have been carried out with a pulsed input signal having a duty cycle less than 10%.

Fig. 4.2 compares the amplifier transient response with and without the compensation capacitor C_C. As predicted by simulations in section 3.3, the amplifier is stable at the quiescent point but, without compensation of the low frequency transconductor pole, a spurious oscillation appears on top of the desired signal when driven at relatively low frequency (500kHz). No instability is observed when C_C is introduced.

The closed loop frequency response for output voltage swings of $1V_{0-pk}$ and $40V_{0-pk}$ respectively are shown in Fig. 4.3. Simulations are also reported for comparison showing a very good agreement. The -3dB bandwidths are 5.5MHz and 6.5MHz for $1V_{0-pk}$ and $40V_{0-pk}$ output swings, respectively. The maximum measured output signal amplitude is $90V_{pk-pk}$.

At high swing, also the slew rate limits the op-amp performance. Fig. 4.4

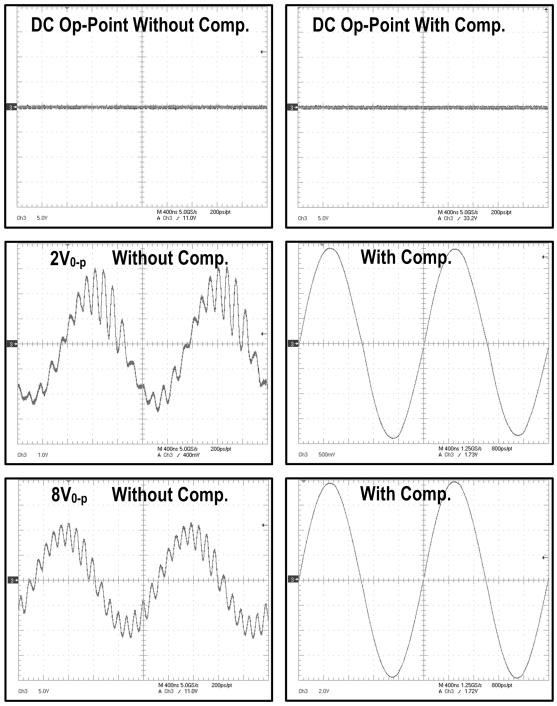

Figure 4.2: Transient waveforms without (left) and with (right) compensation capacitor.

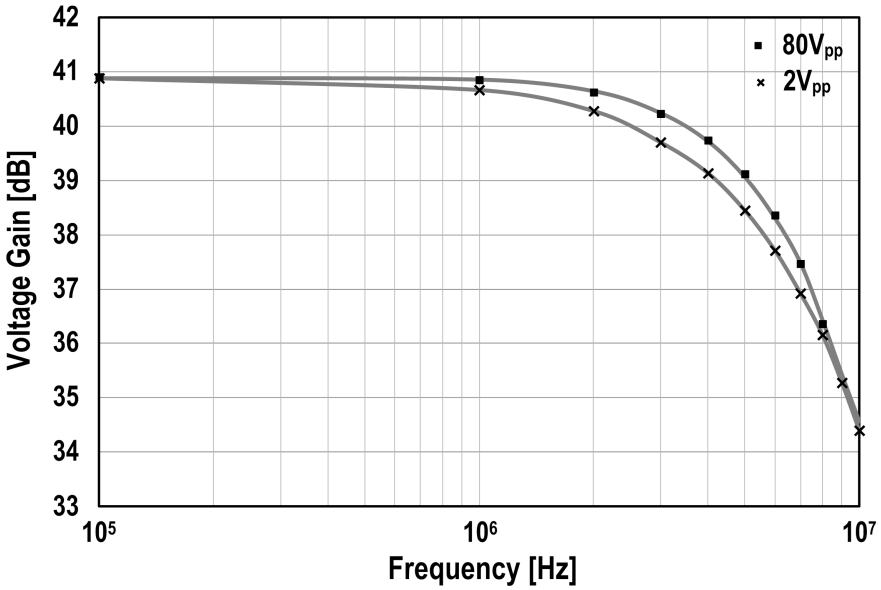

Figure 4.3: Measured (dots) and simulated (continuous line) closed loop frequency response for output voltage swings of 2V and 80V.

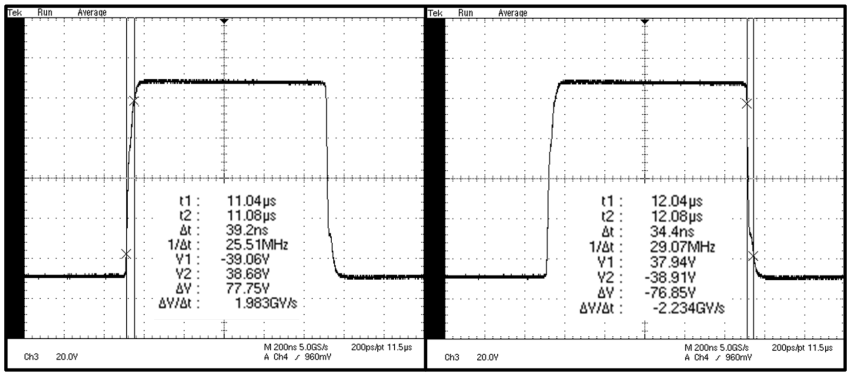

Figure 4.4: Response to an input voltage step of 90V, evidencing a positive and negative slew rate of +2kV/μs and -2.2kV/μs respectively.

shows the response to an input voltage step of 45V, evidencing a positive and negative slew rate of +2kV/μs and -2.2kV/μs respectively. This reflects into a maximum sinusoidal frequency of less than 8MHz not to be subject to slew rate limitations. Slew rate frequency limitation and -3dB bandwidth are of the same order. More margin on the slew-rate would have involved a higher power consumption without a significant bandwidth improvement.

Linearity performances have been analyzed through second harmonic distortion measurements. Gaussian envelops, typical of ultra-sound systems, have been used for testing. Screenshots of the oscilloscope, showing the output signal and the Fourier Transform for a 2MHz sinusoid having Gaussian envelope for various pk-to-pk amplitudes, are shown in Fig. 4.5.

Linearity measurements vs frequency are reported in Fig. 4.6 for an $80V_{pk-pk}$ output voltage and two different closed loop gains of 40dB and 46dB, respectively. Being the output voltage constant, the loop gain reduces correspondingly by 6dB. As predicted by Eq. 3.12, HD_2 is directly proportional to the frequency and inversely proportional to feedback β factor. Simulations

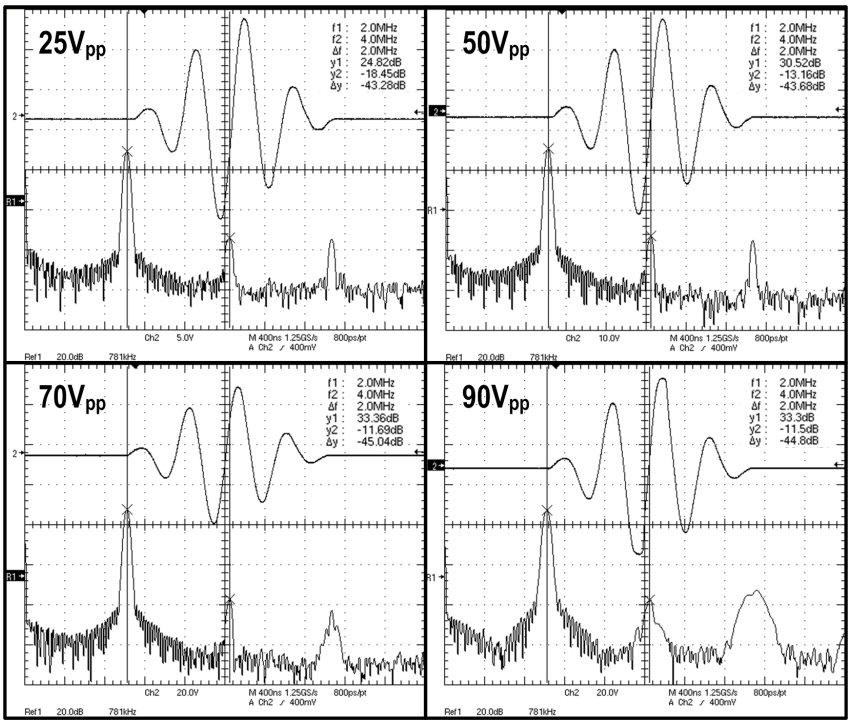

Figure 4.5: Time-domain response and DFT of various peak to peak sine output signals at 2MHz with Gaussian envelope.

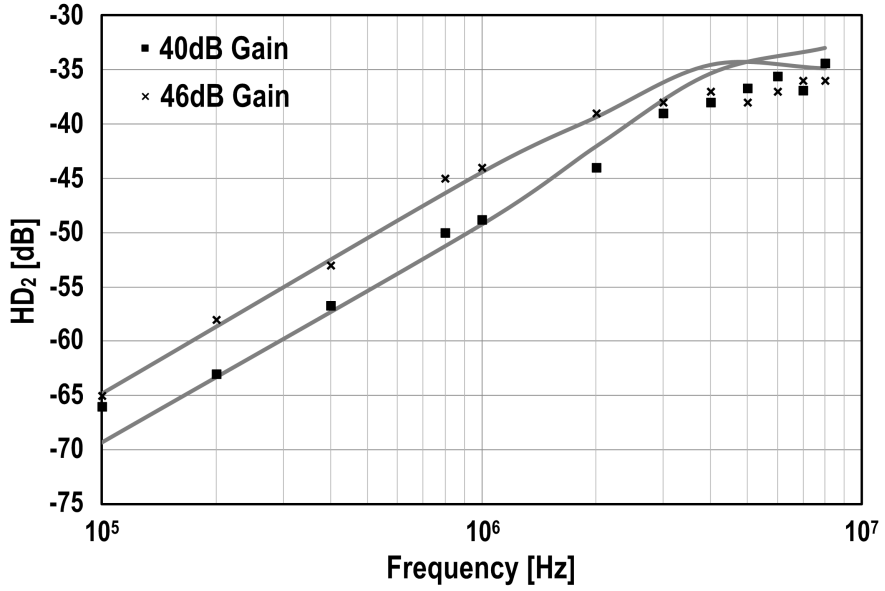

Figure 4.6: Measured (dots) and simulated (continuous line) and HD_2 versus frequency at $80V_{pk-pk}$ output voltage for two different closed loop gains of 40dB and 46dB.

are also reported for comparison demonstrating a good agreement.

The amplifier has been tested also with a real ultrasound transducer (Esaote - LA533) showing similar frequency response and distortion.

Finally Fig. 4.7 shows the estimated power efficiency for continuous-wave operation when the amplifier is driven at 1MHz and 6MHz. The efficiency at $90V_{pk-pk}$ is 70% and 61% respectively.

A summary of measured performances is reported in Fig. 4.8.

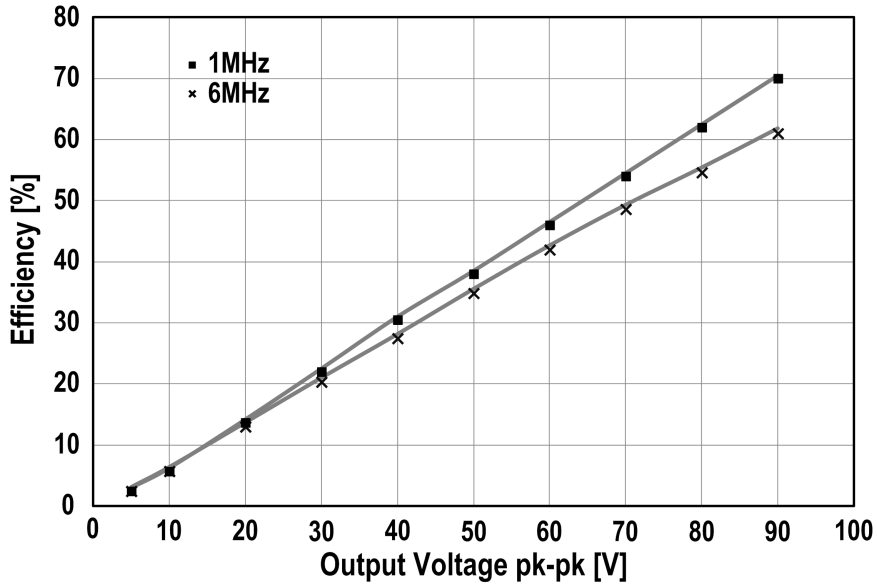

Figure 4.7: Measured (dots) and simulated (continuous line) power efficiency for continuous time operation when the amplifier is driven by a 1MHz and 6MHz input signal.

High Voltage Supply (±HV)	±50V
Low Voltage Supply (±LV)	±2.5V to ±3.5V
Quiescent Power Dissipation	37 mW
Load Impedance	100Ω // 150pF
Maximum Output Voltage (V_{max})	90 V_{pk-pk}
Voltage Gain @ 80V_{pp}	40.9 dB
Bandwidth @ 80V_{pp}	6.5 MHz
Second Harmonic Distortion @ V_{max}	< - 35 dB
Efficiency @ V_{max} , 1MHz	70%
Slew-Rates	+2 / -2.2 kV/µs
Silicon Area	1 mm^2 (Active)
Technology	BCD6-SOI

Figure 4.8: Summary of measured performances.

Conclusions

Linear operational amplifiers for transducers driving in ultra-sound applications are very attractive improving the quality of diagnostic systems. On the other hand, their use is rather limited because they are usually realized with discrete components resulting in large manufacturing costs. In this work, we have leveraged the availability of a BCD-SOI technology and investigated the design of high voltage swing linear amplifier. The analysis carried out in-depth has provided insight useful for circuit design, able to assess large-signal gain and frequency response, distortion and stability. Experiments are in good agreement with simulations and models and show that amplifier performances are adequate for the application. The analysis presented in this work provides also design keys toward improvement to wider operating frequency and/or lower distortion.

List of Figures

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