DATA CONVERTERS FOR SENSOR INTERFACES AND SPACE APPLICATIONS

A Ph.D. Thesis

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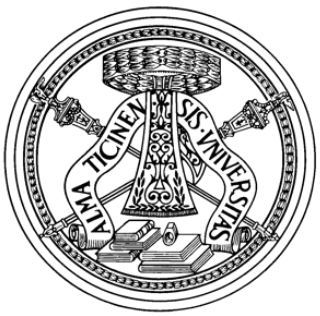

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To my fiancé, Najmeh Rezaei
and my parents

CONTENTS

LIST OF FIGURES

LIST OF TABLES

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ACRONYMS

ADC	Analog-to-digtal converter
AFF	Analog feed-forward
CMOS	Complementary metal-oxide-semiconductor
CMFB	Common mode feedback
dBc	dB to carrier
dB$_{FS}$	dB to full scale voltage
DAC	Digital-to-analog converter
DFF	Digital feed-forward or D flip-flop
DNL	Differential non-linearity
DR	Dynamic range
DD	Displacement Damage
DDD	Displacement Damage Dose
ENOB	Effective number of bits
ELT	Enclosed layout transistor
FFT	Fast Fourier transform
FOM	Figure of merit
$\mathrm{FOM_S}$	FOM based on Schreier's definition

$\mathrm{FOM_W}$	Walden's FOM
GBW	Gain bandwidth product
I&M	Instrumentation and measurement
INL	Integral non-linearity
MIM	Metal insulator metal
MBU	Multiple bit upset
NTF	Noise transfer function
OSR	Oversampling ratio
OTA	Operational transconductance amplifier
PCB	Printed circuit board
PSD	Power spectrum density
SAR	Successive approximation
SFDR	Spurious free dynamic range
SNR	Signal to noise ratio
SNDR	Signal to noise and distortion ratio
STF	Signal transfer function
SEE	Single event effect
SEU	Single event upset
SET	Single event transient
SEL	Single event latch-up
STI	Shallow trench isolation
SOI	Semiconductor on insulator
SOC	system on chip
RHBD	Radiation hardening by design
RHBP	Radiation hardened by process
THD+N	Total harmonic distortion plus noise
TI	Time interleaved
TID	Total ionizing dose
VLSI	Very large scale integration
$\Sigma\Delta$M	Sigma-Delta modulator

CHAPTER 1

INTRODUCTION

As semiconductor technology evolves, more sensory functions can be integrated on a system-on-chip (SoC). Typical sensor applications include image sensors, weight scales, digital voltmeters, as well as temperature, magnetic, pressure, and bio-potential acquisition for wearable devices. An energy- and area-efficient high resolution analog-to-digital converter (ADC) is especially critical for a battery-operated integrated sensor SoC. Sensor applications often involve narrow-band signals with frequencies from DC [1]-[3] up to several hundred Hz [4]-[6]. Analog-to-digital conversion, which takes continuous-time, continuous amplitude signals (voltage, temperature, sound, etc.) and converts them into a series of numbers to be used for digital signal processing, is becoming the key element of the scholarly and industrial applications of measurement and data acquisition, and A/D converters are surrounding (though invisible in most cases) our everyday life.

Since the invention of pulse code modulation (PCM) [7], people from both academy and industry dedicate themselves to the research and development of data converters for over 80 years. The driven force underlying is the requirement of utilizing an ever-increasing computation capability from digital computers to process signals in digital domain. However, due to the analog nature of the real world, the original analog signals should be digitized before being processed in a digital fashion.

Mixed-signal digital-analog IC design, especially analog-to-digital (A/D) and digital-to-analog (D/A) converters, are also of interest to the radiation tolerant market [8]. The need to understand radiation effects and to combat potential radiation damage in semiconductor devices and circuits has been growing in recent years. Space applications, nuclear physics, and military operations in radiation environments are obvious areas where radiation damage can have serious consequences. Radiation threatens the correct functionality of electronics in space, avionics, nuclear and high energy physics

(HEP) applications. Current research efforts within the field of radiation tolerant electronics design are focused on meeting the requirements by using commercial process foundries instead of radiation hardened process foundries (which are dedicated for the purpose of radiation tolerance). In this way the integrated circuits (ICs) are designed with dedicated techniques to withstand radiation effects, an approach that is called "Hardness By Design" (HBD). This allows circuit designers to using state-of-the-art processes to design ICs, while at the same time delivering radiation-tolerant components. In doing so, designers must be aware of the radiation effects against which circuits have to be protected.

1.1 Motivation and Objectives

In the sensor interfaces, especially instrumentation and measurement, there is a growing demand for A/D converters with low or medium bandwidth, but with high absolute accuracy. High linearity and small offset are also among the requirements, as well as low power-consumption and less sensitivity to environmental noise (such as the periodic noise coupled from the mains or digital switching noise). One solution to the problem is the incremental (or charge-balancing) $\Delta\Sigma$ converter, which is basically a first-order $\Delta\Sigma$ A/D converter, operated in transient mode. The converter represents a hybrid between the classical dual-slope converter and the $\Delta\Sigma$ one [9]. The achieved resolutions for incremental ADCs ranges from 16-bit to 22-bit and the BW spans from DC up several kHz at most.

The first motivation of this research activities was to introduce an energy-efficient architectures for high-resolution sensor applications by taking advantage of residue accumulation and hardware-sharing configuration of IADCs with extended-counting technique. The first part of this dissertation dedicated to the design of an innovative time-interleaved incremental with an extended-range SAR ADC for battery monitoring.

The second part of my thesis spent on the radiation hardness by design (RHBD) approaches for the space application. The idea behind RHBD is to remove the radiation tolerance requirements from the hardware level (technology used for the design) and transfer them to the design level. In RHBD, electronic components are manufactured to meet specified radiation tolerance requirement, but the techniques employed to meet these specs are implemented either in the system architecture or in layout and not in the fabrication process. Through a combination of the application of specific design techniques and the leveraging of the increased intrinsic radiation hardness of modern advanced integrated circuit (IC) technologies, it is now possible to fabricate radiation-hardened components using standard complementary metal-oxide-semiconductor (CMOS) processes.

RHBD circuits do impose an area, speed and power consumption overhead compared to the equivalent unhardened circuits in the same process. Nevertheless, due to the fact that radiation hardened process foundries lag 2-3 generation behind commercial process foundries in terms of performance (and availability), the use of commercial process flows are therefore attractive for meeting radiation tolerance requirements at the same time as increasing the performance [10, 11]. The ultimate goal of utilizing commercial IC processes is the instigation of cheaper and faster design and production of radiation tolerant electronics, while maintaining the best possible performance and minimizing RHBD penalties. The radiation effects and hardening techniques to mitigate them constitute a very wide field-of-study. A 10-bit radiation-hardened SAR ADC for the space application has been designed and fabricated in 0.15um RF CMOS commercial process by the LFoundry technology to evaluating the radiation-hardening techniques by design in the mixed-signal analog-digital circuits.

1.2 Thesis outline

This thesis assumes that the reader has a basic knowledge on analog circuit design, layout and is familiar with the semiconductor concepts and physics. The thesis is organized in the following way:
Chapter 2 reviews the fundamentals of Analog to Digital conversion, touching upon the static and dynamic performance metrics of ADCs, also introduce to the reader the most common data converter architectures and provides a discussion on the state-of-the-art of ADCs especially incremental converters with extended range technique.
Chapter 3 explains the design and implementation of an 8-channel 14-bit 33.6V high-voltage time-interleaved extended counting ADC for monitoring the voltage of a stack of 8 Li-Ion batteries. The system uses an 8-channel time-interleaved incremental ADC for the coarse conversion of the battery cell voltages, and a single SAR ADC for the fine conversion to provide the extended resolution. The high-voltage section is limited to 8 innovative H.V switches and a high-voltage sampling capacitor which provide simplicity and reducing the cost of the converter. The remaining part of the circuit operates at a nominal $5-V$ supply. The time-interleaved structure obtains an almost-simultaneous sampling of the battery cells, and the single fine converter limits the mismatch between channels. All channels are measured in $720\mu s$ and the measured residual offset is $642.5\mu V$. The dynamic input range of the system can be as large as 33.6V, and the achieved FoM_S is 129.5dB.
Chapter 4 provides background information on the radiation environment and describes the radiation effects in silicon materials and electronics in general, also the most important radiation induce effects in CMOS devices and ICs have been discussed.
Chapter 5 explains the design techniques that can be used to reduce or completely remove a system susceptibility to the radiation induced effects. A 10-bit radiation-hardened SAR ADC for the space application has been designed and implemented in a commercial process to evaluating the RHBD techniques in the mixed-signal analog-digital circuits. The ADC has been fabricated in a 0.15-μm RF CMOS process 1.8V technology by LFoundry (LF15A PDK). The prototype active area is 212$\times$285 μm^2 and consumes $1.23mW$. It operates with a nominal supply voltage of 1.8V. Post-layout *noise-transient* simulation results show an ENOB equal to 9.6 bits in the band of interest, $[1-10]kHz$, at full scale input voltage. The resulted figure of merit is 792 fj/convesrion-step.
Chapter 6 covers the general conclusions resulting of this thesis work.

REFERENCES

1. R. Wu, Y. Chae, J. H. Huijsing, and K. A. A. Makinwa, “A 20-bit range read-out IC with $50 - nV$ offset and 0.04% gain error for bridge transducers”, *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2152-2163, Sep. 2012.
2. Z. Tan, S. H. Shalmany, G. C. M. Meijer, and M. A. P. Pertijs, “An energy-efficient $15 - bit$ capacitive-sensor interface based on period modulation”, *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1703-1711, Jul. 2012.
3. Z. Tan et al., “A 1.2-V 8.3-nJ CMOS humidity sensor for RFID applications”, *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2469-2477, Oct. 2013.
4. N. Van Helleputte et al., “A multi-sensor biomedical SoC with bio-impedance, 3-channel ECG, motion artifact reduction and integrated DSP”, *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 230-244, Jan. 2011.
5. C.-H. Chen, J. Crop, J. Chae, P. Chiang, and G. C. Temes, “A 12-bit 1 kHz/channel incremental ADC for biosensor interface circuits”, *in Proc. IEEE Int. Sym. Circuits Syst.*, 2012, pp. 2969-2972.
6. A. Agah et al., “A high-resolution low-power oversampling ADC with extended-range for bio-sensor arrays”, *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1099-1110, Jun. 2010.
7. A. H. Reeves, “Electric Signaling System", U.S. Patent 2272070, Feb. 1942.
8. E. Dodd, M. R. Shaneyfelt, J. R. Schwank, J. A. Felix, “Current and Future Challenges in Radiation Effects on CMOS Electronics”, *IEEE Transactions on Nuclear Science*, vol. 57, no. 4, pp. 1747-1763, Aug. 2010.
9. V. Quiquempoix et al., “A low-power 22-bit incremental ADC”, *IEEE J. Solid-State Circuits*, vol. 41, no. 7, pp. 1562-1571, May 2005.
10. W. T. Holman, in *Radiation Effects and Soft Errors in Integrated Circuits and Electronic Devices*, D. M. F. R. D. Schrimpf, ed., (World Scientific, 2004), Chap. Radiation-tolerant Design for High Performance Mixed-Signal Circuits, pp. 69-366.
11. R. Lacoe, “Improving Integrated Circuit Performance Through the Application of Hardness- by-Design Methodology”, *Nuclear Science, IEEE Transactions on 55*, 1903-1925 (2008).

CHAPTER 2

A/D CONVERTERS FOR SENSOR INTERFACES

As semiconductor technology evolves, more sensory functions can be integrated on a system-on-chip (SoC). Typical sensor applications include image sensors, weight scales, digital voltmeters, as well as temperature, magnetic, pressure, and bio-potential acquisition for wearable devices. An energy- and area-efficient high resolution analog-to-digital converter (ADC) is especially critical for a battery-operated integrated sensor SoC. Sensor applications often involve narrow-band signals with frequencies from DC [1]-[3] up to several hundred Hz [4]-[9]. The ADC should achieve high accuracy even in the presence of DC offset voltage and flicker noise. In addition, often the integrated ADC must be multiplexed among many channels. In applications requiring hundreds of channels, such as image sensor [7], [8] or bio-potential acquisition [4]-[9], the integrated ADCs must be highly efficient in terms of power and chip area SoC.

This chapter deals with the background of ADCs aiming for high resolution ($\geq$12-bit). To start with, a general introduction about ADC fundamentals and performance metrics is given. The $\Sigma\Delta$ ADCs are particularly suitable for achieving high resolution and the incremental analog-to-digital converters (IADCs) are often the best choice in low-frequency high-resolution sensor interfaces [1], [3], [5, 9], [9, 10]. Their advantages [9], [10], [11] include simpler decimation filtering, easy multiplexing, and low latency, thus they are selected and are more detailed investigated, spanning from basic ideas to state-of-the-art information, also incremental architecture could be combined with practically any ADC technology including Nyquist-rate ADC, especially Successive Approximation Register (SAR) ADC to perform extended counting [9], [7], [8].

Due to the nature of high resolution of incremental ADCs, we concentrate on structures and methods for attaining more than 14-bit and low-power consumption.

2.1 ADC Fundamentals and Performance Metrics

An ADC is a device that takes an analog input and outputs digital codes since it has both analog and digital functions, it is a mixed-signal device. An ADC has an analog reference voltage against which the analog input is compared. The input signal varies between 0 and Full Scale (FS), and it is converted to a digital word of N-bits. The digital output word signifies what fraction of the reference voltage is the input voltage [12].

The performance of ADCs is determined by a large set of parameters. Readers may refer to more detailed literature such as [13], to have a better understanding of the full set of specifications. Nonetheless, the items listed below are of the most importance and are used in the overall thesis.

2.1.1 Resolution

Determines the minimum quantity of analog signal which can be detected by ADCs. The smallest step that can be discriminated by an N-bit ADC is $V_{LSB} = V_{FS}/2^N$, where V_{FS} represents the full scale range of the converter [13]. The size of the LSB compared to the total code range is sometimes also referred to as resolution of the converter so for an N-bit ADC, thus resolution would be $1/2^N$. For example, a 14-bit ADC with a full scale voltage (V_{FS}) of $2V$ can differentiate the minimum voltage $122.1\mu V$.

2.1.2 Bandwidth

Specifies the maximum frequency of input sinusoid signal which leads to a $\sqrt{2}/2$ attenuation of the amplitude after the A/D conversion.

2.1.3 Quantization Error

The quantization error caused by quantization of an analog (continuous) signal to set of discrete values. For ideal ADC it is V_{LSB}/2. It is modeled as white noise that is uncorrelated to the signal, which is a good estimation for large number of quantization levels [12]. Considering the error as white noise having equal probability lying in the range of $\pm \mathrm{V_{LSB}}/2$ the resulting noise power is given in an equation below;

$$P_{quantizationnoise} = V_{LSB}^2/12. \tag{2.1}$$

2.1.4 Signal-to-noise Ratio (SNR)

The SNR indicates the ratio between input signal power (P_S) and the sum of total noise power (P_N), within in a certain frequency band, which is always expressed in dB format as follows

$$SNR = 10 \times log_{10} \frac{P_S}{P_N}. \tag{2.2}$$

where P_S is the power of the signal

$$P_S = \frac{\left(V_{LSB} \times 2^{N-1}\right)^2}{2}. \tag{2.3}$$

2.1.5 Signal-to-noise-and-distortion Ratio (SNDR)

The SNDR is similarly to the definition of SNR, except the non-linear distortion term. The SNDR can be estimated as

$$SNDR = 10 \times log_{10} \frac{P_S}{P_N + P_H}. \tag{2.4}$$

where P_H refers to the total harmonic distortion generated by circuits or systems. It is noteworthy that SNDR is dependent on the input signal frequency and amplitude, degrading at high frequency and power.

2.1.6 Spurious Free Dynamic Range (SFDR)

It is defined as the ratio of power between fundamental signal to the power of largest harmonic distortion. SFDR is usually measured in dBc (dB to carrier) or in dB_{FS} (dB to full scale range).

$$P_{SFDR} = 10log_{10} \left[\frac{P_{signal}}{P_{spurious}} \right]. \tag{2.5}$$

2.1.7 Total Harmonic Distortion (THD)

The THD is the ratio of the total power of harmonic components to the input signal power [15].

$$THD = \frac{P_2 + P_3 + P_4 + P_5 + P_6 \cdots + P_n}{P_{signal}}. \tag{2.6}$$

where P_{signal} is the power of the fundamental tone that is the signal, and P_n is the power of the n^{th} harmonic. As the number of harmonic distortions are infinite, calculation is restricted to 10 harmonics, also the power of higher order harmonics is almost negligible.

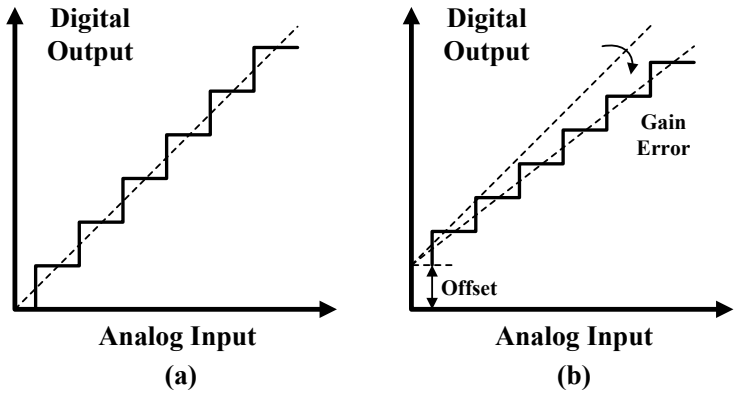


Figure 2.1 Offset and gain error of ADCs.

2.1.8 Offset Error

Quantifies the amount by which the actual characteristic is linearly shifted from its ideal position. Fig. 2.1 (b) illustrates the real characteristic, which is shifted up with an offset compared with the ideal curve shown in Fig. 2.1 (a). Offset error can considerably reduced by calibration [13].

2.1.9 Gain Error

Is defined as the different slopes between the real characteristic curve and the ideal transfer function, which can be seen in Fig. 2.1 (b). The gain error is easily corrected by calibration [13].

2.1.10 Differential Non-linearity (DNL)

DNL is a term describing the deviation between 2 analog quantities corresponding to adjacent input digital codes. Ideally, analog voltages corresponding to 2 adjacent digital codes are exactly one least significant bit LSB apart. DNL is measured as the largest deviation in terms of 1 LSB step, which is shown in Fig. 2.2 (b).

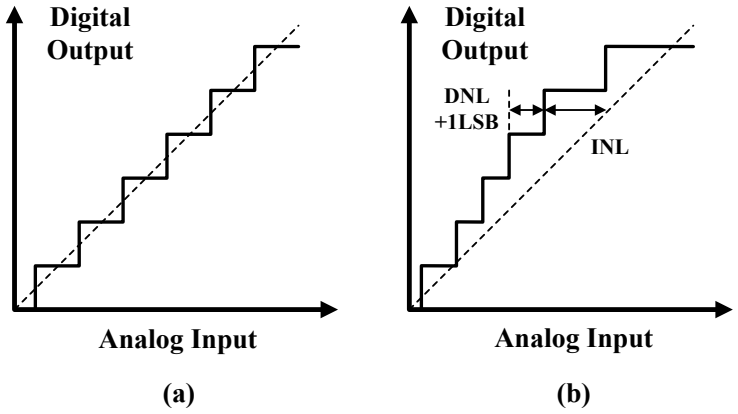


Figure 2.2 Ideal A/D converter versus real A/D converter, showing the DNL and INL concepts.

2.1.11 Integral Non-linearity (INL)

INL is described as the deviation of an actual transfer function from the ideal characteristic, which is represented in LSB or percent of full-scale range. The INL magnitude depends on the position chosen for ideal characteristic. Here, we use end-point INL as illustrated in 2.2 (b). Mathematically INL is best expressed as the sum of DNL for each code [13].

$$INL_i = \sum_{i+=1}^{k} DNL_i \tag{2.7}$$

2.1.12 Effective Number of Bits (ENOB)

ENOB measures the signal-to-noise and distortion ratio with bits. SNDR in dB and ENOB are linked by

$$ENOB = \frac{SNDR - 1.76}{6.02}. \tag{2.8}$$

2.1.13 Figure of Merit (FoM)

FoM is introduced in order to compare the performances between various ADCs which may differ widely in architectures and specifications. One of the most commonly used figure of merit is known as "Walden's" FOM [16] which is defined as

$$FOM_W = \frac{P}{2B_W \times 2^{ENOB}}. \tag{2.9}$$

where P is the power consumption of the ADC. FOM_W is an key parameter to measure ADC's power efficiency and it is expressed in pico-joules per conversion step ($pJ/conv - step$). Another popular figure of merit is Schreier's definition which can be described as

$$FOM_S = SNDR + 10log_{10}\frac{B_W}{P}. \tag{2.10}$$

FOM_S is expressed in dB and its value increases for better performing modulators. According to [17], both FOM_W and FOM_S work well only across a limited range of SNDR. For low-resolution ADCs, evaluation based on FOM_W is more suitable, whereas FOM_S is more appropriate for modulators targeting at high resolutions.

2.1.14 Applications and Categories

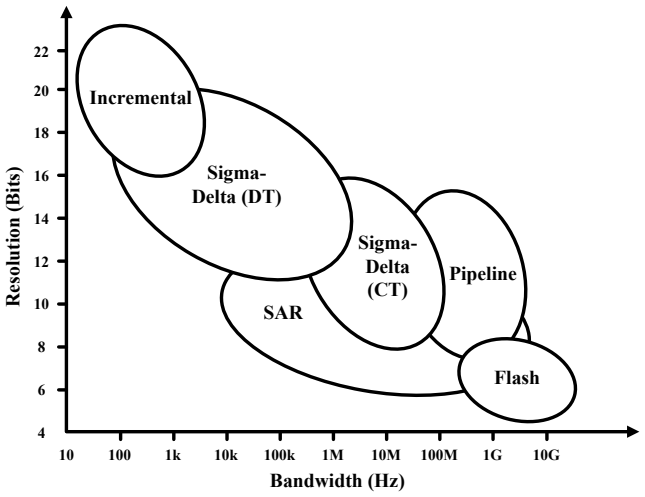


Figure 2.3 ADC architectures for typical resolution and bandwidth requirements.

As mentioned above, data converters are necessary components for the modern electric systems. According to a market survey reported by [18], data converters are becoming the second largest analog component after power management circuits, with unit shipments about 2.9 billion units in 2010 to an expected quantity of around 4.7 billion units by 2015 (stand-alone data converters). Regarding ADCs, the starting point of our study is however, to get familiar with the applications in which ADCs are used. Moreover, for each type of application, corresponding ADC architectures and specifications should be investigated. The typical applications for ADCs are listed as follows

► **Instrumentation and Measurement Applications**: includes applications such as digital multimeter and portable weight scale [19]. The bandwidth of ADCs used in these applications is limited from DC to few kHz, while the resolution requirement is generally more than 16-bit to even 24-bit. Moreover, these ADCs needs to achieve good linearity and low offset. Low-power consumption is also an important factor especially for portable applications. ADCs based on incremental and dual-slope architectures are well suitable to meet these requirements, such as an third-order incremental ADC which attained 22-bit [20].

► **Biomedical and Health Care Applications**: demand for low-power ADCs with low bandwidth and low-moderate resolutions. For example, EEG, ECG and bioimplantable systems require ADCs with data rate less than 200k SPS, and the resolution is between 6-10 bits [21]. In this case, ADCs based on SAR architecture are good choices, such as a 9.1-bit 1k SPS SAR ADC consuming only 53 nW [22].

► **Audio Applications**: generally require ADCs with bandwidth from kHz to few hundreds kHz and THD+N ranging from 60 dB to more than 100 dB. For instance, the voice communication through telephone needs 4 kHz bandwidth and 60-70 dB THD+N. However, high quality DVD audio requires 16-bit to 24-bit resolutions with a sampling rate from 44.1k SPS to 192k SPS. To meet these requirements, $\Sigma\Delta$ ADCs are appropriate candidates. One example is a multi-bit $\Sigma\Delta$ ADC which can obtain 24-bit resolution with 216k SPS output data rate [23].

► **Wireless and Wireline Applications**: demand for modulators with low-medium resolution and large bandwidth. For instance, digital FM (DFM) and LTE-advanced require ADCs with banwidth spanning from 20 MHz to 100 MHz with more than 10-bit resolution. In this case, continuous $\Sigma\Delta$ modulators are appropriate candidates to meet the specification [24]. However, applications such as radar, software-defined radio and multi-channel satellite reception require 2.5-3.0G SPS data rate. One solution is to use the time-interleaved (TI) SAR ADC with 3.6G SPS and 11-bit resolution [25]. Moreover, the 40Gb/s optical QPSK systems require sampling rate more than 24G SPS with 6-bit resolution. In this case, a TI SAR ADC reported in [26] is a good choice which obtained 40G SPS sampling rate and 6-bit resolution with a power consumption less than 1.5 W.

Fig. 2.3 illustrated conventional ADC architectures for typical resolution and bandwidth. It can be seen that DT $\Sigma\Delta$ and incremental types dominate the region when 12-bit or more resolution and less than 2 MHz bandwidth are required.

2.1.15 State of the Art of ADCs

In this subsection, we use the data reported in [17] to investigate state of the art ADCs. The sources of the data are from the results published at IEEE International Solid-State Circuits Conference (ISSCC) and the VLSI Circuit Symposium since 1997 to 2016. Fig. 2.4 plots the power per Nyquist sample with respect to the obtained SNDR. As seen in Fig. 2.4, several ADCs with the best power efficiency in terms of FOM_W were published in ISSCC 2016, such as A $0.35mW$ 12b $100MS/s$ SAR-assisted digital slope ADC in $28nm$ CMOS with FoM_W 2.2/2.6 fJ/conv-step and FoM_S 176.8/177.2 dB [30]. Regarding high resolution ADCs, a 22.3b 1kHz 12.7mW switched-capacitor $\Sigma\Delta$ modulator in [31]

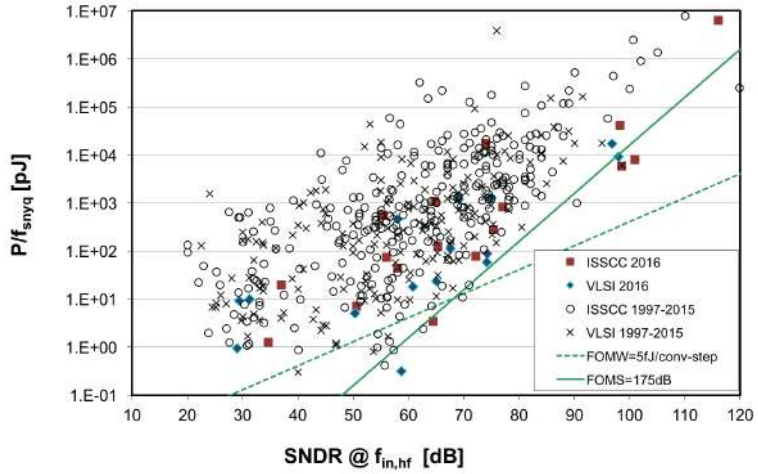


Figure 2.4 Power efficiency of ADCs with respect to SNDR.

with a FoM_S of 197.97 dB and a 6.3 μW 20-bit incremental ADC in [28] with a FoM_S of 182.7 dB, were proposed.

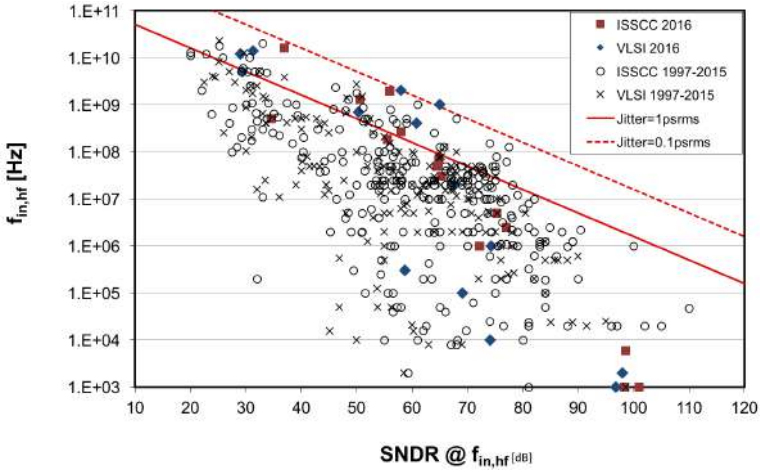


Figure 2.5 Conversion bandwidth of ADCs versus SNDR.

Besides the power efficiency, the achievable bandwidth is also a key parameter. This is because that, in general, when a design is pushed toward the speed limits under a certain technology, the power efficiency is always sacrificed [27]. Fig. 2.5 illustrates the obtained ADCs' bandwidth in terms of SNDR. The dash line represents the performance of an ideal sampler with sinusoid input and a sampling clock with 100 $\mathrm{fs_{RMS}}$ jitter. It can be noticed that ADCs with highest bandwidth over all the resolutions should use a sampling clock with jitter less than 1 $\mathrm{ps_{RMS}}$. However, in order to attain an ADC comparable with state of the art, a better sampling clock with jitter lower than 100 $\mathrm{fs_{RMS}}$ should

be adopted. For instant, the TI pipeline ADC proposed in [29] uses a sampling clock with measured jitter 70 $\mathrm{fs_{RMS}}$, which achieved 14-bit resolution with a 2.5 GSPS output data rate or the cutting edge solution in [32] achieving a FoM_S of 154.4 dB with a sampling frequency equal to 5GS/s and a non-interleaved pipelined ADC architecture.

2.2 ADC Architectures

The first specification which defines a data converter is its type. The conversion algorithm normally provides this kind of information. The types of converters are classified in two main categories: Nyquist-rate and over-sampling. This distinguishes between the following design strategies: using an input that occupies a large fraction of the available bandwidth or using an input-band that only occupies a small part of the Nyquist range.[1] The ratio between the Nyquist limit and the signal band, $\mathrm{f_s}/(2\mathrm{f_B})$, is called oversampling ratio (OSR). Converters with a large OSR are called oversampling converter, whereas Nyquist-rate converters have a small OSR, typically less than 8. Fig. 2.6 illustrates the difference between Nyquist-rate and oversampling. In the former the transition region of the anti-aliasing filter is limited (leading to difficult specifications) and also a large fraction of the total quantization noise power is in the signal band. In contrast, the latter case has a large antialiasing transition region and only a small fraction of the total quantization noise occurs in the signal band. The sampling frequency for oversampling is, obviously, much larger than its Nyquist-rate counterpart, in some cases the OSR can be various hundreds [13, 14]. following subsection briefly reviews the ADC architectures in terms of their type.

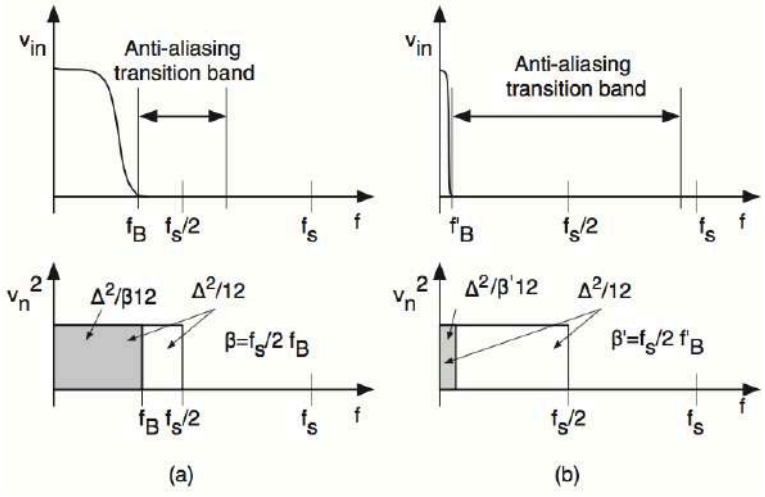


Figure 2.6 Comparing nyquist-rate, (a), and oversampling, (b), strategies [13].

[1]The Nyquist-Shannon sampling theorem states that "A band limited signal, $x(t)$, which Fourier spectrum, $X(jw)$, vanishes for angular frequencies $|\omega| > \omega_s/2$ is fully described by an uniform sampling $x(nT)$, where $T = 2\pi/\varpi_s$." The Nyquist ranges becomes $[0 - f_s]$, where f_s is sampling frequency.

2.2.1 Nyquist Rate A/D Converters

This subsection deals with the architecture, features and limits of Nyquist-rate analog/digital converters. Depending on the bandwidth of the input signal, Nyquist-rate data converters can require either one or multiple clock cycles to implement the conversion algorithm. Since small signal bandwidths enable long conversion periods the algorithm can use high frequency clocks with the sampling period extended over many clock cycles; in contrast, for large bandwidths it is necessary to maximize the time allowed for the circuit operation and so the number of clock periods required for implementing the algorithm must be at a minimum. When the converter uses only one clock cycle the architecture is named full-flash. Furthermore, the throughput of slow converters increases by using the interleaved method which utilizes many converters in parallel or by the pipeline architecture which operates by cascading a number of stages. Although these schemes allow faster sampling-rates they provide output after a latency time, that can give rise to instability when the converter is used in a control system loop [13].

2.2.1.1 Full-Flash ADC

Full-Flash[2] ADC are also known as parallel ADC, as the analog to digital conversion is done for N-bits in parallel. Flash ADC are have a high conversion rate making them suitable for high speed devices. They are suitable for applications requiring very large bandwidth. The downside of this architecture is the huge power consumption which grows drastically with the increase of resolution of the converter, thus making it a good choice only for low resolution (up till 8 bits) applications. This is a major problem as low power applications requiring high speed and accuracy cannot make use of flash ADC. Flash ADC are suitable for application like data acquisition, satellite communication, radar processing, sampling oscilloscopes, and high-density disk drives. Fig. 2.7 shows a typical block diagram of flash ADC, for an N-bit converter the architecture requires $2^N - 1$ comparators. A resistor ladder circuit consisting of 2N resistors, is used to generate distinct reference voltages for the comparators. The reference voltage of each comparator is 1 LSB less than the one preceding it. The comparator performs comparison between the analog input and the reference value if the input is greater it outputs a "1" else a "0" [13, 14]. The quantization step is the dynamic range divided by $2^{\mathrm{n}} - 1$,$\Delta = (\mathrm{V}_{\mathrm{ref}+} - \mathrm{V}_{\mathrm{ref}-})/(2^{\mathrm{n}} - 1)$ with first and last quantization intervals equal to $\Delta/2$. The random and systematic errors affect the generated reference voltages as it happens when the Kelvin divider is used as DAC. Therefore, for a flash type converter, it is essential to use the same kind of resistive material, to use matched contacts and metal interconnections, and to ensure the same resistance orientation in the layout [13].

2.2.1.2 Pipelined ADC

The pipelined ADC architecture as the name reflects employs the pipelined approach for analog to digital conversion, using m-bit identical stages to achieve N-bit conversion. It provides sample rates up to a few hundred Mega samples and resolution up till 16-bits. Reasonably high speed and resolution with comparatively low power consumption and good dynamic performance make it desirable choice for a wide range of applications like Charge Coupled Device (CCD) imaging, ultrasonic medical imaging, digital receivers, base stations, digital video, xDSL, cable modems, and fast Ethernet [33].

The architectural block diagram of a pipelined ADC is shown in Fig. 2.8. It consists of four identical stages of 3-bits (which resolve to 2-bits) and 4-bit flash ADC for the last four bits. The input is v_{in} is held then provided to first stage that utilizes a 3-bit ADC to convert it into a digital code, which is then

[2]The origin of the addition "full" in full-flash can refer to the conversion of the full range. "Partial-flash" converters can refer to a sub-ranging architecture.

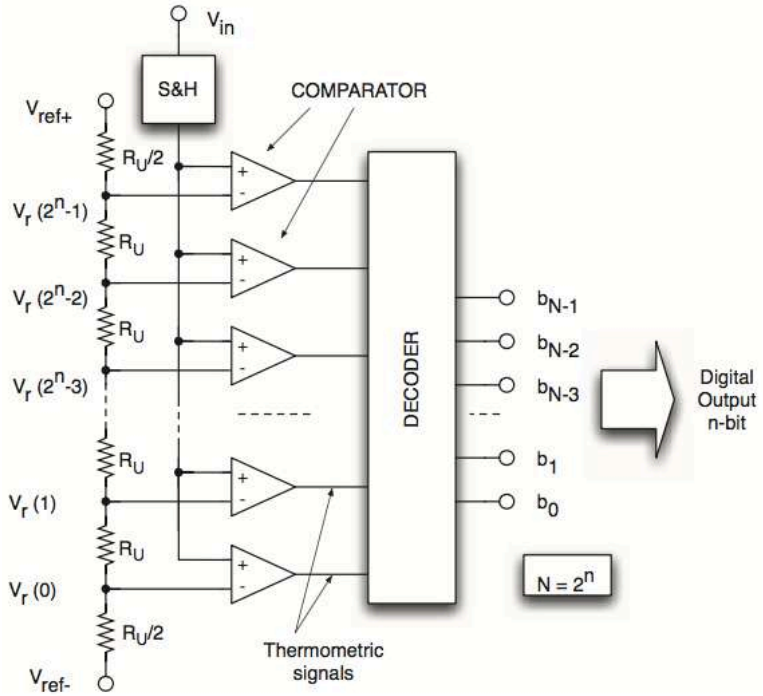


Figure 2.7 Basic block diagram of the full-flash converter [13].

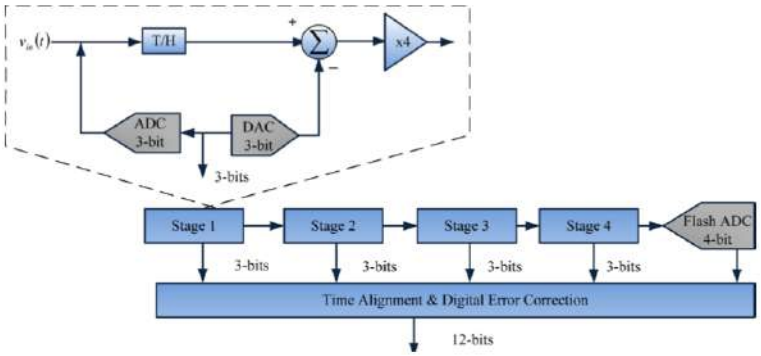


Figure 2.8 Block diagram of pipelined ADC (12-bit ADC with four 3bit stages and a 4bit flash ADC) [33].

fed to a 3-bit DAC which converts it to corresponding voltage level. The v_{in} is sampled and then the output of DAC is subtracted from it, which generates the residue error. As each stage outputs $k = 3$ raw bits, the residues is amplified by a factor of $2^{k-1}=2^2= 4$ before it is sent to the next stage. This gained-up residue continues through the pipeline, providing three bits (raw) per stage until it reaches the 4-bit flash ADC, which resolves the last four LSBs. Bits corresponding to the same sample are time-aligned with shift registers before being fed to the digital-error-correction logic because the bits

are computed at different time points in different stages. When a stage finishes processing a sample it can move to the next sample received from the internal sample and hold, this pipeline action is the reason behind high throughput [33]. With a conversion of one bit per stage, N stages are needed and N samples are simultaneously present in the converter. Additional time is needed for the digital reconstruction and error correction. Therefore the time between the first sampling of the signal and the moment the full digital value is on the output is rather long (N + 3 clock periods). The resulting delay, called latency, will impair the system performance if this converter is part of a feedback loop.

2.2.1.3 Successive Approximation Converters

Where a full-flash converter needs a single clock edge, the successive approximation converter (SAR stands for successive approximation register) will convert the signal in N cycles. Fig. 2.9 shows an abstract flow diagram of a successive approximation algorithm. The output bits a_{N-1} to a_0 are set to 0. In the first cycle the coefficient corresponding to the highest power a_{N-1} is set to 1 and the digital word is converted to a value V_{DAC}. The input level is compared to this value and depending on the result the bit a_{N-1} is kept or set back to 0. This cycle is repeated for all required bits.

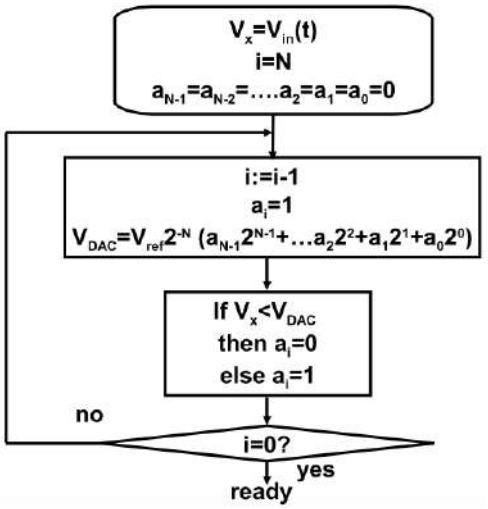


Figure 2.9 A flow diagram for successive approximation [14].

Fig. 2.10 shows a circuit implementation. After the signal is stored in the sample-and-hold circuit the conversion cycle starts. In the register the MSB is set to 1 and the remaining bits to 0. The digital-to-analog converter will generate a value representing half of the reference voltage. Now the comparator determines whether the held signal value is over or under the output value of the digital-to-analog converter and keeps or resets the MSB. In the same fashion the next bits in the output register are determined. The internal clock runs much faster than the sample clock, for every sample a sample-and-hold cycle and N clock cycles are needed. In this scheme the digital-to-analog value approximates the input value. Another implementation reduces the input value by successive subtractions. Offsets in the sample-and-hold circuit or the comparator will generate a shift of the conversion range, but this shift is identical for every code. This principle allows sample rates of tens of MegaHertz. The demands on the various constituent parts of this converter are limited. Main problem is a good sample-and-hold circuit that needs a good distortion specification for relatively low sample periods. Next to the sample

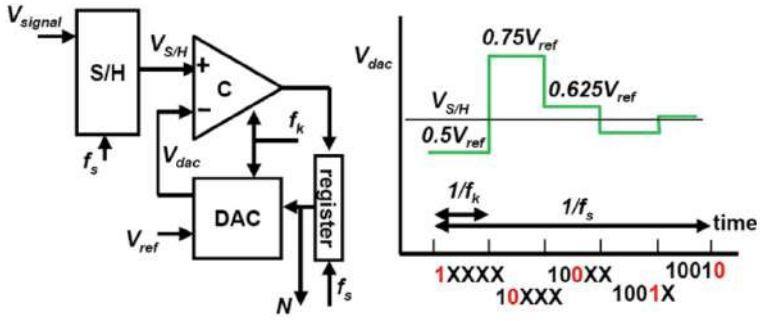


Figure 2.10 A successive approximation analog-to-digital converter with approximation sequence [14].

and hold, the digital-to-analog converter determines the overall linearity and will take up most of the area. The conversion speed is determined by the settling of the digital-to-analog converter. Especially in larger structures with a lot of elements this settling time constant τ_{DAC} can be rather long. For reaching half-an-LSB accuracy in an N bit converter the settling time requirement is:

$$t_{settle} > \tau_{DAC} ln(2^{N+1}). \tag{2.11}$$

For many applications that do not need the maximum conversion speed that is possible in a technology, successive approximation is a safe and robust conversion principle. In applications with a built-in sample-and-hold function (e.g. a sensor output) the combination with a successive approximation converter is appropriate. In combination with a micro-controller, the register function and the timing can be controlled with software. However, special attention must be paid to processor interrupts that can easily disturb the conversion process.

► **SAR Charge-redistribution Conversion**: One of the early fully integrated CMOS successive approximation analog-to-digital converters is known as "charge-redistribution" converters [34]. The principle is shown in Fig. 2.11 and utilizes optimally the properties of CMOS technology: good switches and capacitors. In the sampling phase the input signal is stored on a capacitor bank with a total capacitance value of 16C. "C" is the unit capacitor and is laid-out in a standardized manner. In the second phase the ground plates of the capacitors are switched one after the other from ground to the reference voltage. If the MSB switch is toggled the top plate voltage changes from ground to:

$$V_{top} = -V_{in} + \frac{8C}{C + C + 2C + 4C + 8C} V_{ref}. \tag{2.12}$$

Depending on the original value of the input voltage, the comparator will decide to keep the MSB switch in this position or return to ground. Every bit is subsequently tested. In this implementation the result is a digital code and an output voltage of the digital-to-analog converter that approximates the original input signal.

Fig. 2.12 shows a second example of a successive approximation analog-to-digital converter in standard CMOS technology. The digital-to-analog converter is implemented as a bridged capacitor array. An important difference is that the summation node is not a virtual ground node as it is in the digital-to-analog converter. The voltage swing on the input node of the comparator depends on a correct charge sharing between the capacitors connected. The bridging capacitor and the left hand in

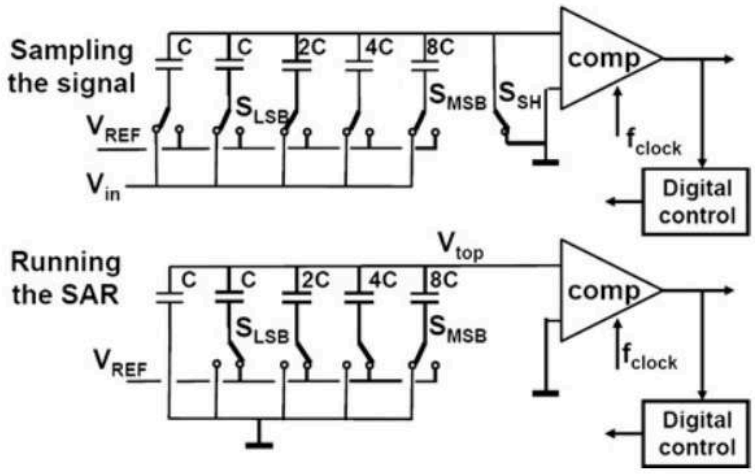


Figure 2.11 A successive approximation analog-to-digital converter based on capacitor switching [14].

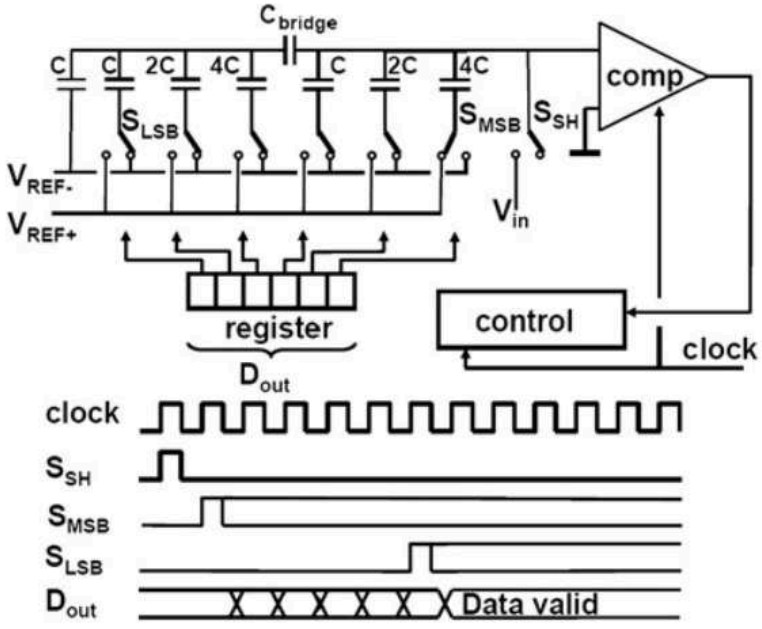


Figure 2.12 A successive approximation analog-to-digital converter based on split capacitor array [14].

series capacitors must sum up to a unit capacitor, so:

$$\frac{C_{bridge}2^kC}{C_{bridge}+2^kC}=C. \tag{2.13}$$

where k is the resolution of the left-hand side array. From this equation the bridge capacitor is found as:

$$C_{bridge} = \frac{2^k}{2^k - 1} C. \tag{2.14}$$

The bridging capacitor can be rounded to unity if k is large [35], thereby avoiding the need for a fraction of a capacitor with various mismatching issues. The conversion cycle starts after the sample is loaded on the capacitors through switch S_{SH}. In this example this action also resets the structure, however, also a separate reset clock cycle and switches can be used. The reference voltages are chosen with equal but opposite voltages with respect to the signal ground level. The purpose of this successive approximation is to make the signal on the input of the comparator equal to the ground level. To achieve that goal in this implementation the MSB-switch in the sampling phase is connected to the plus reference, while the other switches are connected to the negative reference. After the sampling the MSB can be tested and then sequentially all other bits. These successive approximation converters use a limited amount of hardware and good energy efficiencies have been reported [13, 14, 35].

2.2.2 Oversampling A/D Converters

Oversampling converters, initially used for audio-band and high-resolution applications, are now widely used in systems requiring video-band and medium-resolution. The technique, benefits from both noise-shaping and oversampling to give an optimum trade-off between speed and resolution. The key advantage of oversampling is that the signal band occupies a small fraction of the Nyquist interval making it possible to use digital cancellation on the relatively large fraction of the quantization noise that is outside the band of interest. The use an ideal digital filter after the A/D conversion removes the noise from f_B to $f_s/2$ and significantly reduces the quantization noise power by a factor of $f_s/(2f_B)$ leading to

$$V_{n,B}^2 = \frac{\Delta^2}{12} \times \frac{2f_B}{f_s} = \frac{V_{ref}^2}{12 \times 2^{2n}} \times \frac{1}{OSR}. \tag{2.15}$$

where V_{ref} is the reference voltage and n is the number of bits of the quantizer. The definition of the equivalent number of bits shows that an oversampling by OSR potentially improves the number of bits from n to

$$ENOB = n + 0.5 \cdot \log_2 \cdot (OSR). \tag{2.16}$$

where the OSR is the *oversampling ratio*; Equ. 2.16 showing that every increase of the OSR by a factor four potentially improves the converter resolution by 1-bit. The advantage is not so important as, for example, for gaining 5-bit it is necessary to use OSR = 1024. Oversampling is not effective for signals where the assumption that the quantization process can be approximated by white noise is not valid. The signal-to-noise ratio of the conversion of DC-signals cannot be improved by oversampling alone. A helper signal must be present to create the necessary conditions, e.g. in the form of dither. The main advantage of oversampling in analog-to-digital conversion is the extra frequency range that is obtained between the alias band and the band of interest. The specifications of the alias filter can thereby be relaxed, although the higher sample rate will lead to higher power consumption on the digital side.

2.2.2.1 ΣΔ A/D Converters

As mentioned before, one of the most significant breakthroughs in the field of data conversion is ΣΔ modulation. On the basis of oversampling and quantization noise shaping, ΣΔ modulators are

able to tolerate circuit imperfections and thus, the strict requirements of the analog components can be relaxed. The sigma-delta modulator produces a stream of bits even if the input signal is a DC-level. The observation that a sigma-delta modulator has some similarity with a voltage-controlled oscillator is helpful in understanding some aspects of the modulators behavior. Fig. 2.13 shows basic scheme of a sigma-delta modulator.

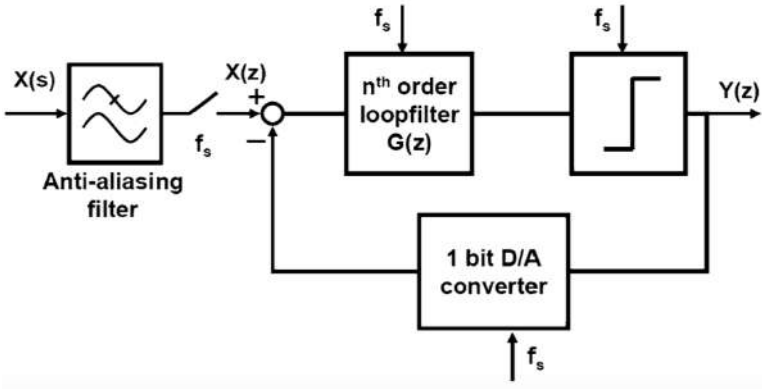


Figure 2.13 Basic scheme of a sigma-delta modulator.

► **First-Order ΣΔ ADC**: A conventional ΣΔ ADC consists of a delayed integrator, a multi-bit quantizer and corresponding DAC, as depicted in Fig. 2.14. The study in z domain gives rise to the transfer function as below

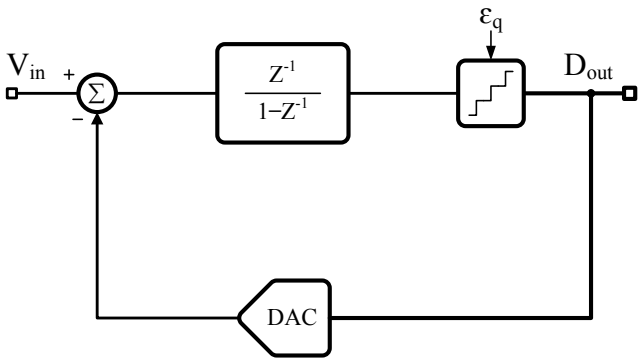


Figure 2.14 First-order ΣΔ ADC block diagram.

$$D_{out}(z) = V_{in}(z)z^{-1} + (1 - z^{-1})\epsilon_q(z) \tag{2.17}$$

As seen in (2.17), both input signal $V_{in}(z)$ and quantization error $\epsilon_q(z)$ contribute to digital output $D_{out}(z)$, by multiplying different transfer functions. For $V_{in}(z)$, the transfer function is called signal transfer function (STF). The transfer function of $\epsilon_q(z)$, however, can be known as noise transfer function (NTF). Thus, using these terms, (2.17) can be rewritten as

$$D_{out}(z) = V_{in}STF(z) + \epsilon_q(z)NTF(z) \tag{2.18}$$

where $STF(z) = z^{-1}$ and $NTF(z) = 1 - z^{-1}$. Since $z = e^{j\omega}$ (F_S normalized to 1 Hz) and by mathematical calculations, the NTF of first-order ΣΔM can be represented by

$$NTF(jw) = 1 - e^{-j\omega} \tag{2.19}$$

Thus,

$$|NTF(w)|^2 = 4sin^2(\frac{\omega}{2}) \tag{2.20}$$

The result shows that the quantization error ϵ_q is high-pass shaped by $|NTF(w)|^2$. Fig. 2.15 plots the power spectrum density (PSD) of D_{out} of first-order ΣΔ ADC. The input signal is -3 dB_{FS} sinusoid waveform at normalized frequency 0.0016. A 2-bit quantizer is used and the DAC has 5 levels. The 2 reference voltages are V_{ref} and -V_{ref}. The full scale voltage V_{FS} is thus equal to $2V_{ref}$. As noticed in Fig. 2.15, the PSD of original ϵ_q is supposed to be white, is high-pass shaped with 20 dB/dec. The achieved SNR is 42.6 dB, which is equivalent to 6.78-bit.

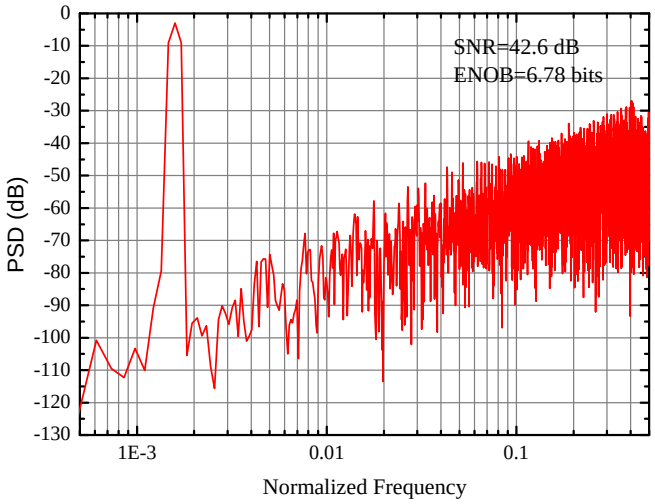


Figure 2.15 PSD (8096-point FFT) of D_{out} of the first-order ΣΔ ADC with -3 dB_{FS} sinusoid waveform input at normalized frequency 0.0016. The OSR is 16.

Besides noise shaping, the second key element of ΣΔ modulation is oversampling. In order to quantitatively describe it, the oversampling ratio (OSR) is defined as $F_S/(2 \times B_W)$. For a fixed B_W, a higher OSR can be obtained by increasing F_S. Consequently, the SNR of ΣΔMs is improved. The reason is that, considering a unilateral representation of the PSD, the power of quantization error is distributed over the first-Nyquist zone. The SNR is calculated by the ration between the power of signal and the power of the noise within B_W. Thus, larger OSR gives rise to reduction of power of quantization error in the band of interest. In this case, the SNR of the corresponding ΣΔM is improved.

The resolution of quantizer b_q can also affect the performance of ΣΔMs, where b_q is defined as $log_2(V_{FS}/V_{LSB})$. Generally, the quantization error can be regarded as white noise, whose power can be estimated by

$$P_{NQ} = \frac{V_{LSB}^2}{12} \tag{2.21}$$

As seen in (2.21), by increasing b_q, the quantization interval V_{LSB} can be smaller, leading to a reduction of the power of quantization error P_{NQ}.

With the previous discussion, the resolution of first-order ΣΔM is determined by OSR and b_q. The relationship between SNR and those design parameters can be expressed as

$$SNR_{1ord,\Sigma\Delta} = 6.02b_q + 1.76 - 5.17 + 9.03 \times log_2(OSR) \tag{2.22}$$

► **Second-Order ΣΔ ADC**: The performance of first-order ΣΔ ADC is limited. One method of boost the performance is increase the order of the structure. Fig. 2.16 shows a second-order ΣΔM which consists of 2 delayed integrators with different coefficients, a multi-bit quantizer and DAC. The study in z domain leads to the transfer function as below

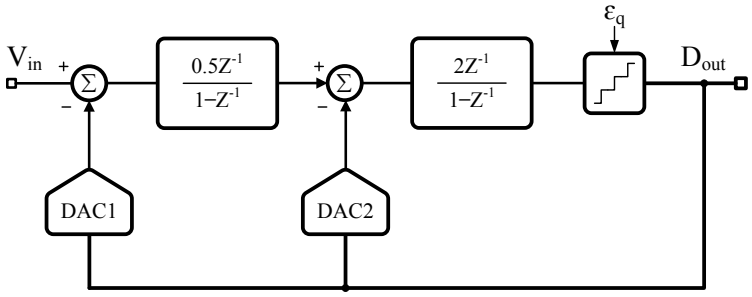


Figure 2.16 Second-order ΣΔ ADC block diagram.

$$D_{out}(z) = V_{in}(z)z^{-2} + \epsilon_q(z)(1 - z^{-1})^2 \tag{2.23}$$

where ϵ_q is high-pass shaped by a second-order NTF. The benefit of second-order structure against first-order scheme is obvious: the power of quantization error within the band of interest experiences a larger suppression because of a second-order NTF. To compare the performance with the first-order architecture, same design parameter are chosen $b_q = 2$ and $OSR = 16$. As noticed in Fig. 2.17, the PSD of ϵ_q is shaped with 40 dB/dec due to the second-order high-pass NTF. The achieved SDR is 58.7 dB, which is equivalent to 9.45-bit.

For a Nth-order ΣΔ ADC whose NTF and STF has a denominator equal to 1, the SNR can be estimated as follows

$$SNR_{Lord,\Sigma\Delta} = 1.78 + 6.02q_b - 10log_2\frac{\pi^2 L}{2L+1} + 3.01(2L+1)log_2(OSR) \tag{2.24}$$

where L, q_b and OSR are the 3 key parameters when designing ΣΔMs. The optimum designs of ΣΔ ADCs are attained by a good tradeoff between these parameters. In general, high-order modulators guarantee high resolution, but a large number of op-amps are needed, which means the power dissipation will be increased. Moreover, high OSR grants good resolution at the cost of increased F_S, which leads to high power consumption in the overall circuit. The use of multi-bit architectures benefits the modulator with extra resolution, however, it increases the design complexity with more comparators required in the quantizer. Another issue comes from the non-linearity of the multi-bit DAC, which should be carefully compensated for in order to prevent performance degradation.

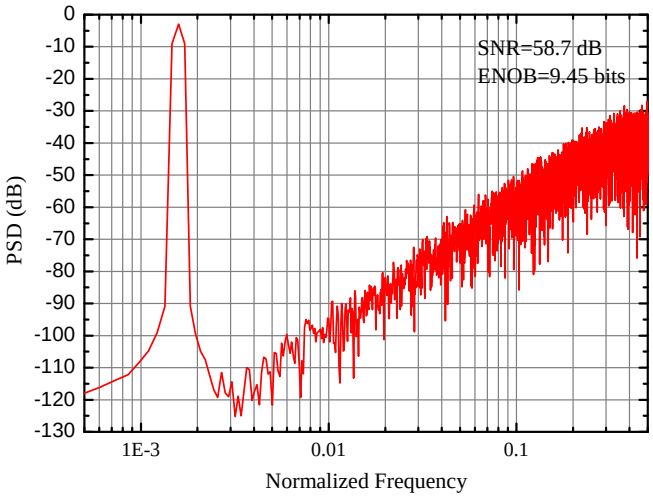


Figure 2.17 PSD (8096-point FFT) of D_{out} of the second-order $\Sigma\Delta$ ADC with -3 dB_{FS} sinusoid waveform input at normalized frequency 0.0016. The OSR is 16.

2.2.2.2 *Incremental A/D Converters*

Incremental ADCs are always used in instrumentation and sensing applications, such as readout of bridge transducers and biomedical acquisition systems [36, 37]. The advantages of incremental ADCs are good linearity, high resolution, low offset and low power dissipation. Although sharing the same structures of $\Sigma\Delta$ modulators ($\Sigma\Delta Ms$), incremental ADCs reset the output of op-amps every N clock periods and provide a sample-to-sample conversion, thus they can be classified as Nyquist-rate data converters.

Incremental ADC comes from the combination of $\Sigma\Delta$M and dual-slope ADC, which was first proposed by Van De Plassche in 1978 [38]. Fig. 2.18 shows the block diagram of a first-order incremental ADC. It is constituted of a delayed-integrator, a comparator and a 2-level DAC. The

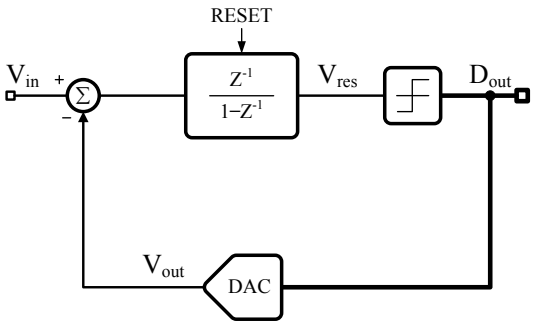


Figure 2.18 First-order incremental ADC block diagram.

working principle is as follows: at the beginning of a conversion cycle, the output of the integrator

is reset. For incremental ADCs, the frequency of input signal ranges from DC to few KHz at most, thus V_{in}, because of oversampling varying slowly, could be regarded as $\frac{\sum_{i=1}^{N-1} V_{in}(i)}{N} = \overline{V_{in}}$. In each clock cycle, V_{in} subtracts V_{out} and the difference is accumulated at the output of integrator, where V_{out} is the analog version of the digital output D_{out}. Since a comparator is used in the modulator, D_{out} has two possible values. Whenever the input of the comparator goes above zero, D_{out} becomes 1, and the corresponding V_{out} is V_{ref}. Otherwise, D_{out} equals to -1 and $V_{out} = -V_{ref}$. At the end of the Nth clock period, the residue voltage at the output of integrator is

$$V_{res}(N) = \sum_{i=1}^{N-1} \overline{V_{in}} - \sum_{i=1}^{N-1} D_{out}(i) V_{ref} \tag{2.25}$$

where $-V_{ref} < V_{res}(N) < V_{ref}$ holds. This is ensured by the stability of the feedback loop. Thus, the input signal can be estimated as

$$\overline{V_{in}} = \frac{\sum_{i=1}^{N-1} D_{out}(i) V_{ref}}{N-1} + \frac{V_{res}(N)}{N-1} \tag{2.26}$$

As seen in (2.26), the first term of right-hand side is the digital estimation of $\overline{V_{in}}$. The quantization error is the second term, which is determined by the residue voltage of integrator $V_{res}(N)$ and the number of clock cycles per sample N. Here, ϵ_q is used to represent the quantization error as below

$$\epsilon_q = \frac{V_{res}(N)}{N-1} \tag{2.27}$$

The quantization error ϵ_q should be within half quantization interval V_{LSB}, thus

$$|\epsilon_q| < \frac{V_{LSB}}{2};\ V_{LSB} = \frac{V_{FS}}{2^{R_{1ord}}} \tag{2.28}$$

where $V_{FS} = 2V_{ref}$ is the full scale voltage and R_{1ord} is the maximum resolution that the first-order incremental scheme plotted in Fig. 2.18 can achieve. By using (2.25)-(2.29), the resolution of first-order incremental scheme can be derived as

$$R_{1ord} = \frac{V_{res}}{\max\{|\epsilon_q|\}} = log_2(N-1) \tag{2.29}$$

Unfortunately, the conversion efficiency of a first-order incremental ADC is low. Methods for increasing the resolution are augmenting the number of clock periods N and using more effective schemes with cascaded accumulators. High-order incremental ADCs, therefore, contain multiple integrators with reset. The key point is to increase the accumulation efficiency, maintain the stability of structure and keep $V_{res}(N)$ minimized [20], [39]-[43].

In order to maintain stability of the loop filter, distributed feedback or feed-forward paths are usually used in incremental ADCs. Although the inaccurate feed-forward coefficients cause error along the accumulation path, it is just a gain factor since the input signal is almost constant. However, it is quite difficult to analyze the error due to the inaccurate feedback coefficients. This is because the feedback signal varies in time and injects signal in different locations. Based on the above analysis, for high-order incremental ADCs, the recommended way to maintain stability is to use multiple feed-forward paths and the adoption of more than 1 DAC should be prevented.

A conventional second-order incremental modulator is discussed here to show how the conversion efficiency changes compared with the first-order structure. As seen in Fig. 2.19, this structure contains

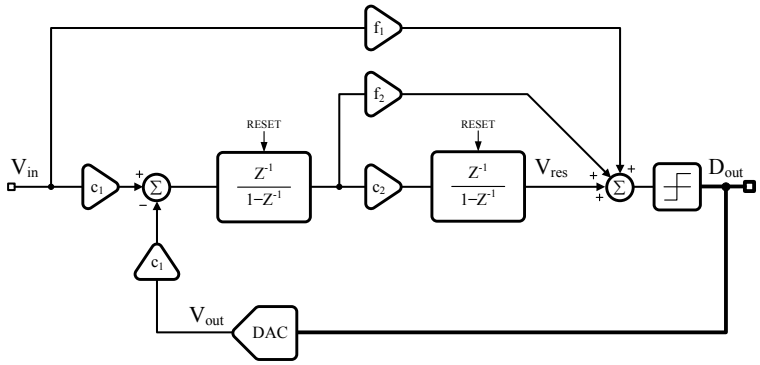


Figure 2.19 Second-order feed-forward incremental modulator block diagram.

2 delayed-integrators. Along the accumulation path there are 2 coefficients c_1 and c_2. In order to keep the loop stable, two feed-forward paths are included with coefficients f_1 and f_2. This scheme also employs a comparator and 2-level DAC. Using the same method, $V_{res}(N)$ for this second-order architecture can be written as

$$V_{res}(N) = c_1 c_2 \sum_{i=1}^{N-1} \sum_{j=1}^{i-1} \overline{V_{in}} - c_1 c_2 \sum_{i=1}^{N-1} \sum_{j=1}^{i-1} D_{out}(i) V_{ref} \tag{2.30}$$

Similarly, the input signal can be represented as a digital estimation part and a quantization error as follows

$$\overline{V_{in}} = \frac{c_1 c_2 \sum_{i=1}^{N-1} \sum_{i=j}^{i-1} D_{out}(i) V_{ref}}{M} + \frac{V_{res}(N)}{M} \tag{2.31}$$

where M is a constant which can be expressed as

$$M = \frac{c_1 c_2 (N-1)(N-2)}{2!} \tag{2.32}$$

Notice that M is a quadratic function of N. It means that the quantization error of second-order architecture can be much smaller than the counterpart of first-order scheme, provided a relative large N is used. The resolution of the second-order structure is derived as

$$R_{2ord} = log_2(M) = log_2 \frac{c_1 c_2 (N-1)(N-2)}{2!} \tag{2.33}$$

To compare the conversion efficiency of first-order and second-order incremental ADCs, (2.29) and (2.33) are used with $N = 1024$ and $c_{1,2} = 1$. The reason that c_1 and c_2 are chosen to be 1 is to simplify the situation. The stability is ensured with proper selection of f_1 and f_2. Both calculations and simulation results show that the first-order structure achieves a maximum resolution 10-bit, while the second-order architecture can obtain 19-bit.

An Lth-order incremental modulator with multiple feed-forward paths, feedback paths and coefficients is illustrated in Fig. 2.20. It consists of L delayed integrators, a comparator and a 2-level DAC. Along the accumulation path, there are L different coefficients $c_{1,2,...,L}$. Moreover, to maintain the stability of the loop filter, L feed-forward paths are introduced with coefficients $f_{1,2,...,L}$. In order to estimate the

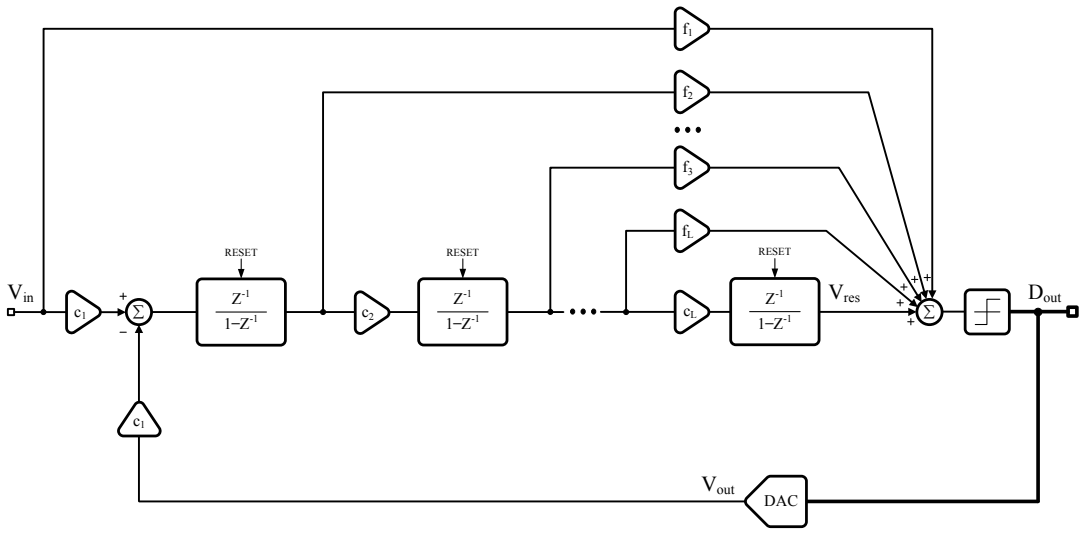


Figure 2.20 L_{th}-order incremental ADC architecture.

resolution of Lth-order incremental ADC, an equivalent model is plotted in Fig. 2.21. In this model, the feed-forward paths are removed since the purpose of them is to maintain stability and they do not affect the conversion efficiency. Using this model, it can be seen that during N clock periods, the difference between c_1V_{in} and c_1V_{out} is continuously injected at the input of the first integrator and then accumulates though L integrators. Hence, at the end of N clock period, the final accumulation result can be expressed as

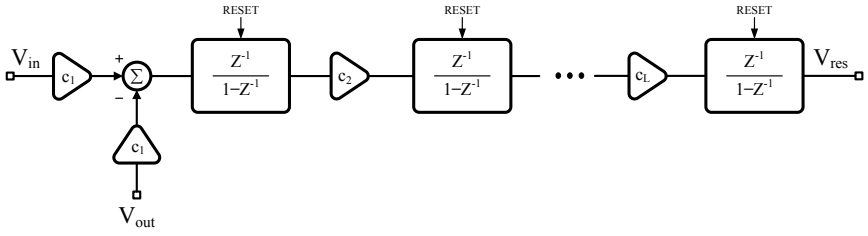


Figure 2.21 The equivalent model of L_{th}-order incremental ADC.

$$V_{res}(N) = c_1c_2...c_L \sum_{i_1=1}^{N-1} \sum_{i_2=1}^{i_1-1} ... \sum_{i_L=1}^{i_{L-1}-1} \{\overline{V_{in}} - D_{out}(i_L)V_{ref}\} \tag{2.34}$$

Thus

$$\overline{V_{in}} = \frac{1}{M} c_1c_2...c_L \sum_{i_1=1}^{N-1} \sum_{i_2=1}^{i_1-1} ... \sum_{i_L=1}^{i_{L-1}-1} D_{out}(i_L)V_{ref} + \frac{V_{res}(N)}{M} \tag{2.35}$$

where

$$M = c_1 c_2 ... c_L \frac{(N-1)(N-2)...(N-L)}{L!} \tag{2.36}$$

By combining (2.34)-(2.36), the resolution of L_{th}-order incremental converter can be written as

$$R_{Lord} = log_2 \frac{c_1 c_2 ... c_L (N-1)(N-2)...(N-L)}{L!} \tag{2.37}$$

2.2.2.3 Time-Interleaved ΣΔ Modulators and Incremental ADCs

There has been considerable research on time-interleaved ΣΔ modulators in the past several years. In [44], block digital filtering is applied to a ΣΔ modulator so that parallel branches are able to operate at a reduced rate. However, a multiplexer on the input and the decimation filter on the output must operate at the full-rate, and a critical path between the two branches exists that would make it difficult to time-interleave by more than two. To overcome this problem, [45] introduced an architecture that both eliminated the critical path and removed the input multiplexer at the expense of images of the input signal occurring at harmonics of the internal sampling frequency between 0 and $f_s/2$ (where $f_s/2$ is the higher effective sampling frequency). This limits the maximum time-interleaved factor for a given OSR.

Time-interleaved ΣΔ modulators can only operate at an OSR equal to the time-interleaving factor if the input samples are split up at the input. However, this requires a high-speed input multiplexer that would need to operate at a very high frequency since a practical ΣΔ modulator would need to operate with an OSR of at least 4. Therefore, it would be very difficult to operate time-interleaved ΣΔ modulators with an OSR equal to the time-interleaving factor.

Incremental ADCs can be time-interleaved by placing N incremental ADCs in parallel, resulting in an effective sampling frequency of $\mathrm{N} \cdot \mathrm{f_s}$. Alternatively, for an OSR of M, this can be viewed as effectively reducing the OSR to M/N, resulting in an increase in the signal bandwidth by N. One major difference between time-interleaved ΣΔ modulators and time-interleaved incremental ADCs is the location of the downsampling operation. Each individual modulator in a time-interleaved incremental ADC down-samples its output so that the individual outputs are at a lower rate than the internal modulator. Therefore, the recombining of the parallel outputs is no faster than the operating frequency of the internal modulators. In contrast to this, time-interleaved ΣΔ modulators down-sample the recombined output, which means that the decimator and down-sampler are all operating at the high rate.

Time-interleaved incremental ADCs have several advantages. First, contrary to time-interleaved ΣΔ modulators, all the circuitry is operating at the sampling rate or slower since it does not require higher-rate multiplexing at the input, or higher-rate downsampling at the output, which significantly reduces the digital power of the decimator. Also, there is no cross-coupling between the parallel branches, which means that there is no critical path to overcome. And lastly, no images of the input signal occur in the output spectrum. These advantages lead to an important result; the time-interleaved incremental ADC can be time-interleaved by the same amount that it is oversampled, resulting in a modulator that over-samples data in each parallel branch (thus reducing the requirements on the DC gain, linearity, etc.) while still attaining the speed of a Nyquist-rate ADC. The challenge is in choosing a modulator where the STF does not attenuate the signal significantly at input frequencies near $f_s/2$.

2.2.3 State of the Art of Incremental Converters and Extended-Range Technique

In order to obtain high resolution incremental ADCs, the order of the scheme L can be increased and the residue voltage V_{res} should be minimized. In 2006, a 22-bit third-order incremental modulator using 2-level quantization was reported in [20], whose scheme is the same as one plotted in Fig 2.20

with $L = 3$. To the best of author's knowledge, it is the incremental modulator which achieved highest resolution in the open literature up to date. Meanwhile, a fourth-order design was proposed in [41] and the obtained resolution is 16-bit.

To minimize V_{res}, a second-order incremental scheme with extended-range was report in [43]. The second-order architecture is the same as the one plotted in Fig. 2.19, while the second-stage is a 9-bit SAR modulator. The key point is that after the first-stage generates a coarse residue voltage V_{res}, the 9-bit SAR stage uses V_{res} to produce a refined residue voltage $\widehat{V_{res}}$ and a digital code. In this case, V_{res} is reduced and the performance of the modulator is improved. With the extended-range technique, the maximum achieved SNDR of the second-order modulator proposed in [43] is 86.3 dB and the FOM_W is 1.46 pJ/conv-step. Another technique which is able to reduce V_{res} and avoid using extra stage was reported in [46, 47]. For example, the modulator proposed in [46] uses a 2-step conversion: the first-step is to use a conventional second-order feed-forward structure as illustrated in Fig. 2.19; the second-step is, however, to reconfigure the hardware to a first-order incremental scheme. Specifically, the second op-amp is configured as a voltage buffer to maintain V_{res} and the first op-amp is adopted to perform a first-order incremental operation. Compared with the aforementioned extended-range technique, the hardward reconfiguration technique is more efficient in terms of power consumption, however, at the expense of a lower output data rate.

Besides DT incremental ADCs, designs of CT counterparts are also in progress. A first-order CT incremental modulator is adopted to build a 16-channel neural interface, due to its implicit anti-aliasing filtering property [36]. Garcia extended the CT incremental converter to a third-order structure, which greatly enhances the conversion efficiency with respect to the first-order counterpart, giving rise to a design with peak SNDR 64 dB and 96 μW power consumption over 2 kHz bandwidth [37]. The low-power consumption is due to the requirement of bandwidth and slew-rate is more relaxed in CT ADCs than that of DT modulators.

Novelties of the designs mentioned above are mostly from architecture level. Aiming for low-power dissipation with good FOM, several novel circuit techniques are used in incremental ADCs published recently [28, 48]. For instance, an incremental modulator based on zoom ADC scheme was reported in [28], which achieved 20-bit resolution. To reduce the power consumption, traditional op-amp based integrators are replaced with inverter based counterparts, which gives rise to a total power consumption of $6.3\mu W$ and the best $FOM_S = 182.7dB$ up to now. In [48], a conventional second-order incremental structure is implemented with a self-timed technique instead of traditional synchronized clock scheme. The charge transfer circuits based on gated current source (GCS) and zero-crossing detector (ZCD) are utilized to replace the op-amp based integrators. This design obtained 14-bit resolution, which is relatively low compared with the already achieved performance using conventional schemes and circuit techniques. However, it is still a good trial in order to implement all digital incremental ADCs, especially with the continuously scaled CMOS technology.

REFERENCES

1. R. Wu, Y. Chae, J. H. Huijsing, and K. A. A. Makinwa, "A 20-bit $\pm 40mV$ range read-out IC with $50-nV$ offset and 0.04% gain error for bridge transducers", *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2152-2163, Sep. 2012.
2. Z. Tan, S. H. Shalmany, G. C. M. Meijer, and M. A. P. Pertijs, "An energy-efficient 15-bit capacitive-sensor interface based on period modulation", *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1703-1711, Jul. 2012.
3. Z. Tan, *et al.*, "A 1.2-V 8.3-nJ CMOS humidity sensor for RFID appli- cations", *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2469-2477, Oct. 2013.
4. N. Van Helleputte, *et al.*, "A multi-sensor biomedical SoC with bio-impedance, 3-channel ECG, motion artifact reduction and integrated DSP", *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 230-244, Jan. 2011.
5. C.-H. Chen, J. Crop, J. Chae, P. Chiang, and G. C. Temes, "A 12-bit 1 kHz/channel incremental ADC for biosensor interface circuits", *in Proc. IEEE Int. Sym. Circuits Syst.*, 2012, pp. 2969-2972.
6. A. Agah, *et al.*, "A high-resolution low-power oversampling ADC with extended-range for bio-sensor arrays", *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1099-1110, Jun. 2010.
7. J.-H. Kim, *et al.*, "A 14 b extended counting ADC implemented in a 24 MPixel APS-C CMOS image sensor", *IEEE ISSCC Dig. Tech. Papers*, pp. 390-392, Feb. 2012.
8. Y. Oike and A. El Gamal, "CMOS image sensor with per-column sigma delta ADC and programmable compressed sensing", *IEEE J.Solid-State Circuits*, vol. 48, no. 1, pp. 318-328, Jan. 2013.
9. J. Markus, J. Silva, and G. C. Temes, "Theory and applications of incremental delta sigma converters", *IEEE Trans. Circuits Syst. I*, vol. 51, no. 4, pp. 678-690, Apr. 2004.
10. V. Quiquempoix, *et al.*, "A low-power 22-bit incremental ADC", *IEEE J. Solid-State Circuits*, vol. 41, no. 7, pp. 1562-1571, Jul. 2006.
11. S. Kavusi, H. Kakavand, and A. El Gamal, "On incremental sigma-delta modulation with optimal filtering", *IEEE Trans. Circuits Syst. I*, vol. 53, no. 5, pp. 1004-1015, May 2006.
12. Nicholas Gray, *ABCs of ADCs*. Rev 3, June 2006 Copyright 2003, 2004, 2006 National Semiconductor.
13. F. Maloberti, *Data Converters*. Springer-Verlag, 2007, ISBN 9780387324852.
14. Marcel J.M. Pelgrom, *Analog-to-Digital Conversion*. Springer Dordrecht Heidelberg London New York, 2010.
15. M. Gustavsson, *CMOS A/D Converters for Telecommunications*. Linkoping University 1998.
16. R. H. Walden et al., "Analog-to-digital converter survey and analysis", *IEEE J. Selected Areas in Communications*, vol. 17, no. 4, pp. 539-550, Apr. 1999.
17. B. Murmann, *ADC Performance Survey 1997-2016*, [Online]. Available: http://www.stanford.edu/m̃urmann/adcsurvey.html, 2016.
18. Gabriele Manganaro, *Advanced Data Converters*. Cambridge: University Press, 2012.
19. J. Markus, J. Silva, and G. C. Temes, in *Proc. Custom Integrated Circuits Conference (CICC)*, pp. 41-48, Sept. 2006.
20. V. Quiquempoix et al., "A low-power 22-bit incremental ADC", *IEEE J. Solid-State Circuits*, vol. 41, no. 7, pp. 1562-1571, May 2005.
21. Chao Yuan and Yvonne Y. H. Lam, "A 281-nW 43.3 fJ/Conversion-Step 8-ENOB 25-kS/s asynchronous SAR ADC in 65nm CMOS for biomedical applications", in *Proc. IEEE Int. Symp. on Circuits and Systems (ISCAS)*, pp. 622-625, May 2013.

22. Dai Zhang, Ameya Bhide and Atila Alvandpour, “A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13-μ m CMOS for Medical Implant Devices”, *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1585-1593, Jul. 2012.
23. Texas Instruments, “High-Performance, Two-Channel, 24-Bit, 216kHz Sampling Multi-Bit Delta-Sigma Analog-to-Digital Converter". [online]. Available: http://www.ti.com, 2013.
24. M. Bolatkale et al., “A 4 GHz Continuous-Time $\Sigma\Delta$ ADC With 70 dB DR and -74 dBFS THD in 125 MHz BW”, *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2857-2868, Dec. 2011.
25. E. Janssen et al., “An 11b 3.6GS/s Time-Interleaved SAR ADC in 65nm CMOS”, *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 464-465, Feb. 2013.
26. Y. M. Greshishchev et al., “A 40GS/s 6b ADC in 65nm CMOS”, in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 390-391, Feb. 2010.
27. B. Murmann, “A/D Converter Trends: Power Dissipation, Scaling and Digitally Assisted Architectures”, in *Proc. Custom Integrated Circuits Conference (CICC)*, pp. 105-112, Sept. 2008.
28. Youngcheol Chae, Kamran Souri and Kofi A.A. Makinwa, “A 6.3μW 20b incremental zoom-ADC with 6ppm INL and 1μV offset”, in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 276-277, Feb. 2013.
29. Brian Setterberg1 et al., “A 14b 2.5GS/s 8-Way-Interleaved Pipelined ADC with Background Calibration and Digital Dynamic Linearity Correction”, in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 466-467, Feb. 2013.
30. L. Chun-Cheng, “A 0.35mW 12b 100MS/s SAR-assisted digital slope ADC in 28nm CMOS”, *Solid-State Circuits Conference (ISSCC), 2016 IEEE International*, pp. 462-463, Feb. 2016.
31. M. Steiner, N. Greer, “A 22.3b 1kHz 12.7mW switched-capacitor $\Sigma\Delta$ modulator with stacked split-steering amplifiers”, *Solid-State Circuits Conference (ISSCC), 2016 IEEE International*, February 2016.
32. Ahmed M.A. Ali, et al., “A 14-bit 2.5GS/s and 5GS/s RF sampling ADC with background calibration and dither”, *VLSI Circuits (VLSI-Circuits), 2016 IEEE Symposium on*, Sep. 2016.
33. MAXIM Application Note 1023 Understanding pipelined ADCs. March 2001.
34. J.L. McCreary, P.R. Gray, “All-MOS charge redistribution analog-to-digital conversion techniques I”, *IEEE Journal of Solid-State Circuits 10*, 371-379 (1975).
35. A. Agnes, E. Bonizzoni, P. Malcovati, F. Maloberti, “A 9.4-ENOB $1V$ 3.8μW $100kS/s$ SAR ADC with time-domain comparator”, *in International Solid-State Circuits Conference, Digest of Technical Papers (2008)*, pp. 246-247.
36. R. Wu, Y. Chae, J.H. Huijsing, and K.A.A. Makinwa, “A 20-b $\pm$40mV Range Read-Out IC With 50-nV Offset and 0.04% Gain Error for Bridge Transducers”, *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2152-2163, Sept. 2012.
37. Julian Garcia, Saul Rodriguez and Ana Rusu, “A Low-Power CT Incremental 3rd Order $\Sigma\Delta$ ADC for Biosensor Applications”, *IEEE J. Solid-State Circuits*, vol. 60, no. 1, pp. 25-36, Jan. 2013.
38. R. J. van de Plassche, “A sigma-delta modulator as an A/D converter", *IEEE Trans. Circuits. Syst.*, vol. CAS-25, no. 7, pp. 510-514, Jul. 1978.
39. Robert, J. and Valencic, V., “Offset and Charge Injection Compensation in an Incremental Analog to Digital Converter”, in Proc. European Solid-State Circuits Conference, pp. 45-48, Sept. 1985.
40. Robert, J. and Deval, P., “A second-order high-resolution incremental A/D converter with offset and charge injection compensation”, *IEEE J. Solid-State Circuits*, vol. 23, no. 3, pp. 736-741, Jun. 1988.
41. Colin Lyden et al., “A single shot sigma delta analog to digital converter for multiplexed applications”, in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, pp. 203-206, May 1995.
42. Caldwell, T. C. and Johns, D. A., “Incremental Data Converters at Low Oversampling Ratios”, *IEEE Trans. Circuits. Syst. I*, vol. 57, no. 7, pp. 1525-1537, Apr. 2010.

43. Ali Agah et al., "A high-resolution low-power incremental ΣΔ ADC with extended range for biosensor arrays", *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1099-1110, Jun. 2010.

44. R. Khoini-Poorfard, L. B. Lim, and D. A. Johns, "Time-Interleaved Oversampling A/D Converters: Theory and Practice", *IEEE Trans. Circuits Sys. II*, vol. 44, pp. 634-645, Aug. 1997.

45. K. Lee, Y. Choi, and F. Maloberti, "Domino Free 4-Path Time-Interleaved Second Order Sigma-Delta Modulator", *Proc. IEEE Int. Symp. Circuits and Systems*, pp. 473-476, May 2004.

46. C.-H. Chen et al., "Two-step incremental analogue-to-digital converter", *Electronics Letters*, vol. 49, no. 4, pp. 250-251, Feb. 2013.

47. C.-H. Chen et al., "Multi-step extended-counting analogue-to-digital converters", *Electronics Letters*, vol. 49, no. 1, pp. 30-31, Jan. 2013.

48. Chao Chen, Zhichao Tan, Michiel A. P. Pertijs, "A 1V 14b Self-Timed Zero-Crossing-Based Incremental ΣΔ ADC", in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 274-275, Feb. 2013.

CHAPTER 3

AN 8 CHANNEL 14-BIT 33.6V H.V TIME-INTERLEAVED EXTENDED COUNTING ADC FOR BATTERY MONITORING

This chapter describes a $14-bit$ $33.6V$ high voltage drain extended time-interleaved extended counting ADC for monitoring the voltage of a stack of 8 Li-Ion batteries. This work has done in collaboration of my colleague Dante Gabriel Muratore as well as support from AMS Italy. The maximum nominal input voltage of the A/D converter with extended-range is equal to $33.6V$ and the converted voltage range for each battery is within $3-4.2V$ range. The architecture is consist of two section, a high-voltage track $\&$ hold interface which included high-voltage switches and a single high-voltage sampling capacitor and a low-voltage part which operates at a nominal $5V$ and included an 8-channel interleaved incremental extended counting ADC as coarse conversion and a single SAR ADC for the fine conversion, which convert all the channels in 720 μs. The chip has been prototyped in a 0.35-μm triple-well $5V$ H.V CMOS process with drain extended MOS high-voltage devices. Its active area is $1300 \times 650 \mu m^2$ and the measured total power consumption is $3.64mW$. The measured input referred noise and residual offset are 177.9 μV and 642.5 μV, respectively. The IC has a $0.2mV$ resolution and the achieved FoM_s is 129.5 dB.

3.1 Introduction

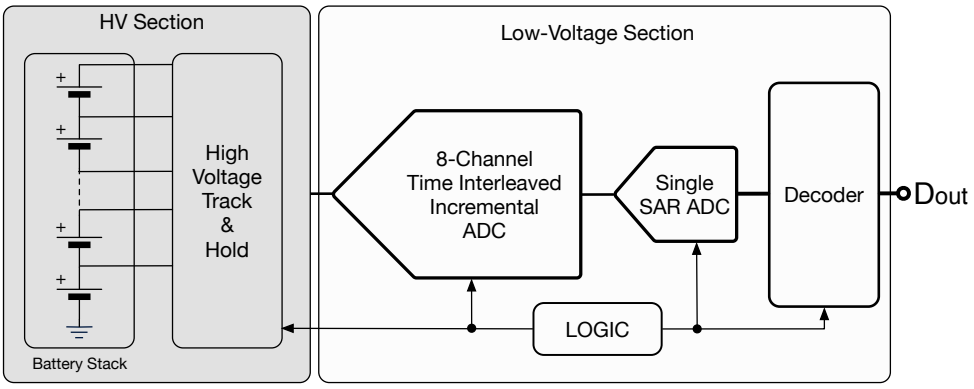
Intelligent monitoring, charging and protection of the electric vehicles' (EV) rechargeable Li-Ion batteries are critical aspects of the system to ensure efficiency and safety [1]. The management of Li-Ion batteries used in EVs also required to measure the voltage across each cell battery almost

simultaneous, ex. $1ms$ with an accuracy bellow $1mv$. Simultaneous measurement of the cell voltage, along with the battery discharge current is critical to accurately measure battery impedance and predict battery capacity. Most IC technologies are not able to interface directly to the complete cell stack because of the high voltage. This creates a significant challenge in designing a robust and cost-effective battery management system (BMS). While previous works [2]-[6] present ICs and BMS for use in EVs, they require external components for the device-to-device communication interface, consume large quiescent current and lack active cell balancing [7]. Having multiple high-voltage section grows the silicon area; moreover, sampling the inputs sequentially is not optimal since a common request is to provide the A/D result almost simultaneous sample, this requirement comes from the high dynamic load change seen by the batteries and from the necessity to measure all the cell voltage under the same condition.

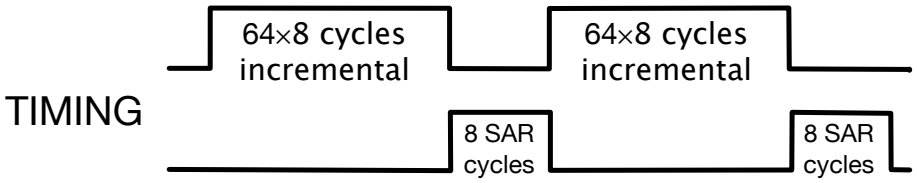
This design could monitor up to a stack of 8 batteries, with a relatively simple and innovative high-voltage section. The time-interleaved structure of this work obtains an almost-simultaneous sampling of the battery cells.

The solution in [8] uses a parallel approach with multiple level shifters and multiple ADCs. Although this provides a simultaneous conversion, inter-channel mismatch becomes a major limitation to the achievable resolution in this kind of architectures, while using a single fine converter in our design limits the mismatch between channels.

Fig. 3.1 shown the battery monitor architecture and its simplified timing diagram; This design employs the 8-channel extended counting ADCs in a time-interleaving manner, [9, 10], made by a 6-bit frist order incremental converter and a single 8-bit SAR ADC.



(a)



(b)

Figure 3.1 (a) Battery monitor architecture , and (b) its simplified timing diagram.

The track & hold uses a single high-voltage capacitor and 8 high-voltage innovative sampling switches of the each battery cell voltage. The architecture shares the comparator and $1-bit$ DAC in both coarse and fine step, thus a hardware-sharing has been performed to improve the energy efficiency, as well as using a single SAR ADC for all the 8-channels, avoid any possible mismatch.
The ADC dynamic range is set based on the Li-Ion battery charge-discharge profile [11], Fig. 3.2 shown a typical battery discharge profile, which resulting in a conversion range from 3 to 4.2 V. This IC has fabricated in a 0.35-μm triple-well $5V$ H.V CMOS process with drain extended MOS

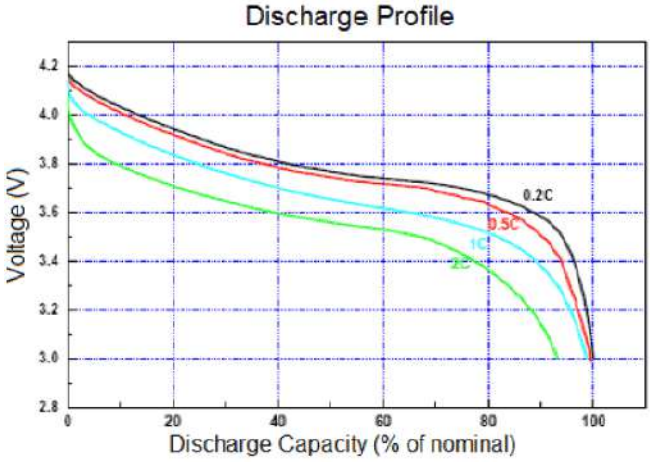
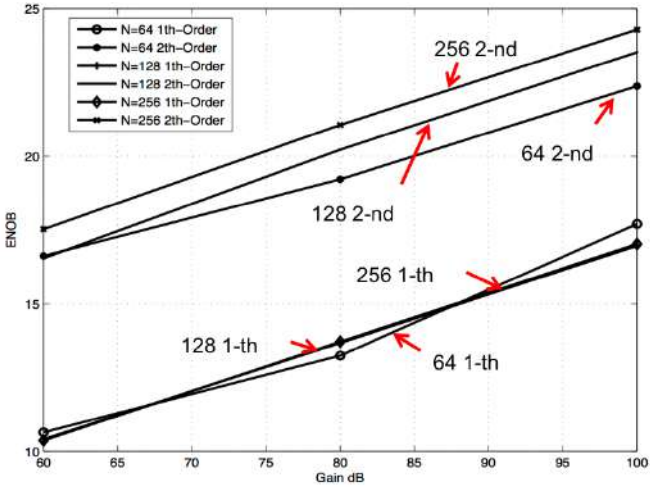


Figure 3.2 Typical battery discharge profile [11].

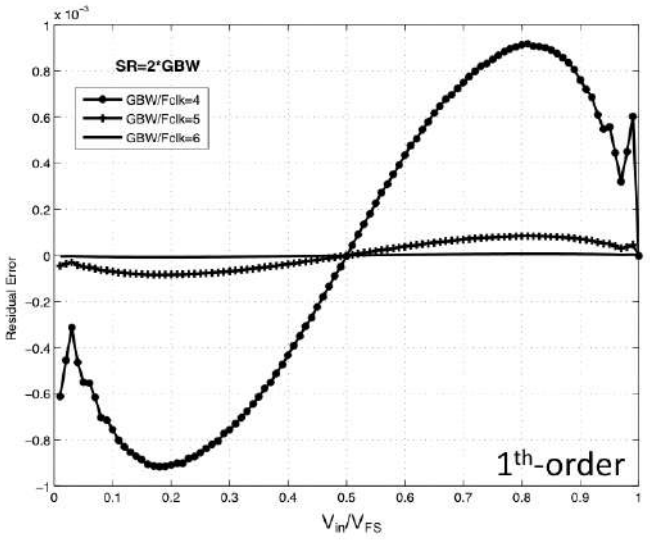
high-voltage devices. The prototype active area is $1300 \times 650 \mu m^2$. The master clock frequency and the measured total power consumption are $1MHz$ and 3.64 mW, respectively. The measured input referred noise is 177.9 μV and The residual offset is 642.5 μV.

3.2 Proposed Architecture

An 8-channel time-interleaved first-order incremental ADC with an oversampling ratio (OSR) equal to 64, operate as a coarse conversion, resulting resolution equal to $6-bit$. Each incremental step require 10 clock cycles (1 for global reset, 1 for a dummy channel, and 8 for all the sampling channels), resulting in 640 clock cycles for the coarse stage. To improve the resolution of the ADC an extend counting technique has been used, once the coarse step is completed, the incremental converter circuit is re-arranged as a SAR ADC for the residual voltage conversion, fine step. The fine conversion is carried out in 10 clock cycles for each of 8-channel, resulting in 80 clock cycles for whole fine step. Thus totally, 720 clock cycles are required for measuring the whole battery stack. By considering the $f_{CLK} = 1MHz$, the sampling rate of the overall ADC would be equal to $11.1KS/s$ ($1.39KS/s$ for each channel). A two-stage op-amp with high DC gain and adequate bandwidth has been implemented, in order to achieve the $14-bit$ resolution for the entire ADC. Simulation level results, Fig. 3.3, show that a DC gain of 115 dB and a bandwidth of 20MHz obtained by a chopper stabilized two-stage amplifier (with a cascade as first stage) match the requirement. The comparator is a dynamic latch [25] with a single stage preamplifier.



(a)



(b)

Figure 3.3 (a) Maximum achievable ENOB with an extended range incremental ADC versus op-amp DC gain (b) Residual errors caused by slew-rate and bandwidth for the 1^{th} order incremental ADC with a given op-amp DC gain equal to $100dB$.

3.2.1 8-channel Time-Interleaved Incremental ADC as Coarse Conversion Phase

The ADC architecture during the incremental phase has been shown in Fig. 3.4(a). A single high-voltage MIM capacitance, C_S, works as sampling element for all the 8-channels. A capacitor, C_{CM} which is nominally equal to C_S and implemented as high-voltage, provide a shift voltage equal to $V_{CM,B} = 3.6V$, so that a reference voltage of $\pm 0.6V$ makes the conversion range from 3 to $4.2V$.

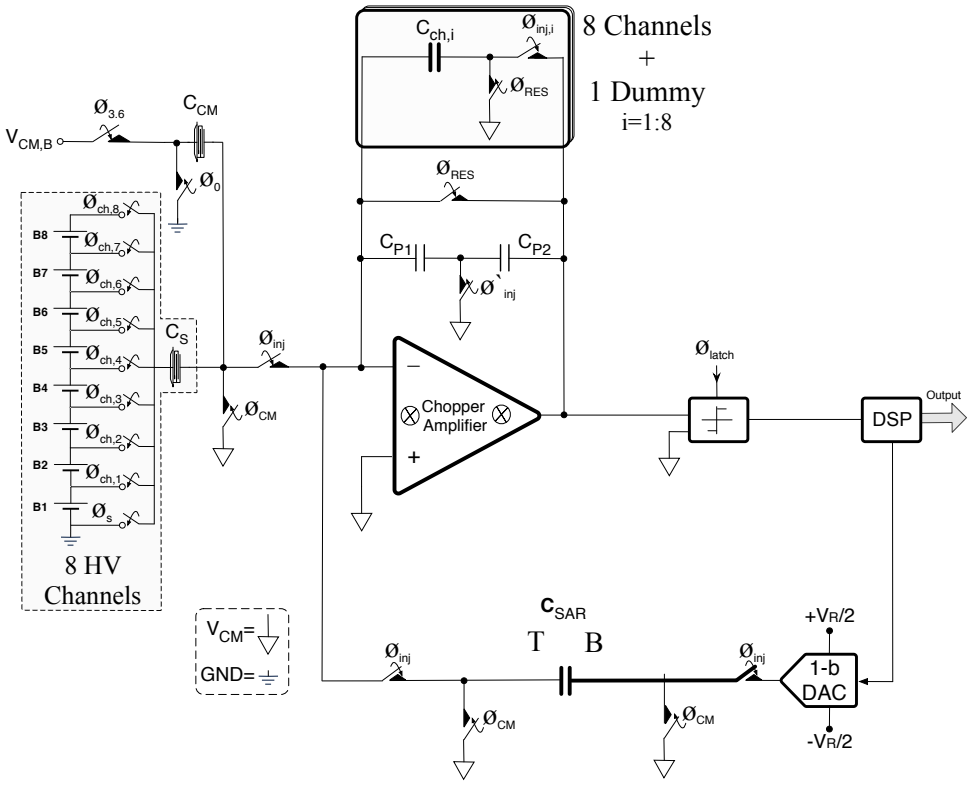
Eight nominally equal capacitors connected in feedback, $C_{ch,i}$, accumulate the charges in a time-interleaved fashion, and the capacitive array bank, C_{SAR}, made by a combined 5b-binary and 3b-C2C structure (Fig. 3.7(a)), performs the function required by the $\Sigma\Delta$ incremental operation as an injection element.
The left plate of C_S top-up by one cell at each cycle and injects into the virtual ground, together with C_{CM} and C_{SAR}, thus the total charge injected is equal to:

$$Q_{inj,in} = C_s V_{B,i} - C_{CM} V_{CM,B} + C_{SAR} \frac{V_R}{2}(2k_i - 1). \tag{3.1}$$

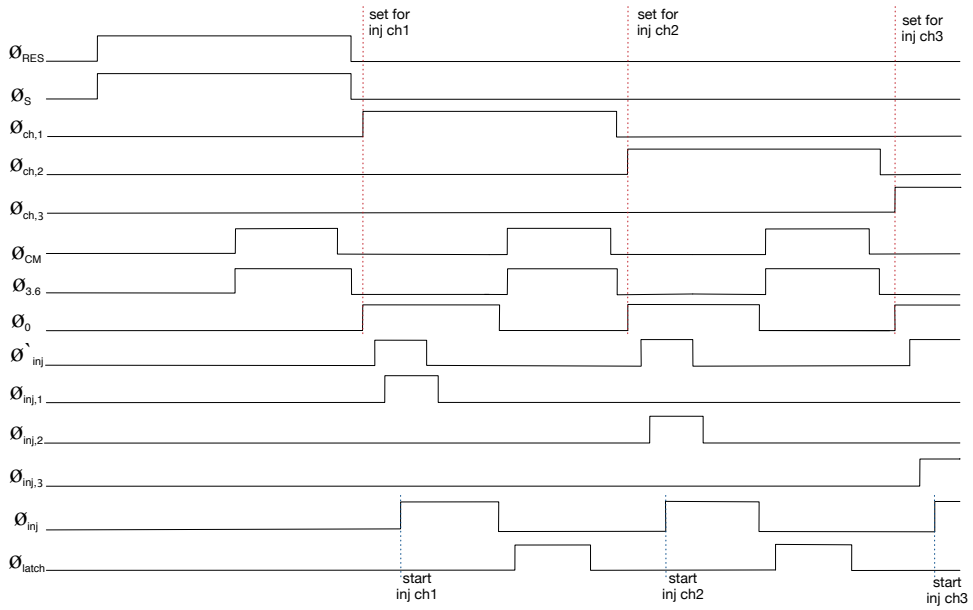
where k_i is the output of the comparator at each cycle, $V_R = 1.2V$ the reference voltage, and $V_{B,i}$ the battery cell voltage.
C_{CM} is implemented as high-voltage capacitor in order to be nominally equal to C_S, and C_{SAR} is designed to achieve a gain of incremental stage equal to one. By adjusting the value of V_R any possible gain error is compensated.
Time-interleaved architectures which share the operational amplifier could suffer from crosstalk issue between the parallel channels. In addition, it is needed to maintain the charge exactitude at the summing node, which is the input node of the op-amp. Injecting some charge related to an off-channel during the active phase of another channel, would result in a crosstalk issue. This typically happened due to charge injection of the sampling switch which are open. Our proposed architecture is tolerated to crosstalk issue, cause there is only one single injecting element, C_S, as well as an "set and then inject" approach has used. The Fig. 3.4(b) shows the phasing digram of incremental step which has been done by a complex logic, the left plate of the injecting capacitor, C_S, is always connected to the analog ground voltage, and whenever there is a switching activity on this side, the injecting switch on the right side is kept open. It means that in Fig. 3.4(b), whenever the track&hold phases $\phi_{ch,i}$ are changing, ϕ_{inj} has logic 0 value and ϕ_{cm} binds the summing node to the V_{CM} (common-mode voltage), to avoid any possible crosstalk between channels.
There is a global reset before each conversion, thus all the feedback capacitors, $C_{ch,i}$, are discharged to virtual ground. To prevent a clock feedthrough mismatch on the first battery voltage measurement, V_{B1}, a dummy channel has been implemented to absorb the charge injected by the feedback reset switch when it is opening. Two capacitors C_{p1} and C_{p2}, Fig. 3.4(a), has been implemented to avoid the open loop connection by providing a feedback path to the op-amp when there is no channel capacitor, $C_{ch,i}$, in operation. The summation value of $C_{p1} = 900fF$ and $C_{p2} = 100fF$ in feedback path is equal to $90fF$.
After a full incremental cycles ($N_{inc} = 64$), the residual charge stored into each feedback capacitor, $C_{ch,i}$, is:

$$Q_{RES,i} = \sum_{i=1}^{N_{inc}} C_{SAR} \frac{V_R}{2}(2k_i - 1) - N_{inc}(C_S V_{B,i} - C_{CM} V_{CM,B}). \tag{3.2}$$

Since the signal is accumulated 64 times and the noise is quadratically superposed 64 times, the incremental phase attenuates the KT/C noise request by $\sqrt{64} = 8$ [27].
Other proposed solutions, [2]-[4], use a low-pass filter in front of ADC, which is typically implemented with external component and results into a filter pole in the range of $[0.1 - 10]KHz$. Our proposed design, the 64 times sampling of the battery voltage introduces a low-pass FIR filter with 64 taps. Thus relaxing the requirement to use external components and then reduces the cost.
The use of chopping technique in the op-amp [14]-[17], significantly reduces the input referred offset. The charge injection mismatch caused by the opening of the switches connected to virtual ground, is the main source of the residual offset. The op-amp and its layout has been designed in a way that it maintains the error always below $1/2$ LSB and thus no extra calibration is required.



(a)



(b)

Figure 3.4 (a) Circuit schematic of battery monitor during incremental conversion (b) Timing diagram of phases for first 3-channel during incremental conversion.

3.2.2 8-bit SAR ADC as Fine Conversion Phase

At the end of the coarse step the residual charges have been stored on the feedback capacitor, $C_{ch,i}$, the 64×8 incremental cycles give a $6 - bit$ resolution for each channel. To extend the total resolution of the entire A/D converter, the architecture is re-arranged into a form of SAR ADC. Fig. 3.5 shows the circuit schematic of battery monitor during SAR phase.

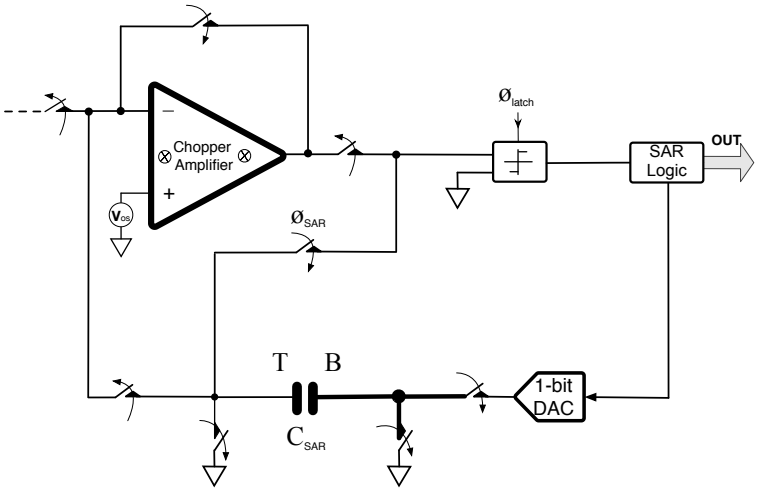


Figure 3.5 Circuit schematic of battery monitor during SAR conversion.

To perform SAR algorithm to generate the $LSBs$, it is necessary to transform the residual voltage from $C_{ch,i}$ capacitors into C_{SAR}. This operation has been done in two step. To compensate the offset of op-amp as a source of error in the time-interleaved incremental ADC phase, a chopping technique has used in the incremental A/D conversion phase, however, in this case since the operation is single, the chopping technique is not effective during the charge transfer from the feedback channel capacitor, $C_{ch,i}$, to the capacitive bank array, C_{SAR}. Instead, an auto-zero technique is used. Fig. 3.6(a) shows the transfer of the residual voltage from the $C_{ch,i}$ capacitors to C_{SAR}, the C_{SAR} array is reset to the offset of the op-amp in an auto-zero fashion [18], resulting:

$$Q_{C_{SAR}} = V_{OS} C_{SAR}. \tag{3.3}$$

$$Q_{C_{ch,i}} = Q_{RES,i}. \tag{3.4}$$

Then in second step, Fig. 3.6(b), the C_{SAR} is connected in feedback and the residual charge in $C_{ch,i}$ is injected into it. In this way, the residual charges are sequentially transferred to C_{SAR} in order to perform the SAR conversion cycles. The final charge in the C_{SAR} would be:

$$Q_{C_{SAR}} = Q_{RES,i} + V_{OS} C_{SAR} - V_{OS} C_{ch,i}. \tag{3.5}$$

The error in the charge transfer to C_{SAR}, due to the offset, in this phase, depends on the mismatch between $C_{ch,i}$ and C_{SAR} capacitors, which has been calculate as:

$$V_{err} = V_{OS} \frac{(C_{SAR} - C_{ch,i})}{C_{SAR}}. \tag{3.6}$$

To mitigate this error, the best option would be to choose capacitor C_{SAR}, large enough, to ensure V_{err} is negligible. Using always the same capacitive bank array, C_{SAR}, for the fine conversion, relax the mismatch requirements to the feedback channel capacitors, $C_{ch,i}$ as well.

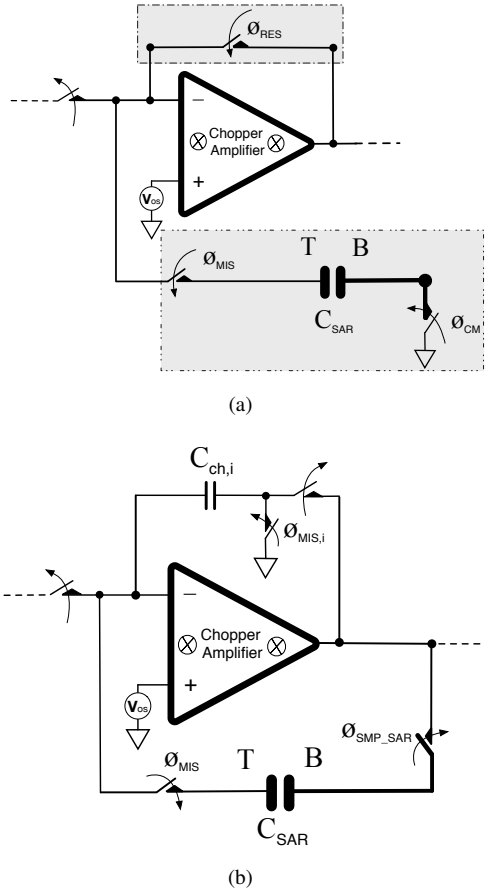


Figure 3.6 Mismatch cancellation technique during charge transfer to C_{SAR} (a) Auto-zero step (b) Charge transfer from feedback-channel capacitors, $C_{ch,i}$, to C_{SAR} capacitive bank array.

The SAR A/D converter uses the same comparator of the incremental phase converter as well as the 1-bit DAC switches to control the bottom plates of the C_{SAR} capacitive bank array. Since both incremental and SAR steps use C_{SAR} capacitive bank array for balancing the input, there is no mismatch between the two phases. Moreover, input sampling and voltage shift also use the same type of high-voltage capacitors. A minor issue can rise from the mismatch between the feedback channel capacitors, $C_{ch,i}$, which generate the voltage driving the comparator during the incremental phase. Since the mismatch changes the amplitude but not the sign, the possible error is in the dynamic output of the op-amp. To avoiding harmonic distortion it needs to keep the op-amp operation in the linear region.

3.3 Circuit and Layout Blocks Design and Implementation

In this section, the circuital design of the main blocks of the A/D converter are described. It consists of a track&hold circuit block, DAC array, operational amplifier and a voltage comparator. Also a complex logic circuit has been implemented to generating the control signals (Fig. 3.4(b)).

3.3.1 C_{SAR} DAC Array & $C_{ch,i}$ Feedback-Channel Capacitors

The relaxed accuracy constrains of the fine conversion step allow using a DAC array, C_{SAR}, made by a combined 5-bits Binary-weighted fashion and 3-bits C-2C structure, as shown in Fig. 3.7(a).

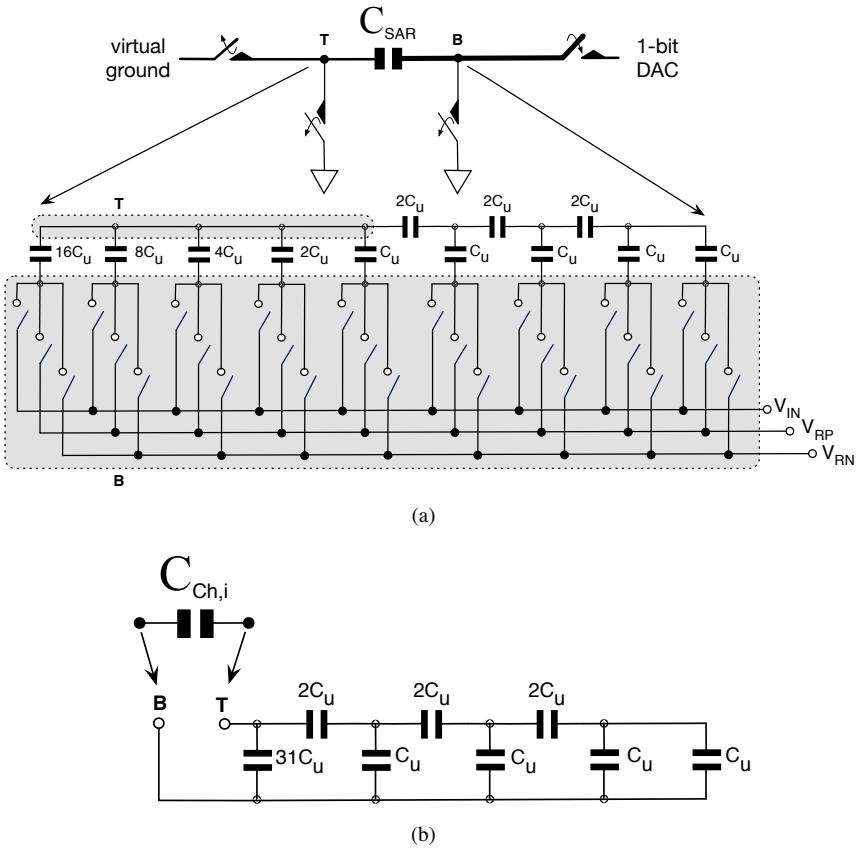


Figure 3.7 (a) C_{SAR} array circuit schematic during SAR A/D conversion phase, $5-bits$ are implemented as a binary weighted element and $3-bits$ use a $C-2C$ structure (b) Circuit implementation scheme of feedback channel capacitor, $C_{ch,i}$.

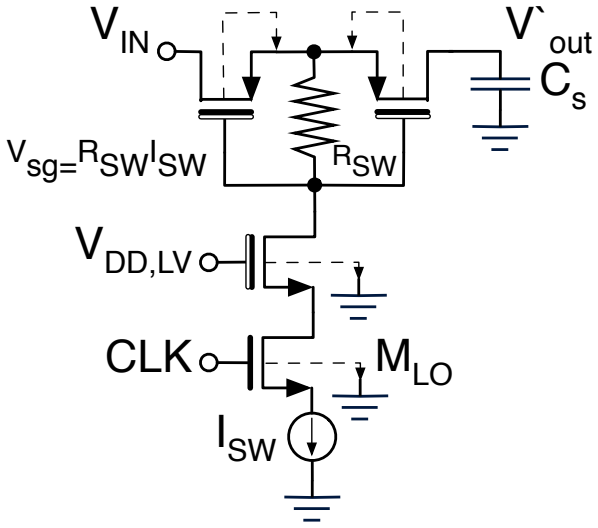
The array is composed by 41 poly unity capacitors $C_u = 40fF$, resulting in a total capacitance of $C_{TOT} = 1.64pF$. The capacitor C_{SAR} is a special unit, in the incremental phase it operates as an injection element to realize sigma-delta incremental function and in the fine conversion phase it is used as basic block of the SAR ADC which is necessary for the extended counting technique. in this way

a hardware-sharing has been performed to improve the energy efficiency of the entire A/D converter. Fig. 3.7(b) shows the structure of feedback channel capacitors, $C_{ch,i}$, which has the equivalent value of C_{SAR} during the incremental phase. The capacitors $C_{ch,i}$ and C_{SAR} are designed to achieve a gain of incremental stage equal to 1.

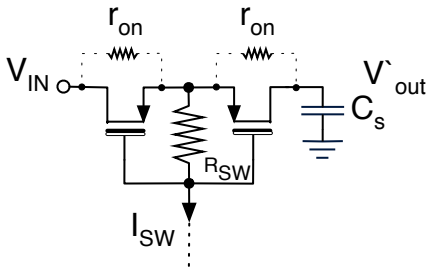
3.3.2 High Voltage Track&Hold Switch

A high-voltage bi-directional switch which is driven by a low-voltage logic control has been shown in Fig. 3.8(a). The scheme commonly used in high-voltage A/D converter front-end. It consists of a back-to-back high-voltage drain extended $pMOS$ [19] configuration which avoids diode forward biasing when the biasing of the switch reverses and a high-voltage drain extended $nMOS$ transistor [19] which its gate has been tied to $V_{DD,LV} = 5V$ to ensure that the drain nod of Low-voltage transistor (M_{LO}) does not exceed ($V_{DD,LV}$-V_{th}) voltage.

A low-voltage clock signal CLK, is used to turn on the high-voltage switch. When the clock signal



(a)



(b)

Figure 3.8 (a) Schematic view of standard high-voltage track&hold switch (b) offset due to non-liner r_{on}.

is high, the current I_{SW} through the resistor R_{SW} generates the proper V_{gs} to turn on the transistors.

The conventional standard solution is appropriate to use for low accuracy or logic signals, however, for precise and high accuracy applications the solution is unsuitable, as the sampled voltage has been affected by a non-liner offset in this approach. Fig. 3.8(b) shown the equivalent on-resistance (r_{on}) of the standard H.V switch, flowing of the current I_{SW} though R_{SW}, used to turn on the transistors, also leaking through one of the two back-to-back pMOS transistors and causes a non-linear drop ΔV that generates an offset affecting the sampled voltage. The $R_{SW} \times I_{SW}$ gives the value of V_{gs}, on-condition of the switch. The choice of the V_{gs}, the R_{SW} and the speed of the switch would determine the minimum non-linear r_{on}. In fact, the size of transistors have a maximum limit, since their gate capacitance and the value of R_{SW} give rise to a time constant ($\tau_{R_{SW}C_G}$) that might limit the speed operation of the switch. By using the lower values of R_{SW} it is possible to reduce the $\tau_{R_{SW}C_G}$, however, it would increase I_{SW} and enlarge the generated offset. The speed of H.V switch operation critically affects the on-resistance of the switch. Transistor level simulation results, confirm that the offset which is cause by $I_{SW} \times r_{on}$, for a sampling frequency of $1MS/s$, is much bigger than the required LSB. Fig. 3.9 shows the transistor level simulation sampling error as a function of input voltage for the conventional H.V switch (Fig. 3.8(a)).

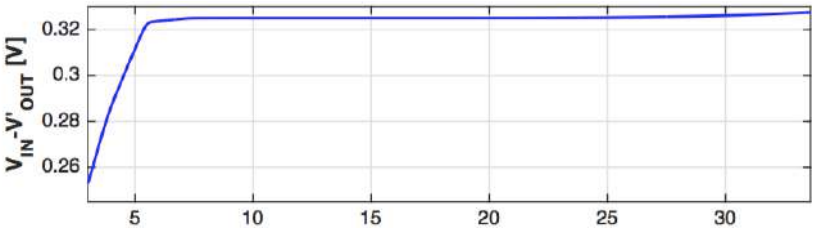


Figure 3.9 Sampling error as a function of the input voltage for conventional H.V switch implementation (Fig. 3.8(a)).

The error is non linear and could be as large as $320mV$. In particular, for input voltage lower that 5V, the drop across the switch is lower since the low input voltage is pushing the current mirror implementing the current generator I_{SW} in the triode region, which decreasing the I_{SW} value.

Our proposed solution, shown in Fig. 3.10(a), solves the problem by using a matched dummy structure that generate the proper V_{gs}, in this way, no static current flows through the sampling switch and the required accuracy is achieved. The control voltage is then used to drive the actual switch. By choosing the sampling period T_S much larger than the time constants $\tau_{r_{on}C_S}$, the non-linearity of the on-resistance (r_{on}) would be ineffective. The proposed solution use an optimal power, speed and silicon area tradeoff, which leads to $I_{SW} = 80\mu A$, $R_{SW} = 50K\Omega$ and $W/L = 10/1\ \mu m/\mu m$. The high voltage sampling capacitor value is equal to $C_S = 1.6pF$ that gives an on-resistance $r_{on} \simeq 5K\Omega$ leading to a time constant as low as $\tau_{r_{on}C_S} = 8ns$.

Fig. 3.11 shows the transistor level simulation sampling error as a function of input voltage for the proposed solution (Fig. 3.10(a)), as evident it works very well. It shows an error that is a linear function of the input voltage and is just $1.5\mu V$ at the nominal full scale voltage $V_{IN} = 33.6V$.

The Fig. 3.10(b) shown the layout view of the proposed switch, the simple and innovative structure of the switch result in an area-per-switch equal to $0.006mm^2$, outstandingly smaller than the other solutions, [20, 22]. Besides that, the circuit implementation does not require high-voltage capacitors to perform.

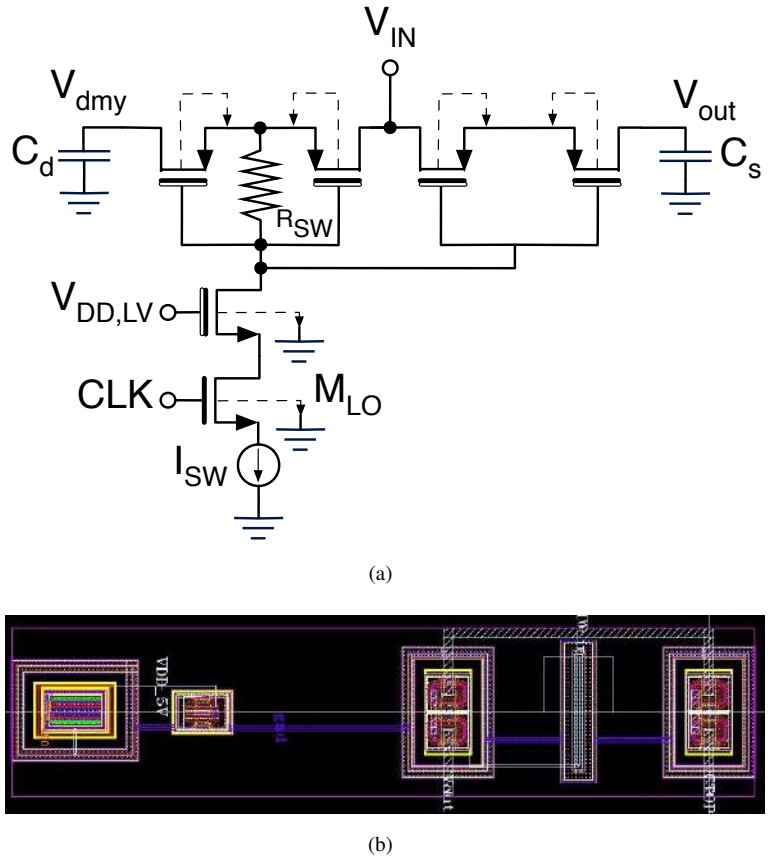


Figure 3.10 Proposed high-voltage track&hold switch with dummy structure (a) Schematic view (b) Layout view.

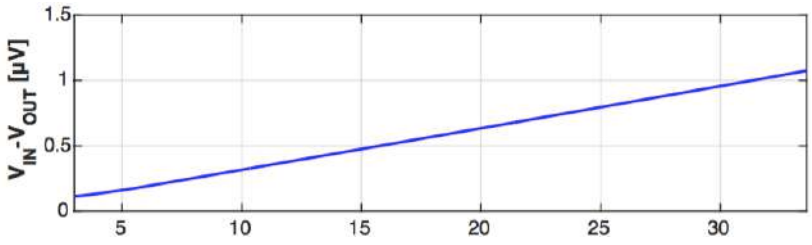
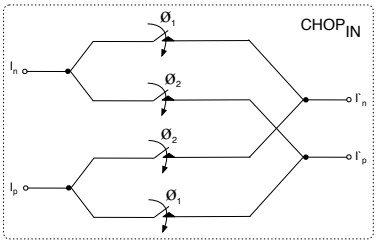


Figure 3.11 Sampling error as a function of the input voltage for proposed solution with dummy structure (Fig. 3.10(a)).

3.3.3 Operational Amplifier Implemented with Chopping Technique

The operational amplifier has designed to meet the requirement needed for the entire 14-bit ADC [27, 28]. The Fig. 3.12(b) shown the schematic of the designed op-amp with chopping technique, it is a two stage op-amp, a telescopic cascade as first stage and an inverter with active load as second stage.



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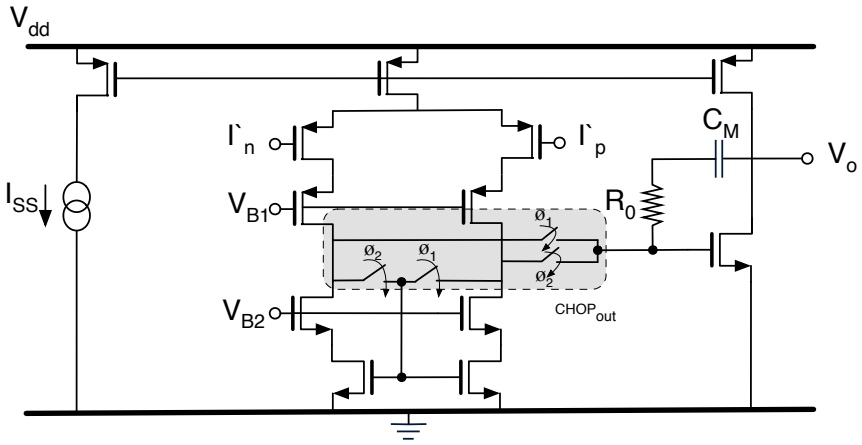

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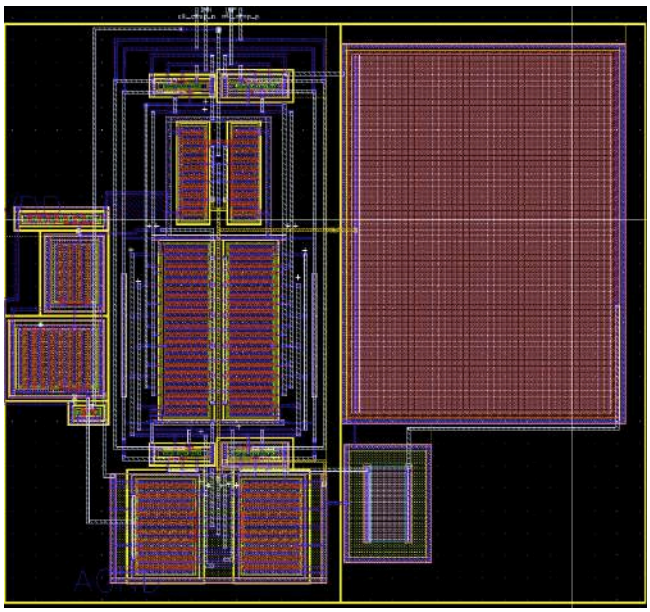


(c)

Figure 3.12 (a) Schematic view of the input chopping network of the operational amplifier (b) Schematic view of the operational amplifier included output chopping network (c) Layout view of the entire operational amplifier and chopping networks.

The operational amplifier is miller ($C_M = 4pF$) compensated with a *zero-nulling* resistance ($R_0 = 550\Omega$) which provide a phase margin of $65°$. It could drive a capacitive load as large as $2pF$. The first stage uses a high-compliance current mirror for increasing the voltage room for the input pair and the current generator. Its bias current is equal to $I_{SS} = 100\mu A$ and it achieves a DC gain of $120dB$ and a unity bandwidth of $20MHz$. The charge injected by capacitors, C_S, C_{CM}, C_{SAR}, provided by equation (3.1) does not consider the offset of the operational amplifier. When taking into account the offset of the op-amp, equation (3.1), turns into:

$$Q_{inj,in} = C_S\left(V_{B,i} - V_{OS}\right) + C_{CM}\left(-V_{CM,B} - V_{OS}\right) + C_{SAR}\left(\tfrac{V_R}{2}(2K_i - 1) - V_{os}\right). \tag{3.7}$$

Where V_{OS} is the offset of the op-amp. for calculation simplicity, assuming that all the injecting capacitors, C_S, C_{CM}, C_{SAR}, are equal and named C_{inj} (in fact they are nominally equal by the value), then equation (3.7) becomes:

$$Q_{inj,in} = C_{inj}\left(V_{B,i} - V_{CM,B} + \tfrac{V_R}{2}(2K_i - 1) - 3V_{OS}\right). \tag{3.8}$$

Eventually, the residual charge at the end of the incremental phase for each channel would be equal to:

$$Q_{RES,i} = C_{inj}\left(\sum_{i=1}^{N_{inc}} \tfrac{V_R}{2}(2K_i - 1) - N_{inc}(V_{B,i} - V_{CM,B}) - 3N_{inc}V_{OS}\right). \tag{3.9}$$

The equation (3.9) shows an error due to offset injection at each clock cycle. The residual voltage is derived from the residual charge, by simply dividing it by the channel feedback (integrator) capacitor, $C_{ch,i}$, for simplifying the calculation, again considering it equal to C_{inj} for all the 8-channel, resulting in a residual voltage equal to:

$$V_{RES,i} = \sum_{i=1}^{N_{inc}} \tfrac{V_R}{2}(2K_i - 1) - N_{inc}(V_{B,i} - V_{CM,B}) - 3N_{inc}V_{OS}. \tag{3.10}$$

The equation (3.10) shows an error due to offset which is much larger than the LSB. Typically, the auto-zero or chopping techniques [23, 24, 25] is used for the cancellation of the offset and the flicker noise. The proposed op-amp design uses a chopped operational amplifier to mitigate this issue.

The chopper technique transposes the input signal to high frequency by modulation, as done by the multiplier M_1 of Fig. 3.13(a), and then demodulates it back to the baseband with the multiplier M_2 after amplification. The modulating signal is a square-wave signal, $m(t)$, with period $T = \frac{1}{f_{chop}}$. After the first modulation, offset and $1/f$ noise (V_{OS} and V_n, respectively) corrupt the signal, but they are transposed to high frequency by the action of M_2. Fig. 3.13(b)-(d) depicts the spectra of the signal involved in the relevant points of the processing chain. The $1/f$ frequency noise added to input of A_1, modulated by M_2 and replicated at multiple of f_{chop}, is possibly lowpass filtered by the finite bandwidth of A_1 [23].
The M_1 and M_2 multiplier are implemented in the op-amp architecture by the input chopping network, $CHOP_{IN}$, as shown in Fig. 3.12(a) and output chopping network, $CHOP_{OUT}$, in Fig. 3.12(b).
Anyhow, due to mismatch issue in IC fabrication process, still there is a residual offset ($V_{os,res}$) at the end of incremental phase conversion even with the use of chopping technique, The $V_{os,res}$ affects the residual voltage equation (3.10) in the equal way as the original offset (V_{OS}), resulting equation (3.10) turns into:

$$V_{RES,i} = \sum_{i=1}^{N_{inc}} \tfrac{V_R}{2}(2K_i - 1) - N_{inc}(V_{B,i} - V_{CM,B}) - 3N_{inc}V_{os,res}. \tag{3.11}$$

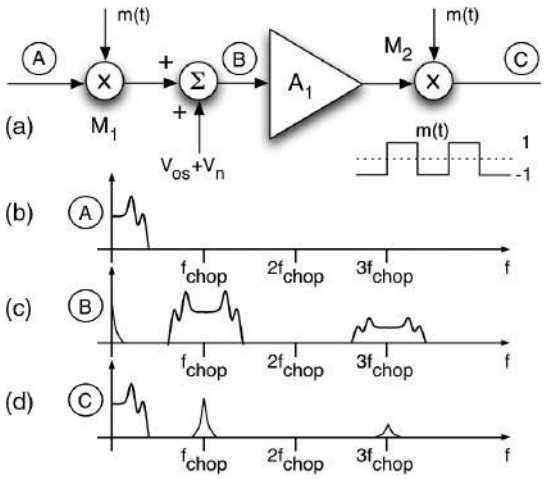


Figure 3.13 Chopper technique basic sheme [23].

The input voltage could be retrieved from equation (3.11) as:

$$(V_{B,i} - V_{CM,B}) = \left[\frac{\sum_{i=1}^{N_{inc}}(2K_i - 1)}{2N_{inc}}\right] V_R - \frac{V_{\mathrm{R}ES,i}}{N_{inc}} - 3V_{os,res}. \tag{3.12}$$

Where the first part is the digital representation of the input signal, the second part the quantization error, and the last part the final offset error. Thus, the final residual offset ($V_{os,res}$) has to give an error that is negligible to compare with the LSB of the SAR stage as the extended range fine converter. Therefore, the $V_{os,res}$ required to be lower that:

$$V_{os,res} < \frac{V_R}{3 \times 2^{N_{SAR}}}. \tag{3.13}$$

With $V_R = 1.2V$ and $N_{SAR} = 8bits$, the $V_{os,res}$ should not be higher that $1.5mV$. The request are not so difficult to satisfy with the use of chopping technique.

3.3.4 Voltage Comparator

The schematic view of the implemented voltage comparator is shown in Fig. 3.14, it composed of a single-ended stage with active load preamplifier for improving the kickback noise [13] performances and a conventional dynamic sense-amplifier based latch [25].

In dynamic latched comparators, the current only flows during the regeneration. When $CLOCK$ is low (*reset phase*), the transistors M_{4a}/M_{4b} and M_{5a}/M_{5b} reset the output nodes and the drains of the differential pair (M_{1a}/M_{1b}) to V_{DD}. M_6 is OFF and no supply current exists. When $CLOCK$ goes high, the reset transistors are switched OFF; the current starts flowing in M_6 and in the differential pair. Depending on the input voltage, one of the cross-coupled inverters that make the regeneration, (M_{2a}/M_{3a}) or (M_{2b}/M_{3b}) , receives more current, determining the final output state. After regeneration is completed, one of the output nodes is at V_{DD}; the other output and both drains of the differential pair have a 0-V potential. There is, in this situation, no supply current, which maximizes power efficiency. The nodes where the drains of (M_{1a}/M_{1b}) connect have rail-to-rail excursion, originating a large kickback noise. There is, in this type of comparators, another kickback

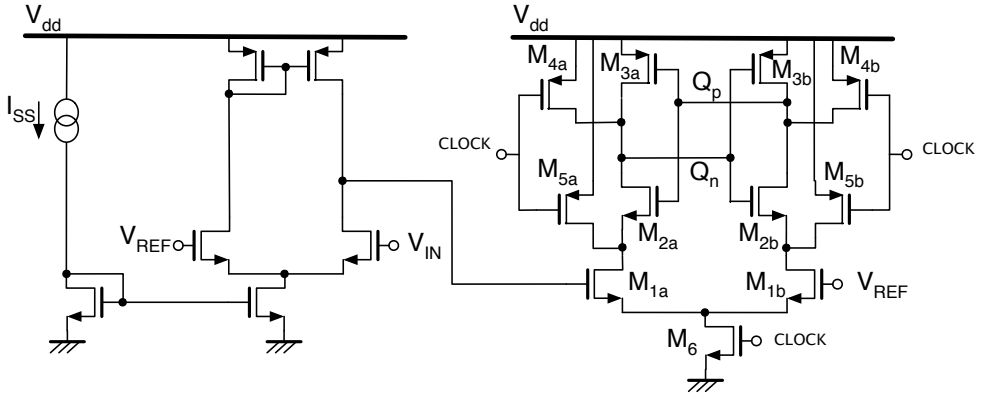


Figure 3.14 Schematic view of the voltage comparator.

noise source: the variation of the operating region of the differential pair transistors. In the *reset phase* there is no current flowing, and (M_{1a}/M_{1b}) are in cutoff. In the beginning of the *regeneration* phase, the current starts flowing in (M_{1a}/M_{1b}), and their V_{DS} is large; these transistors are, therefore, in saturation. When the voltages at their drains approach 0 they will enter the triode region. These operating region changes are accompanied by variations in their gate charges, thereby causing input voltage variations. To mitigate the kickback noise a per-amplifier before the latch has been used. A biasing current equal to $25\mu A$ ensures a bandwidth large enough to accommodate the $1MHz$ clock operation.

3.4 Measurement Results

Fig. 3.15 shown the battery monitor IC layout view. This ADC has been fabricated in a $0.35 - \mu m$ triple-well $5V$ HV CMOS process with drain extended MOS high-voltage devices. The microphotograph of the prototype has shown in Fig. 3.16, its active area is $1300 \times 650\mu m^2$.

The nominal supply voltage of the chip is $5V$ and the main circuit blocks of active area has been magnified and highlighted in the Fig. 3.16, the high voltage section is formed by a high voltage battery common-mode injecting capacitor, C_{CM}, and a high voltage sampling capacitor, C_S with a well matched layout and the high voltage track&hold switches. The low voltage analog section is consist of the op-amp, the voltage comparator, and the (8-channel feedback, 1 dummy channel, 1 SAR/injection array bank) capacitors. The large area occupied by the high-voltage front-end is due to comply with the minimum ESD distance rules of the used technology. Finally, the low-voltage digital logic section that provides all the control signals to the entire system. Fig. 3.17 shows the testing board that was implemented for the measurement setup. The high-voltage section provides the input signals to the battery monitor IC, and the low-voltage section generates all the reference voltages (V_{RP}, V_{RN}, V_{CM} and $V_{CM,B}$) and the supply voltages (AV_{DD} and DV_{DD}) for the ADC chip.

The measurement has done by my collage Dante in the MIT laboratory, the digital output was collected by use of a logic analyzer and the data was processed in Matlab software. To measure the input referred noise and residual offset, 300 repeated measurement has done on channel 1, with the input value equal to V_{CM}, which is the half scale of the converter. The Fig. 3.18 shows the histogram

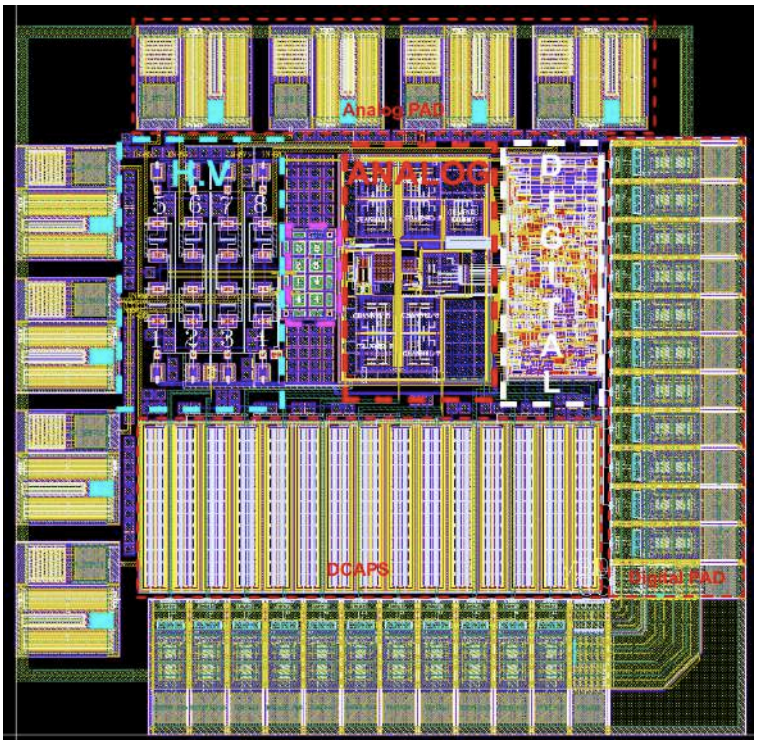


Figure 3.15 Layout view of battery monitor IC.

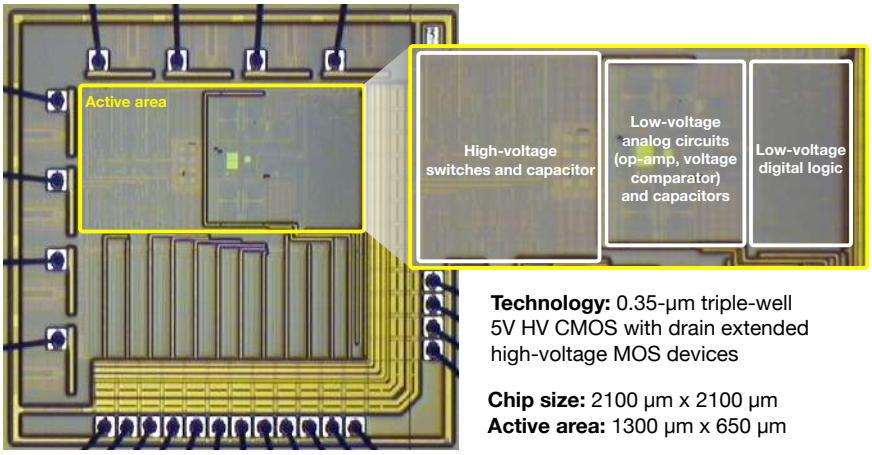


Figure 3.16 Battery monitoring chip microphotograph included magnified view of active area.

result. The mean value of the results give the residual offset equal to $642.5\mu V$ and their variance provide the input referred noise equal to $177.9\mu V$.

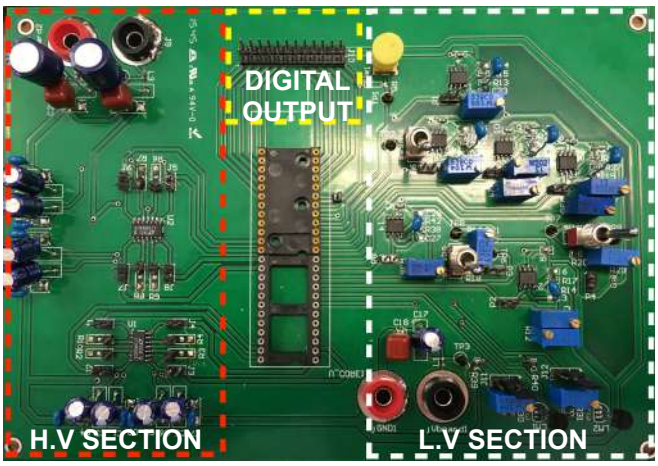


Figure 3.17 Battery monitor IC testing board.

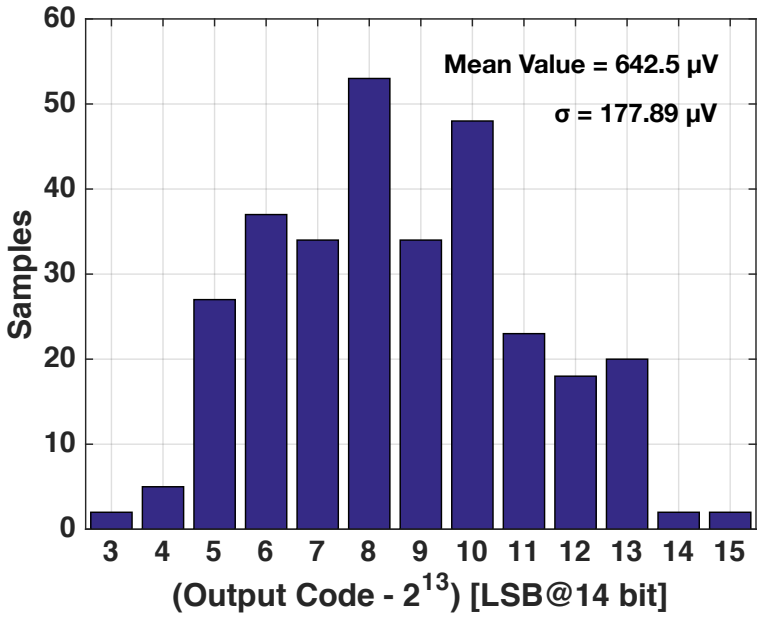


Figure 3.18 Histogram of 300 repeated measures with V_{in}=V_{CM}.

The measured output spectrum with a full scale input sine wave ($V_p = 0.6V$) at $f_{in} = 2.78Hz$, $f_{CLK} = 1MHz$ and 2^{18} FFT points, applied on channel 8, has shown in the Fig. 3.19. The SNDR is 76.7dB which result in an ENOB equal to 12.45 bit. The harmonic tones amplitude is very low and limits the SFDR at -96dB_{FS}.

The measured INL, Fig. 3.20, resulting from the histogram of a full scale input sine wave on channel 4, is in the $[-2, 0.5]\,LSB$ range. The endpoint fit line INL shows a good linearity of the high-voltage

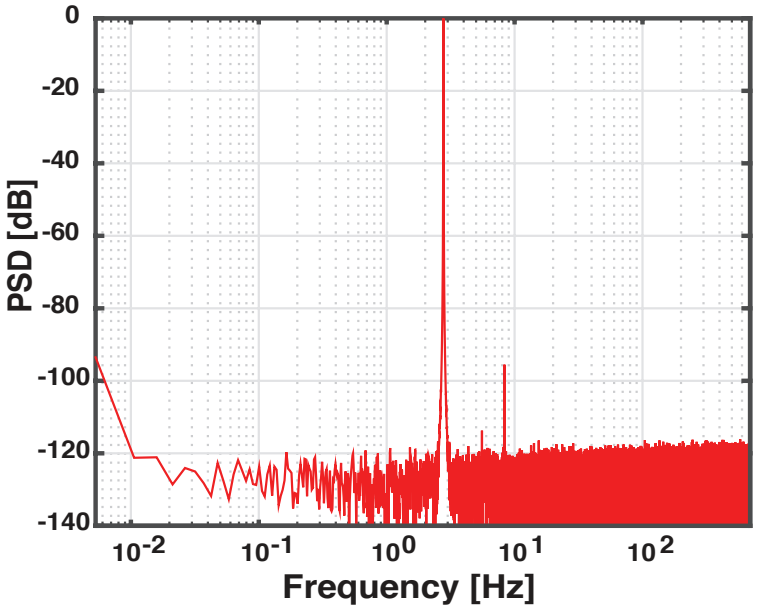


Figure 3.19 Measured output spectrum @FS $f_{in} = 2.78Hz$, $f_{CLK} = 1MHz$, 2^{18} FFT points.

capacitor C_S in the $\pm 0.6V$ range. Similar both static and dynamic results have been collected from all the channels. The linearity over the full 33.6V range depends on the voltage coefficients of the high-voltage capacitors, $C_s(V) = C_S(0)(1 + \alpha V)$. Fig. 3.21, shows the nonlinearity error of the measured outputs (average of 100 measurements) when the same input ($V_{B,i} = 3.6V$) is applied to all the channels. The result is the difference with respect to the first channel output and is expressed in LSBs ($14 - bit$). The error is almost the same for all the available chips and can be corrected in the digital domain.

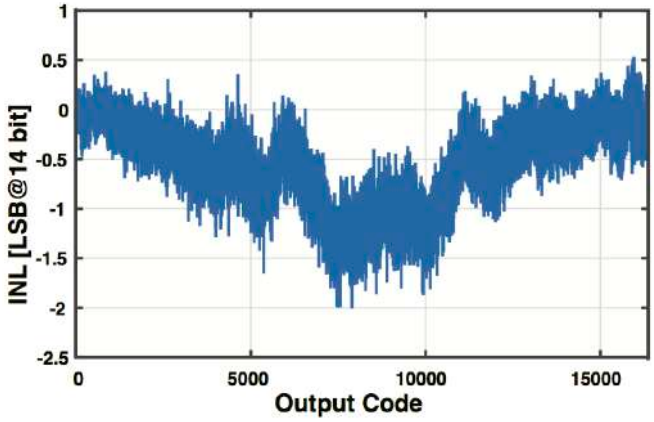


Figure 3.20 Measured INL resulting from the histogram of a $FS_{sinwave}$ on channel 4.

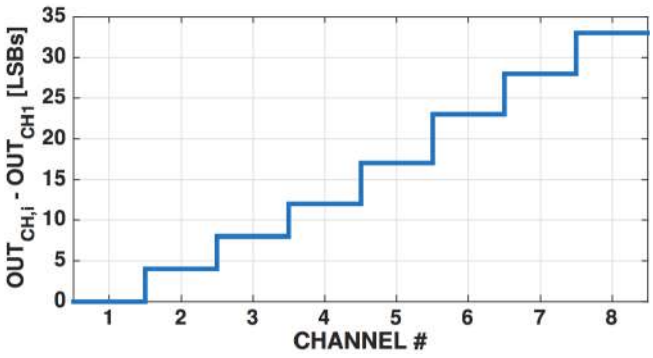


Figure 3.21 Measured output (average of 100 measurements) of the battery monitor IC when the same input ($V_{B,i} = 3.6V$) is applied to all the channels.

The entire system power breakdown with the main clock frequency equal to $f_{CLOCK} = 1MHz$ has depicted in Fig. 3.22. As expected the digital logic has consumed almost 59% of the total power consumption. The total power consumption of the entire chip is equal to $3.64mW$.

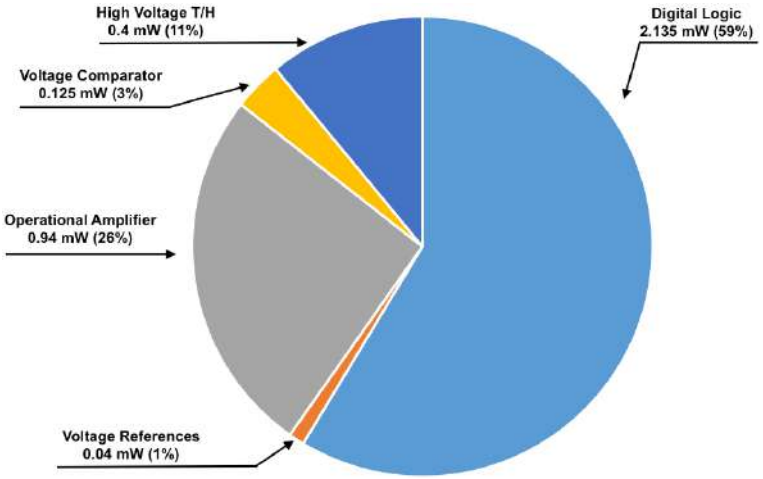


Figure 3.22 Measured battery monitor power breakdown.

The battery monitor performances has summarized in table 3.1 and a comparison with the state-of-art solutions has been provided. The comparison has performed by using the Schreier figure of merit, $FoM_s = SNR + 10LOG(BW/P)$, [26]. In this work, the measured SNR is $76.7dB$, the bandwidth is equal to $700Hz$ and the total power consumption is $3.64mW$. The parameters resulting in a FoM_S equal to $129.5dB$. The achieved results are competitive, considering that the works reported in [2] and [4] could measure only up to 6 cells. The IC in [8] implements a parallel solution that uses 6 transimpedance amplifiers (TA) as level shifters, and 6 $\Sigma\Delta$ ADCs. It is important to remark that design solutions in [8] increased the complexity of the circuit, that lead to an increase of the IC area

Table 3.1 Performance summary and comparison table.

	Proposed Design	Texas Ins. [2]	Linear Tec. [3]	Analog Dev. [4]	JSSC2014 [8]
Supply Voltage	$\mathbf{5V}$	$[7.2-27]V$	$[10-55]V$	$[8-30]V$	$5.2V$
Cell Input DR	$\mathbf{1.2V}$	$4.5V$	$5V$	$4V$	$2.5V$
Resolution	$\mathbf{214\mu V}$	$380\mu V$	$1.5mV$	$980\mu V$	$2.3mV$
ENOB	$\mathbf{12.45b}$	$13.5b$	$11.7b$	$12b$	$10.1b$
SNR	$\mathbf{76.7dB}$	$83dB$	$72.2dB$	$74dB$	$62.5dB$
Offset	$\mathbf{642.5\mu V}$	calibrated	$500\mu V$	$610\mu V$	–
Measured Cells	**8**	6	8[a]	6	6
Bandwidth	$\mathbf{700Hz}$	$11.9KHz$	$55.5Hz$	$83.3KHz$	$200KHz$
Total Power Consumption	$\mathbf{3.64mW}$	$13.1mW$[b]	$10.7mW$[b]	$42.5mW$[b]	–
$\mathrm{FoM_S}$	$\mathbf{129.5dB}$	$142.6dB$	$109.4dB$	$136.9dB$	–

[a] Reduced to 8 for this comparison. [3] can measure up to 12 cells.
[b] Estimated power consumption - 25% of total power consumption.

and larger power consumption. In addition, the inter-channel matching becomes a major concern in parallel architectures.

3.5 Conclusions

This chapter, proposed a battery monitor system up to 8 Li-Ion battery cell stack. The architecture use an 8-channel time-interleaved incremental converter for coarse conversion and use a single SAR A/D converter to extended the entire ADC range, as fine converter. The use of the same ADC for all the channels in the fine phase relaxes the matching requirements in the time-interleaved structure. The design has a relatively simple and innovative high-voltage track&hold with LV logic control interface, achieving high linearity and accuracy while low cost. The battery monitor IC has a resolution of approximately $214\mu V$ and a total power consumption of $3.64mW$ with an occupied active area of $1300 \times 650\mu m^2$. The ADC measures all the 8-channels in a total of $720\mu s$. The measured residual offset is $642.5\mu V$. The input dynamic range of the chip is in the range of $[0-33.6]V$ and the resulted figure of merit is equal to $129.5dB$. The description of the system level architecture and implementation design of this ADC architecture, were published and presented in the [27]-[28], by the author.

REFERENCES

1. N. Noda, "21^{st} century cars and ICs", *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco, 2010.
2. Texas Instruments, "Stachable HEV/EV Li-Ion Battery Monitor and Protector", *BQ76PL536A-Q1 Data Sheet*, TX, USA 2011.
3. Linear Technology Corp., "Multi-cell Battery Stack Monitor", *LTC 6803 Data Sheet*, CA, USA 2011.
4. Analog Devices., "Lithium Ion Battery Monitoring System", *AD7280A Data Sheet*, OR, USA 2011.
5. Lee, J., "Battery management technology for an electric vehicle", *Int. Symp. Low Power Electronic Design, ISLPED*, 2010.
6. A. Affani, et. al., "Battery choice and management for new-generation electric vehicles", *IEEE Trans. Ind. Electron*, vol. 52, pp. 1343-1349, Oct. 2005.
7. Y. Barusokov, *Battery Cell Balancing: What to Balance And How*. [Online]. Available: *http://focus.ti.com/download/trng/docs/seminar/ Topic-Battery Cell Balancing-What to Balance and How.pdf*, 2010.
8. K. Kadirvel, J. Carpenter, R. Shoemaker, J. Ross, P. Huynh, B. Lum-Shue-Chan, "A stackable, 6-cell, Li-ion, battery management IC for electric vehicles with 13, 12-bit $\Sigma\Delta$ ADCs, cell balancing, and direct-connect current-mode communications", *IEEE Journal of Solid-State Circuits*, vol. 49, no. 4, pp. 928-934, April 2014.
9. A. Agah, K. Vleugels, P. B. Griffin, M. Ronaghi, J. D. Plummer, B. A. Wooley, "A High-Resolution Low-Power Incremental $\Sigma\Delta$ ADC With Extended Range for Biosensor Arrays", *IEEE Journal of Solid-State Circuits*,Vol. 45, Issue: 6, pp.1099-1110, June 2010.
10. J. De Maeyer, P. Rombouts, L. Weyten, "A double-sampling extended-counting ADC", *IEEE Journal of Solid-State Circuits*, Vol. 39, Issue: 3, pp. 411-418, March 2004.
11. Texas Instruments, *Characteristics of Rechargeable Batteries*. [Online]. Available: *http://www.ti.com/lit/an/snva533/snva533.pdf*, 2011.
12. T. Kobayashi, K. Nogami, T. Shirotori, and Y. Fujimoto, "A current- controlled latch sense amplifier and a static power-saving input buffer for low-power architecture", *IEEE J. Solid-State Circuits Conf. Dig. Tech. Papers*, vol.28, pp.523-527, Apr. 1993.
13. P. M. Figueiredo, J. C. Vital, "Kickback Noise Reduction Techniques for CMOS Latched Comparators", *IEEE Transactions on Circuits and Systems?II: EXPRESS BRIEFS*, vol. 53, no. 7, Jul. 2006.
14. X. Yang, J. Yang, L. Lin, C. Ling, "Low-power Low-noise CMOS Chopper Amplifier", *Anti-Counterfeiting Security and Identification in Communication (ASID), 2010 International Conference on*, Aug. 2010.
15. C. C. Enz, E. A. Vittoz, F. Krummenacher, "A CMOS Chopper Amplifier", *Solid-State Circuits Conference, 1986. ESSCIRC '86. Twelfth European*, pp. 77-79, Sep. 1986.
16. A. Bakker, J. H. Huijsing, "A CMOS chopper opamp with integrated low-pass filter", *Solid-State Circuits Conference, 1997. ESSCIRC 97. Proceedings of the 23rd*, pp.200-203, Sep. 1997.
17. A. Bilotti, G. Monreal, "Chopper-stabilized amplifiers with a track-and-hold signal demodulator", *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol.46, no.4, pp. 490-495, Apr. 1999.
18. C. C. Enz, G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization", *Proceedings of the IEEE*, Vo. 84, Issue. 11, pp. 1584-1614, Nov. 1996.
19. J. Mitros, C.-Y. Tsai, H. Shichijo, M. Kunz, A. Morton, D. Goodpaster, D. Mosher, and T. Efland, "High-voltage drain extended mos transistors for 0.18μm logic cmos process", *Electron Devices, IEEE Transactions on*, vol. 48, no. 8, pp. 1751-1755, Aug 2001.

20. D. Yilmaz Aksin, I. Ozkaya, "25V sampling switch for power management data converters in $0.35\mu\mathrm{m}$ CMOS with DNMOS", *ESSCIRC, 2009. ESSCIRC 09. Proceedings of*, pp. 136-139, Sep. 2009.

21. I. Ozkaya, C. Gurleyuk, A. Ergul, A. Akkaya, D. Yilmaz Aksin, "A 50V input range 14bit $250kS/s$ ADC with $97.8dB$ SFDR and $80.2dB$ SNR", *European Solid State Circuits Conference (ESSCIRC), ESSCIRC 2014 - 40th*, Nov. 2014.

22. L. Xu, B. Gönen, Q. Fan, J.H. Huijsing, K.A.A. Makinwa, "A $110dB$ SNR ADC with $\pm 30\mathrm{V}$ input common-mode range and $8\mu\mathrm{V}$ Offset for current sensing applications", *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, pp. 90-91, Feb. 2015.

23. M. Belloni, E. Bonizzoni, A. Fornasari, F. Maloberti, "A Micropower Chopper-CDS Operational Amplifier", *IEEE Journal of Solid-State Circuits*, vol. 45, no. 12, Dec. 2010.

24. C. C. Enz, E. A. Vittoz, F. Krummenacher, "A CMOS Chopper Amplifier", *IEEE Journal of Solid-State Circuits*, vol. SC-22, no. 3, pp. 335-342, Jun.1987.

25. J. F. Witte, K. A. A. Makinwa, J. H. Huijsing, "A CMOS Chopper Offset-Stabilized Opamp", *IEEE Journal of Solid-State Circuits*, vol. 42, no. 7, pp. 1529-1535, Jul. 2007.

26. R. Schreier and G.C. Temes, "Understanding Delta-Sigma Data Converters", *New York: Wiley*, 2005.

27. M. Baghbanmanesh, F. Maloberti, "On the design of incremental data converters with extended range", *Circuits & Systems (LASCAS), 2015 IEEE 6th Latin American Symposium on*, Sep. 2015.

28. M. Baghbanmanesh, F. Maloberti, "Multichannel time interleaved ADC for sensor interfaces", *2016 $12th$ Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, Jul. 2016.

CHAPTER 4

RADIATION INDUCED EFFECTS IN ELECTRONIC DEVICES

Commercial integrated circuits (ICs) may not have an adequate level of immunity to radiations to guarantee good reliability in harsh environments. Radiation hard circuits undergo a set of qualification tests, before being used in space (satellites) or in nuclear applications (high energy physics, nuclear power plants, medical equipments for radiology and radiotherapy). However, is worth remarking that every electronic equipment can be affected by low dose rate radiation, due to various sources: e.g., natural radioactivity in materials, high energy cosmic rays, X-ray scanners in airports, etc. The evolution of IC fabrication technology towards ever more dense integration scale has a twofold effect on radiation tolerance: at modern nano-scale size, devices are more tolerant to cumulative (long-term) effects, but on the other hand they are more prone to soft errors due to single events [1]. Therefore, design of complex integrated systems should account for such effects.

4.1 Radiation Environments

Electronic devices are often exposed to radiation effects, and the most frequently associated radiation environment is the naturally-occurring space radiation environment. Put in simple terms, space electronics are exposed to radiation from the Van Allen belts, solar flares, solar wind and cosmic rays. Spacecraft and satellites in earth-orbit encounter large amounts of radiation from the Van Allen radiation belts, which are regions of trapped protons and electrons, see Fig. 4.1, The inner Van Allen belt contains mainly protons with energies up to 30 MeV, whereas the outer Van Allen belt contains

fast moving electrons and slow moving ions, that are trapped in the magnetosphere, with energies which can exceed 100 MeV. The particle flux in these regions depends highly on the altitude, orbital inclination as well as the solar activity. Traditionally radiation has only been a problem in areas with elevated levels of radiation, such as space and particle accelerators. Nowadays device scaling has lead to that electronics are susceptible to radiation damage on a terrestrial level as well. This subchapter briefly discusses some environments where electronics are used and might require radiation hardening.

4.1.1 Space

Radiation levels in space depends on the proximity of extraterrestrial bodies. Always present are the galactic cosmic rays consisting of ions from other parts of the galaxy or deep space. Added to this are the constant flux of particles from stars if 'within'a solar system. These include x-rays, protons and electrons with protons being the dominant particle type. Close to stars and planets there can also be areas with higher particle density due to the magnetic field surrounding these bodies. Close to the earth there are two such belts, one at approximately 35768 km above the surface near the geosynchronous orbit consisting mostly of electrons, and one at approximately 500 km (varies rather much) near the low earth orbit consisting mostly of protons [3]. Both these fields are illustrated in Fig. 4.1.

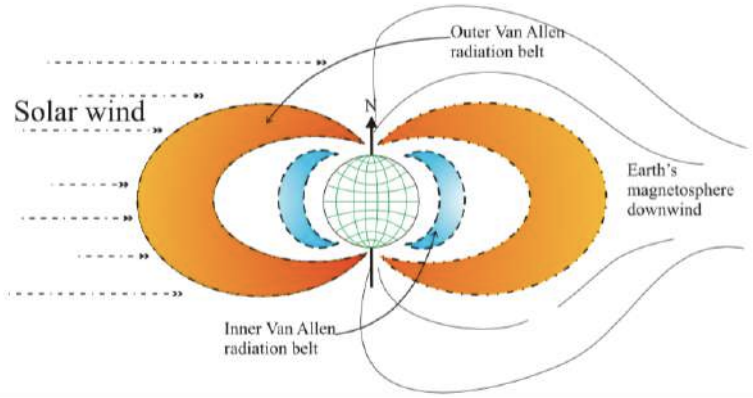


Figure 4.1 Near earth particle belts [3].

4.1.2 Terrestrial

Electronic devices also encounter hazardous radiation environments in the Earths atmosphere. Galactic cosmic rays, which originate from outside the solar system, consist of low flux, highly energetic particles up to the GeV range. These particles produce intense ionization and are very hard to shield against. When cosmic rays interact with atmospheric nuclei, nuclear spallation reactions take place and induce production of high energy neutrons and pions [4]. Fig. 4.2 illustrates the terrestrial nuclear cascade shower as a result of incoming cosmic rays. As in the geo-space environment, the particle-flux and energy in the Earths atmosphere depend highly on altitude as well as events in the intergalactic space weather. Therefore, the radiation impact on electronics is higher for avionics applications then for ground based applications [6]. Cosmic rays can also induce soft errors in electronics at sea level [5]. The main radiation sources causing soft errors in electronics at sea level are cosmic ray induced neutrons and pions, and microelectronic packaging induced alpha particles [5] . As neutrons

and pions interact with silicon, nuclear reaction takes place and the resulting high energy secondary particles scatter in all directions. Furthermore, natural radiation environments are not the only radiation environments hazardous for electronics. Man-made radiation environments can also induce errors on electronic devices. Such environments are encountered in, but not limited to, nuclear power plants, medical applications and warfare.

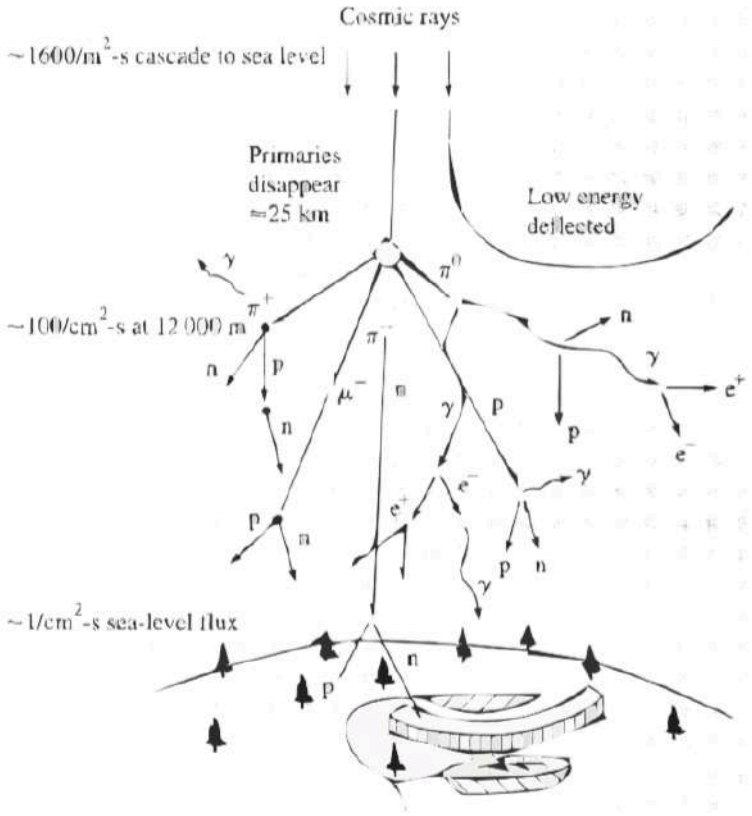


Figure 4.2 Terrestrial radiation environment, adapted from [5].

4.1.3 Particle Accelerators

Particle accelerators usually produce particles with a wide range of energies. Depending on where in the accelerator the electronics are located different levels of radiation hardness must be met. Sensory equipment close to the area where the experiment take place must usually be able to sustain large amounts of radiation while most of the electronics used for processing data are placed further away and might not require any radiation hardness at all. One example would be a detector in the large hadron collider (LHC) in which the lifetime total ionizing dose (TID) is expected to be 250 Mrad (SiO_2) and the displacement damage dose (DDD) 2.5 ů 1015 $\mathrm{n/cm^2}$ (1 MeV neutron equivalent) [7].

4.2 Interaction Between Radiation and Silicon

Energetic particles incident on a solid material lose their energy through ionizing and non-ionizing processes as they travel through the material. Depending on what type of particle it is and its kinetic energy it will participate in one or more of these processes. Charged heavy particles like protons and ions loose their energy through both ionizing and non-ionizing processes while lighter charged particles like electrons lose their energy mostly through ionizing processes. Heavy non-charged particles like neutrons lose their energy through non-ionizing processes. The interaction between external radiation (photons like X-rays and γ-rays, charged particles like protons, electrons, and heavy ions, or neutral particles) and a semiconductor may cause two main phenomena: ionization and displacement [8].

4.2.1 Ionization Phenomenon

When radiation interacts with the semiconductor material, an electron in the valence band may acquire enough energy to pass in the conduction band. Therefore, an electron-hole pair (HEP) is generated: a free electron is present in the conduction band and a hole in the valence band. If an electric field exists in the ionization region (e.g., in biased devices), HEPs are separated and carriers move within the semiconductor, giving an extra (parasitic) current. Then, the carriers may recombine, or remain trapped, or drift into an electrode. The ionization phenomenon is measured with the **Linear Energy Transfer** (LET) [8]. The LET indicates the quantity of energy lost by the incident particle along its path into the target material. The LET depends on atomic number of the particles and on energy of the particle, target material and the collision location:

$$LET = \frac{dE}{\rho.dx}\left[MeV.\frac{cm^2}{mg}\right]$$

where ρ is the density of the target material, and $\frac{dE}{\rho.dx}$ indicates the average energy transferred into the target material per length unit along the particle trajectory.
Ionization effects can be divided into two main categories:
► **Temporary Ionization Effect**: is due to HEP separation and generation of a parasitic current;
► **Fixed Ionization Effect**: is due to trapping of carriers in insulators, where the mobility of carriers is lower than in the semiconductor, or at the interface between insulator and semiconductor; when positive charges are trapped, a shift of device parameters occurs, and circuit performance may be affected.

4.2.2 Displacement

When a neutral particle interacts with the silicon lattice, it transfers energy to lattice atoms. A transferred energy greater than 20 eV can displace a silicon atom, which moves toward an interstitial position, and the displaced atom can displace other atoms along its trajectory. Defects due to atom displacement in the silicon lattice act as energy levels within band-gap. These levels alter electric properties of semiconductor (e.g., life time of minority carriers, doping density, mobility, etc.) [9].

4.3 Radiation Effects on ICs

Damaging effects due to radiation can be divided into two major categories: cumulative effects due to a long-time exposure to radiation, and single event effects due to the interaction with a single particle.

From the viewpoint of circuit performance, cumulative effects can be divided into total ionizing dose (TID) effects, caused either by charged particles (e.g., electrons or protons), or by photons (X-rays and γ-rays), and displacement damage dose (DDD) effects, caused by massive particles (e.g., neutrons, protons, or heavy ions) [8]. Galactic cosmic rays, cosmic solar particles and trapped protons in radiation belts are the main sources of energetic particles causing single event effects (SEE). The single event effect are initially non-destructive events in electronic devices. However, SEEs can also result in semiconductor degradation (both over time and instantly) by causing radiation damage to local or global parts of the device. Therefore, single event effects in electronics are often categorized in soft and hard errors. Single event effects have received recognition ever since the 1950s, and their nature has been researched thoroughly ever since then [5]. Soft errors are commonly related to the post impact state of high energy ionizing particles interacting with semiconductor materials at locations close to sensitive circuit nodes of active devices. Hard errors on the other hand are errors that cause destructive damage to transistors and other semiconductor materials. Hard errors often occur over time due to cumulative effects, and can therefore be avoided if the potential hard error inducing effects are discovered and corrected in time [10]. This following subsections briefly describes the most common cumulative and single event, both non-destructive and destructive, radiation effects encountered in electronic devices and ICs.

4.3.1 Cumulative Effects

In CMOS integrated circuits, the most sensitive region to cumulative effects are the field oxide isolation (thick oxide) and gate oxide isolator (thin oxide), which are related to electron-hole pair generation in the oxide, leading to unwanted charge build-up and insulator degradation [11].

4.3.1.1 Total Ionizing Dose (TID)

When incident charged particles lose their kinetic energy through ionizing processes the long-term damages that occur are collected under the name total ionizing dose (TID). TID refers to the total amount of energy that is deposited by incident particles into a material, and is usually measured in rads. The main process by which TID affects a device is charge buildup in its dielectrics. One of the most commonly used dielectrics in transistors today are silicon dioxide, the effects described in 4.2.1 will refer to that. Alternate dielectrics are being investigated more and more because of current leakage in the gate due to thin layers of dielectric in modern manufacturing processes. When a MOS transistor is exposed to high-energy ionizing irradiation, electron-hole pairs are created in the oxide (both gate oxide and field oxide). Almost all TID effects in CMOS transistors are related to electron-hole pair generation in the oxide [13]. The generated carriers induce the buildup of charge, which can lead to device degradation. Fig. 4.3 illustrates the cross section of the physical layout of a standard MOS transistor. The effects of TID radiation in a MOS device will be mainly on:

1. gate oxide, which can result in threshold voltage shift;

2. channel edges, which can result in turning on of the parasitic edge transistor;

3. isolation oxide, which can result in increased inter-device leakage, or even complete loss of device isolation.

The processes by which charge gets trapped in silicon dioxide when a charged particle strikes it are illustrated in Fig. 4.4 and are:

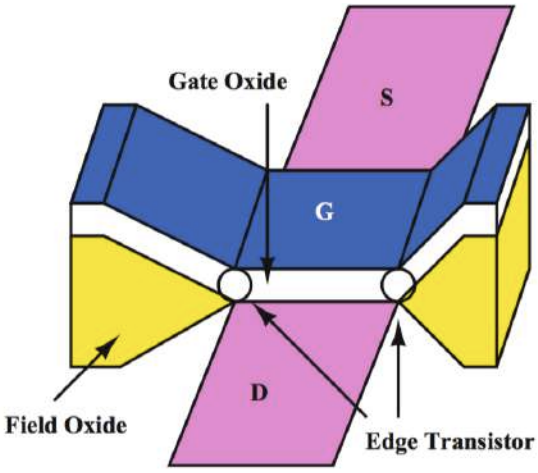


Figure 4.3 Illustration of the physical layout of a standard MOS transistor [2].

1. High-energy electrons and protons ionize atoms, generating electron-hole pairs. The generated electron-hole pairs can generate secondary electron-hole pairs if their energy are high enough. In this way, one incident electron or proton can generate thousands of electron-hole pairs. Taking into account the hole yield and initial electron-hole recombination, the total number of holes generated in the oxide N_{ot} is given by [14]:

$$N_{ot} = f(E_{ox}).g_0.D.t_{ox}, \tag{4.1}$$

where $f(E_{ox})$ is the hole yield as a function of oxide electric field, D is the total dose, and t_{ox} is the oxide thickness. g_0 is a material-dependent parameter giving the initial charge pair density per rad of a dose (g_0 = $8.1 \times 10^{12} pairs/cm^3$ per rad for SiO_2 [14]).

2. The immediate recombination of a fraction of the generated electron-hole pairs. Most electron-hole pairs are not recombined since the electron mobility is much higher than the hole mobility, the electrons will leave the oxide in a matter of picoseconds [13]. The electric field applied across the oxide also affects how many electron-hole-pairs that will recombine since it will force the electrons and holes apart.

3. The generated holes that have not recombined will move through the silicon dioxide through a process called polaron hopping. A hole will move by hopping between localized states in the oxide. The direction decided by the electric field in the oxide. Due to its charge, as a hole moves through the oxide it causes a distortion of the local potential field of the oxide lattice. This local distortion increases the trap depth at the localized site, which tends to confine the hole to its immediate vicinity. This distortion follows the hole as it moves through the oxide, the charge of the hole combined with its strain on the oxide is called a polaron, this is why the process is called polaron hopping [13].

4. The holes that have not become trapped deep in the oxide will either leave the oxide, get trapped close to the surface of the oxide as a border trap or participate in the formation of an interface trap at the surface of the oxide, Fig. 4.5 [13].

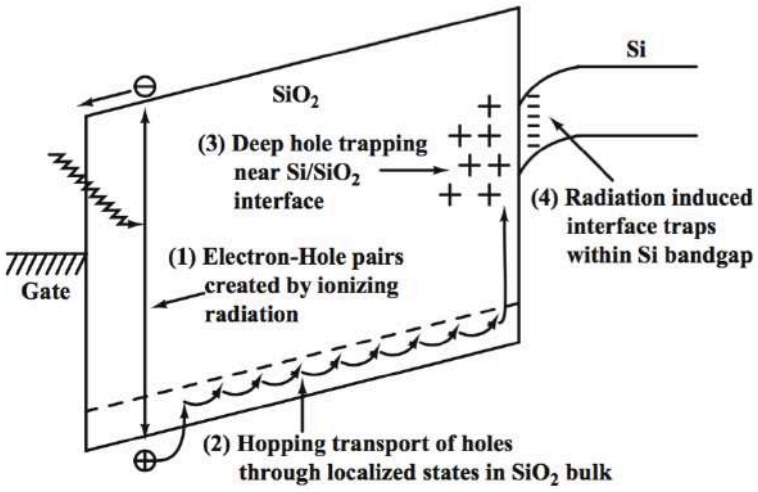


Figure 4.4 Main process by which charge is trapped in silicon dioxide [15].

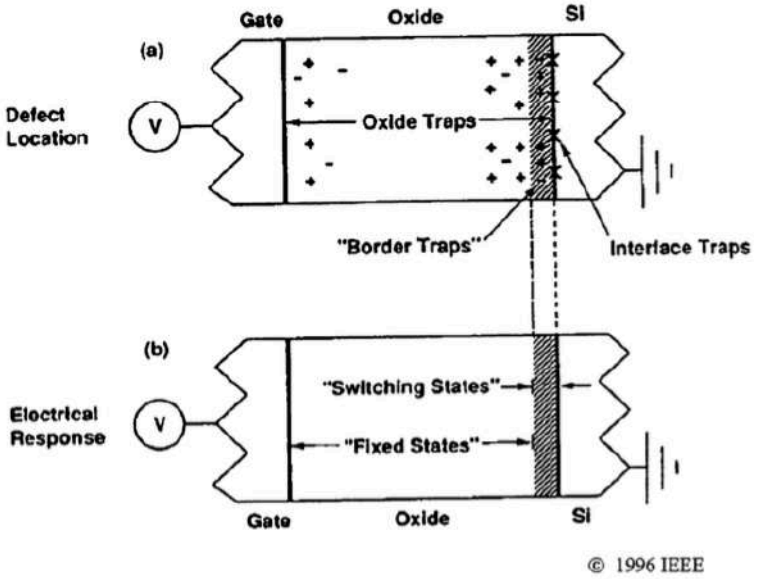


Figure 4.5 Image a) shows the location of TID defects. Image b) shows which of these traps that have a permanent charge and which are switching [15].

► **Oxide Traps**: two types of defect centers are participating in the formation of charge buildup in silicon dioxide, these defects are called E' centers. E_δ is a relatively shallow trap responsible for the transportation of holes within the oxide, the polaron hopping. E_γ is a significantly deeper trap [15]. Most of the E_γ traps are located along the the border of the oxide, close to the neighboring silicon. These defects have the ability to communicate with the neighboring silicon by transferring charges, and

thereby switch state. The charges are transferred either by simple capture and re emission or tunneling [15]. Since these defects are close to the border and are able to exchange charge they are called border traps or switching states. The E_γ located deeper in the oxide will act more like permanent traps. Once a hole has been trapped at a E_γ trap deep in the silicon dioxide it will act as a permanent charge. Oxide traps have a net positive charge in both n- and p-channel devices. Both of these defects can be seen in Fig. 4.5.

► **Interface Traps**: as the name indicates, interface traps are located at the surface between an oxide and neighboring silicon. Interface traps act very much like border traps in that they can switch state but since they are situated immediately on the surface of the oxide there is essentially no barrier for trapping and de-trapping carriers. This will reduce the carrier mobility and recombination rates in the silicon adjacent to the oxide and thus affect devices that rely on those. In general, threshold interface traps are usually net positive in p-channel transistors and net negative in n-channel transistors. The formation of interface traps differ from the formation of oxide traps. It is believed that hydrogen ions (protons) are released as holes "hop" through the oxide or as they are trapped near the oxide interface. At the interface, hydrogen atoms can participate in a reaction leading to the formation of interface traps [13].

The amount of charge that can be trapped in an oxide depends on its thickness, the thicker the oxide is the more charge can be trapped. As technologies have continued to shrink, so has the thickness of the oxides. This has been beneficial in terms of TID damage since less charge can get trapped, charge buildup in the gate oxide in modern technology nodes is therefore nearly non-existing. However the thinness of the dielectrics have caused problems as electrons can tunnel through them, increasing leakage currents. In order to prevent this leakage dielectrics with higher dielectric constants are being explored as they would allow the usage of thicker dielectrics with decreased tunneling leakage as a consequence. How these alternative dielectrics react to radiation seems to differ from material to material. Materials like Nitrided and Reoxidized Nitrided Oxides seems to be resistant to TID damage despite being much thicker than their silicon dioxide counterparts. Some materials like Hafnium Dielectrics have, at least in initial studies, been more susceptible to oxide traps than silicon dioxide [15]. Further testing of the materials and devices built from them is still required.

4.3.2 Single Event Effects

Single event effects are a collective name for scenarios where one incident particle causes an effect on a device or circuit level that propagates to system level. SEEs can be divided into soft-errors, that can be solved while the device is still working (such as a transient current), hard-errors that requires a power cycling or reconfiguration (such as a flipped memory bit or latch-up) and permanent-errors such as a broken transistor. The most sensitive place, the place where a SEE is most likely to originate, is in a reverse biased pn-junction. When an incident particle strikes the reverse biased pn-junction a track of generated electron-hole-pairs forms a cylindrical volume with very high carrier concentration. A tunnel shaped extension of the depletion region will form deep into the substrate while the generated electrons will start to drift towards the n-type material effectively creating a short across the pn-junction. The remaining carriers will proceed to diffuse towards the critical node where they get collected. This process is described in Fig. 4.6.

With each new device scaling the charge used to store one bit of information gets smaller. The charge deposited by one incident particle is however constant. This leads to that the number of SEEs increases as device scaling continues. Depending on where in the device/circuit the particle strike, different SEEs occur. The most common SEEs are described in the following subchapters.

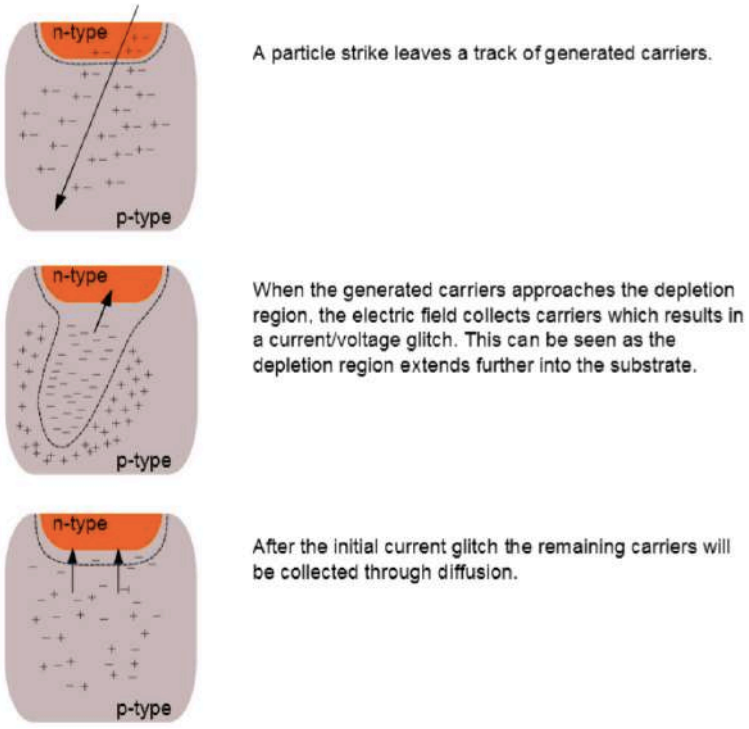


Figure 4.6 Conceptual description of a pn-junction struck by a particle [17].

4.3.2.1 Single Event Transients

SETs occur when a particle strike creates enough free charge to create a pulse that propagates through a part of combinatorial logic. This can happen in both analog and digital circuits but the events that decides if they cause damage differs. A SET is created when a particle strikes the drain of a transistor Fig. 4.7. If the particle deposits enough charge, the pn-junction will be upset and a short between the bulk and drain will form, giving the drain the same voltage as the bulk. The duration of this short depends on how fast the transistor can deliver enough charge to restore the reverse biasing of the pn-junction. The transistors current drive and the capacitive load on the drain therefore decides how wide the initial SET will be. Single event transients are of great concern for analog electronics such as comparators [6, 18]. Mitigation techniques primarily involve capacitive hardening and in some cases digital correction techniques.

Analog Single Event Transients: ASETs appear as spikes and glitches in the output voltage of an analog circuit. Depending on the circuits function and what follows it the ASET may or may not cause damage.

Digital Single Event Transients: In order for a DSET to cause damage a certain sequence of events must happen.

1. A SET is generated in a sensitive logic node.
2. It propagates down a logic path to a memory element, like a flip-flop.

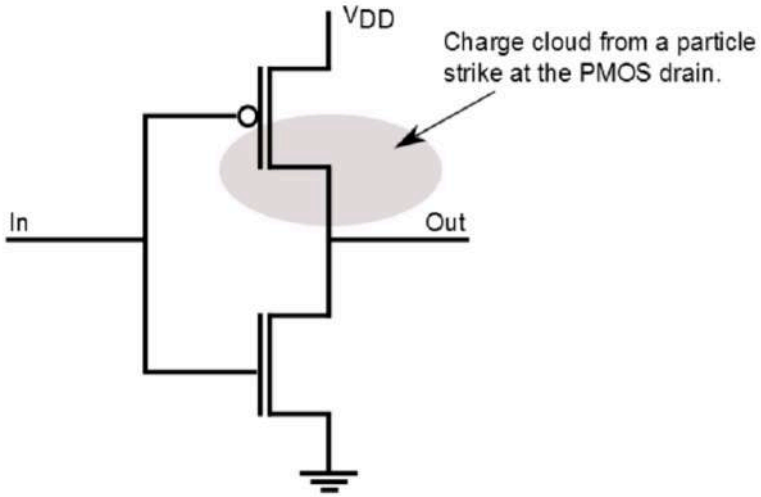


Figure 4.7 Illustration of a pn-junction struck by an incident particle.

3. It arrives at the memory element with sufficient amplitude and duration to change the memory state.
4. It arrives during the setup and hold time of the memory element, i.e. the 'window of vulnerability'.

Depending on where in the digital logic the SET latches, masked, latent and unmasked errors can occur [19]:

- A masked error is an error that is present in a memory element but does not affect the output nor the functionality of the system.
- A latent error is an error that does affect the output but not in a critical way, for example one faulty pixel in an image.
- An unmasked error is an error that affects the output in a critical way, making it unusable.

4.3.2.2 Single Event Upsets

A SEU can be defined as a change in the logic state of a latched logic element from a logic one to a logic zero or vice-versa. SEU occur when high energy particles alter the charge deposition in critical nodes in such a way that it results in a bit error. SEU are defined to be non-destructive events, and therefore the affected logic can be rewritten or reset to regain proper operational behavior [6]. An example would be a SRAM cell whose nodes storing the information are struck by a particle and thereby makes them change state, Fig. 4.8. SETs can lead to SEUs if in the chain there are flip-flop or registers (Fig. 4.9) [11].

4.3.2.3 Multiple Bit Upset

Multiple bit upsets (MBU) are upsets resulting from a single high velocity charged particle strike, passing through several sensitive nodes in an electronic device, and thereby changing the logic state

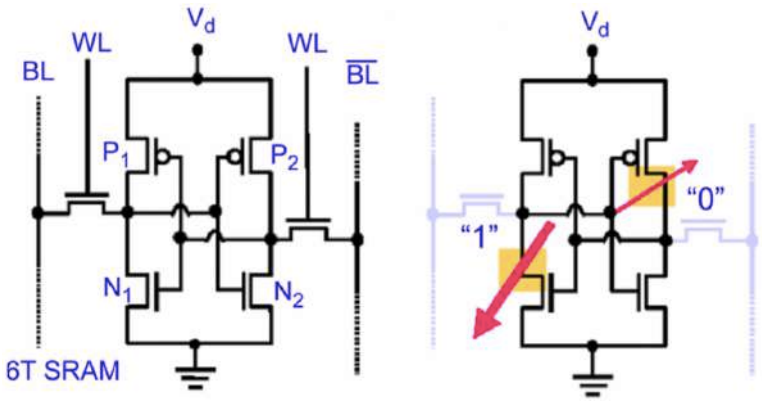


Figure 4.8 A particle strike in one node of a SRAM cell can cause a change in the node's stored voltage state which can propagate to the other node, upsetting the cell [27].

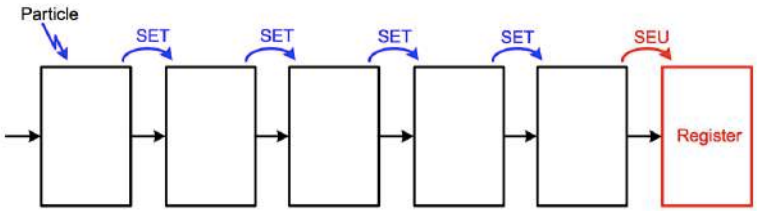


Figure 4.9 Effect of SET propagation [11].

in several adjacent latched logic elements. For high velocity particle strikes, the number of bit upsets has been shown to be highly dependent on the impact angle of the particle [21]. MBUs can also occur as a result of proton induced- as well as terrestrial neutron induced nuclear reactions that produce secondary ionizing particles which interact with capacitive nodes in close proximity of the initial strike [22]. However, due to the technology feature size scaling trends, the device sensitivity to MBUs is expected to keep increasing in high density ultra deep-sub-micron designs [23, 24].

4.3.2.4 Single Event Latch-ups

SEL can occur in CMOS logic when the parasitic p-n-p-n structure between the source contacts are activated, Fig. 4.10. The p-n-p-n path resembles a semiconductor controlled-rectifier (SCR) that is stable in either its off- or on-state.

Normally the n-well is maintained at the same potential as the PMOS source, and the p-substrate at the same potential as the NMOS source. This prevents the SCR from latching, keeping it in its off-state. However, a particle strike may cause the voltage in either the n-well or the p-substrate to drop and thereby make the SCR latch in its conductive state, effectively creating a short between the supply rails. In order to return the SCR to its off-state a power cycling is usually required. Latch-up can also be caused by voltage transients in the supply rails which is why shallow trench isolation or guard bands are used in modern CMOS technology nodes.

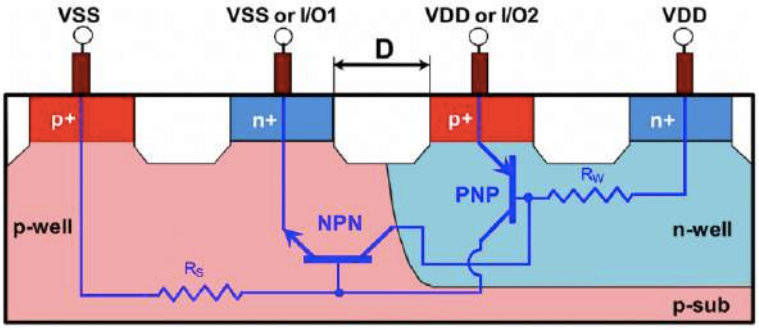


Figure 4.10 Illustration of the p-n-p-n SCR between the source contacts in a CMOS technology [25].

4.4 Transistor-Structures and Properties in RHBD Applications

When designing circuits for radiation tolerant applications, the designer must primarily evaluate the transistor behavior for the targeted radiation environment. For these types of applications, transistor behavior is highly dependent on process choice as well as technology node [24]. The primary concern regarding transistor behavior is described in terms of TID induced leakage. Several approaches have been proposed to counter the effects of TID, and thereby retain stable transistor operation in harsh radiation environments using standard commercial CMOS processes.

4.4.1 Impact of Technology Scaling on Radiation Tolerance

Technology scaling trends in commercial processes have brought about both positive and negative effects in terms of radiation tolerance. The TID induced leakage currents and threshold voltage shifts have been substantially reduced as a consequence of using thinner gate oxides [27]. Contemporary commercial processes exhibit little sensitivity to radiation induced threshold voltage shifts due to the reduced possibility of radiation induced positive charge getting trapped in the thin oxide layers [27]. Furthermore, the utilization of STI instead of Local Oxidation of Silicon (LOCOS) for inter device isolation has contributed to large reductions in TID induced leakage currents. These factors are some of the main reasons RHBD has been made a realistic possibility. Reports have also shown that thin gate oxides are adequate for operating in heavy ion environments, without great risk of gate oxide breakdowns [30]. On the other hand, the impact of technology scaling has also contributed to smaller feature sizes (such as 90 or 65 nm) which in turn result in less nodal capacitances which make devices more prone to SEUs due to less energy may result in a SET. Additionally, as the device sizes shrink, higher density is achieved which thereby enables a single particle hit to upset several devices in close proximity. In contrast to thin gate oxides, isolation oxides are thicker and therefore enable for TID induced positive trapped charge, and thereby need to be taken into account when designing circuits for radiation tolerant applications.

4.4.2 Total Ionizing Dose Effects in CMOS

Since the mechanism behind TID damage is charge trapped in isolation oxides, commonly silicon dioxide, the volume and location of isolation oxides both inside and close by a CMOS determines

its susceptibility to TID damage. Traditionally the gate oxide has been the major contributor to TID damage in a CMOS. The charge trapped in the gate oxide would alter the CMOS's threshold voltage, Fig. 4.11, the total threshold voltage shift ΔV_{th} is the sum of the threshold voltage drifts due to oxide-trapped charge and interface-trapped charge, given by

$$\Delta V_{th} = \Delta V_{ot} + \Delta V_{it}. \tag{4.2}$$

Meanwhile,

$$\Delta V_{ot} \propto \frac{N_{ot}}{C_{ox}} \propto t_{ox}^2. \tag{4.3}$$

where N_{ot} is the total oxide-rapped charge and is proportional to t_{ox}, and C_{ox} is inversely proportional to t_{ox}; At high dose rates, neutralization of oxide-trapped charge will hardly occur and ΔV_{ox} can be large. Conversely, interface-trapped charge will have had insufficient time to build up and ΔV_{it} is normally small [13]. Therefore, the total threshold-voltage shift is usually dominated by ΔV_{ot} in this case.

Another important TID effect is increasing the drain-to-source leakage in n-channel transistors since they would not be turned off properly and reducing the current drive in p-channel transistors since they would not be turned on properly. However, due to transistor scaling the gate oxide in modern technology nodes is so thin that the charge buildup is either not present or very small [15]. It is also likely that any charge trapped in the gate oxide will be compensated for, or annihilated, by electrons tunneling through the gate oxide.

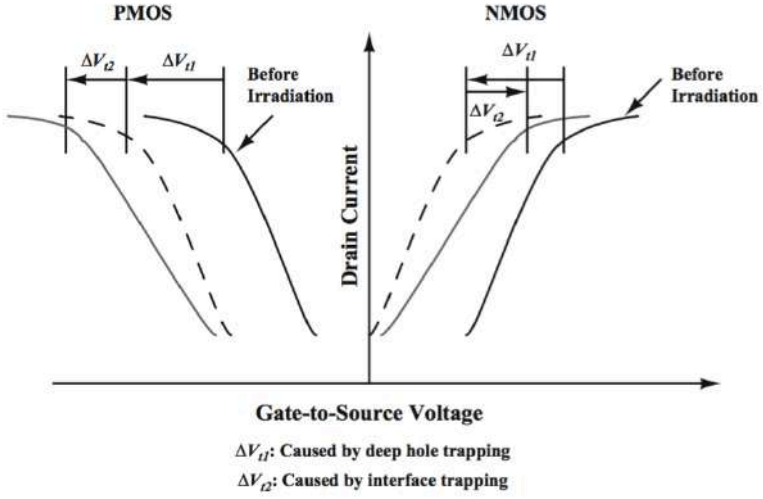


Figure 4.11 Shift in threshold voltage due to charge trapped in the gate oxide [15].

The use of shallow trench isolation (STI) to prevent latch-up in modern CMOS technology nodes is currently the main contributor for charge buildup and thus TID damage [16]. In general STI is implemented as shown in Fig. 4.12.

As the charge trapped in oxides are predominately positive, NMOS and PMOS transistors are affected differently. The basic mechanism for leakage is that positive charge trapped in an oxide adjacent to a p-type silicon layer enables currents to flow from one isolated region to another, However, edge leakage is not a critical problem for PMOS transistors, since for PMOS transistors the effect

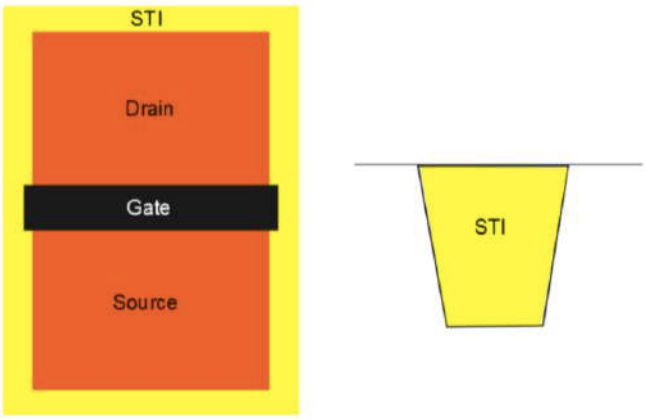


Figure 4.12 Shallow trench isolation in a CMOS technology.

of oxide-trapped positive charge is to shift an already negative threshold voltage even further in the negative direction. Places where this can occur are:

1. Drain-to-source leakage in one NMOS as shown in Fig. 4.13(a). Leakage parasitic NMOSs will form along the edges of the drain and source where the gate overlaps the STI. This will contribute to the off state drain-to-source leakage and a reduction of the threshold voltage Fig. 4.13(b).

2. Device-to-device leakage between two different NMOSs as shown in Fig. 4.14(a).

3. NMOS drain/source-to-n-well leakage as shown in Fig. 4.14(b). If a conducting line (metal or poly) happens to be routed over the isolation oxide area, any positive bias presented on the line might turn on this parasitic field oxide transistor into inversion due to the radiation-induced negative threshold voltage shift. In this case, a leakage path exists between different devices, which might lead to complete loss of inter-device isolation.

The path marked 1 contributes to the intra-device source-to-drain off-state leakage Fig. 4.13(a). This leakage path is formed by the positive charge trapped at the Si-SiO2 interface along the sidewalls of the trench. These effects were seen in the nMOS devices. pMOS devices show very little response to radiation, as expected since their edges do not turn-on when positive charge is trapped [31]. Inter-device (or device-to-device) is the other type of leakage current caused by trapped charge in STI. The leakage path marked 2 in Fig. 4.13(a) corresponds to the device-to-well leakage current. This leakage path runs from a drain or source region of an nMOS transistor to an adjacent nWELL and is caused by trapped positive charge in the bottom of the STI trench.

4.4.3 TID Effects in Advanced CMOS Technologies

As described above the radiation-induced threshold voltage shift is proportional to t_{ox}^2. This means that CMOS technology scaling would reduce a MOSFETs susceptibility to the radiation-induced damage in gate oxide [15]. This is primarily due to the fact that the trapped charge buildup in gate oxides scales with t_{ox}. Moreover, the positive trapped holes are further annihilated or compensated by tunneling electrons from the gate channel [16]. Enhanced CMOS gate oxide hardness (on the order of 1-3

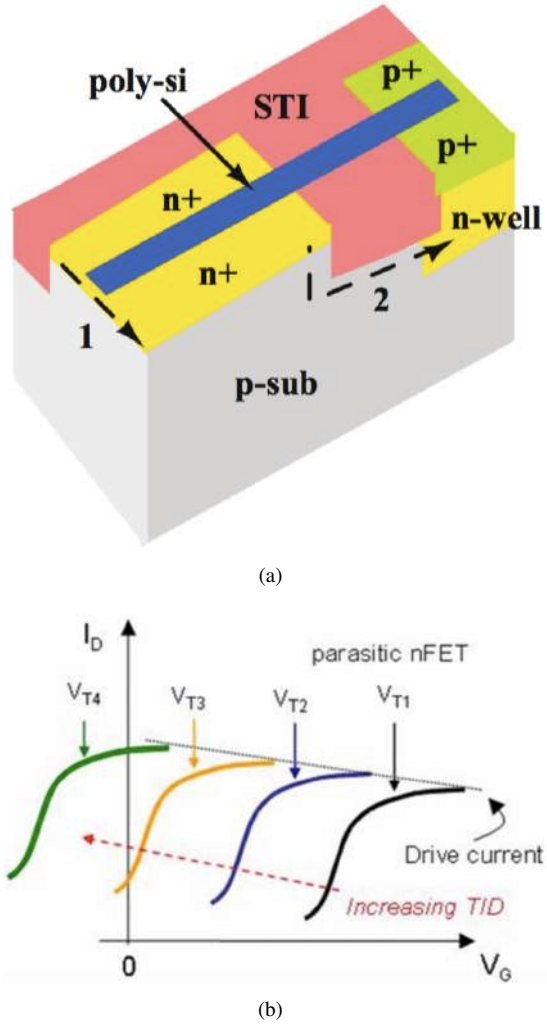
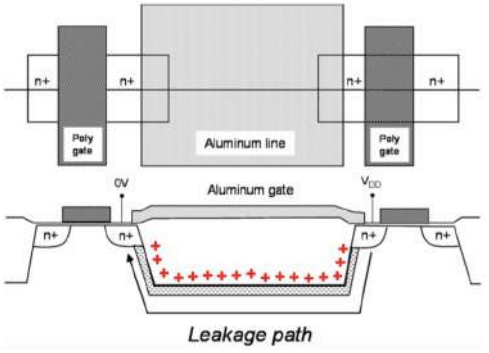
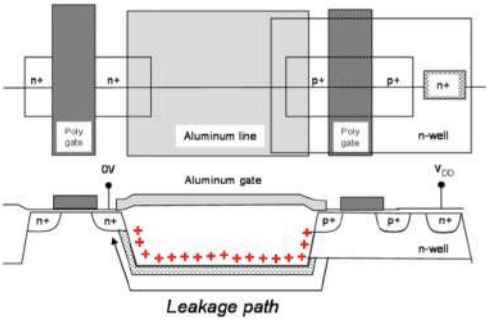


Figure 4.13 (a) Parasitic nMOS associated with the n-channel CMOS, and (b) the effects of increased TID exposure on the threshold voltage and drive current of a parasitic nMOS [15].

kGy(SiO_2)) has been observed at small technology nodes, e.g., 0.18- and 0.13-μm CMOS [4]. At these nodes, gate oxide thicknesses t_{ox} are smaller than 4 and 2 nm, respectively, which are very close to the approximate distance for a high-probability electron tunneling ($\sim$3 nm) [16]. The increased TID hardness of commercial CMOS technologies has been proved experimentally and reported in several publications [29, 31]. The above analysis suggests that as technology scaling continues, the radiation-induced threshold shift of CMOS transistors would become negligible. This is also the primary reason that RHBD has become a realistic option over the past few years, while more circuits were designed at smaller technology node ($< 0.18\mu$m). As soon as transistors under irradiation can maintain being functional without significant threshold voltage shifts, all other radiation effects (e.g., leakage, gain error, offset, etc.) can somehow be mitigated through compensation or calibration techniques. While



(a)



(b)

Figure 4.14 (a) Illustration of nMOS device-to-device leakage , and (b) Illustration of nMOS drain/source-to-n-well leakage [15].

the gate-oxide-trapped charge appears to be no longer an issue for advanced CMOS technologies, radiation-induced charge trapping in the isolation field oxide still leads to increased leakage currents and device performance degradation [32, 34]. This is mainly due to the fact that the STI oxide of modern CMOS technologies does not scale down with the gate size to the same extent. Nevertheless, it is possible with RHBD circuit or layout techniques to eliminate these effects.

4.4.4 Single Event Effects in CMOS

A CMOS contain two reverse biased pn-junctions, one at the source and one at the drain. As described in 4.3.2 SEEs are originating from these junctions, most commonly the drain. When incident particles travel through the large volume of doped substrate material beneath the pn-junctions electron-hole-pairs are generated which give rise to SEEs. Separating the pn-junctions from the substrate material is thus one way to reduce the susceptibility of SEEs which is why semiconductor on insulator (SOI) transistors, are interesting when designing radiation hard circuits [35]. Due to the impact of technology scaling, deep sub-micron implementations of SEU tolerant topologies are highly affected by the charge sharing between sensitive nodes [36]. Charge sharing implies that the charge generated from a particle hit is shared between transistors in close proximity.

REFERENCES

1. Eishi H. Ibe, *Terrestrial Radiation Effects in ULSI Devices and Electronic Systems*. Hoboken, NJ : Wiley-IEEE Press, 2014. - 268 p.
2. Y. Cao, P. Leroux, M. Steyaert, *Radiation-Tolerant Delta-Sigma Time-to-Digital Converters*. Heidelberg New York : Springer, 2015, ISBN 978-3-319-11841-3.
3. A. Johnston, "Radiation effects in optoelectronic devices", *Nuclear Science, IEEE Transactions on*, vol. 60, pp. 2054-2073, June 2013.
4. E. I. Y. Y. H. K. Takashi Nakamura, Mamoru Baba, *Terrestrial Neutron-Induced Soft Errors In Advanced Memory Devices* (World Scientific, 2008), Chap. 1.2 General Description of the SEE Mechanism.
5. J. F. Ziegler, H. W. Curtis, H. P. Muhlfeld, C. J. Montrose, B. Chin, M. Nicewicz, C. A. Russell, W. Y. Wang, L. B. Freeman, P. Hosier, L. E. LaFave, J. L. Walsh, J. M. Orro, G. J. Unger, J. M. Ross, T. J. O Gorman, B. Messina, T. D. Sullivan, A. J. Sykes, H. Yourke, T. A. Enger, V. Tolat, T. S. Scott, A. H. Taber, R. J. Sussman, W. A. Klein, C. W. Wahaus, "IBM Experiments In Soft Fails In Computer Electronics", *IBM Journal of Research and Development*, 40 (1996).
6. D. M. F. R. D. Schrimpf, *Radiation Effects and Soft Errors in Integrated Circuits and Electronic Devices* (World Scientific, 2004), Chap. Hardness Assurance for Commercial Microelectronic.
7. F. Faccio, B. Allongue, G. Blanchot, C. Fuentes, S. Michelis, S. Orlandi, and R. Sorge, "Tid and displacement damage effects in vertical and lateral power mosfets for integrated dc-dc converters", *in Radiation and Its Effects on Components and Systems (RADECS)*, 2009 European Conference on, pp. 46-53, Sept 2009.
8. A. Camplani, S. Shojaii, H. Shrimali, A. Stabile, V. Liberali, "CMOS IC Radiation Hardening By Design", *Electronics and Energetics* Vol. 27, No.2, June 2014, pp. 251-258.
9. J. Srour, C. Marshall, P. Marshall, "Review of displacement damage effects in silicon devices", *Nuclear Science, IEEE Transactions on*, vol. 50, pp. 653-670, June 2003.
10. R. C. Bauman, *in Radiation Effects and Soft Errors in Integrated Circuits and Electronic Devices*, D. M. F. R. D. Schrimpf, ed., (World Scientific, 2004), Chap. SoftErrors in Commercial Integrated Circuits, pp. 15-25.
11. U. Gatti, C. Calligaro, E. Pikhay, Y. Roizin, "Radiation-hardening methodologies for flash ADC", *Analog Integrated Circuits and Signal Processing*, May 2016, Volume 87, Issue 2, pp 141-154.
12. J. R. Schwank, M. R. Shaneyfelt, D. M. Fleetwood, et al., "Radiation effects in MOS oxides", *IEEE Trans Nucl Sci*, 55(4):1833-1853, 2008.
13. J. Schwank, M. Shaneyfelt, D. Fleetwood, J. Felix, P. Dodd, P. Paillet, and V. Ferlet-Cavrois, "Radiation effects in mos oxides", *Nuclear Science, IEEE Transactions on*, vol. 55, pp. 1833-1853, Aug 2008.
14. F. B. McLean, T. R. Oldham, "Basic mechanisms of radiation effects in electronic materials and devices", *Tech. Rep. HDL-TR-2129*, Harry Diamond Laboratory. www.dtic.mil/dtic/tr/fulltext/u2/a186936.pdf. Accessed 12 March 2013.
15. H. Barnaby, "Total-ionizing-dose effects in modern cmos technologies", *Nuclear Science, IEEE Transactions on*, vol. 53, pp. 3103-3121, Dec 2006.
16. A. Cester, A. Paccagnella, "Switching oxide ionizating radiation effects on ultra-thin oxide MOS structures", *Schrimpf RD, Fleetwood DM (eds) Radiation effects and soft errors in integrated circuits and electronic devices*,World Scientific, Singapore, 2004
17. T. C. May, "Soft errors in VLSI: Present and future", *IEEE Trans. Comp., Hybrids, Manufact. Technol.*, vol. 2, pp. 377-387, Dec. 1979.
18. D. M. S. Buchner, "Single Event Transients in Linear Integrated Circuits", *IEEE Nuclear and Space Radiation Effects Conference Short Course*.

19. V. Ferlet-Cavrois, L. Massengill, and P. Gouker, “Single event transients in digital cmos: a review”, *Nuclear Science, IEEE Transactions on*, vol. 60, pp. 1767-1790, June 2013.

20. R. Lacoe, “Improving integrated circuit performance through the application of hardness-by-design methodology”, *Nuclear Science, IEEE Transactions on*, vol. 55, pp. 1903-1925, Aug 2008.

21. A. Tipton, X. Zhu, H. Weng, J. Pellish, P. Fleming, R. Schrimpf, R. Reed, R. Weller, and M. Mendenhall, “Increased Rate of Multiple-Bit Upset From Neutrons at Large Angles of Incidence”, *Device and Materials Reliability*, IEEE Transactions on 8, 565-570 (2008).

22. F. Wrobel, “Use of nuclear codes for neutron-induced nuclear reactions in microelectronics”, *In On-Line Testing Symposium, 2005. IOLTS 2005. 11th IEEE International*, pp. 82-86 (2005).

23. G. Swift and S. Guertin, “n-flight observations of multiple-bit upset in DRAMs”, *Nuclear Science*, IEEE Transactions on 47, 2386-2391 (2000).

24. M. Baze, B. Hughlock, J. Wert, J. Tostenrude, L. Massengill, O. Amusan, R. Lacoe, K. Lilja, and M. Johnson, “Angular Dependence of Single Event Sensitivity in Hardened Flip/Flop Designs”, *Nuclear Science*, IEEE Transactions on 55, 3295-3301 (2008).

25. A. Oberoi, M. Khazhinsky, J. Smith, and B. Moore, “Latch-up characterization and checking of a 55 nm cmos mixed voltage design”, *in Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD)*, 2012 34th, pp. 1-10, Sept 2012.

26. L. Gonella, F. Faccio, M. Silvestri, S. Gerardin, D. Pantano, V. Re, M. Manghisoni, L. Ratti, and A. Ranieri, “Total Ionizing Dose effects in 130-nm commercial CMOS technologies for HEP experiments”, *Nucl. Instrum. Methods Phys. Res.*, A 582, 750-754 (2007).

27. R. Lacoe, “Improving Integrated Circuit Performance Through the Application of Hardness- by-Design Methodology”, *Nuclear Science*, IEEE Transactions on 55, 1903-1925 (2008).

28. R. Lacoe, “CMOS scaling, design principles and hardening-by-design methodologies”, *IEEE Nuclear and Space Radiation Effects Conference*, Short Course Notebook, 2003.

29. L. Ratti, L. Gaioni, M. Manghisoni, et al, “Investigating degradation mechanisms in 130nm and 90 nm commercial CMOS technologies under extreme radiation conditions”, *IEEE Trans Nucl Sci*, 55(4):1992-2000

30. L. Massengill et al., “Heavy-ion-induced breakdown in ultra-thin gate oxides and high-k dielectrics”, *Nuclear Science*, IEEE Transactions on 48, 1904-1912 (2001).

31. R. C. Lacoe, J. V. Osborn, R. Koga, S. Brown, D. C. Mayer, “Application of Hardness-By-Design Methodology to radiant-Tolerant ASIC Technologies”, *IEEE Trans. Nucl. Sci.*, vol. 47, no. 6, December 2000, pp. 2334-2341.

32. F. Faccio, G. Cervelli, “Radiation-induced edge effects in deep sub-micron CMOS transistors”, *IEEE Trans Nucl Sci*, 52(6):2413-2420, 2005.

33. P. Dodd, M. Shaneyfelt, J. Schwank, and J. Felix, “Current and future challenges in radiation effects on cmos electronic”, *Nuclear Science, IEEE Transactions on*, vol. 57, pp. 1747-1763, Aug 2010.

34. A. H. Johnston, R. T. Swimm,GR. Allen, T. F. Miyahira, “Total dose effects in CMOS trench isolation regions”, *IEEE Trans Nucl Sci*, 56(4):1941-1949, 2009.

35. R. Schrimpf, M. Alles, D. Fleetwood, D. R. Ball, M. J. Gadlage, and F. El-Mamouni, “Design and evaluation of soi devices for radiation environments”, *in SOI Conference (SOI)*, 2010 IEEE International, pp. 1-4, Oct 2010.

36. O. A. Amusan, L. W. Massengill, M. P. Baze, B. L. Bhuva, A. F. Witulski, J. D. Black, A. Balasubramanian, M. C. Casey, D. A. Black, J. R. Ahlbin, R. A. Reed, M. W. McCurdy, “Mitigation Techniques for Single-Event-Induced Charge Sharing in a 90-nm Bulk CMOS Process”,*Device and Materials Reliability*, IEEE Transactions on 9, 311-317 (2009).

CHAPTER 5

A 10-BIT RADIATION-HARDENED SAR ADC FOR SPACE APPLICATION

This project presents a rad-hard 10-bit 1MHz SAR ADC for space applications. This work was done in collaboration with RedCatDevies, Italy specially Dr. Umberto Gatti and its goal was to design an radiation tolerant ADC by using rad-hardened techniques at architecture, circuit and layout levels. The design takes into account the different effects of the radiation that could damage the circuits in harsh environments. A conventional SAR ADC with charge redistribution capacitive DAC was implemented in order not to mix-up possible inaccuracy of the converter itself with the effect of radiations, thus this simple structure and safe performance allowing a better understanding of radiation impacts on mixed analog-digital circuits. The ADC has been fabricated in a 0.15-μm RF CMOS process 1.8V technology by LFoundry (LF15A PDK). The prototype active area is 212$\times$285 μm^2 and consumes $1.23mW$. It operate with a nominal supply voltage of 1.8V. Post-layout *noise-transient* simulation results show an ENOB equal to 9.6 bits in the band of interest, $[1-10]KHz$, at full scale input voltage. The resulted figure of merit is 792 fj/convesrion-step.

5.1 Introduction

Throughout this decade, the space industry has been signaling an increased interest in robust integrated circuit design for use in space missions [1, 2, 3]. In the past, radiation hardening of electronic components is achieved via process modification by rad-hard foundries, which is so-called radiation hardened by process (RHBP). While RHBP has the advantage of being an extremely reliable

means of achieving hardened components, it is susceptible to low-volume concerns such as yield, process instability, and high manufacturing costs [4]. Traditional circuits used in space applications are designed using radiation hardened processes and may consume relatively large amounts of power. However, with the decline in the RHBP market and with new semiconductor technologies emerging, new mitigation techniques need to be employed in order to successfully suppress the impact of soft errors on modern electronic devices [5]. In order to leverage these limitations, the RHBD approach was proposed. In RHBD, electronic components are manufactured to meet specified radiation tolerance requirement, but the techniques employed to meet these specs are implemented either in the system architecture or in layout and not in the fabrication process. Through a combination of the application of specific design techniques and the leveraging of the increased intrinsic radiation hardness of modern advanced integrated circuit (IC) technologies, it is now possible to fabricate radiation-hardened components using standard complementary metal-oxide-semiconductor (CMOS) processes. These recent years, several papers have been published on exploring potential advantages with low voltage commercial CMOS technology in radiation tolerant digital CMOS design [6, 7, 8]. The experimental results have shown the immunity up and over 300 krad (Si) TID induced leakage current [9] and demonstrated the validity of the adopted RHBD approach and allow designers defining rad-hard corners that constrain the analog circuits design. With the use of circuit- and layout-level soft error mitigation techniques, digital and analog mixed-signal circuits may become relevant for hazardous radiation environments, and even space applications. ICs in the space environment requires the employment of radiation tolerant components to be able to safely operate during the whole system life. Radiation hardening by design techniques are used to improve the radiation hardness of a device, circuit or system without changing the manufacturing process. RHBD is used because it is usually cheaper than a special manufacturing process and it allows the use of commercial process technology with low cost. In general it involves redesigning devices and circuits, adding redundancy and temporal filtering to mitigate the effects induced by radiation.
Generally three main approaches have been considered to develop rad-hard components [9]:

- process enhancements (radiation hardening-by-process, RHBP [10]);
- design enhancement (radiation hardening-by-design, RHBD [11]);
- shielded packages (radiation hardening-by-shielding, RHBS).

RHBP uses solutions involving dedicated fabrication processes or specific technologies (i.e. SOI, SiGe, Chalcogenide phase change materials, etc.). RHBP represents the best solution if RHBD and specific processes are used, but it shows several disadvantages [9]:

1. generally dedicated processes (SOI or SiGe) are expensive;
2. the maturity of such processes is not comparable with standard ones;
3. specific manufacturing variations (extra masks, specific doping profiles, etc.) need to obtain radiation hardening lead to low yields and low repeatability.

In general RHBP represents an effort that can be supported only by large silicon foundries, but rad-hard market represents a niche (because of low volumes). Moreover, these special processes are usually under US ITAR restrictions [12].

RHBS uses customized packages (e.g. Rad-Pak®[13]). The effectiveness of shielding depends on the radiation environment. For this reason, custom solutions shall be studied case by case and typically a shielding package is heavier than a comparable ceramic part. Their effectiveness against high energy

particles is also a concern. An estimate of trapped proton fluxes transmitted by plane aluminum shields of various thicknesses (from 0.5 to 2 g/cm^2 aluminum) for a low earth polar orbit (700 $km - 97°$) during minimum solar activity showed a great residual transmitted fluxes for proton energies ranging from a few MeV to about 500 MeV [14].

While RHBP and shielded packages have been already employed for the development of commercial rad-hard analog components, very few examples exists of analog RHBD. They mainly come from the research or from high-energy physics experiments [15].

5.2 Radiation Hardening Techniques by Design (RHBD)

Over the course of the past decade, the TID radiation hardness of commercial CMOS technologies has been evolving rapidly, due to the continual shrinking of the gate oxide thickness. However, there is no guarantee of the same radiation tolerance level among different processes at the same technology node provided by different manufacturers, since the radiation hardness is not a parameter that commercial semiconductor foundries monitor [16]. Moreover, the TID effects in a given CMOS technology are very much linked to the exact thickness of the gate oxide, imperfection levels in the isolation SiO_2 region, etc. Unfortunately, those parameters are usually not modeled in CMOS devices, which makes the prediction of the impact of irradiation on a CMOS circuit very difficult. They are also often not disclosed by the manufacturer, complicating the semiconductor level modeling of radiation effects. Therefore, besides choosing a more advanced CMOS technology for radiation-hardened designs, RHBD techniques are also required in the circuit to ensure its reliability and performance even under an extreme radiation level.

An effective use of RHBD relies on the assumption that the process to be used must be standard. RHBD on CMOS technology may count on the following advantages:

1. maturity of the process and very high repeatability;
2. low cost;
3. availability from many silicon foundries;
4. Multi Project Wafer (MPW) approach (low cost and quick prototyping, low volume productions);
5. RHBD technical solutions are easily portable.

RHBD techniques can be employed during the whole design phase of a CMOS chip. In general, they can be separated into three hierarchical levels:

1. System and Architecture Level (RHBD-AL);
2. Circuit and Device Level (RHBD-CL);
3. Layout Level (RHBD-LL).

as illustrated in Fig. 5.1. Each level will be discussed in details in the following sections.

The target technology for this project is a standard 0.15-μm RF CMOS, whose size allows for compact mixed-signal circuits, while guaranteeing good rad-hard performance. More scaled CMOS processes (such as 90 or 65 nm) involves a reduction of the gate oxide thickness and seem to be more TID "tolerant". However, both SEU (shorter channels and reduced critical charge for SET/SEU triggering) and SEL are expected to be worse.

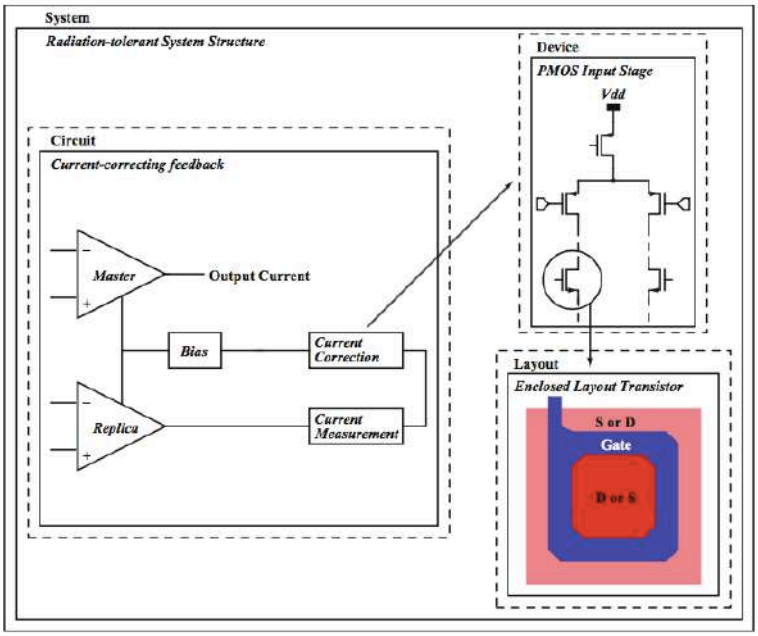


Figure 5.1 Radiation hardened by design strategy.

5.2.1 Architecture Level Radiation Hardening Design (RHBD-AL)

Architecture-level RHBD is the most effective way to assure the radiation hardness of an electronic device. When an electronic system is required to perform certain functions in a radiation environment, one should first consider choosing a system structure which provides the highest radiation tolerance. A good example is the selection of a suitable analog-to-digital converter (ADC) for radiation-hardened applications. ADCs have various architectures, such as the flash, pipeline, successive approximation (SAR), dual slope integrating, and delta-sigma type. For a given specification in terms of resolution, power consumption, and dynamic range, all those ADC types might be suitable. However, they indeed have different radiation tolerance levels. Several commercial ADC parts from different manufacturers were compared in [17], to examine their gamma radiation performance. Based on compression provided on [17], half flash converters performed worse than others presented there as they suffered from functional failure at relatively lower cumulative dose. The linearity parameters, the conversion time exhibited significant deterioration. The integrating converters, $\Sigma\Delta$ ADCs, have shown highly radiation tolerant. The radiation behavior of the SAR ADC is depended on the way the DAC logic is implemented. The overall radiation performance of SAR ADC was average with higher tolerance observed in the dc parameters (tri-state current, conversion time) as well as linearity issues (offset error, INL) as compared to the Flash ADC, however their functional failure threshold was also found to be lower than that of either IADC or $\Sigma\Delta$ ADC. The SAR ADC architecture was chosen in this design, due to simple structure rather than complex structure of IADC or $\Sigma\Delta$ ADC, which gives us the possibility to not mixing-up possible inaccuracy of the converter itself with the effects of radiations, thus this simple structure and safe performance allowing a better understanding of radiation impacts on mixed analog-digital circuits.

5.2.2 Circuit- and Device-Level Radiation Hardening Design (RHBD-CL)

Despite an appropriate system architecture could offer better radiation tolerance, it might suffer from circuit-level failures due to radiation. Therefore, one must identify all radiation susceptible components in the system, and make sure that they can achieve the required radiation tolerance level. The device-level RHBD approach tackles CMOS radiation hardness assurance issues by selecting appropriate transistor types and geometries (width and length) for circuit implementation. For instance, in old CMOS technologies, PMOS transistors are preferred for radiation-hardened designs since their threshold voltage shifts only cause performance variations rather than functionality failures. Moreover, a transistor's TID effects have also dependencies on its geometry. As described in [18] and [19], for the same technology, a transistor with longer gate-length shows much less radiation-induced threshold voltage shifts and leakage currents compared to short-gate-length devices. Therefore, during the actual circuit design phase, we have to take into account all these practical issues and carefully choose devices'types and geometries, e.g., using transistors with the minimum gate-length should be avoided. This will in return give you significantly enhanced circuit's radiation tolerance. For those reason, we need to apply RHBD techniques at the circuit and device level. In this project, circuit-level RHBD techniques are demonstrated in the design of D-FF digital block by using a *Logic-CAP* in critical nodes, which will be further discussed in 5.3.2.1.

5.2.3 Layout Level Radiation Hardening Design (RHBD-LL)

Layout-level RHBD techniques have been proved to be very effective in eliminating single-event latch-up and preventing radiation-induced leakage currents. One example is the enclosed layout transistor (ELT) for ultra-high radiation-hardness applications [15], and to avoid SEL, physical design must minimize parasitic resistances associated with the PNPN structure, which acts as a PNP and an NPN BJT stacked next to each other in normal CMOS ICs, this could be achieving by designing a large number of contacts and in placing n-well and bulk contacts as close as possible to n-well/p-substrate junctions, to reduce the resistive path. The goal is to avoid SELs and reduce SETs and SEUs, but it is also the main domain where TID solutions are adopted to reduce long term dose effects.

5.2.3.1 Edge-less Transistors (ELT)

An Edge-less transistors (ELT) has a closed gate shape, which separates the drain and the source region of the CMOS transistor. A typical layout of the ELT is shown in Fig. 5.2. Such a layout arrangement eliminates the parasitic transistors originally located at two edges of a conventional CMOS device. The radiation-induced MOS transistor off-state leakage current has then been greatly reduced. The idea behind an enclosed annular transistor is that it has no active diffusion areas that are adjacent to any isolation oxides that is overlapped by polysilicon (gate), Fig. 5.2. This means that it can not be any source-to-drain leakage along an isolation oxide sidewall due to radiation induced parasitic transistors. This makes the annular transistor much less sensitive to the effects of charge buildup in isolation oxides, i.e. TID damage. Other homologous transformations of the standard ELT transistor layout can be found in [20, 21]. Main drawbacks of the ELT transistor are its relatively large area and inaccurate modeling. When using ELTs, the internal side of the ring-shaped transistor should be used as the drain terminal of the MOS device, and the external side should be the source terminal. In this way, the design minimizes the area of the drain, which is the most sensitive node for SEE, thus reducing the cross-section.

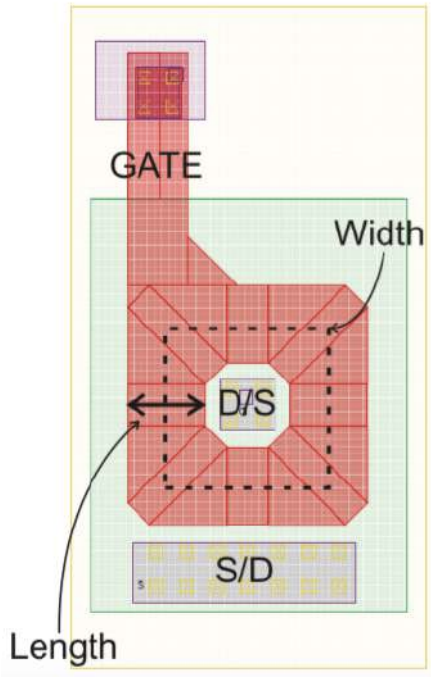


Figure 5.2 Layout view of a edge-less transistor (ELT).

5.2.3.2 Guard Rings

In order to prevent inter-device leakage, diffusion ring can be used to surround adjacent NMOS and PMOS devices respectively. The highly doped diffusion ring will introduce a very high voltage threshold in the bulk between two devices and thus prevent leakage between them. The immunity to latch-up is guaranteed by isolation techniques, i.e. by surrounding the facing PMOS and NMOS with non-interrupted polarization rings. Moreover, the use of guard rings around transistors of the same type biased at different voltages reduces inter-device leakage, since positive charges trapped in the STI oxide cannot induce a parasitic channel between n-type diffusions at different voltages. Those techniques are applied wherever in the ADC layout. Compared to conventional layout design, ELTs and guard rings require a larger silicon area. Therefore, a higher level of radiation tolerance can be achieved only at the expense of a larger area [22].

5.3 Implementation of 10-bit SAR ADC RHBD

The implementation of 10-bit charge redistribution SAR ADC in 0.15 μm RF CMOS process technology at 83.3KS/s ($f_{CLK} = 1MHz$) with power supply voltage of 1.8V is described by adopting the RHBD approaches for the circuits and layout level, such as:

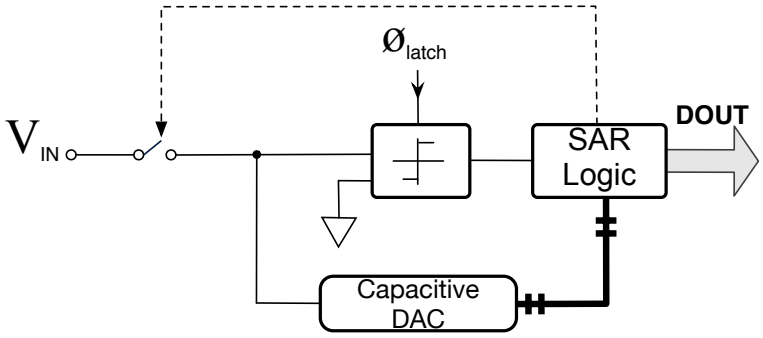
- Switches based on ring-shaped MOS.

- Isolation techniques for latch-up prevention.
- Enhancing the critical charge in the sensitive nodes with respect to SET and SEU.

SAR architecture consists of both combinational and sequential logic. Since large systems are built up using combinational and sequential logic blocks which operate in conjunction, the SAR architecture can be regarded as a scaled model of a larger system. By analyzing the SET and SEU tolerance of the hardened SAR architectures, a better understanding will be provided on how the different mitigation techniques compare.

5.3.1 Architecture

The Fig. 5.3(a) shows the architectural block diagram chosen for our SAR ADC. Successive Approximation Register (SAR) A/D (analog to Digital) converters based on charge redistribution are frequently used when area and power consumption are most important factors for the design of the converter on the integrated circuit. SAR ADCs are sequential converter that take N clock cycles to convert an analog input into an N-bit digital representation. They are frequently chosen over flash ADCs for medium to high-resolution application, since flash ADCs over 10 bits are not commercially viable. Additionally, SAR ADCs usually present better speed of conversion than Σ-Δ ADCs.



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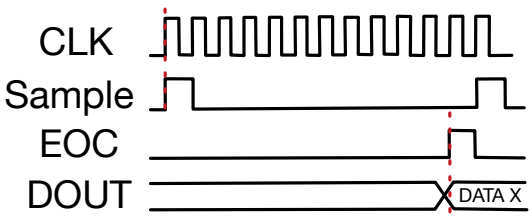


(b)

Figure 5.3 (a) SAR ADC architecture with capacitive DAC (b) Its simplified timing diagram.

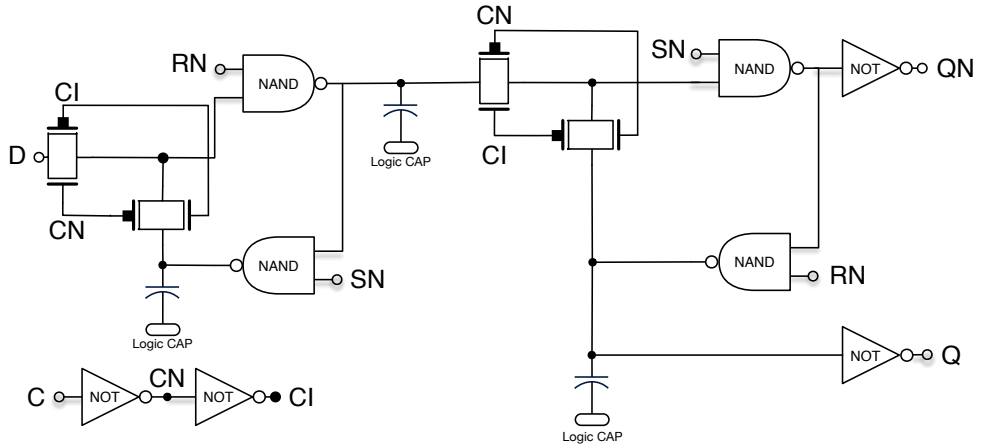
The low power feature of this kind of converters maybe a desired benefit to critical applications such as satellite control, instrumentation systems, and wireless sensor networks. These applications maybe subjected to environmental interactions, such as radiation effects and electromagnetic interference, and, despite that, it is desirable that the embedded converters perform well in such conditions.

Another motivation to study this kind of converter is that it is commonly present in programmable commercially available mixed-signal platforms, such as SmartFusion [23]. Such kind of programmable mixed-signal (MS) circuits offer characteristics like fast prototyping, design flexibility and the reduction of the analog expertise level required from mixed-signal designers. For all these reasons, programmable analog and MS circuits have become an important platform to electronic systems design, including those oriented to critical applications, such as avionics and space systems, as well as nuclear and particle accelerator facilities.

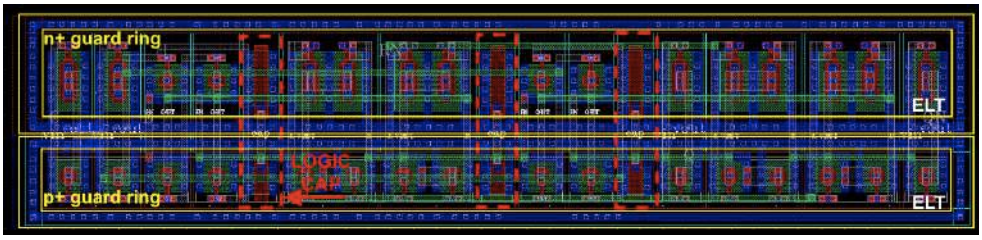
The D/A converter usually contains a binary-weighted capacitor array. In each conversion, first the analog input is sampled and stored in the capacitor array and then the output of the DAC is compared to the common mode voltage (V_{CM}) for N clock cycle. The output of the DAC successively follows the V_{CM} voltage at the comparator's input and reaches V_{CM} at the end of each conversion. The Fig. 5.3(b) shows the simplified timing diagram of the charge redistribution SAR ADC.

5.3.2 Digital Logic

5.3.2.1 Enhanced Delay Type Flip-Flop Logic Block



(a)



(b)

Figure 5.4 (a) Enhanced transmission-gate based set/reset delay type flip-flop circuit schematic (b) Layout of the proposed D type flip-flop.

The Fig. 5.4(a) illustrated the schematic of enhanced transmission gate based set/reset D Flip-Flop which has been widely used in the conventional SAR Logic. It could be noted that in order to mitigate single event effects, extra capacitances, implemented with MOS transistors, have been added to the sensitive nodes, named *Logic Cap*, which shown in Fig. 5.5(a).

The logic cap is used to make hardened the critical nodes of D-FF for incident particle, in this way, critical charge values increase, thus reducing SEUs (a higher LET is required to upset) and SETs. The critical charge is the minimum possible charge that could generates a voltage able to upset a logic port;

$$Q_{Crit} = C_{Node} \times \Delta V \tag{5.1}$$

where C_{Node} is the total capacitance incident on the critical node of the D-FF. The critical nodes shall be enough capacitive to be resilient to the critical charge released by the heavy ion. By increasing the capacitance value of logic-cap it is possible to improve more immunity to SEE. However a trade-off with respect to logic speed shall be found; it's realized with two MOS, a W/L equal to 2.4/0.60 for PMOS and 1.2/0.60 for NMOS was considered to be suitable with respect to the typical charge created by particles. Fig. 5.5 shows the schematic and layout of logic-cap, which has been implemented with a standard conventional CMOS layout.

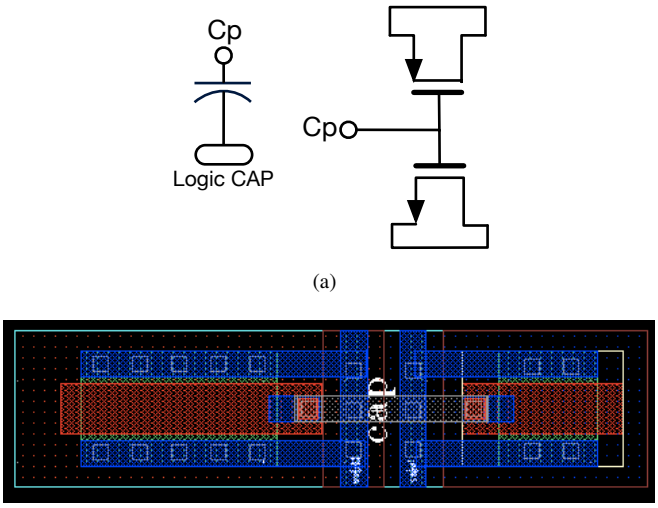


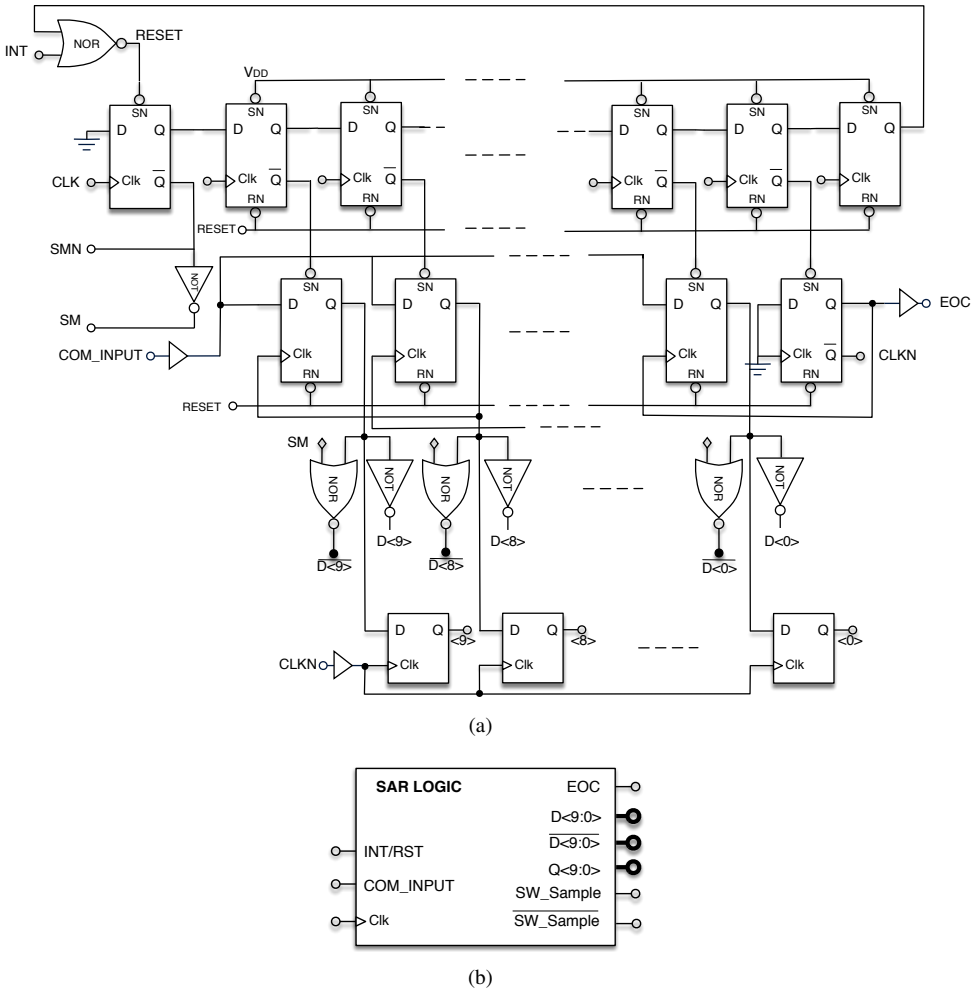
Figure 5.5 (a) Symbol and circuit schematic of logic-cap (b) Layout of the logic-cap.

The Fig. 5.4(b) illustrated the layout of our proposed RHBD technique D-FF, an extensive use of ELT shapes guarantees resiliency to TID and to avoid SEL (latch-up) a careful guard-ring in layout has been used.

5.3.2.2 Successive Approximation Register (SAR) Control Logic

SAR control logic block architecture shown in Fig. 5.6(a) was proposed in [24] and is commonly used in SAR ADCs due to its straightforward design technique. This control logic encompasses a ring counter and a code register. The ring counter is in fact a shift register. For each conversion, in clock cycle 0, the EOC signal is high and all Flip Flops outputs are reset to zero, and for the rest of cycles

EOC is low. In the next clock cycle, the most significant flip flop is set to one which corresponds to MSB of the digital word to the DAC. Then the counter shifts '1' through the flip flops from MSB to LSB.



(a)

(b)

Figure 5.6 (a) Conventional SAR control logic block diagram (b) SAR control logic symbol.

In each clock cycle, one of the outputs in the ring counter sets a flip flop in the code register. The output of this flip flop which is set by the ring counter is used as the clock signal for the previous flip flop. At rising edge of the clock, this Flip Flop loads the result from the comparator. At the end of each conversion, EOC signal turns to high. This type of SAR logic, converts each sample in 12 clock cycles to obtain a 10-bit resolution.

The flip flops which are employed in this structure, has described in section 5.3.2.1. The total of 34 D-FF has been used in this SAR control logic.

In Fig. 5.7 a part of SAR logic layout view is shown. It is possible to identify the use of ELT shapes and multiple guard-rings in order to guarantees resiliency to TID and SEEs. It is particularly important

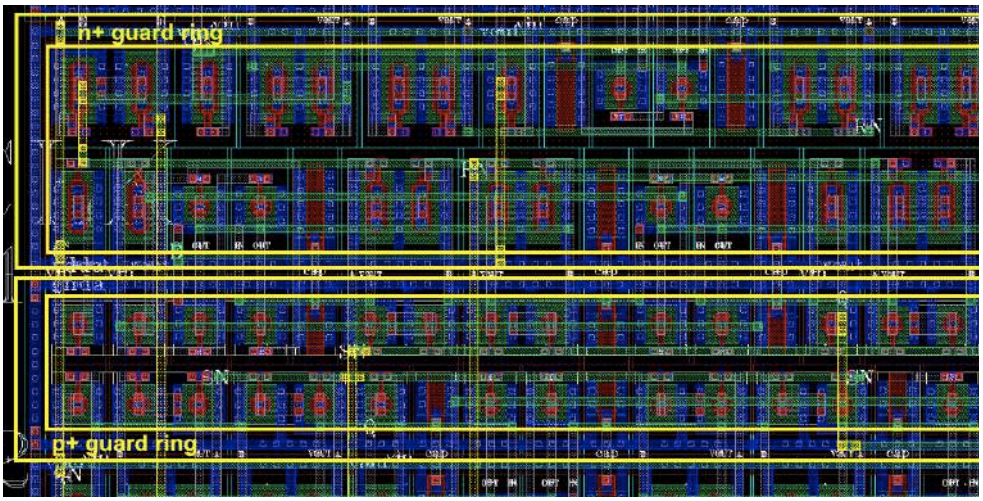


Figure 5.7 a part of SAR logic layout view in 0.15μm RF CMOS technology.

that all the digital chain of each row is realized with robust logic cells since SETs can lead to SEUs if in the chain there are flip-flop or registers. The Fig. 5.8 illustrated the entire layout view of SAR control logic implemented in this project.

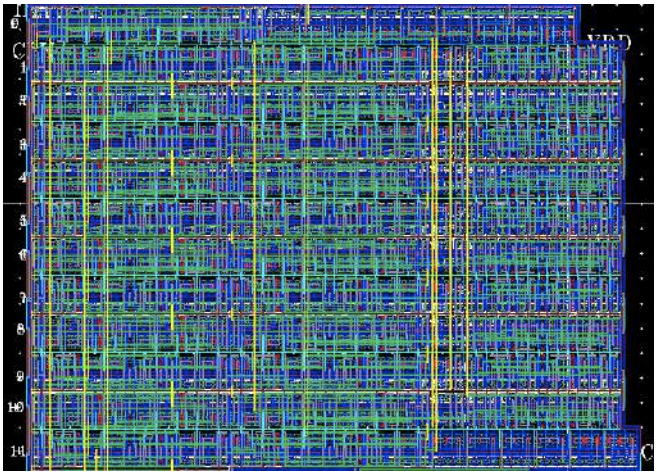


Figure 5.8 Layout view of SAR control logic.

5.3.3 Split Binary-Weighted Capacitor Array DAC

A split binary-weighted capacitor array has been chosen as DAC, 7-bit as MBS and 3-bit in LSB, the schematic view is shown in Fig. 5.9(a). The capacitors have been implemented with Metal-Insulator-Metal (MIM) material with double stack that assures higher specific capacitance. They consist of

a metal bottom plate, dielectric, and thin conductive top plate. The stacked MIM comprises two capacitors in parallel, thus yielding twice the capacitance for the same area. In literature it appears that a damage to the dielectric layer has no impact on MIM capacitor performance. To improve decoupling performance, the MIM is placed on top of n-well connected to a quiet analog supply as shown in Fig. 5.9(b).

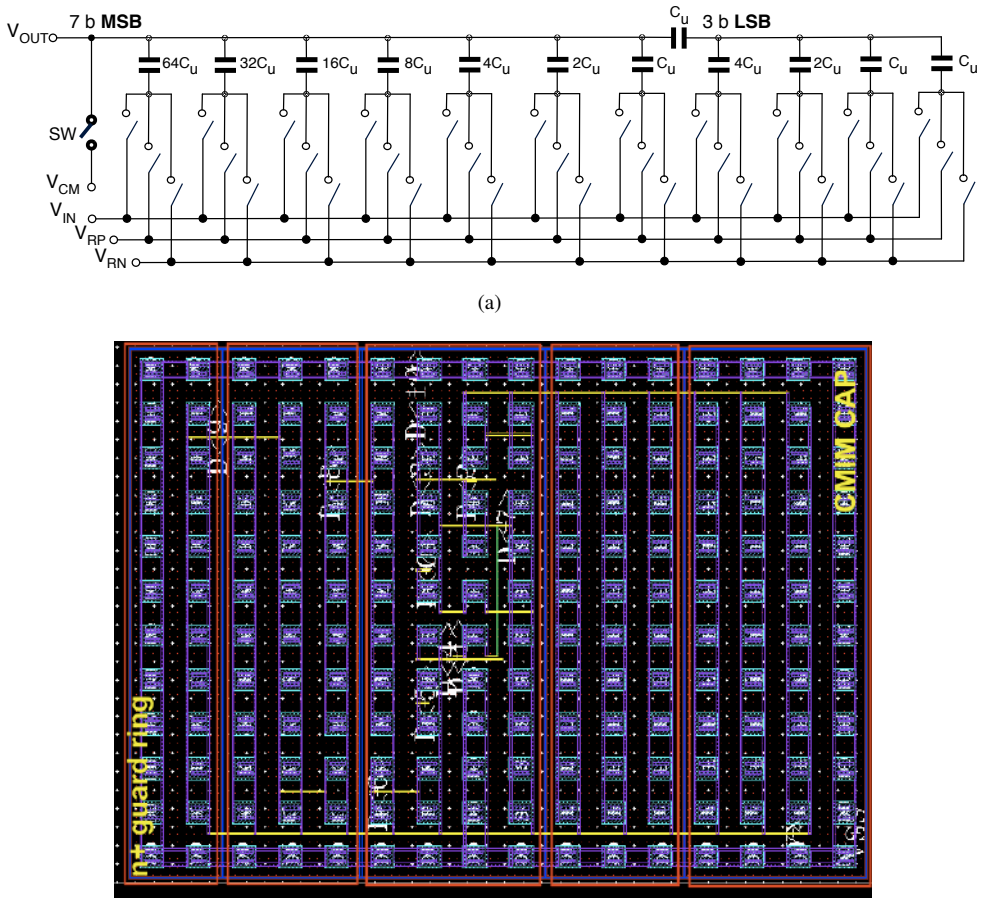


Figure 5.9 (a) Schematic view of split binary-weighted capacitor array DAC (b) Layout view.

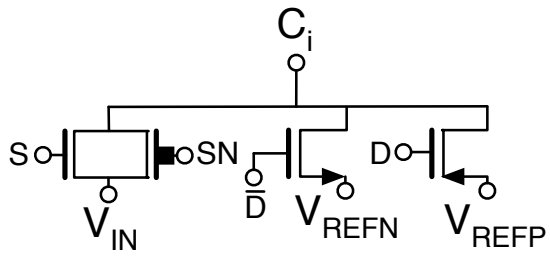
The linearity of ADC is restricted by the linearity of the DAC which is caused by the capacitor mismatch. Therefore, choosing an appropriate value for the unit capacitance is vital. Reducing the unit capacitance value improves the linearity but deteriorates the noise performance at the same time due to KT/C thermal noise. The minimum value of the unit capacitor is limited by several factors including KT/C thermal noise, capacitor matching and the value of the parasitic capacitances. A unit capacitance of $26.7fF$ is chosen in this design. The values of the other capacitors in the DAC array are defined based on the unit capacitance.

5.3.3.1 Switches Implementation

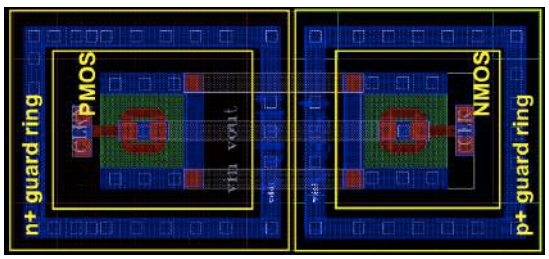
In analog and mixed-signal design the sizes of switches are always the results of a trade-off. Two main phenomena shall be considered:

- The R_{on} of the complementary MOS shall allow enough speed and linearity;
- The clock feed-through shall be kept at minimum.

The first condition pushes for using complementary switches with higher aspect ratio, while the clock feed-through pulls for minimum MOS dimensions. But radiation robustness introduces additional constraints, such as ETL shape so the minimum width is not corresponding to minimum process width of technology because of the ELT shape, for example, in our design Fig. 5.10(b): $\mathrm{W_{NMOS}} = 2.33\mu\mathrm{m}$ with minimum possible $L = 160nm$ (due to enclosed transistor it is not possible to use minimum L of technology) and $\mathrm{W_{pmos}}= 4.62\mu\mathrm{m}$, while the process minimum are $W = 320nm$ &$L = 150nm$, which are well above minimum allowed by the technology. NMOS switches can properly pass a zero logic value while PMOS switches can pass a strong one. On the other hand, CMOS transmission gate combined both features of NMOS and PMOS switch and is capable of properly passing both zero and one. It also benefits from low on-resistance. In this design,



(a)



(b)

Figure 5.10 (a) Schematic view of bottom plate DAC switch block (b) complementary switch layout view.

The positive reference voltage (V_{REFP}) is set to V_{DD}; therefore PMOS switch is used for V_{REFP}. The negative reference voltage (V_{REFN}) is set to ground (GND); thus NMOS switch is employed to ground the bottom plate as V_{REFN}. Since V_{in} varies from 0 to 1.8V at full scale, CMOS TG is chosen for V_{in}. Fig. 5.10(a) shows the schematic views of bottom plate switch. The leakage current contribution of the top plate switch is significant in this low speed design since most of the time this switch is off and it only turns on during the sampling phase. The leakage current of the top plate switch

adversely affect the linearity of the DAC and consequently the linearity of ADC. In order to alleviate this problem, a stack of NMOS switches are used in series; this top plate switch block is depicted in Fig. 5.11(b) and Fig. 5.11(c) are presented its layout view.

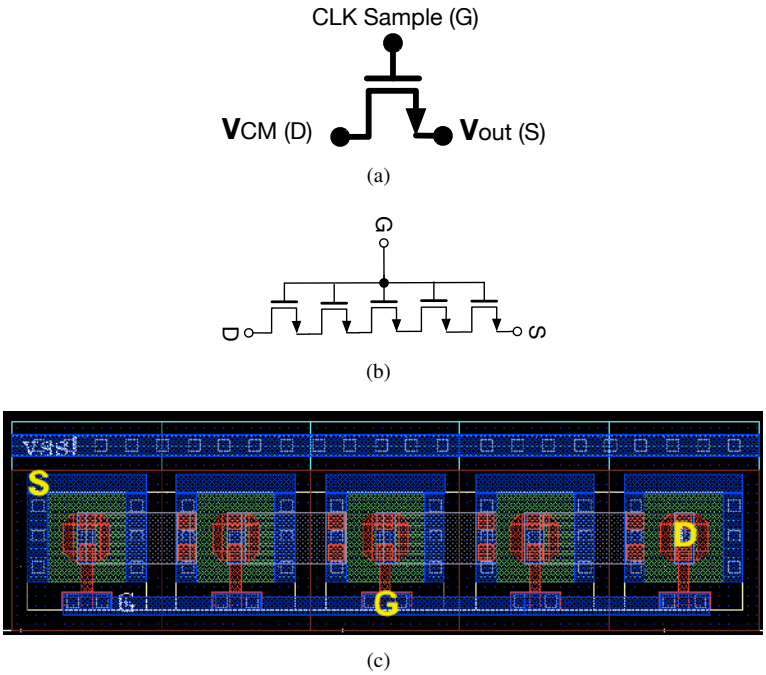


Figure 5.11 (a) Top plate switch symbol (b) schematic view of top plate switch block (c) top plate switch layout view.

5.3.4 Comparator

The comparator is an essential part in the SAR ADC to perform the binary search algorithm. It has to discriminate voltage values lower than one LSB which is $V_{LSB} = {}^{1}/_{2^N}$, in a N-bit ADC. In addition, since it is usually the most power-hungry part of the ADC, a power-efficient solution has to be found during the design. In this work, the comparator is composed a single stage preamplifier and a dynamic sense amplifier latch and inverters, as shown in Fig. 5.12. The proposed structure has been chosen for the following main reasons:

- Pre-amplification is required to overcome the offset voltage of the dynamic latch, especially for small input voltage values;
- The kickback noise coming from the dynamic latch and might affecting the capacitive array is reduced due to the presence of the preamplifier.

The single stage preamplifier provide a DC gain of $20dB$ and a biasing current equal to $100\mu A$ ensures to achieving a large enough bandwidth for the comparison operation.

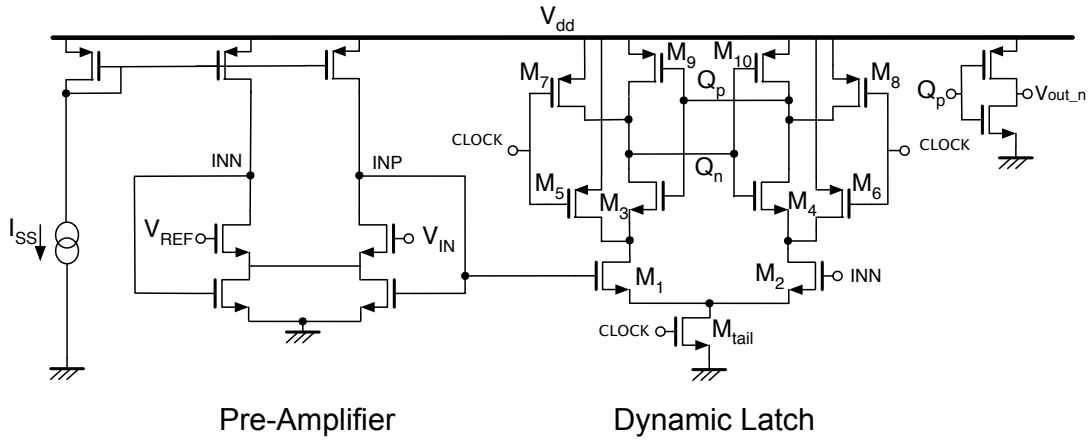


Figure 5.12 Schematic view of voltage comparator.

5.3.4.1 Dynamic Sense Amplifier Latch

The standard dynamic sense amplifier latch [25] shown in Fig. 5.12 has been chosen to reduce the power consumption. When clock signal is low, in reset phase, the reset transistors are switched on and charge the output nodes as well as drain nodes of the input transistors to supply voltage. Current source transistor (M_{tail}) is off, thus, no current flows through the circuit during the reset phase. When clock signal turns to high, reset transistors are disabled and the tail transistor is turned on. The inverters of the cross coupled circuitry inside the latch receive different amount of current depending on the input voltage and start to regenerate the comparator's output. In other words, the drain voltage of each input transistors (M_1, M_2) start to discharge from V_{DD} to ground with different rates depending on their input voltage. Once the drain voltage of either of the transistors drops below $V_{DD} - V_{th}$, NMOS transistor of the inverter is turned on and output node starts to discharge and positive feedback is activated. Once the output node reaches $V_{DD} - |V_{th}|$ the PMOS transistor of the other inverter is turned on. Consequently, the output voltage is regenerated and after regeneration phase one of the outputs is 1 while the other is 0.
Voltage comparator is the only analog block of a SAR ADC. As described in the section 4.4.2, in the radiation environment, TID effects, causes variations in transistors parameters, i.e. increase of parasitic currents, increase or decrease of threshold voltages, and decrease of transconductance, g_m. The latter consequences could have a strong impact on analog circuits performance, since the accuracy of analog functions depends on transconductance and output resistance of transistors, thus a careful layout design of the voltage comparator has been implemented as shown in Fig. 5.13. Besides the countermeasures against radiations, which forced to apply RHBD layout level techniques, we followed conventional rule-of-thumbs for mixed-signal layout as well:

- Separated analog and digital supplies;
- Supply and ground pad/pin placed side-by-side;
- Inter-digitated device layout [26], to improve matching performance between transistors with common node;

- $V_{in}, V_{REFP}, V_{REFN}$ traces implemented with multiple metal layers to minimize series resistance.

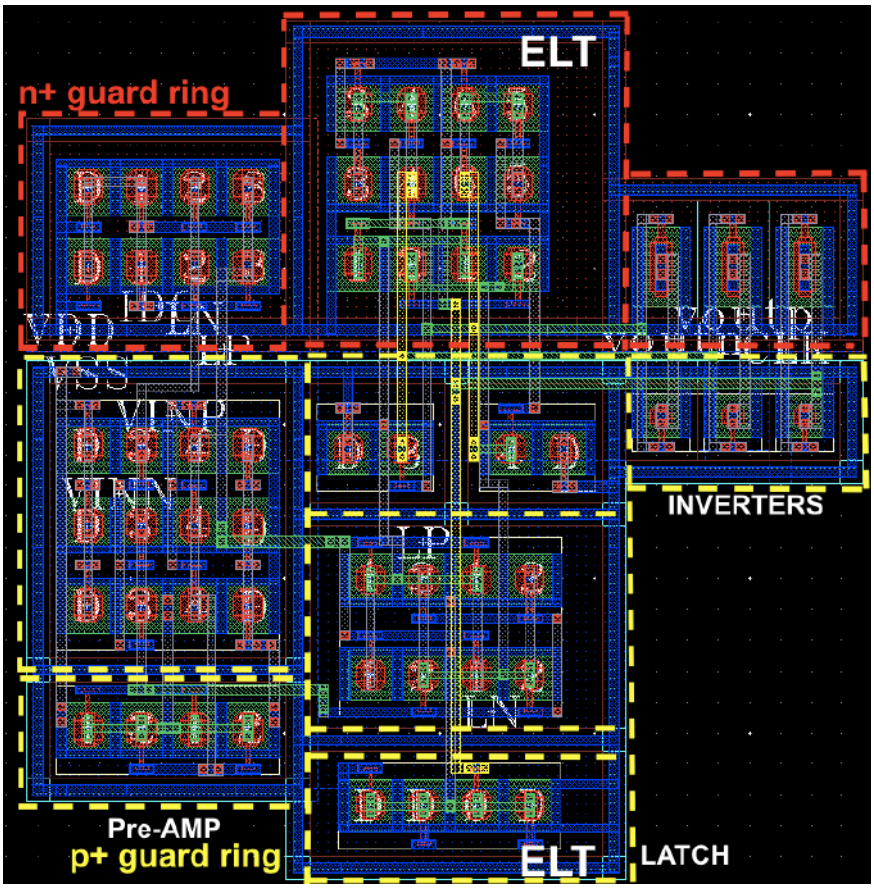


Figure 5.13 Layout view of voltage comparator.

To protect against TID effects, all the NMOS and PMOS have been implemented based on edgeless transistors (ELT shape). The use of guard rings around transistors of the same type biased at different voltages reduces inter-device leakage as well as provide the immunity to single event latch-up (SEL) effect.

5.4 Post-layout Simulation Results

The ADC has been fabricated in a 0.15-μm RF CMOS process 1.8V technology by LFoundry (LF15A PDK). The prototype active area is 212×285 μm^2. Fig. 5.14 depicts the chip microphotograph and the main circuit blocks have been highlighted. The large area occupied by the capacitor DAC array is due to comply with MIM clearance spacing design rules of the used technology. Obviously the SAR

logic layout occupied large area, due to use of ELTs and guard rings, which provide a higher level of radiation tolerance at the expense of a larger silicon area.

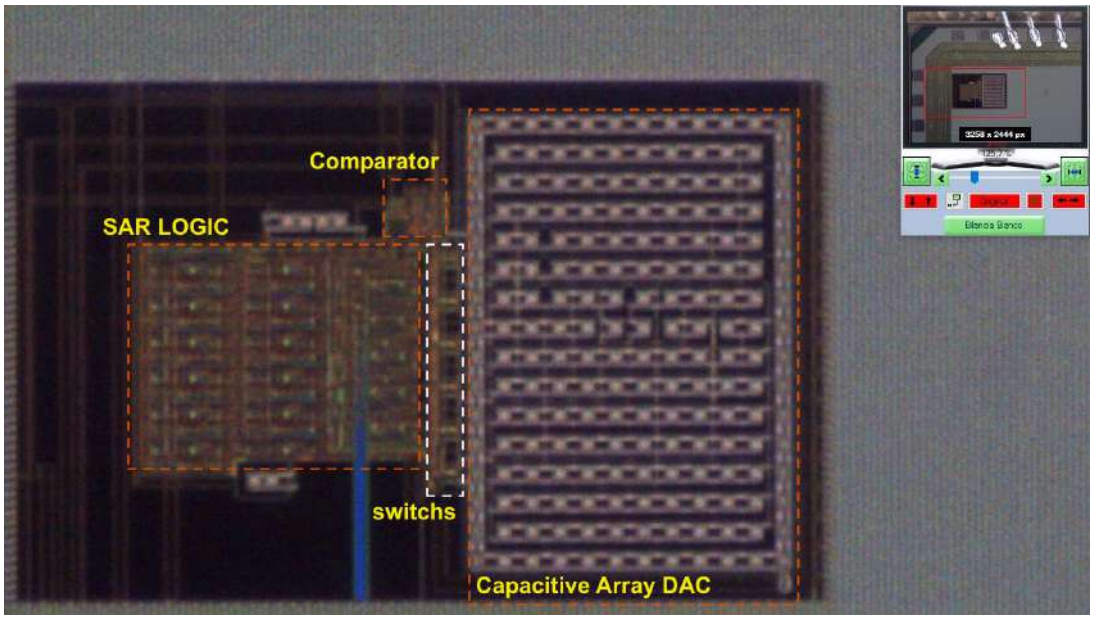


Figure 5.14 10-bit SAR ADC RHBD chip microphotograph.

5.4.1 Dynamic Performance Evaluation

The ADC has been verified at a post-layout *noise-tran* extracted view level, Fig. 5.15 shows the post-layout simulated output spectrum for an input frequency f_{in} =1.0579 KHz @FS (0.9 V_p of sinusoid wave) and $CLK = 1MHz$ and 1024 FFT point. The achieved signal to noise and distortion ratio ($SNDR$) is 59.1dB, that results in an effective number of bit ($ENOB$) equal to 9.6 $bits$. The spurious free dynamic range ($SFDR$) is limited by a tone at 32KHz with amplitude 77.2dB. The tone amplitude is -3dB below the specification so it does not introduce an issue.

5.4.2 Power Consumption Measurement

Fig. 5.16 shows the post-layout simulated ADC power breakdown. The total power consumption (@f_{CLK}=1MHz and V_{supply}=1.8V) is 1.23 mW. Main contribution to this are the digital logic (49.9%) and voltage comparator (46%). The rest are consumed by the SAR ADC V_{REFP} (4%) and V_{CM}.

Table 5.1, summarizes the 10-bit SAR ADC RHBD performances. The figure of merit has been calculated based on,

$$FoM = \frac{P_{Tot}}{2^{ENOB} \times 2.f_{CLK}} \text{ [27].} \tag{5.2}$$

In this design the SNR, the clock frequency and the power consumption are 59.1dB, 1MHz and 1.23mW, respectively. Thus the resulting FoM is 792 fj/conv.-step.

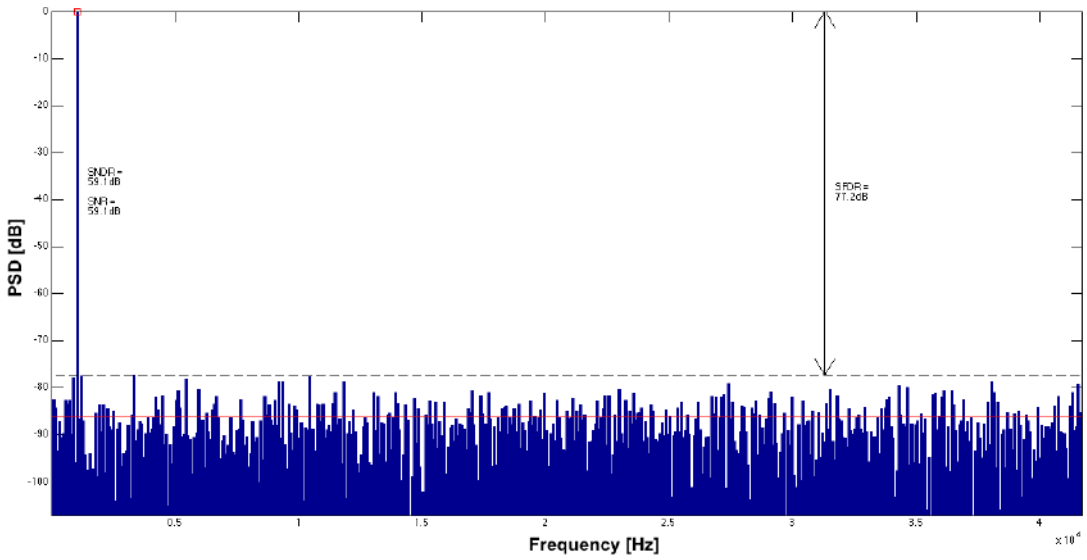


Figure 5.15 Post-layout simulated output spectrum of @FS $f_{in} = 1.0579KHz$ and $f_{CLK} = 1MHz$ and 1024 FFT point.

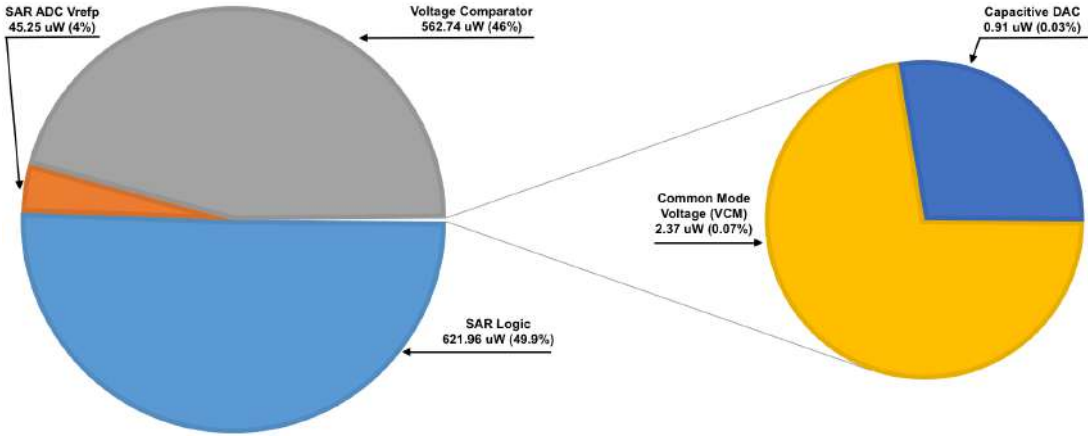


Figure 5.16 Post-layout simulated RHBD SAR ADC power breakdown.

5.5 Conclusions

In this work, the design and analysis of a 10-bit SAR ADC for the radiation environments in a $0.15 - \mu m$ commercial RF CMOS technology has been demonstrated. Circuits designed with the proposed approaches are more tolerant to both total ionizing dose (TID) and to single event effects (SEEs). The main drawback of the techniques for radiation hardening by design is the increase of silicon area, compared with a conventional design. The most area-hungry block for a SAR ADC

Table 5.1 RHBD SAR ADC performance summary.

Parameter	Value	Unit
Technology	0.15	μm
Resolution	10	$bits$
ENOB	9.6	$bits$
Supply Voltage	1.8	V
SNDR (f_{in}=1.057 KHz @FS)	59.1	dB
SFDR	77.2	dB
CLK Frequency	1	MHz
Total Power	1.23	mW
FoM	792	$fj/conv. - step$
Chip Active Area	212 $\times$ 285	μm^2

RHBD is usually the capacitive DAC array and the SAR logic implemented with edgeless transistors and the dual guard-rings (isolation techniques). The effects due to the interaction between radiation and mixed-signal analog-digital circuits have been studied. The design also emphasizes some circuit and layout design techniques developed to avoid or to mitigate radiation effects. It is important to remark that design solutions to improve radiation hardness lead to an increase of the IC area. Nevertheless, they should be adopted when robustness in radiation environment is an important parameter. In addition, RHBD techniques in comparison with other approaches (RHBP or RHBS) can be applied to different commercial fabrication processes in order to increase the overall radiation hardening. A test chip has been fabricated in the 0.15-μm RF CMOS process from LFoundry (LF15A PDK) with the goal of evaluating different TID and SEEs mitigation techniques.

REFERENCES

1. P.-S. Y. Gary K. Maki, "Radiation Tolerant Ultra Low Power CMOS Microelectronics: Technology Development Status", *NASA Earth Science Technology Conference*, (2003).
2. K. L. J. G. C. P. Ken Li, Mike Xapsos and R. F. Stone, "Single Event Effect and Total Ionizing Dose Testing of CULPRiT Reed Solomon Encoders", (2004).
3. M. Xapsos, "Technology Readiness Overview: CMOS Ultra-Low Power Radiation Tolerant (CULPRiT) Integrated Circuits", (2004).
4. R. Lacoe, "CMOS scaling, design principles and hardening-by-design methodologies", *IEEE Nuclear and Space Radiation Effects Conference*, Short Course Notebook
5. D. M. F. R. D. Schrimpf, *Radiation Effects and Soft Errors in Integrated Circuits and Electronic Devices* (World Scientific, 2004), Chap. Hardness Assurance for Commercial Microelectronic.
6. C. Calligaro, A. Arbat, Y. Roizin, D. Nahmad, "A 15 Mrad(Si) 512Kbit Rad-Hard SRAM in a standard 0.18 ?m CMOS technology", *Proceedings of RADECS 2012*, Sep. 2012.
7. C. Calligaro, et al., "Radiation-hardened techniques for CMOS flash ADC", *Proceedings of ICECS 2014*, Marseille (pp. 1-4).
8. U. Gatti, C. Calligaro, "A Family of Rad-Hard ADC with Flash Architecture", *Radiation and Its Effects on Components and Systems (RADECS), 2015 15th European Conference on*, 04 January 2016.
9. U. Gatti, C. Calligaro, E. Pikhay, Y. Roizin, "Radiation-hardening methodologies for flash ADC", *Analog Integrated Circuits and Signal Processing*, May 2016, Volume 87, Issue 2, pp 141-154.
10. N. F. Haddad, et al., "Incremental enhancement to SEU hardened 90 nm CMOS memory cell", *IEEE Transactions on Nuclear Science*, 58(3), 975-980, 2011.
11. L. Clark, et al., "Optimizing radiation hard by design SRAM cells", *IEEE Transactions on Nuclear Science*, 54(6), 2028-2036, 2007.
12. US Department of State, Code of Federal Regulations Title 22 Foreign Relations, Part 121 The United Stated Munitions List, 121.8 End-items, components, accessories, attachments, parts, firmware, software and systems, National Archive and Records Admin., Rev. April 1, 1999.
13. D. G. Millward, D. J. Strobel, "The effectiveness of Rad-Pak ICs for space-radiation hardening", *Proceedings of electronic components and technology conference*, pp. 913-916, 1990.
14. T. Bion, J. Bourrieau, "A model for proton-induced SEU", *IEEE Transactions on Nuclear Science*, 36(6), 2281-2286, 1989.
15. G. Anelli, et al., "Radiation tolerant VLSI circuits in standard deep sub-micron CMOS technologies for the LHC experiments: Practical design aspects", *IEEE Transactions on Nuclear Science*, 46(6), 1690-1696, 1999.
16. PE. Dodd, MR. Shaneyfelt, JR. Schwank, JA. Felix, "Current and future challenges in radiation effects on CMOS electronics", *EEE Trans Nucl Sci* 57(4),1747-1763, 2010.
17. V. Agarwal, SD. Birkar, "Comparison of gamma radiation performance of a range of CMOS A/D converters under biased conditions", *IEEE Trans Nucl Sci*, 52(6):3059-3067, 2005.
18. L. Ratti, L. Gaioni, M. Manghisoni, et al., "Investigating degradation mechanisms in 130nm and 90 nm commercial CMOS technologies under extreme radiation conditions", *IEEE Trans Nucl Sci*, 55(4):1992-2000
19. MR. Shaneyfelt, DM. Fleetwood, PS. Winokur, et. al., "Effects of device scaling and geometry on MOS radiation hardness assurance", *IEEE Trans Nucl Sci*, 40(6):1678-1685, 1993.
20. P. Leroux, S. Lens, R. Voorspoels, et. al., "Design and assessment of a circuit and layout level radiation hardened CMOS VCSEL driver", *IEEE Trans Nucl Sci*, 54(4):1055-1060, 2007.

21. WJ. Snoeys, TAP. Gutierrez, G. Anelli, “A new NMOS layout structure for radiation tolerance”, *IEEE Trans Nucl Sci*, 49(4):1829-1833, 2002.

22. M. Benigni, V. Liberali, A. Stabile, and C. Calligaro, “Design of rad-hard SRAM cells: A comparative study”, *in Proc. IEEE Int. Conf. on Microelectronics (MIEL)*, NiÍ, Serbia, May 2010, pp. 279-282.

23. ACTEL. “SmartFusion cSoC Handbook: datasheet”, 2012.

24. T.O. Anderson, “Optimum Control Logic for Successive Approximation Analog-to-Digital Converters”, *Computer Design*, vol. 11, no. 7, pp. 81-86, 1972.

25. T. Kobayashi, K. Nogami, T. Shirotori and Y. Fujimoto, “A current-controlled latch sense amplifier and a static power-saving input buffer for low-power architecture”, *Solid-State Circuits, IEEE Journal*, vol.28, no.4, pp.523-527, Apr. 1993.

26. Analog Integrated Circuits Course, *Layout of Analog CMOS Integrated Circuit - IMS*. [Online]. Available: *http://ims.unipv.it/Courses/download/AIC/Layout02.pdf*, 2006.

27. F. Maloberti: "Data Converters"; Springer-Verlag, 2007, ISBN 9780387324852.

CHAPTER 6

CONCLUSIONS

This chapter concludes the thesis. A summary that briefly introduces the motivation and results of the thesis is presented. Following the summary section the author current publications has been listed.

6.1 Summary

This thesis has focused on designing and implementation of analog to digital converters for sensor interfaces and the space application where the radiation effects is the main issue. An energy-efficient high-resolution and high accuracy ADC is usually the key building block in many sensor SoC applications, and a $\Sigma\Delta$-type ADC is usually the best candidate. The first part of this thesis, explored new architectures and circuits techniques for the time-interleaved incremental ADC which recycle the incremental blocks to perform extended counting in a form of SAR ADC.
Chapter 2 briefly reviews the fundamental of analog to digital conversion and providing the static and dynamic performance metrics of ADC definitions, then presents a short overview on the most common ADC architectures and provide an analysis on the evolution of these topologies in the last decades. A summary of the state-of-the-art of incremental converters with extended-range techniques has provided. As a result of this study, incremental analog-to-digital converters (IADCs) are appeared to be the best choice in low-frequency high-resolution sensor interfaces. Using hardware-sharing, hybrid schemes of an IADC and a nyquist-rate ADC can further improve the energy efficiency and reduce the area of an integrated ADC on a sensor SoC.

In chapter 3, the battery monitor system was presented. An 8-channel first order time-interleaved incremental ADC as coarse conversion and a SAR ADC approach was used to extend the dynamic range as fine conversion. The use of the same ADC for all the channels in the fine step relaxes the matching requirements in the time-interleaved structure, and allows a high-resolution converter with very simple analog blocks. The design has a relatively simple and innovative high voltage track&hold with low-voltage logic control which interfaces the analog to digital converter with the Li-Ion battery stack, achieving high linearity and accuracy while low cost. The battery monitor IC has a resolution of about $0.2mV$, consuming $3.64mW$ with an area of $1300 \times 650\mu m^2$. All channels are measured in $720\mu s$. The measured residual offset is $642.5\mu V$. The dynamic input range of the system can be as large as 33.6V, and the achieved figure of merit (FoM_S) is 129.5dB.

The second part of this thesis, has explained the affects of high energy radiation on silicon, electronic devices and ICs. The main radiational environment has introduced and general techniques to harden integrated circuits from these effects has studied. Radiation environments such as those found in space missions, satellites, advanced weaponry, instrumentation for nuclear power plants and high energy physics applications can alter the behavior of electronic devices and integrated circuit. The reason for that is the radiation induced particles interact with the materials of the devices (especially silicon) changing their characteristics. Therefore one should take special care when designing electronic circuits for radiation environments to avoid the damages caused by radiation effects. Such protection can be provided by using dedicated radiation tolerant manufacture processes (RHBP). However these radiation tolerant processes are more expensive and less developed than state of art commercial technologies. Furthermore, the scaling down of the technology improved the radiation tolerance of the circuits due to the decreasing of the gate oxide thickness. This had motivated the study of radiation tolerant design and layout techniques (RHBD) to be used in commercial technologies especially designing and implementation of ADC for the space application.
Chapter 4, provides background information on the radiation environment and an overview on the radiation effects in electric circuits has presented. The most common errors originated by radiation in the integrated circuit and CMOS commercial technology have reviewed.
In chapter 5, the radiation hardening techniques by design (RHBD) has reviewed. To evaluate the radiation induced effects in commercially fabricated ICs a test chip has been fabricated in the 0.15-μm RF CMOS process 1.8V technology by LFoundry (LF15A PDK). A 10-bit conventional SAR ADC with charge redistribution capacitive DAC architecture was chosen, in order not to mix-up possible inaccuracy of the converter itself with the effect of radiations, thus this simple structure and safe performance allowing a better understanding of radiation impacts on mixed analog-digital circuits. The prototype active area is 212$\times$285 μm^2 and consumes $1.23mW$. It operate with a nominal supply voltage of 1.8V. Post-layout noise-transient simulation results show an ENOB equal to 9.6 bits in the band of interest, $[1 - 10]KHz$, at full scale input voltage. The resulted figure of merit is 792 fj/convesrion-step.
Based on the work of this thesis and recent publications, a sigma-delta and incremental ADC architecture constitutes a potentially interesting option for rad-hard ADC topology. The analog part of the circuit should be less immune to radiations effects, because ideally all faults introduced by extra-charges in integrators capacitors are transformed in out-of-band noise by the modulator.

6.2 Author Publications

1. M. Baghbanmanesh; F. Maloberti, “On the design of incremental data converters with extended range”, *Circuits & Systems (LASCAS), 2015 IEEE 6th Latin American Symposium on*, Sep. 2015.

2. M. Baghbanmanesh; F. Maloberti, “Multichannel time interleaved ADC for sensor interfaces”, *2016 12th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME)*, Jul. 2016.