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VERY LOW POWER SUCCESSIVE APPROXIMATION A/D CONVERTER FOR INSTRUMENTATION APPLICATIONS

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TO MARTA

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Introduction

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- Research Goals
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1.1 Motivations

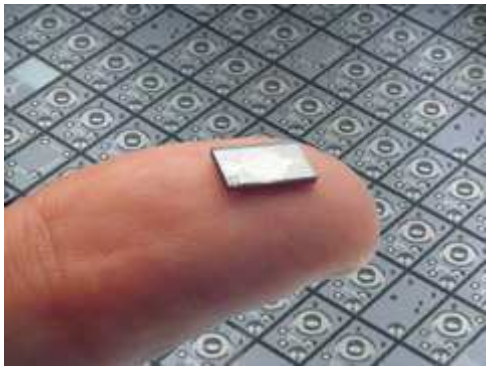
In recent years the medical evolution allows us to get always better results, for example now is possible to understand the causes of some illness and prevent them with particular attention, or also when the illness is already done, it is possible to eliminate every trace and consequence of its passage. Unfortunately this ideal world has not been reached yet. Sometime there are illnesses which are not possible to take care of definitively, and require a continuous control for how much and what medicines are necessary to not worsen the conditions of the patient. To solve completely the effects of this typology of illnesses, unfortunately, is not possible using electronic science but it can help this type of patient for getting better their style of life. For example, people with diabetes have to constantly hold under observation own glucose level in blood and, consequently, to inject the required dosing of insulin to avoid possible dangerous crises.

The Gluco-test used for measuring glucose by introducing the drop of blood token from capillary in the finger.
Source: www.118pescara.it

There are almost 250 million people affected by diabetes worldwide and the number is expected to grow over the next decade due to population growth, ageing and life style. Without proper treatment, diabetes can lead to cardiovascular disease, kidney failure, blindness, nerve damage, and ultimately death. Diabetes is a leading cause of death in most developed countries. These people usually control their glucose level by stinging their own finger and withdrawing a drop of blood. This drop will be insert in a particular machine which can analyze the blood and returns the glucose level found. When the person knows the value then can assume the right dosage of insulin by injection with syringe. Electronic science, in this environment, had designed test machine for analyzing blood always smaller and the required quantity of blood to ensure a correct value is always less. These last technological steps allow to keep under control the critical parameter everywhere, using a little machine with dimension comparable with a normal mobile phone.

Syringe typically adopted by diabetic people for injecting the correct insulin dosage, the shape is studied for children use.
Source: www.bioblog.it

That practice is recommended to do at least 3-4 times at day, near the meals, when the ingestion of food introduces a large variation in the value of the glucose. Naturally, during a day, there are a lot of factor which gives their own contribution to glucose variation and the ideal think to do is a permanent control of glucose level. Recent studies thinks possible to read the glucose without taking blood, but reading the small effects of the glucose variation on interstitial liquid of the skin. The difficult of this technique is that these effects are very little, but the high advance level of electronic micro-sensors used allows to study alternative ways. The other problem is to inject the right dosage of insulin. To solve these problems is now possible to use a micro-infusion pump. The purpose of this micro pump is to release exactly the correct dosage of liquid. It is based on Nanopump realized in MEMS technology.



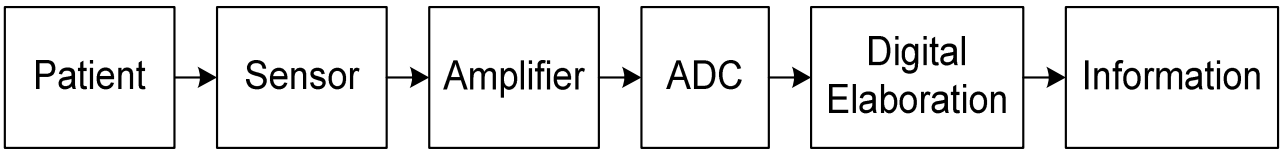
The breakthrough Nanopump, which relies on microfluidic MEMS technology.
Source: www.st.com

With injections, the insulin just sits there... in a little pool. The level of activity directly affects when that insulin goes into bloodstream. If people are just sitting at a desk, it will go into the system more slowly. But if people go for a walk or a run, it will go into the system much more quickly. This makes blood sugars even harder to control with injections. Pumps continuously send a little bit of insulin every few minutes (like a pancreas) so people don't have this inconsistency problem. And it is a different insulin fast-acting, predictable insulin.

The Nanopump in use.
Source: www.diabetescaregroup.info

Naturally the described example of the diabetes is only a little application of how electronics can change in better the life of people. Anyway this example allows to illustrate all the possible applications for electronic research. In fact it requires a system for data acquisition, a system for elaboration of the data, memorize the history of data and apply a possible solution for the problem. Really is not possible to close the loop because of health laws. In fact they require the human intervention for applying the therapy, but in theory it is possible to design an electronic circuit which allows to read the glucose rate in the blood and decide how much insulin inject by micro-infusion pump. Anyway this example can help us to synthesize the main rings of the chains

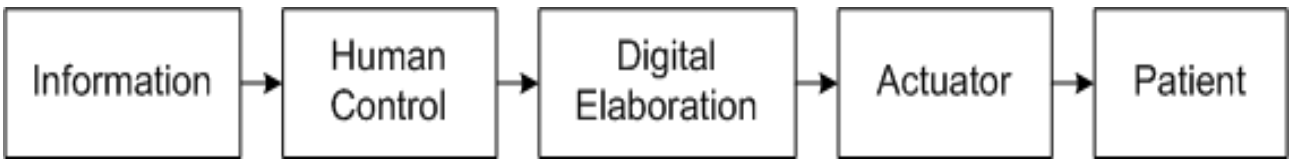
for realizing the entire system. In the following figure the block diagram of the measurement system is done, and the electronic part was detailed better.



Block Diagram for measurements of parameters

Observing this chain is possible to understand how much the electronics is an important part of the entire system. The first block in control the parameters chain is the sensor, this important device has the purpose to react with elements under test (possibly only that one) and to convert the information to electric parameter. For example a micro-strip of opportune sensible paper can increase its electric resistance with contact to the element. Naturally in this case the piece of sensible paper can be used only once. To measure the variation of resistance in this sensor is possible to apply a voltage in the extreme parts and “read” the current which flows in the circuit. Usually the variation of resistance are very little and then also the expected current variation are very little. To read the information, then, it is mandatory to use an amplifier with the purpose to widen the dynamic range of the information signal. This analogical signal is used by an Analog to Digital Converter (ADC) for converting to a number, with opportune approximation. The obtained number is the value of the measured current. The block of digital elaboration knows the transfer function of the sensor and its purpose is to calculate the value of the desired parameter knowing the value of the current. The useful value of the under observation parameter is done by an opportune display which can be read to the human operator.

The second proposed chain is relative to the care application to the patient.



Block Diagram for carrying out the care

In this chain the starting point is the knowing of the value of the parameter under observation. The first block is done by the human control which has the purpose to know how to do and must to apply the desired therapy by a particular device. Then the device has to know how has to do. After

human control by an opportune keyboard, the transmitted information are elaborated digitally. In this case the digital elaboration block knows the transfer function of the actuator and calculates the exact behavior which it has to have for applying the desired care. Then the information which digital block gives to actuator is the exact behavior that the ladder one has to do.
How was written before both the chain are very important for improving the quality of life and electronics has an important role in this environment.
The most important issue which electronics has to solve is make portable devices which can do the same controls and the same therapies. To make a portable devices means to adopt very little circuits, and a very low power circuits which allow to use a little batteries.
This one is the most important challenge that electronics has to solve next years.

1.2 Research goals

The purpose of this work is to realize a very low power Analog to Digital Converter (ADC) for biomedical application. The specs required by this types of application are not very pumped neither as it regards the bandwidth neither as it regards the resolution bit. The research has focused on the design of an ADC based on Successive Approximation Algorithm, with a sampling rate of 100 kS/s and a resolution of 10 bit. The design is oriented to minimize the power consumption, keeping in account the state of the art in ADC design. The main steps of this work are the study of the best architecture which allows to reach the goals, to choice the architecture of each main block which compose the system and, to design all the system with particular care to the power consumption. After the design on silicon of the ADC the work include to design an opportune testing board whit the purpose to characterize the specs of ADC.

1.3 Thesis Organization

The work started with consideration about the ideal study of ADC, which specs are considered for characterizing the system. Then it continues with the choice of architecture and the design of the main block which are present in the system. A design of the entire system, keeping in account the limits of each block and the required specs. Finish the design on silicon of the entire system, the work includes also the test of chip. There a study for knowing how is the best method to understand the real specs of the just realized ADC has been done. The obtained results of these tests on silicon of the ADC conclude the work.

This thesis is divided into 7 chapters:

Ch. 1. Introduction. In this chapter are underlined the main motivation which bring to realize of an ADC with the adopted specs, underlined a possible application;

Ch. 2. Ideal ADC. In this chapter are described the main specs which are related to an ADC, in particular are studied the static and dynamic specs, are been done some consideration about the purpose of this work, and the state of the art used in the type of environment to which this work aim;

Ch. 3. Principle of operation of S.A. A/D converter . In this chapter the main is considered the architecture of the successive approximation algorithm with the study of the issues in implementation. The state of art concludes the chapter.

Ch. 4. Design of each Basic Building Block. In this chapter are explain the main issues in designing, the way to obtain a low power implementation and some innovative solution for improving the power consumption are given.

Ch. 5. Experimental Results. In this chapter the measure done are explain, the main indication to implement the test board and the performance of the test chip are done. The comparison with state of art concludes the chapter.

Ch. 6. Conclusions. In this chapter are reported the conclusion about the main project of the PhD activity.

Ch. 7. Other activities. In this chapter are summarized the other activities done in this PhD period of research.

2

Ideal ADC

- Basic A/D Conversion Concepts
- Specifications
- Operation Issues

2.1 Basic A/D Conversion Concepts

An analog-to-digital converter quantizes an analog signal into a digital code at discrete time points. According to the sampling theorem, the input signal band is limited to half of the sampling frequency to avoid aliasing with the sample rate repeated spectra. The so-called Nyquist rate A/D converters can digitize frequencies up to this frequency. In this chapter the quantization process is explained and parameters describing the performance of an analog-to-digital converter are presented. Considerations relating to the specification of the A/D converter resolution and sample rate as a part of the system design of a radio receiver are covered as well.

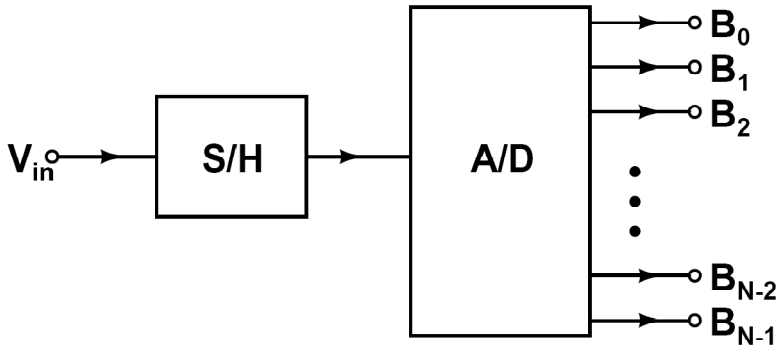


Fig. 2.1: General block diagram of an A/D converter.

An analog-to-digital converter performs the quantization of analog signals into a number of amplitude-discrete levels at discrete time points. A basic block diagram of an A/D converter is shown in Fig. 2.1. A Sample-and-Hold (S/H) amplifier is added to the input to sample the analog input and to hold the signal information at the sampled value during the time needed for the conversion into a digital number. The analog input value V_{in} is converted into an N-bit digital value using the equation:

$$\frac{V_{in}}{V_{ref}} = D_{out} + e_q = \sum_{i=0}^{N-1} B_i \cdot 2^i + e_q. \qquad (2.1)$$

In the equation, V_{ref} represents a reference value, which may be a reference voltage, current or charge. B_{N-1} is the most significant bit (MSB) and *B*0 is the least significant bit (LSB) of the converter. The quantization error e_q represents the difference between the analog input signal V_{in}

divided by R_{ref} and the quantized digital signal D_{out} when a finite number of quantization levels is used.

From equation (2.1) is possible extrapolate the D_{out} value as:

$$D_{out} = \sum_{i=0}^{N-1} B_i \cdot 2^i \tag{2.2}$$

The sampling operation of analog signals introduces a repetition of input signal spectra at the sampling frequency and multiples of the sampling frequency. To avoid aliasing of the spectra, the input bandwidth must be limited to not more than half the sampling frequency (Nyquist criterion). It is essential to understand analog-to-digital converter specifications to get an insight into the design criteria for converters. The DC-specifications for the static linearity are widely known. Dynamic specifications of A/D converters give a better insight into the applicability of a converter in a telecommunications system, where linearity and spectral purity are essential.

The main purpose of A/D is to perform a conversion of the real world, which is a continuous amplitude, continuous time analog signal into digital codes, which are discrete time, discrete amplitude electrical signals. An A/D converter takes a range of possible analog values, which are real numbers, and divides it into smaller sub ranges. Usually the sub ranges have the same size and they are referred to as steps (an exception are ADC for codes which have logarithmic scaled steps). The analog to digital conversion is a process that involves two phases: the sampling of the analog input signal applied and the quantization, which means compare it to a reference voltages and translate this comparison into a binary representation.

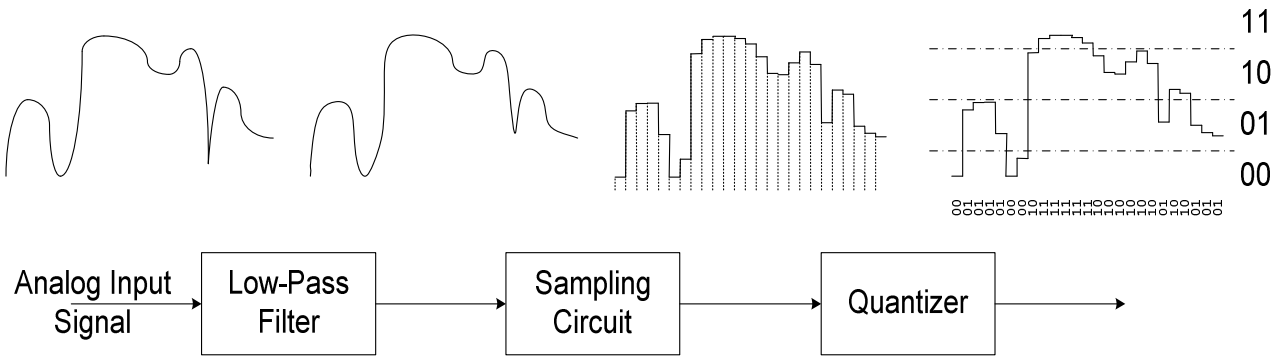


Fig. 2.2: Block Diagram of an A/D Converter with Low-Pass Anti-Aliasing filter.

As shown in Fig. 2.2, the input signal first goes through a low pass filter, which has the purposes to limit the input bandwidth and to remove the unwanted out-of-band noise, avoiding its

aliasing in the actual signal band during the sampling phase. After the filter, the signal is sampled, which means that the continuous time signal is represented as a succession of a samples which are kept for a fixed time called “sampling time”. Next step is the quantization, which elaborates the sampled signal approximating its value to the nearest fixed reference voltage. Depending on the resolution of the converter and for a given input swing, the quantization step (the different between two consecutively reference voltages) is wider or narrower. In the done example in Fig. 2.2, a two bits resolution A/D converter was supposed, and then it include four quantization steps.

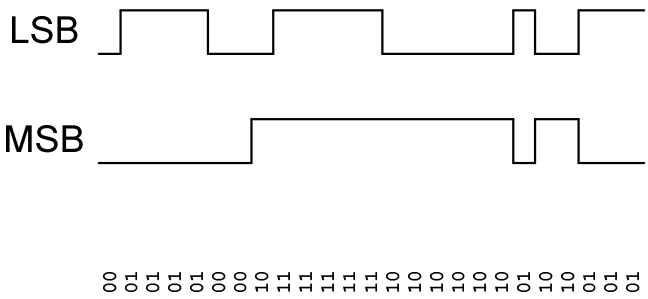


Fig. 2.3: Two Bits Digital Output Signals.

The final phase of elaboration has the purpose to do the correct digital representation, of the quantized signal, in output, as shown in Fig. 2.3.

2.2 Specifications

To define a data converter is important to know its typology. The algorithm used for obtaining the conversion allows to know this propriety. The main types of data converter are two: the Nyquist-rate and Oversampling-rate conversion. These two type of conversion defines two defined modes for obtaining the result of conversion: the most important difference between the two methods consist of the occupation bandwidth of the input signal respect of the available in according with the Nyquist criterion. The first type, in fact, search to reduce the sampling frequency (f_S) and then the occupation bandwidth is almost the theory value, while the second type of converter wants to use the advantages of oversampling allows to have in order of noise. So, it is defined the ratio between the Nyquist limit ($f_s/2$) and the signal bandwidth (f_B), and it is called oversampling ratio (OSR).

$$OSR = \frac{f_S}{2 \cdot f_B} \tag{2.3}$$

Converters with a large OSR are called oversampling converter, opposite to Nyquist-rate converters. The ladder one type are called the ones which have no or have a very small OSR, typically less than 8, to allow, anyway, the use of an opportune filter.

Figg. 2.4 and 2.5 show the difference between Nyquist-rate and Oversampling-rate converters. In the former one the transition region of the anti-aliasing filter is limited (leading to difficult specifications) and also a large fraction of the total quantization noise power is in the signal band.

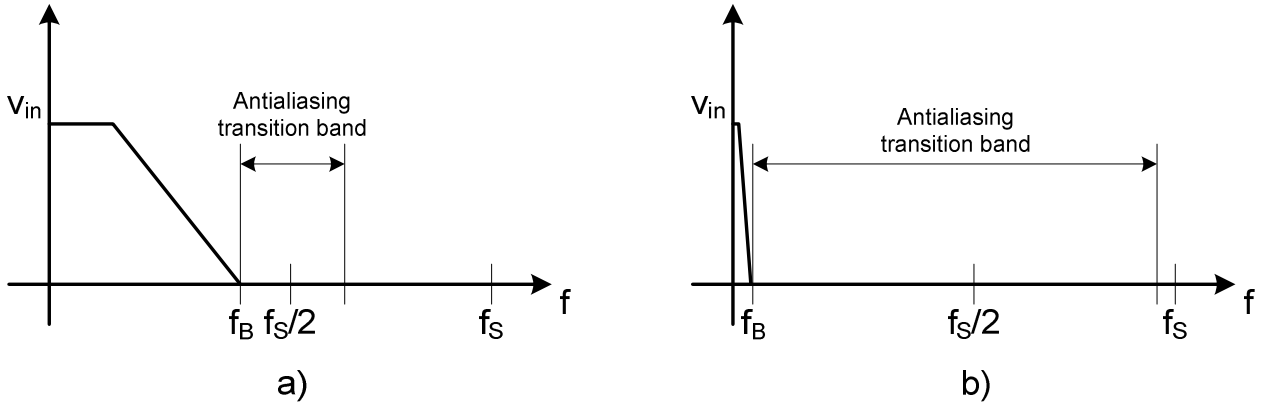


Fig. 2.4: Bandwidth in Nyquist-rate (a) and Oversamplig-rate (b) Converters.

In contrast, the latter one case has a large anti-aliasing transition region and only a small fraction of the total quantization noise occurs in the signal band. The sampling frequency for oversampling is, obviously, much larger than its Nyquist-rate limit, in some cases the OSR can be some hundreds.

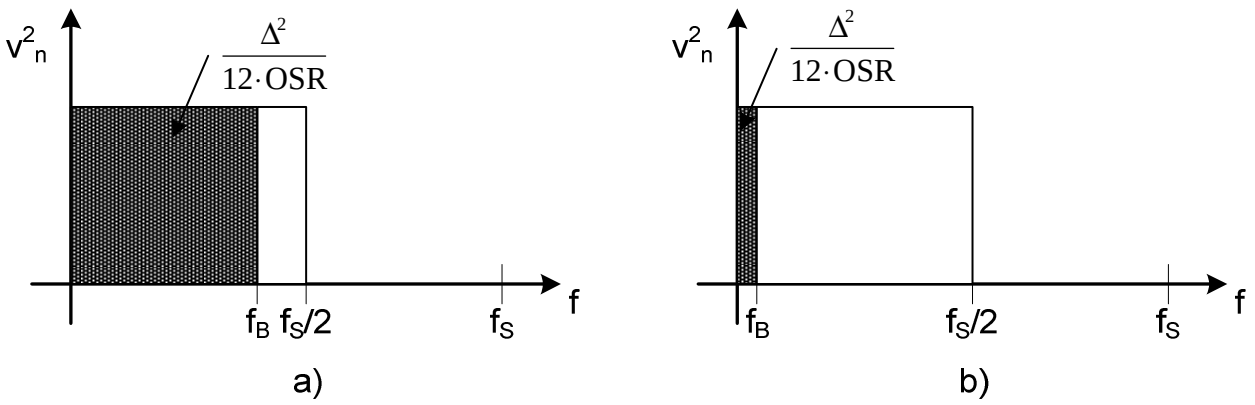


Fig. 2.5: Noise in Nyquist-rate (a) and Oversamplig-rate (b) Converters.

• Another specification which define a data converter is the Type of Analog Signals. In fact the analog input or output of a data converter can be fully-differential, pseudo-differential or single-ended. For maximum noise rejection, use fully-differential inputs. Fig. 2.6 shows an example of a fully-differential ADC Tracking and Hold (T/H) input structure. During track mode, $C^{(+)}_{sample}$ charges to $[V_{IN}^{(+)} - V_{DD}/2]$ and $C^{(-)}_{sample}$ charges to $[V_{IN}^{(-)} - V_{DD}/2]$.

When the T/H switches to hold mode, $C^{(+)}_{sample}$ and $C^{(-)}_{sample}$ connect together in series, such that the voltage sample presented to the ADC is the difference of $V_{IN}^{(+)}$ and $V_{IN}^{(-)}$. The differential architecture in conjunction with acceptable input bandwidth in the T/H are key ingredients for good dynamic common-mode rejection.

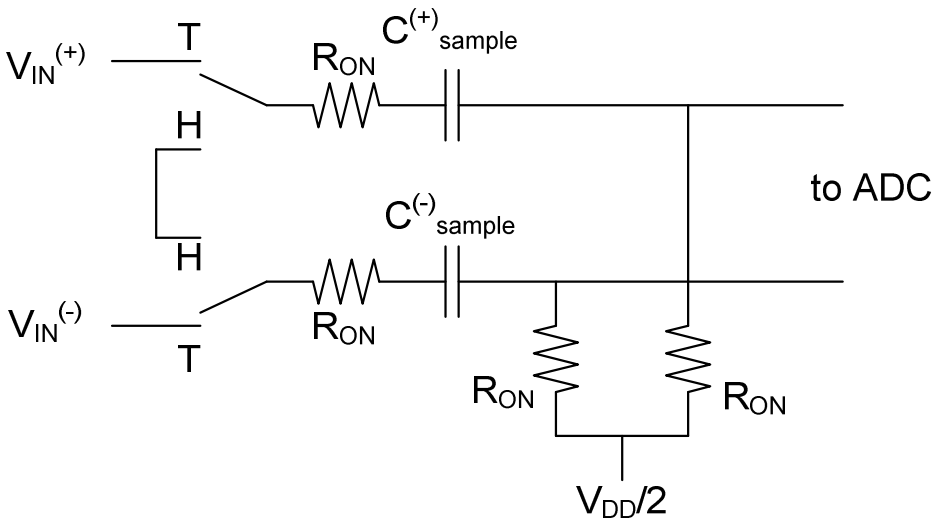


Fig. 2.6: Fully Differential T/H stage.

In noisy environments, it is possible that coupled-noise could cause the differential inputs to exceed the ADC's allowable input voltage range. For best performance, reduce the input signal range to ensure that the ADC input range is not exceeded. Another key advantage of differential signals is the increased dynamic range. With power supplies dropping from 1.8V to 1.2V, design engineers are looking for ways to achieve greater input dynamic range. In theory, given the same voltage range for single-ended and fully-differential inputs, the fully-differential inputs will have double the dynamic range (Fig. 2.7 a). This is because the two differential inputs can be 180° out of phase, as shown in Fig 2.7 b.

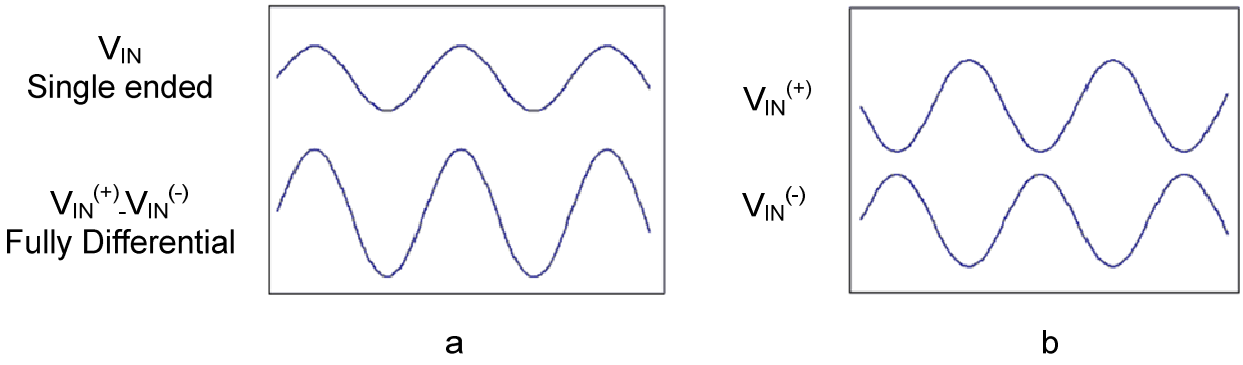


Fig. 2.7: Single-ended vs. fully-differential (a), $V_{IN}^{(+)}$ and $V_{IN}^{(-)}$ 180° out of phase (b).

The Pseudo-differential inputs are similar to fully-differential inputs in that they separate signal ground from the ADC ground, allowing DC common-mode voltages to be canceled (unlike single-ended inputs). However, unlike fully-differential inputs, they have little effect on dynamic common-mode noise. In Fig. 2.8, sampling only occurs on the input $V_{IN}^{(+)}$ signal. The signal common, $V_{IN}^{(-)}$, is not sampled. During the 'TRACK' mode, the sampling capacitor charges through the series resistor R_{ON}. During the 'HOLD' mode, the sampling capacitor connects to $V_{IN}^{(-)}$ and an inverted input signal is presented to the ADC for conversion. Because sampling only occurs on the $V_{IN}^{(+)}$ input, $V_{IN}^{(-)}$ must remain within ±0.1LSB during the conversion for optimal performance.

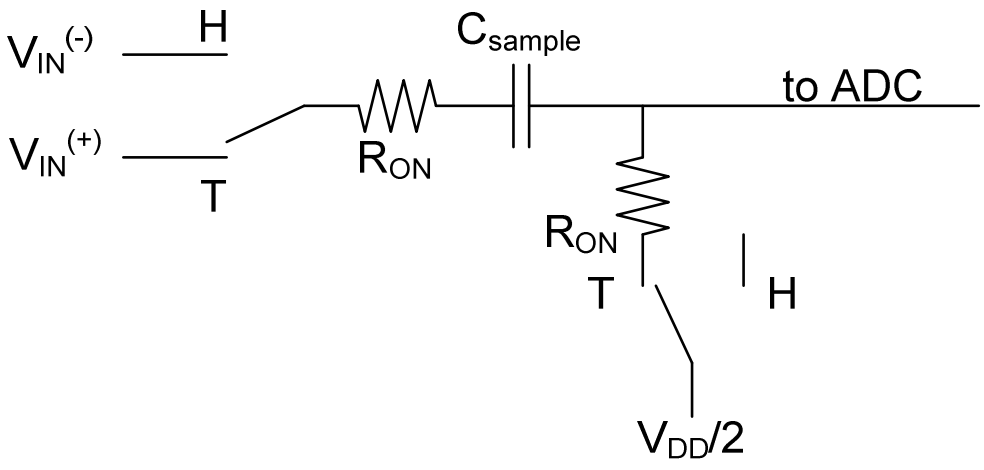


Fig. 2.8: Pseudo Differential T/H stage.

An alternate method of implementing pseudo-differential inputs samples $V_{IN}^{(+)}$ and $V_{IN}^{(-)}$ sequentially, and the difference of the two voltages is provided as the conversion result. For dynamic signals, the phase of $V_{IN}^{(+)}$ and $V_{IN}^{(-)}$ will not match during sampling resulting in distortion. Select an ADC with fully-differential inputs for dynamic time-varying signals. A typical

application for pseudo-differential inputs is measuring sensors that are biased to an arbitrary DC level.

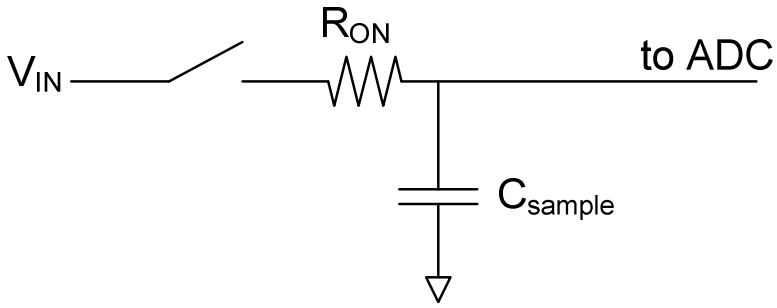


Fig. 2.9: Single Ended T/H stage.

Single-ended inputs are generally sufficient for most applications. In single-ended applications, all signals are referenced to a common ground at the ADC. Each channel uses a single input pin. The analog ground pin is shared between all inputs for multi-channel systems. DC offset and/or noise in the signal path will decrease the dynamic range of the input signal. Single-ended inputs are ideal if the signal source and ADC are close to each other (i.e., on the same board so that signal traces can be kept as short as possible). Single-ended inputs are more susceptible to coupled-noise and DC offsets. However, signal conditioning circuitry can reduce these effects. Fig. 2.9 shows a simplified example of a track-and-hold (T/H) input of a single-ended ADC. The sampling capacitor is switched to the input pin through a series resistance during the 'TRACK' mode. The switch opens when the T/H enters 'HOLD' mode (during the actual conversion process) and the ADC converts the voltage across the sampling capacitor into a digital code.

- Resolution (or quantization step): it is the number of bits which are used into an ADC to represent its analog input at the output. The resolution, together with the reference voltage, determines the minimum detectable voltage.
- Dynamic range: it is the ratio between the largest signal level the converter can handle and the noise level, expressed in dB. The dynamic range determines the maximum SNR.

Other specifications are describing of the digital settings. These features are specified by a given set of parameters. These ensure the proper interfacing with internal or external circuits and are useful for the synchronization of logic signals within the data converter. The specifications given below are the ones most commonly used in commercial data sheets.

- Logic levels: the logic levels are a good definition of non overlapping ranges in amplitude which are used to represent the logic state. In particular, to keep in accont

that the output of the ADC is realized by a bus of N wire which can change their voltage. If the voltage at each wire is in the first range, it corresponds to level logic 0 or 1 if the voltage is in the other one. Usually are widely used the definition of the logic standard family (like the CMOS or TTL).

- Encode or clock rate: is the range in which the frequency of the clock can ensure the correct operation of the device, and are ensured the performances of the specifications. This range can be very large, some decade or more. Usually the best point to operate with data converter is when it is used at the maximum clock rate or a little bit less (about 25%) for guarantying the specification.
- Clock timing: it specifies the features of the clock. When the clock is not generated on chip, but supply from external, it is better to regenerate its inside the integrated circuit by edge-triggered flip-flops. That circuit has the purpose to ensure a correct features of the clock, respect to the better condition for chip. The duty cycle of the clock can be chosen depending of the internal circuit requirements. A 50% duty cycle is normally the designed for external supply.
- Clock Source: the main purpose of the clock signal injected to the chip, usually, is the one to do the timing operation of the converter. To generate an external clock requires a particular attention about the jitter, and is possible to consider the use of an internal circuit which generate the clock using a differential input sine wave. The main advantage of this choice is that the high precision sine wave can be generated by an external crystal clock oscillator (with or without external filters). This ensures an accurate zero-crossing times. Internal amplifiers, under saturation, are widely used to square the input sine wave and thus generate the required internal clock.
- Sleep Mode: this type of operation is included in the commercial chip, because a common issue is that the converter has not to work continually, but must come back in working mode in very fast time. So, a sleep mode allows to use a different power-down which has the purpose to turn off the main bias currents and minimizes the power consumption. An opportune digital input pin allows to activate the power-down mode. The power-up and the power-down activation times depend on the time constant associated with the sleep circuit, but usually are much faster than the time takes for turn on the chip completely.

Static Specifications

The static behavior of a data converter is done by the input-output transfer characteristic. Ideally the input-output characteristic is represented by a staircase with uniform steps over the entire dynamic range.

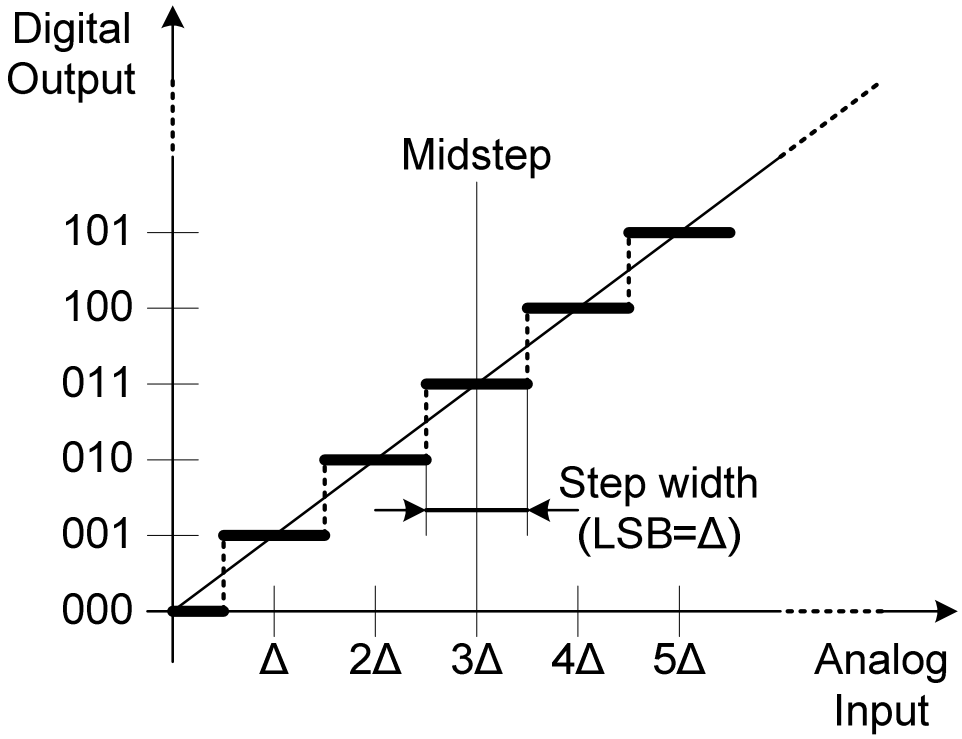


Fig. 2.10: Ideal Input-Output Transfer Function in A/D Converter.

The first steps of these staircase can be as the ones represented in Fig. 2.10. In that example are given the first step of a generic ADC with no defined number of bit, but it is possible to observe that the first (and then the last) steps are Δ/2. These particular in characteristic means that the full-scale range is divided by 2^n-1 instead of 2^n to give Δ. Fig. 2.10 allows also to observe the quantization interval which can be encoded using both digital code or midstep point. Fig. 2.11 shows the related quantization error introduced at the output by approximating the analog input with the nearest digital word.

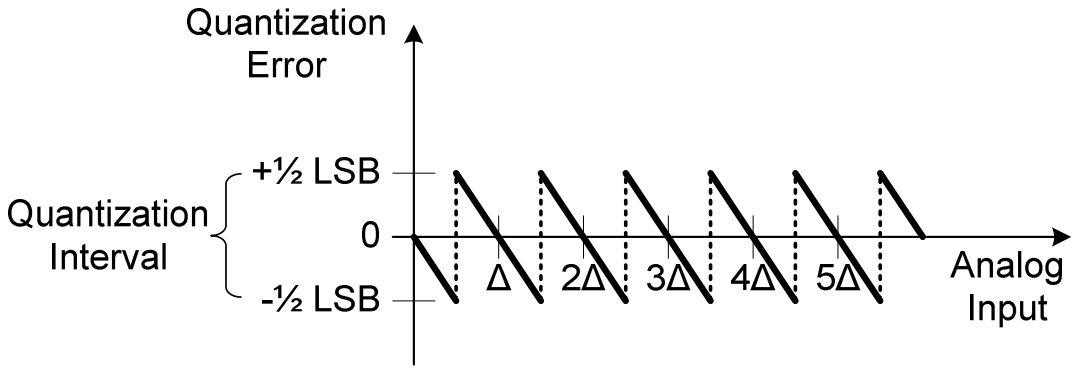


Fig. 2.11: Quantization Error in A/D Converter.

As known, and is also possible to observe in Fig. 2.11, the quantization error ranges is included between ±Δ/2 and it is equal to zero at the midstep. In the real converters there are some deviations from the ideal transfer characteristic, and in particular the real transition are not at the correct voltage value. Random errors on the step size produce a characteristic as the ones shown in Fig. 2.12, while a parabolic error on the interpolating curve bring to obtain that the first steps are shorter than the ideal ones, while the last step are larger than the ideal ones, as shown in Fig. 2.13.

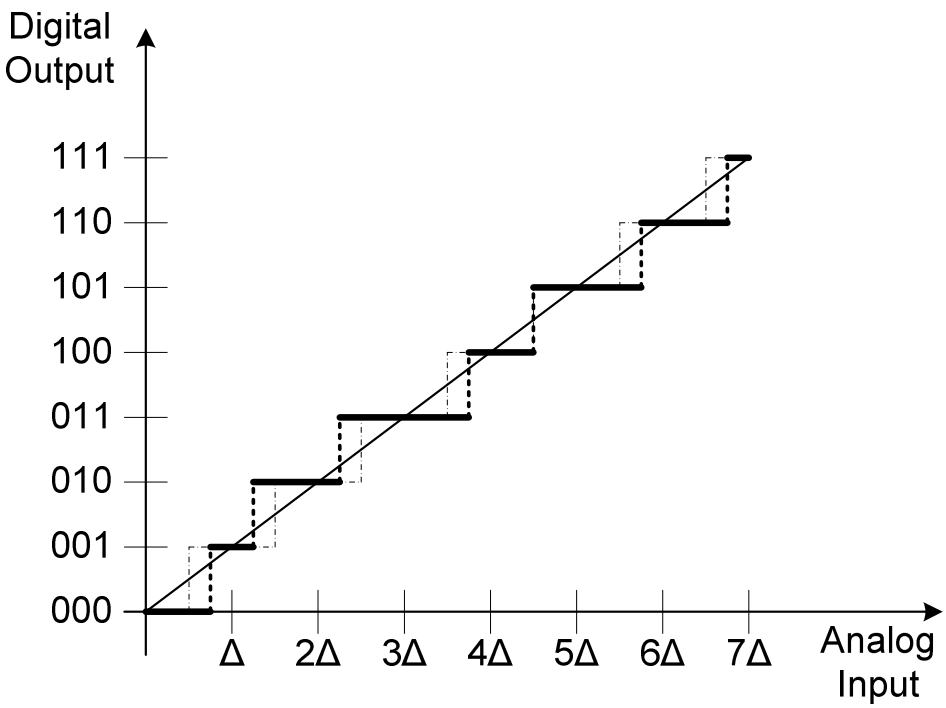


Fig. 2.12: Example of a Real I/O characteristic of 3 bit A/D Converter with random errors in step size.

The curve of Fig. 2.12 shows an almost random variation of the quantization intervals. There is no correlation between successive errors. The figure also shows the interpolating curve as a straight line running from the origin to the full scale. The characteristics of Fig. 2.13 display small quantization intervals at the beginning and large quantization intervals at the end of the curve.

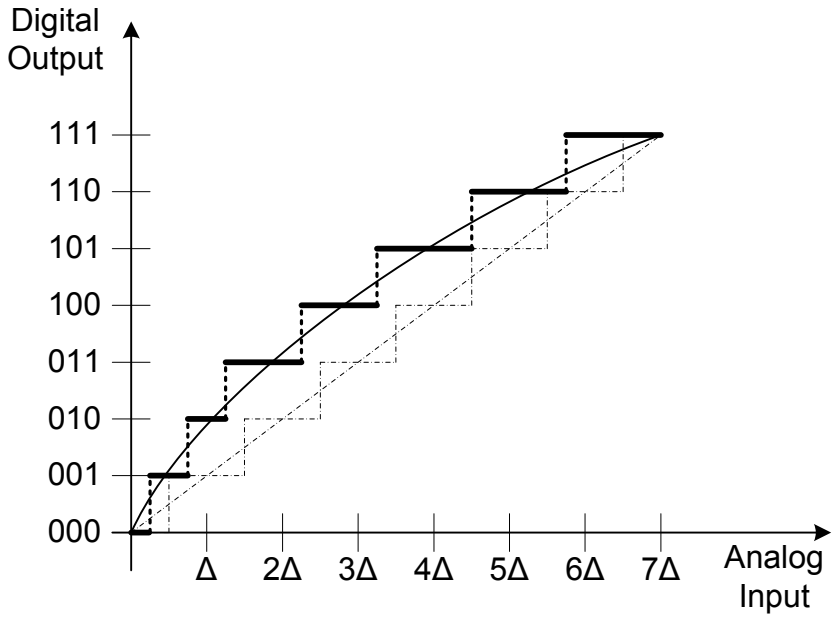


Fig. 2.13: Example of a Real I/O Transfer Function of a 3 bit A/D Converter with errors in linearity.

Both characteristic are not equal to the ideal and desiderated input-output transfer function. To understand and measure better how much that curves are not "good" are defined the following static specifications:

- Analog Resolution: it is the smallest analog increment of the input signal which do to change of a 1 LSB the output code. The analog resolution of a N bit converter where the V_{FS} is the analog input range of the converter, is equal to

$$AR = \frac{V_{FS}}{2^N} \tag{2.4}$$

- Analog Input Range (V_{FS}): is the value of the range that must applied to the A/D converter for generating a digital response which include the word 00…0 and 11…1. The analog input range is the value of the peak-to-peak single ended voltage or the peak-to-peak differential signal in fully differential structure.

- Offset: can be measured as the value of the digital word at the output when the analog input signal is equal to zero. The offset is a translation of the I/O characteristic without compromise the linearity in conversion. Fig. 2.14 shows the comparison between the ideal I/O transfer function with a possible A/D converter characteristic corrupted by offset. Typically the offset is measured in LSB, but it is possible to indicate the value of the offset in absolute value (volts or amperes), or as % or *ppm* of the full scale.

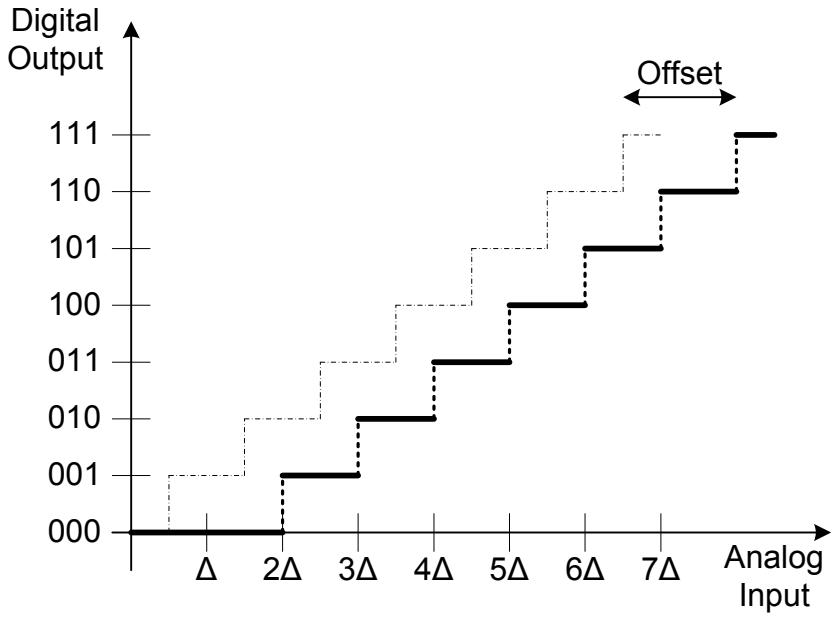


Fig. 2.14: Offset Error introduced into an Input-Output A/D Characteristic.

- Gain error: the error on the inclination of the straight line interpolating the transfer curve is called “gain error”. In ideal converter that line has a slope of D_{FS}/V_{FS}, where D_{FS} and V_{FS} are the full-scale digital code and full-scale analog range respectively. In Fig. 2.15 is possible to observe the comparison between the ideal input-output diagrams with the one relative to a real ADC corrupted by gain error.

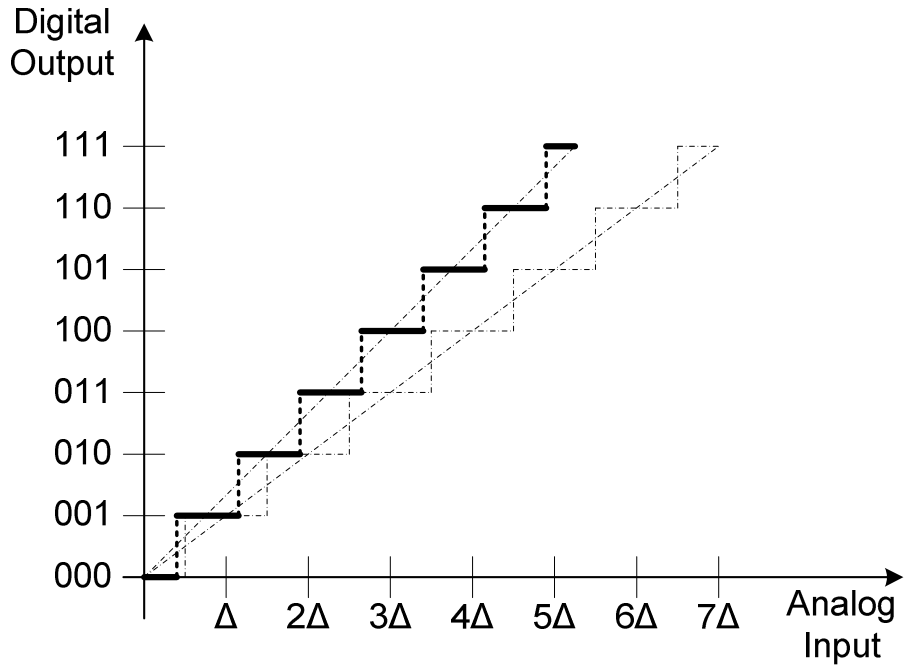


Fig. 2.15: Possible Input-Output A/D Characteristic Corrupted by a Gain Error.

- Differential non-linearity error (DNL): is the deviation of the step size of a real data converter from the ideal width of the bins Δ. Assuming that X_k is the transition point between successive codes $k-1$ and k, then the width of the bin k is $\Delta_r(k) = (X_{k+1} - X_k)$;
  the differential non-linearity is:

$$DNL(k) = \frac{\Delta_r(k)-\Delta}{\Delta} \tag{2.5}$$

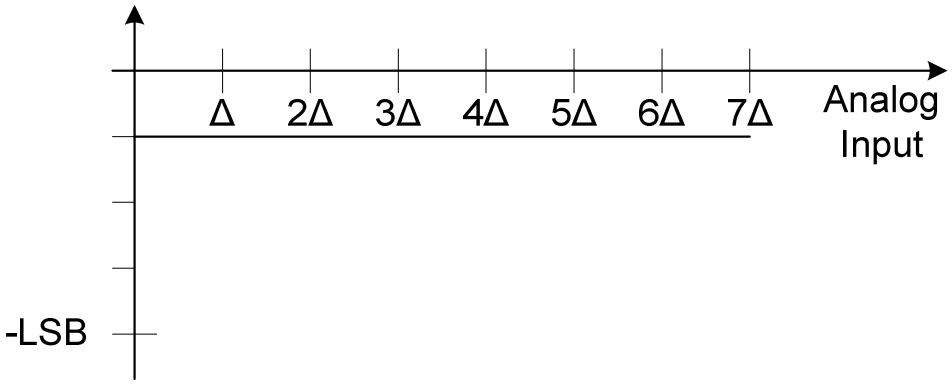


Fig. 2.16: DNL of an A/D Characteristic Corrupted by a Gain Error (Fig. 2.15).

For better understanding the mean of DNL, the correspondent DNL of the just said errors are reported in the following. In particular the gain error shown in Fig. 2.15 has a DNL as reported in Fig. 2.16.

Another possible error is the linearity error as done in Fig. 2.13, where the line which follow the input-output characteristic is not linear. In that example is possible to observe that the steps of quantization are shorter than ideal in the low level of input and larger than ideal in the upper part of the input range. So the correspondent DNL curve is reported in the Fig. 2.17.

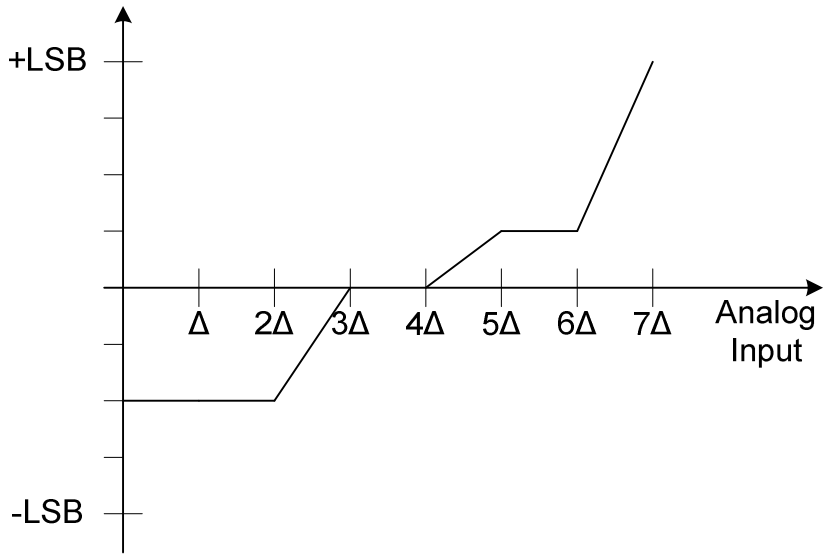


Fig. 2.17: DNL of an A/D Characteristic Corrupted by Linearity (Fig. 2.13).

The last example in DNL curve is done by a random variation of the dimension of the step, as done in Fig. 2.12. The correspondent DNL is done in Fig. 2.18.

In general the value of DNL is considered acceptable if it is included into the range ± ½ LSB. In fact it requires that the maximum error between the real dimension of a step is not so different if compared with the ideal width. In Fig. 2.19 is shown a DNL curve of a 10 bit A/D Converter, and the maximum range of the curve is a little bit more than 0.4 times the LSB.

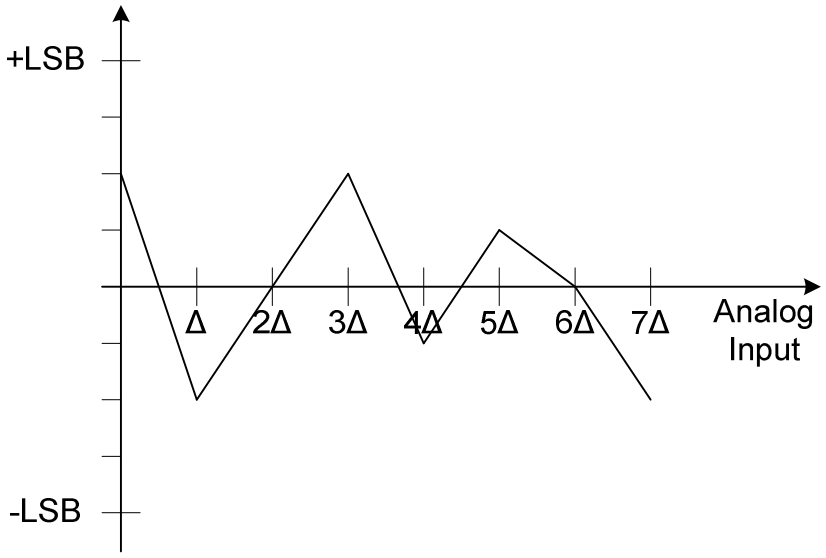


Fig. 2.18: DNL of an A/D Characteristic Corrupted by Random Errors (Fig. 2.12).

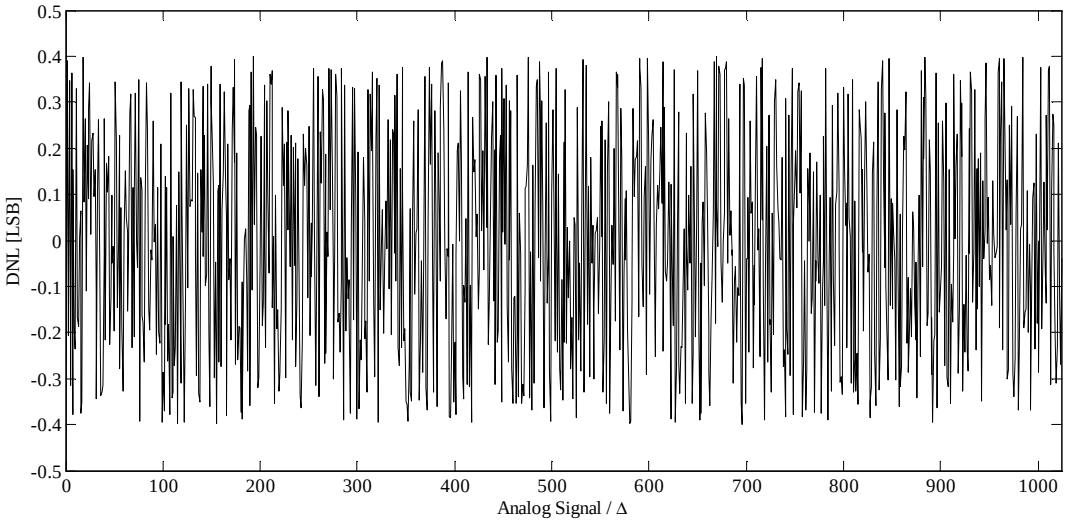


Fig. 2.19: Example of a typical DNL of a 10 bit A/D Converter with random errors.

- Monotonicity: is the ADC feature that produces output codes that are consistently increasing with increasing input signal and consistently decreasing with decreasing input signal. Therefore, the output code will always either remain constant or change in the same direction as the input. The non monotonic characteristic is very dangerous,

in particular in A/D Converter used into a control loop. In fact their response can be considered as a decreasing of a controlled voltage, instead the input voltage is increasing. To avoid these problems are widely used some circuits which ensure the monotonicity also if the error in that step can be very large.

- Hysteresis: is the limit that denotes a dependence of the output code on the direction of the input signal. If this happens hysteresis is the maximum of such differences.

- Missing code: this denotes when digital codes are skipped or never appear at the ADC output. Since missing codes cannot be reached by any analog input the corresponding quantization interval is zero. Therefore, the DNL becomes −1.

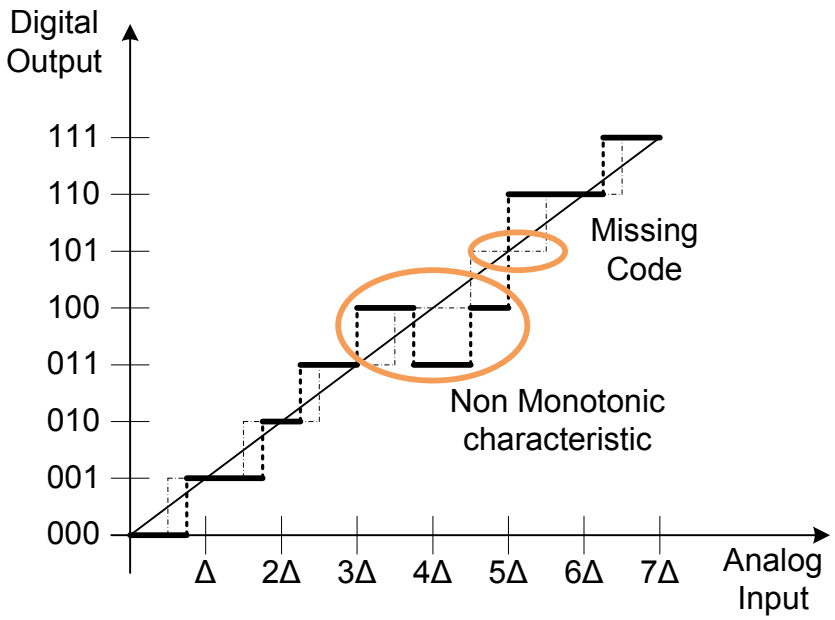


Fig. 2.20: Example of a Input-Output Characteristic of A/D Converter with non Monotonic step and Missing Code.

- Integral nonlinearity (INL): sometimes it is called relative accuracy, is defined as the deviation of the output code of a converter from the straight line drawn through zero and full-scale excluding a possible zero offset. The nonlinearity should not deviate more than _1=2 LSB of the straight line drawn.

This INL boundary implies a monotonic behavior of the converter. Monotonicity of an analog-to-digital converter means that no missing codes can occur. is a measure of the deviation of the transfer function from the ideal interpolating line. The INL, so defined, does not start from zero and shows an INL climbing up.

The INL, as for the DNL, is measured in LSB. It can also be measured using absolute value (Volts or Amperes), or as % or *ppm* of the full scale. For better understanding the mean of INL, the correspondent INL of the just said errors are reported in the following. In particular the gain error shown in Fig. 2.15, which has a DNL as reported in Fig. 2.16, corresponds an INL as reported in Fig. 2.21.

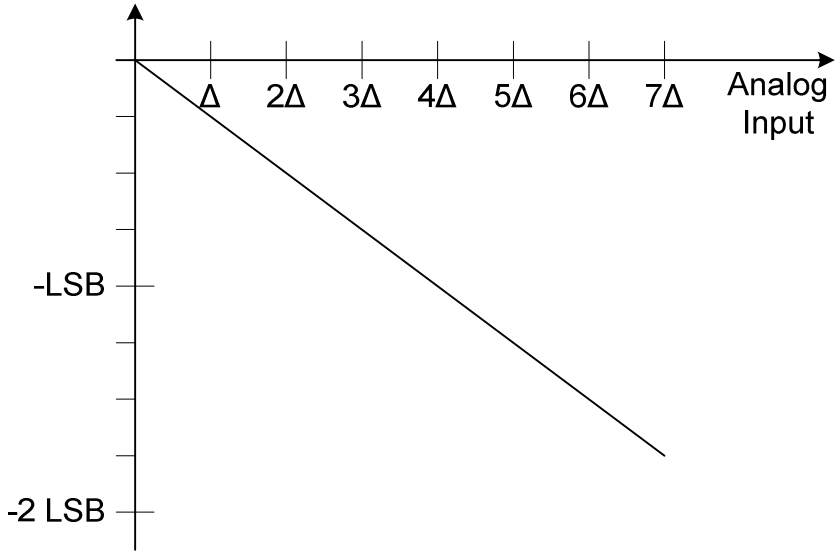


Fig. 2.21: INL of an A/D Characteristic Corrupted by Gain Error (Fig. 2.15).

Another possible error is the linearity error as shown in Fig. 2.13, where the line which follow the input-output characteristic is not linear, but the extreme points are anyway equal to ideal. At that error characteristic corresponds the DNL curve is reported in the Fig. 2.17 and the INL in the following Fig. 2.22.

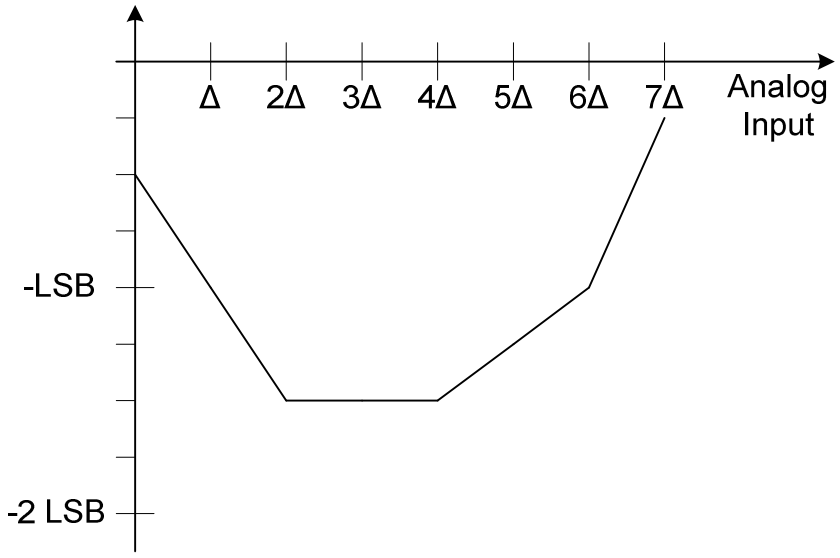


Fig. 2.22: INL of an A/D Characteristic Corrupted by Linearity (Fig. 2.13).

The last example in INL curve is done by a random variation of the dimension of the step, as done in Fig. 2.12. The correspondent DNL is done in Fig. 2.18 and the INL is done in Fig. 2.23.

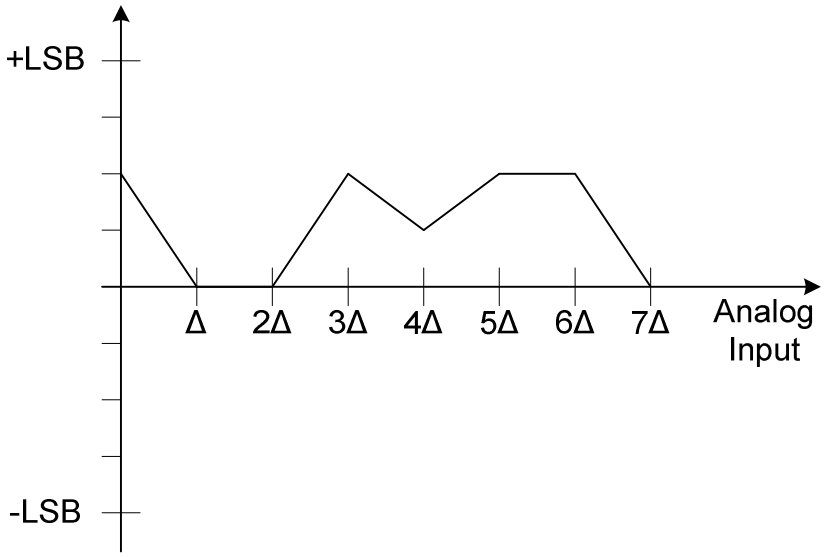


Fig. 2.23: INL of an A/D Characteristic Corrupted Random Errors (Fig. 2.12).

Using this definition of INL, is possible to write the value of each point of INL curve as a function of DNL curve, in particular:

$$INL(m) = \sum_{i=1}^{m} DNL(i) \tag{2.6}$$

Another definition of the integral non-linearity measures the deviation from the endpoint-fit line. The use of the endpoint-fit line corrects the gain and offset error. This definition corrects the two limits and shows zeros at the two endings of the quantization range. In this way obtained curve is more informative for estimating harmonic distortion. In fact other factor as offset or gain error are compensated for underlining the distortion. So the other possible way to write INL curve as a function of DNL curve is:

$$INL(m) = (1 + G) \cdot \sum_{i=1}^{m} DNL(i) \tag{2.7}$$

where G represents the gain error introduced by the converter.

With this definition of INL is opportune to think that the INL correspondent to an input-output curves corrupted by offset (Fig. 2.14) or gain error (Fig. 2.15) are equal to a line on zero. While the INL curve correspondent to the linear error of Fig. 2.13, became the curve of Fig. 2.24 instead of the Fig. 2.22.

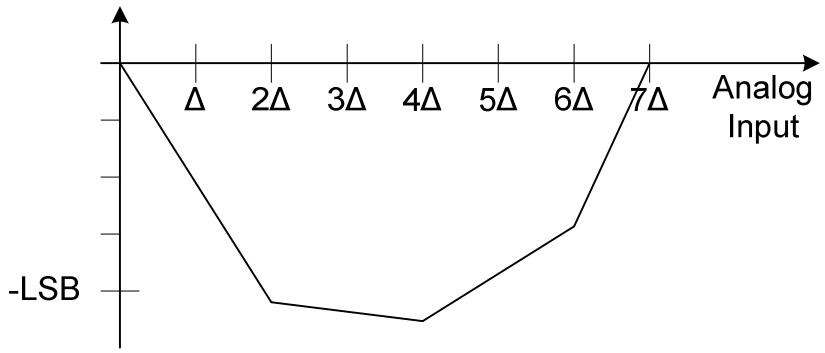


Fig. 2.24: INL of an A/D Characteristic Corrupted by Linear Error (Fig. 2.13).

The following figure (Fig. 2.25) reports the INL curve of a 10 bit A/D Converter corrupted with random errors. In that picture is possible to observe that the linearity of the converter is very corrupted, in fact it introduces errors until 3 bit. The related DNL is shown in Fig. 2.19.

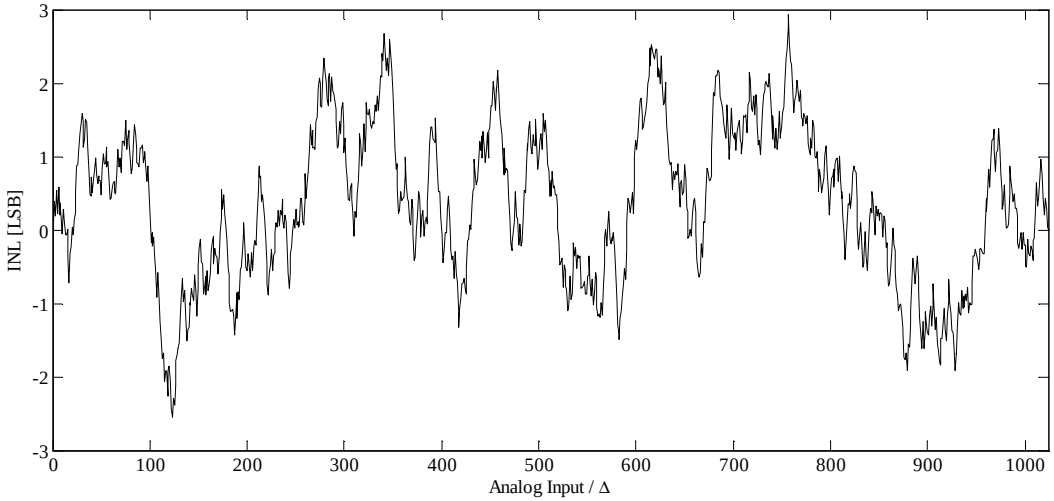


Fig. 2.25: Example of a typical INL of a 10 bit A/D Converter (Referred to DNL in Fig. 2.19).

The DNL and INL provide information with different consequences on the noise spectrum. Assume the DNL is separated into its correlated and uncorrelated parts. The running sum of the correlated fraction is the main source of the INL. If the INL is few LSB over the entire range then the correlated part of the DNL is in the order of INL divided by the number of bins. It becomes a negligible fraction: looking at the DNL spectrum it is difficult to predict how large the INL can be. The accumulation of the uncorrelated part of the DNL looks like a noise and can be added to the quantization error. The quantization error and the uncorrelated part of the INL are treated as noise terms. Since the correlated part of the DNL is usually negligible we can view a large DNL as a source of extra noise. Its running sum is added to the quantization and degrades the SNR. A large INL means large deviation of the transfer curve from the straight line thus causing harmonic distortion.

- Power Dissipation is the power consumed by the device during normal operation or during stand-by (or power-down) conditions.

Dynamic Specifications

Dynamic specifications of converters are fundamental to characterize completely the converter, especially for their applicability in a digital processing system. These specifications include information about sampling rate, dynamic range, distortion and ratio between the signal power and noise. The following presented specifications, are obtained with a full scale input signal ($\pm V_{ref}$), unless otherwise specified Furthermore, they come under input signal frequency and amplitude.

- Sampling Rate: it defines the number of time per second it samples the input signal. According to the Nyquist criterion, there is a minimum lower bound for the sampling frequency, to ensure no loss of "information" during the sampling process of a band-limited, finite energy signal.

- Input Bandwidth: the resolution of an ADC is a function of the frequency of the input signal. In ideal data converter system the maximum analog bandwidth is equal to half the sampling frequency. In practice, the noise introduced at the output of the converter can increase severally. For this reason, the analog input bandwidth of the A/D converter is defined as the maximum frequency for which the full scale input of an ADC leads to reconstructed output 3dB below its low frequency value.

- Input Signal Swing: it indicates the allowable range of value for the input. The input signal swing indicates the maximum and the minimum values that the input signal may have without driving the ADC out of range or resulting in an unacceptable level of distortion.

- Signal to Noise Ratio (SNR): The quantization process introduces an irreversible error, which sets the limit for the dynamic range of an A/D converter. Assuming that the quantization error of an ADC is evenly distributed, the power of the generated noise is given by

$$e_q^2 = \frac{\Delta^2}{12} \tag{2.8}$$

where Δ is the quantization step. If a single-tone sine wave signal with a maximum amplitude is adopted for a converter with a large number of bits (N ≥ 5), the signal *rms* power is given by

$$SP = \frac{V_{FS}^2}{4 \cdot 2} \tag{2.9}$$

Being $\Delta = \frac{V_{FS}}{2^N}$, the signal-to-noise ratio (SNR) for a single-tone sinusoidal signal can be obtained to be

$$SNR = 20 \cdot log_{10}\left(2^N + \sqrt{\frac{3}{2}}\right) = (6.02 \cdot N + 1.76)dB \tag{2.10}$$

When determining the SNR, the ratio between the frequency of the sine wave and the sampling frequency should be irrational. If the input signal deviates from the sine wave, the constant term, which depends on the amplitude rms value of the waveform, differs from 1.76 dB. Eq. 2.10 indicates that each additional bit, N, gives an enhancement of 6.02 dB to the SNR. If oversampling is used, which means that the sample rate F_S is much larger than the signal bandwidth, the quantization noise is averaged over a larger bandwidth and the signal-to-noise ratio becomes larger, written as

$$SNR = 20 \cdot log_{10}\left(2^N + \sqrt{\frac{3}{2}}\right) \cdot \sqrt{OSR} =$$
$$= \left(6.02 \cdot N + 1.76 + 10 \cdot log_{10}(OSR)\right)dB \tag{2.11}$$

where the oversampling ratio OSR is given by (2.3).

In the Nyquist rate A/D converters, the signal bandwidth is normally equal to F_S=2 resulting in an OSR equal to one, while Eq. 2.11 suggests that the signal-to-noise ratio increases by 10 dB per decade of oversampling.

- Total Harmonic Distortion: any nonlinearity in an A/D converter creates harmonic distortion. In differential implementations, the even order distortion components are ideally canceled. However, the cancellation is not perfect if any mismatch or asymmetry is present. The total harmonic distortion (THD) describes the degradation

of the signal-to-distortion ratio caused by the harmonic distortion. By definition, it can be expressed as an absolute value with

$$THD = \frac{\sqrt{\sum_{j=2}^{N_H+1} V^2(j \cdot f_{sig})}}{V(f_{sig})} \tag{2.12}$$

where N_H is the number of harmonics to be considered, $V(f_{sig})$ and $V(j \cdot f_{sig})$ the amplitude of the fundamental and the *j-th* harmonic, respectively.

- Signal to Noise and Distortion Ratio (SNDR or SiNaD): a more realistic figure of merit for an ADC is the signal-to-noise and distortion ratio, which is the ratio of the signal energy to the total error energy including all spurs and harmonics. SNDR is determined by employing the sine-fit test, in which a sinusoidal signal is fitted to a measured data and the errors between the ideal and real signal are integrated to get the total power of noise and distortion. If all tones and spurs other than the harmonic distortion are considered as noise, the signal-to-noise ratio can be obtained from the SNDR by subtracting the total harmonic distortion from it

$$SNR = SNDR - THD \tag{2.13}$$

where SNDR and THD are given in absolute values. Therefore the SINAD is the ratio between the root-mean-square of the signal and the root-sum-square of the harmonic components plus noise (excluding dc). Since static and dynamic limitations cause a non-linear response the SINAD is dependent on both the amplitude and frequency of the input sine wave.

- Dynamic Range: it is defined as the input signal power for which the value of SNR is equal to zero. It can be measured by obtaining the value of SNR whit the input power variation. This parameter is widely used in specifics of converters that do not obtain their maximum SNR at 0dB.

- Input Impedance: is the impedance between the input terminals of the ADC. At low frequency the input impedance is a resistance: ideally, it is infinite for voltage inputs and zero for current inputs (thus leading to an ideal measure of voltage or current.) At

high frequency the input impedance is dominated by its capacitive component. Often, a switched capacitance structure performs the input sampling. In this case the specification provides the equivalent load at the input pin. At very high frequency the input impedance of the ADC must be the matched termination of the input connection.

- Settling Time: is the time at which the step response of an ADC enters and remains into a fixed digital number. The input step can be considered has the sample of Sample and Hold block.

- Clock Jitter: it is the standard deviation of the sampling time. Usually it is used to consider the errors introduced by clock jitter like a noise with white spectrum.

- Equivalent Input Referred Noise: it is a measure of the total electronic noise produced.

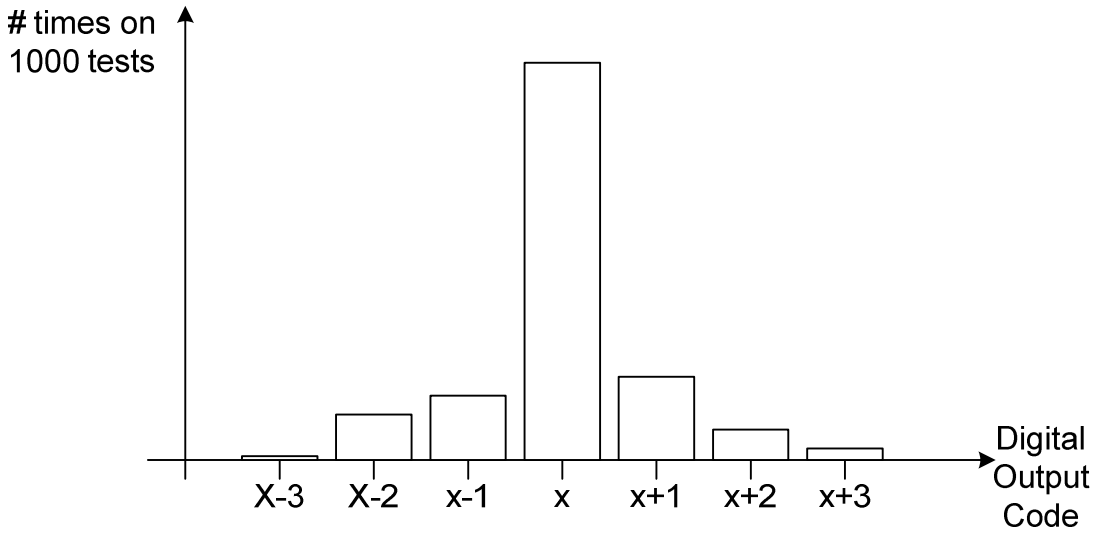


Fig. 2.26: Example of an output histogram of an ADC with dc input signal.

The result is that for a constant dc input the output is not fixed but there is a distribution of codes centered around the output code nominally encoding the input. With a large number of output samples the code histogram is approximately Gaussian. The standard deviation of the distribution defines the equivalent input referred noise.

- Effective Number **o**f Bit (ENoB): it is an alternative mode to write the SNDR. In fact the value of SNDR is often indicated in dB, while it is possible to indicate as number of bit. Therefore this value take the name of effective number of bit because of noise limits, even if the output of ADC has an higher number of digital signals. For calculating the ENoB is then used:

$$ENoB = \frac{[SNDR]_{dB} - 1.76}{6.02} \tag{2.14}$$

- Effective Resolution Bandwidth (ERBW): it is the analog input frequency at which the SNDR drops by 3 dB compared to its low frequency value. The ERBW represents the effective signal bandwidth of the input signal that can be converted. The ERBW should be severally low than the Nyquist limit.

- Figure of Merit (FoM): this parameter indicates the power effectiveness of an ADC. In first is possible to assume that the total power supply is consumed mainly for obtaining a larger bandwidth of the converted signal (BW) and an higher equivalent number of bits (ENoB). The definition of FoM is

$$FoM = \frac{P_{TOT}}{2^{ENoB} \cdot F_S} \tag{2.15}$$

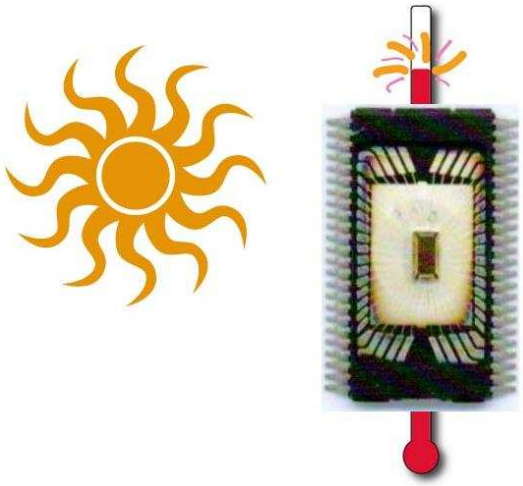
2.3 Operation Issues

From experimental setup strongly depends the test of a data converter for obtaining the correct value of the upper quoted parameters. The most important thing to do for beginning to test the just arrived chip with on board an Analog to Digital converter is to define correctly the exact specifications are need to describe the operation of the converter. In fact an ADC for communications require to define accurately the spurious frequencies, the inter-modulation components, while ADC for precision has to have a limited static errors, and so on. The second step on analysis is to design with care the board and it is useful to examine how the operational environment can influence the performance which are measured. There are two important conditions of operation to keep in account: supply voltage (and relative noise) and the temperature

variation. A data-converter must be tested not only at the nominal supply voltage and room temperature but also within given ranges. For example the supply voltage fluctuation of about 5% or a little bit more must be kept in account. Also the temperature range should be from −20°C to 85°C (consumer applications) or −55°C to 125°C (military applications), and naturally over all range the specifications must be verified. Specifications within a restricted range of supply voltages or temperatures don't properly represent the on-field use. To design a good chip include the maintaining of performance over a wide range of supply voltage or temperature is difficult especially for high resolution devices. For example to ensure 14 bit over the full range of voltage and temperature means to ensure as good as 600 ppm/V (5V supply) or 0.3 ppm/°C (consumer applications) . When measuring or using a data converter it is important to ensure that the printed circuit board (PCB) does not influence negatively the results. In general, about power supply, the couplings and the ground connections are critical issues. Often, high performance data-converters use separate pins for the analog and the digital supplies even though the pins are usually connected to a single supply generator on the PCB. This method exploits the bonding inductances to decouple the analog and digital internal supplies. Besides, in order to obtain good VDD or ground terminations, it is needed to ensure proper connection between the external supply generators and the pins, better if realized with insulated cable. The length of the connecting lead must be as short as possible: they are equivalent to inductors. Another good point to obtain a good power supply is to include an additional low pass filter with a very high constant time, in this way the high spurious frequency are notably reduced. To avoid ground loops between two sides of the PCB is a very important thing, in fact it can realize undesired oscillation of the circuit. The possibility to use a two-layer board is indicated only for low frequency measures, instead high frequency signals require a multi-layer boards with separate ground and power planes, in this way is possible to reduce mutual induction between signals. The master clock and reference voltages are other important signals that are supplied through the PCB, but is also very important to separate the digital part of the PCB from the analog, in fact a possible capacitance between analog input signal and clock can compromise the correct operation of the chip on test. Another important point about

Temperature variations have effects on the performance of the chip

the clock is to avoid the correlated clock jitter, because it can degrade the performances. Therefore, it is not just necessary to use signal generators with low jitter but it is also important to preserve this feature in the phase generator. The PCB traces leading the clock must be short with a solid ground plane underneath to avoid undesired mutual induction to critical signal, like reference voltages. This particular shape of the microstrip create a transmission line and enables impedance matching. When low-speed data converters use external references it is necessary to utilize a clean voltage generator whose output impedance is low enough to avoid internal fluctuations greater than 1 LSB. This is not easy as the discrete-time operation of the data-converter draws large pulses of current to charge and discharge capacitances. In general, to avoid ambiguity and to help in the testing of parts, some manufacturers provide evaluation boards (or their layout) and give detailed guidelines explaining the evaluation procedures about realize standard circuits or testing the performances of the sold chip. In fact, the set of parameters given in data sheets assume that their measure is done in optimum specified conditions. The main purpose of these information is to avoid conflicts between part provider and customers, the manufacturers should give very clear information on the necessary setup, features and accuracy of instruments to use in the experimental set-up.



Temperature variations have effects on the performance of the chip

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3

Principle of Operation of SAR A/D Converter

- Principle of S.A. Algorithm
- Architecture
- State of the Art

3.1 Principle of Successive Approximation Algorithm

Successive-approximation A/D converters are a type of converter with feedback or cyclic converters. They are those in which the signal circulates in a closed loop, i.e. it uses the same blocks in every conversion step. This is in contrast with other type of converters, like cascade structure, where the signal proceeds from one block to the next one. In general is used to consider cyclic converters are those containing pre-subtraction. The main purpose of subtraction is first made here which is then followed by a comparison from the first estimated value. The basic structure of a feedback converters is shown in Fig. 3.1.

The analog input is compared with an already available V_{DAC}. The difference voltage ε, representing the error signal, is then used to produce a new improved estimation. These estimated values are developed in the circuits of the feedback loop. According to the state of the comparator, the block labeled "Digital Logic" has the purpose to control the counter to start counting in forward direction for a positive error signal and in a backward direction for a negative error signal. For a modulo two counter, the output is in binary form. The DAC connected in the feedback loop now delivers the required first estimate V_{DAC} of the input signal. In the next cycle, this value is subtracted from the input to give the error signal ε. The process is terminated after n clock cycles when the error signal becomes $|\varepsilon| < \frac{LSB}{2}$.

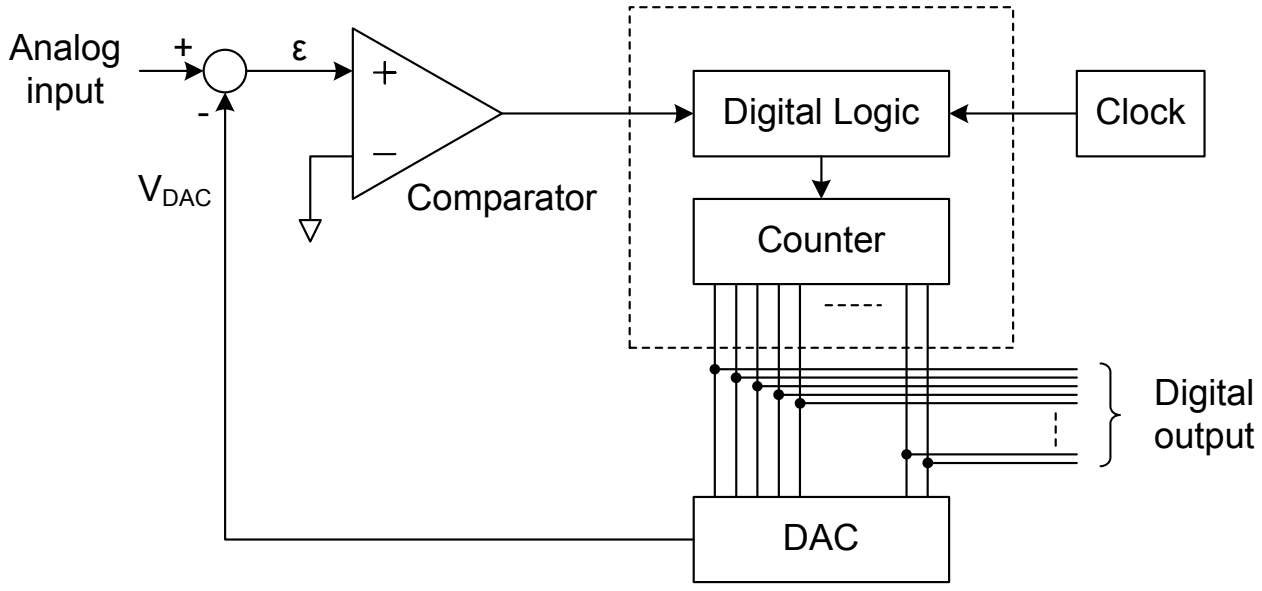

Fig. 3.1: General block scheme of a feedback A/D converter.

However, due to circuit noise and drift, even if ε = 0, a stable state is never maintained, and the counter contents bounces up and down by one LSB in tracking the input value until conversion is stopped. Since the estimated value successively approaches the input signal until the error is diminished to a predefined value, this method is sometimes also called “servo technique” when referring to early mechanical motor-driven approach. The two blocks labeled “Digital Logic” and “Counter” become relatively simple in the case when the converter is to implement the successive approximation method, i.e. one bit per cycle. Then the two blocks essentially reduce to a Successive Approximation Register (SAR), shown in dashed lines in Fig. 3.1.

There is a distinct advantage to this structure. Any type of D/A converter in the feedback path will allow an A/D converter to be constructed. D/A converters are conceivably simpler than A/D converters. So if the technology easily leads to a D/A converter, the A/D converter is obtained by completing the loop circuit.

The realization of this technique in the simplest form has been favored for a long time due to the fact that most of the components required are available as standard integrated circuits. A Successive Approximation A/D Converter illustrated in Fig. 3.2.

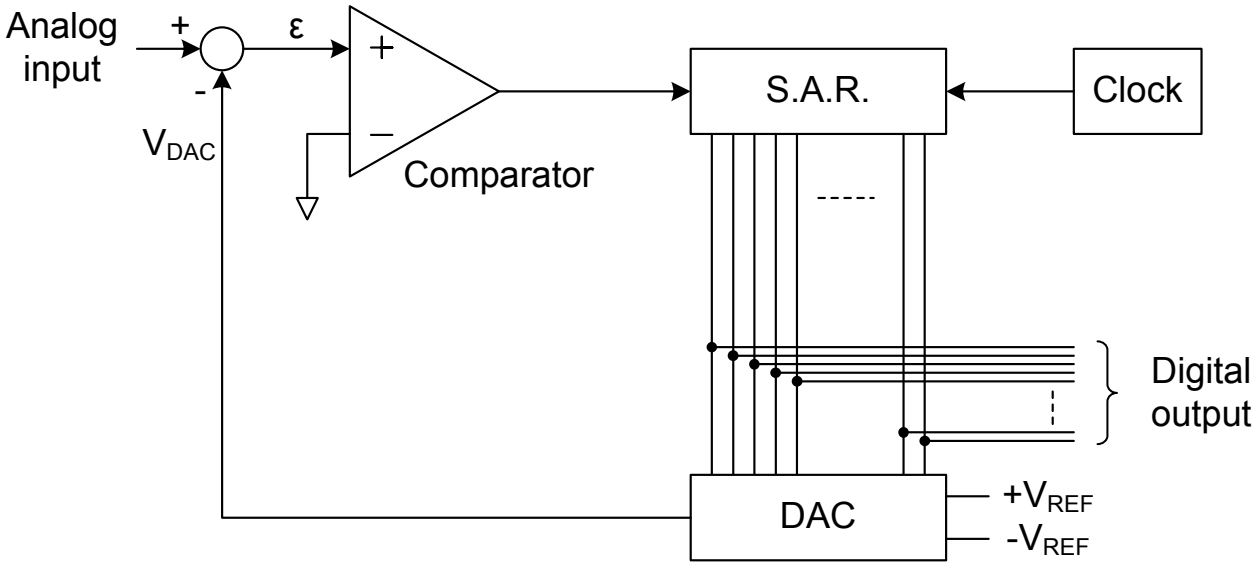

Fig. 3.2: General block scheme of a Successive Approximation A/D converter.

In the block labeled “S.A.R.”, given in more detailed form in Fig. 3.3, are considered the condition of the value of the output of the comparator for each step of conversion. A successive

approximation converter consist of D/A converter, controlled by decision logic, whose output is compared with the input analog voltage. The input voltage is fed to + input of the subtraction node, while the output of the internal DAC goes to the - input. When the conversion is starting, the register is cleared and the block labeled “Logic” in Fig. 3.3 has the main purpose to impose the value of the MSB equal to the logic value 1. So the value of error ε is greater than 0 if the unknown input signal is greater than the output of DAC, otherwise the contrary. Anyway the output of the comparator is equal to the right logic value of the MSB. The procedure continues considering each other bit with the same procedure, at which stage the conversion is completed.

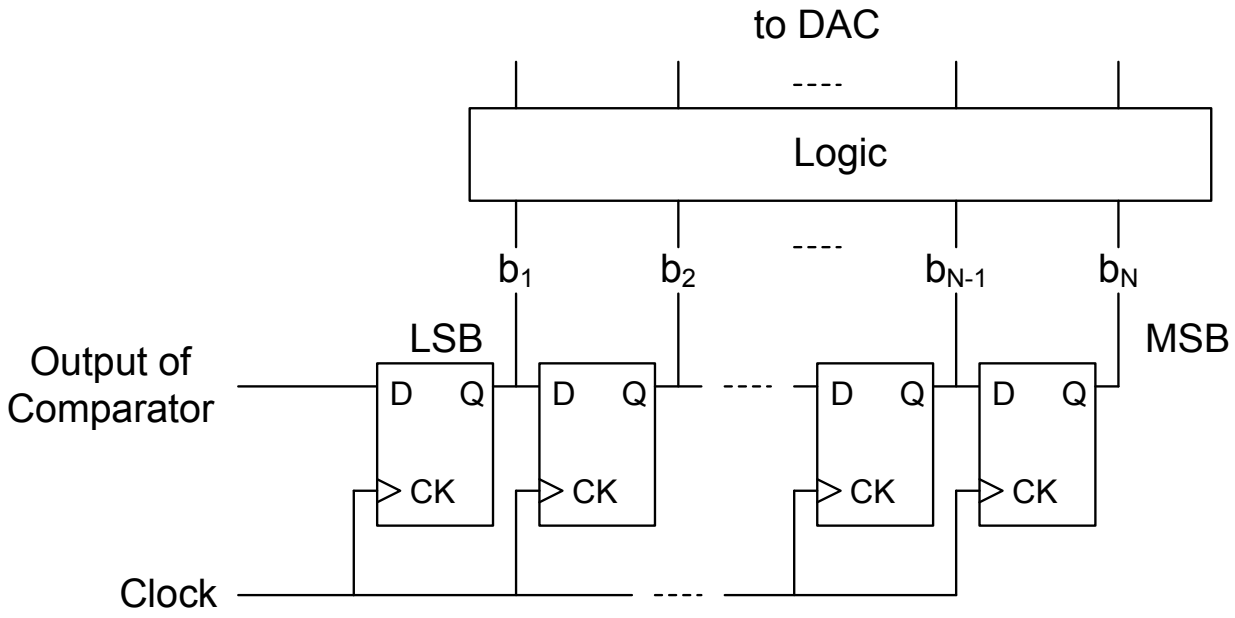

Fig. 3.3: General block scheme of a Successive Approximation A/D converter.

It is then possible to consider that the successive approximation algorithm, at the base of the SAR converter, is one of the most popular approaches for realizing A/D converters due to their reasonably quick conversion time. To understand the basic operation of successive-approximation converters, knowledge of the search algorithm referred to as a “binary search” is helpful. As an example of a binary search, consider the game of guessing a random number from 1 and 128 where one can ask only question that have a “yes/no” response. The first question might be, “Is the number greater than 64?” If the answer is yes, then the second question asks whether the number is greater than 96. However, if the first answer is no, then the second question asks whether the number is greater than 32. The third question divides the search space in two once again and the process is repeated until the random number is determined. In general, a binary search divides the

search space in two each time, and the desired data can be found in N steps for a set of organized data of size 2^N. Referring to the Fig. 1.12, the operation of successive approximation A/D converter will be depicted graphically. The logic is initially set to force the MSB to "1", and all other bits to "0", which places the internal DAC output at one-half full scale ($½ \cdot V_{FS}$).

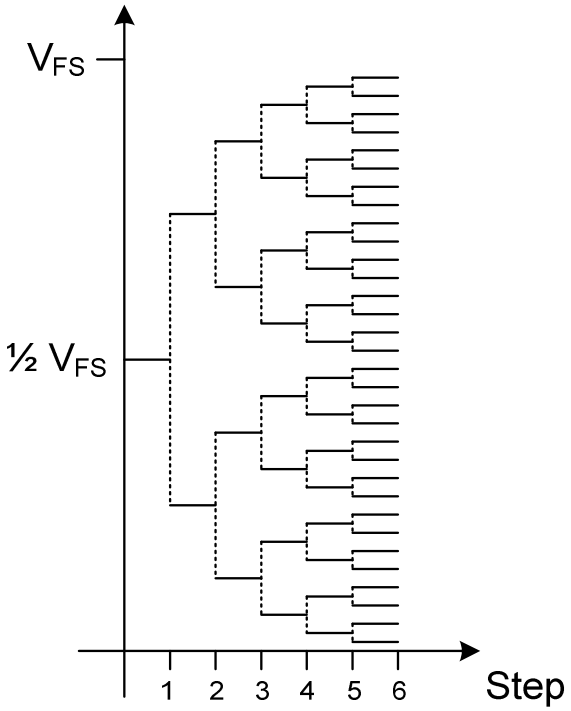

Fig. 3.3: General scheme of sequence of DAC output at each step.

During the time interval from 0^{th} to 1^{st} step, the DAC output is compared to incoming analog signal. If the input is greater than the DAC output, the logic "1" at b_N is permanently stored. If the input is less than the DAC output, the logic "1" is removed from b_N and a logic "0" is permanently stored in b_N. Then the logic "1" is applied to b_{N-1}. This adds $¼ \cdot V_{FS}$ to the DAC output, setting it to either $¼ \cdot V_{FS}$ or $¾ \cdot V_{FS}$, depending on the previous comparison. During the interval from 1^{st} to 2^{nd} step, the DAC output is again compared to the input signal. If the input is greater than the DAC output, the logic "1" at b_{N-1} is permanently stored. If the input is less than the DAC output, the logic "1" is removed from b_{N-1} and a logic "0" is permanently stored in b_{N-1}. This sequence is repeated for each bit. The final state of all the bits will be the digital word that represent the analog input. Note that the number of approximation is equal to the number of bits. Hence, the logic recycling is at a minimum. Conversion speed of the successive approximation A/D converter is based on the settling time of the MSB logic ladder network and comparator. In a single rate conversion unit, conversion time would be N times the time required for one bit. Since only one comparator is used and ancillary hardware is limited to logic and ladder networks, the successive approximation technique

provides an inexpensive average speed solution. Successive approximation converters are primarily used where either an input signal is continuously varying at relatively high speed or where a succession of approximation A/D converter the accuracy of the converter can be no better than the accuracy of the internal DAC and may be considerably worse. The operation of a three bit successive operation ADC is illustrated in transition diagram of Fig. 3.4.

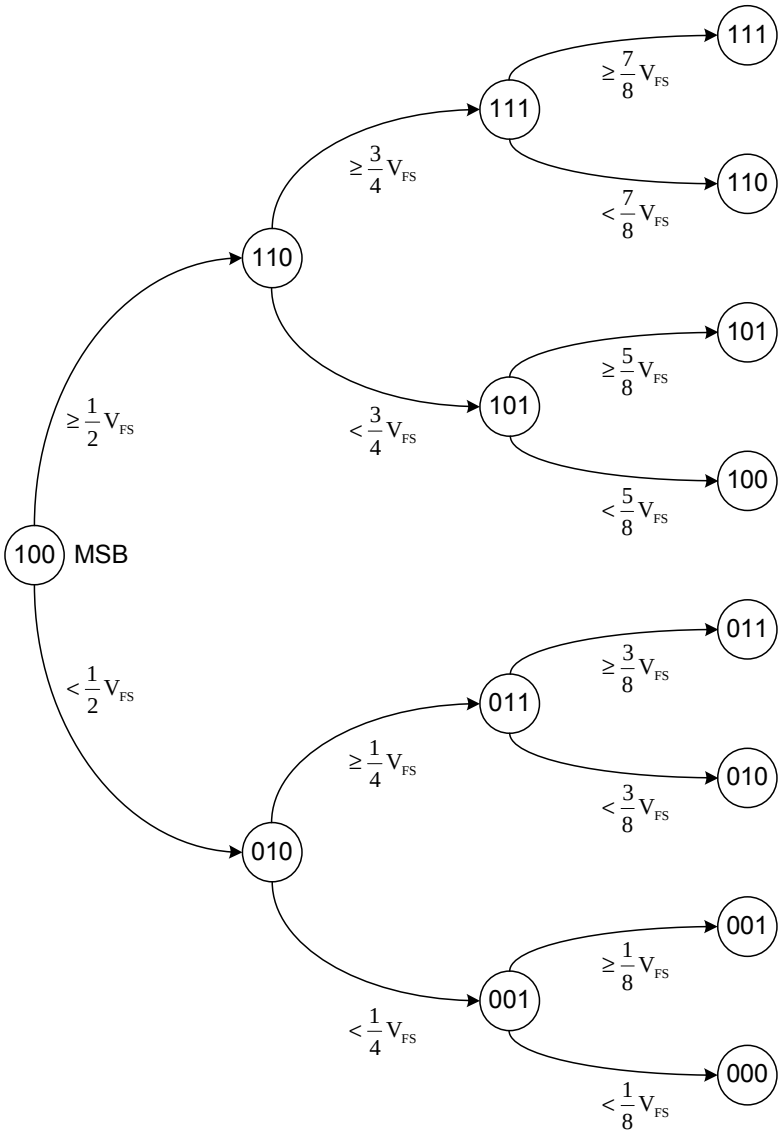

Fig. 3.4: Operation principle of 3-bit SA-ADC.

In the most straight-forward implementation, successive approximation converter require N clock cycles to complete N-bit conversion. A flow-graph for signed conversion using a successive approximation approach is shown in Fig. 3.5.

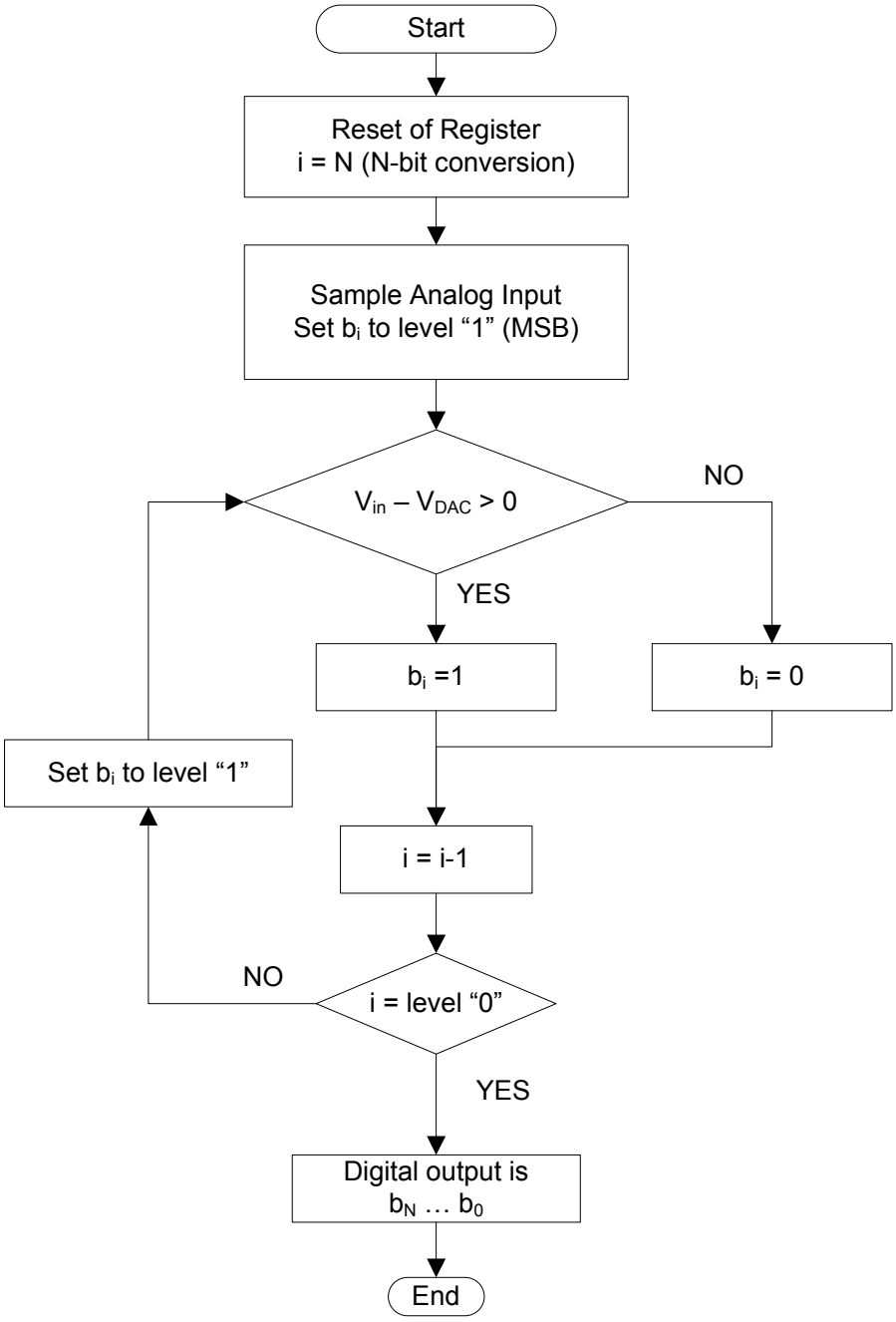

Fig. 3.5: Operation principle of general N-bit SA-ADC.

From a comparison between successive approximation algorithm with other feedback converters, like counter ramp ADC, results to be faster but exhibits a poorer differential linearity. The conversion word rate is limited by the fact that each bit must successfully tried before continuing to the next step. This means the the A/D circuits must respond completely with some time left over before the next step begins, if the operation is not to be marginal and if large conversion errors are to be avoid. In each step of the process sufficient time must first be allowed

for the DAC to reach its final value within its accuracy constraints. Also, sufficient time must be allowed for the comparator to recover from its previous inputs and to generate an output dependent upon its new input from the DAC. The accuracy of the system is a function of the quantizing error and the errors in the electronic circuit, that is, the DAC, the analog comparator, and reference voltage source. As with any electronic process the accuracy of the measurement decreases as the speed conversion increases. The increase in error is logarithmic since it is basically a function of the fundamental time constant equation. The timing diagram, done in Fig. 3.6, shows the sequence for a typical A/D conversion.

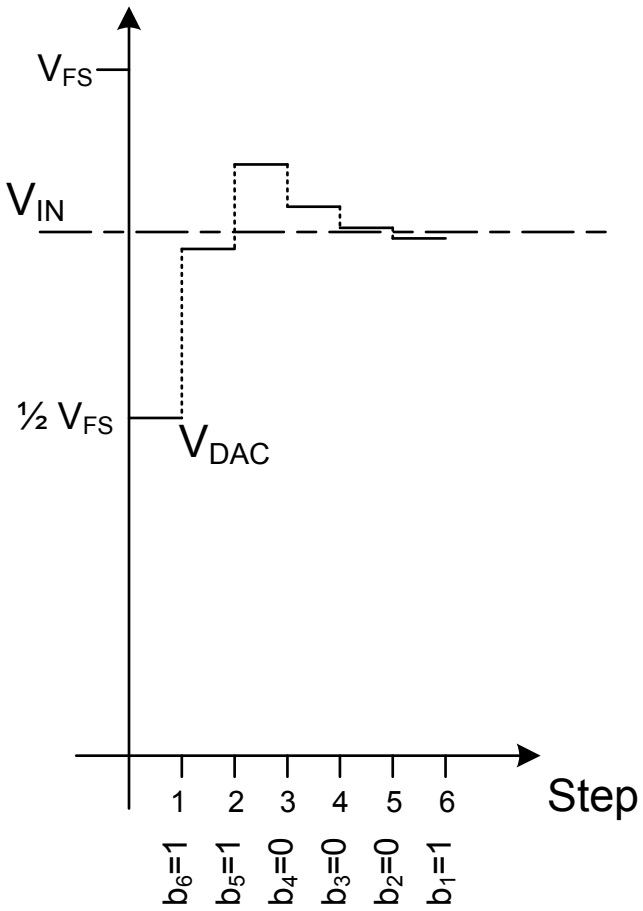

Fig. 3.6: Timing Diagram of 6-bit SA-ADC.

In particular is possible to observe that the sampled analog input signal is constant for all time which the conversion takes. Besides the output signal of the DAC follows the continuous variation based on the value of the previous bit and from the comparison between them results the effective value of the following bit.

3.2 Architecture

The Fig. 3.2 reports the general scheme of a successive approximation converter. From that figure is possible to extract that the main basic building block of the entire system are:

1. The Sample and Hold block;
2. The subtraction node;
3. The DAC in feedback path;
4. The comparator;
5. The Successive Approximation Register and its digital logic.

The designing of each block must keep in account all the introduced errors because of non-idealities of its component, and to consider that the effect on the output due these errors must be negligible than the LSB of the converter.

1. The first block, the Sample and Hold (S&H), has the function to take, according to the sampling theorem, samples from a continuous voltage and then to hold the level for a certain time interval. During this "hold" period, further processing of the sampled waveform takes place, as A/D conversion for example. In this section, useful definition as well as the relationships describing the associated errors in a S&H process are presented. A useful criterion for the total error is that given by quantization. Low-loss capacitors are used as an intermediate storage medium. A simplified S&H circuit is shown in Fig. 3.7.

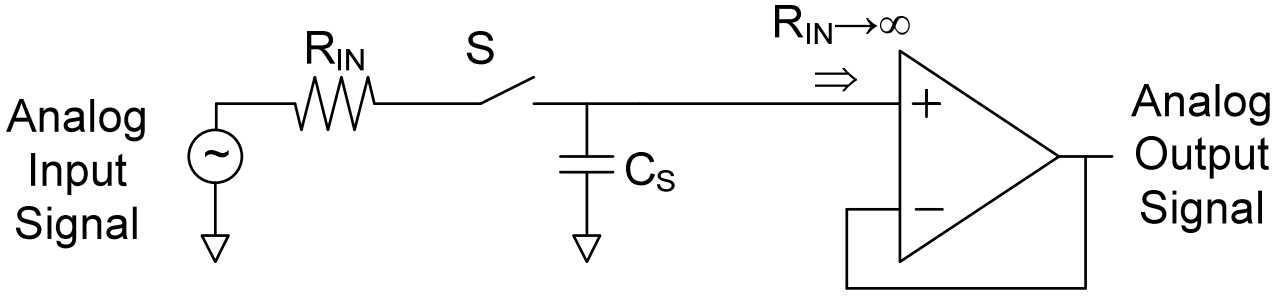

Fig. 3.7: Sample and Hold circuit.

The signal source, having an internal resistance R_1 and an open-circuit voltage V_{IN}, charges capacitor C_S through the switch S. During the charging period t_A (called acquisition time), the switch is turned on and the sample is taken. Afterwards the switch is turned off for the hold period t_H during which the sampled amplitude is kept constant. To avoid loading of the hold capacitor C_S

by any output circuit, a buffer amplifier, or another circuit with very high input resistance, is used. If necessary, a second buffer stage is introduced at the input of the S&H circuit so that C_S is charged without loading the signal source. The sum of t_A and t_H represents the actual sampling period T_S which has to fulfill the condition TS < ½·BW due to the sampling theorem, where BW is the bandwidth of the input signal.

In practice, the sampling process deviates from theory. For instance, the sampling pulse has a finite width t_A (Fig. 3.8) during which the capacitor charges to the value of the signal voltage (within a certain error band) through the resistance $R_\varepsilon = R_1 + R_S$, with R_S the switch ON-resistance.

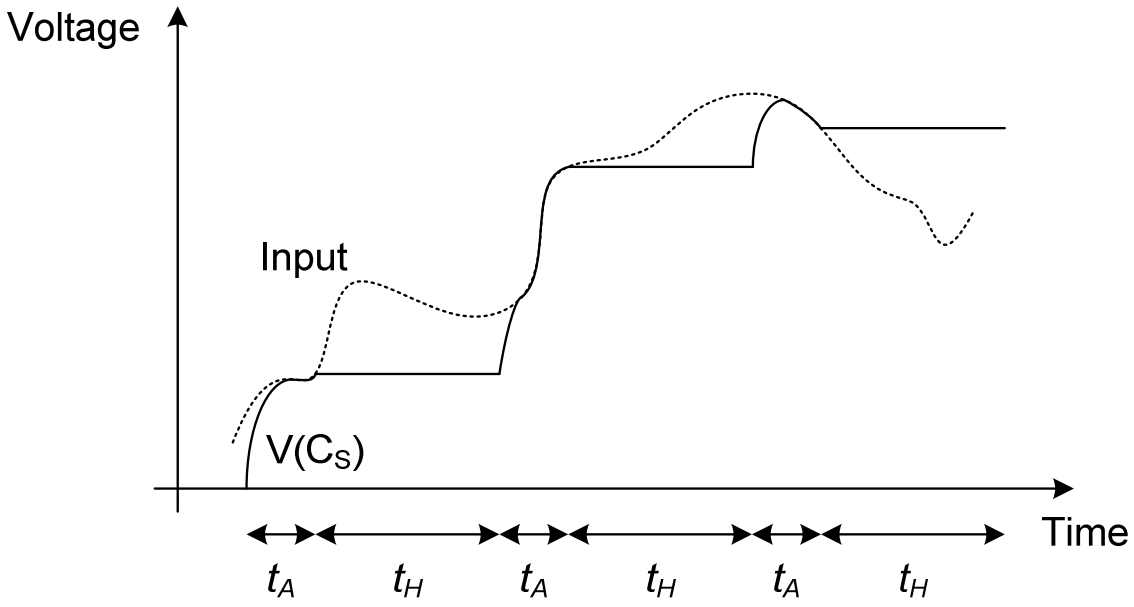

Fig. 3.7: Sample and Hold circuit.

If the time constant could be made such that RC→0, the S&H would act as an analog gate during the sampling interval t_A. This operation is called “natural sampling” and there is no attenuation of the signal, depending on its frequency as long as it is situated within the bandwidth BW. Holding the sampled value during the time $0 < t_H < T_S$ (flat-top sampling) a shaping of the signal spectrum given by the function

$$\frac{\sin(\pi \cdot f_{IN} \cdot t_H)}{\pi \cdot f_{IN} \cdot t_H}. \tag{3.1}$$

For $R \cdot C_S \ll t_A$ the capacitor voltage approaches steady state during the sampling interval. Assuming a nearly constant signal level within this time, then CS charges exponentially so that the signal is reached within an accuracy of –LSB/2. This condition leads to

$$e^{-\frac{t_A}{R \cdot C_S}} \leq 2^{-(N+1)} \tag{3.2}$$

if the S&H is used in front of an N-bit A/D converter.

The first-order low-pass response of the RC-section in the tracking mode (switch closed) must also be considered. For a LSB/2 decrease of the amplitude at the maximum signal frequency f_{IN} = BW, the 3-dB bandwidth has to be

$$f_{3dB} = BW \cdot \frac{a}{\sqrt{(1-a^2)}} \tag{3.3}$$

where $a = 1 - 2^{-(N-1)}$, the normalized amplitude at f_{IN} = BW for a permissible error of LSB/2. For example, if N = 10 bit, a required bandwidth $f_{3dB} = 32 \cdot$ BW is needed. This formula is also valid for any amplifier with a first-order low-pass response in front of an A/D converter. If the time constant is no longer small compared with the acquisition time t_A; some averaging of the signal during sampling time t_A takes place. As a worst-case estimation, integration of the signal during t_A is assumed, i.e. $R \cdot C_S \gg t_A$, such that the signal can vary by a considerable number of quantizing steps without the capacitor voltage being able to track it. In this case, the frequency response can be approximated by the function

$$\frac{\sin(\pi \cdot f_{IN} \cdot t_A)}{\pi \cdot f_{IN} \cdot t_A}. \tag{3.4}$$

The sin(x)/x decrease due to the hold time t_H has an influence only if the S&H is used as a stand-alone unit. If a S&H is in front of an A/D converter, it is important that the S&H reaches and tracks the signal during acquisition time. An abrupt transition from sample to hold should occur when the sampling pulse changes state. This does not always happen in practice.

First, there is a certain delay between the sampling pulse and the actual sample-to-hold transition of the circuit. This delay can be divided into a constant so-called “aperture delay time”, which can be taken into account, and an aperture uncertainty time t_A which is changing from sample to sample because it depends at least on the signal level and the slew rate. This aperture uncertainty is difficult to measure and can only be estimated in many cases.

A further condition is obtained by considering the necessary decoupling between the signal source and the hold capacitors throughout t_H. Although a very high OFF-resistance of the switch is assumed, the actual isolation is not perfect due to the capacitor C_P shunting it. A capacitive voltage divider is therefore established. Thus by using the same LSB/2 criterion as before, we get

$$\frac{C_P}{C_S} \leq 2^{-(N+1)}. \tag{3.5}$$

Other sources of errors are present in S&H system and are always related to the switch. In fact usually the switch is realized with a MOS transistor. When the MOS is turned on it suffers from wideband thermal noise, much like a resistor. This causes random fluctuations in the device's drain current, which are continuously integrated by the capacitor. When the MOS is later turned off, the integral of the noise current is "sampled" onto the capacitor. Thus an error component is added to the signal charge. Wheel the MOS switch turns off, two other error sources manifest themselves. As the gate voltage swings quickly from one supply rail to the other, charge is driven off the bottom plate of the gate overlap capacitance onto the data storage node. This is called *clock feedthrough*. Simultaneously, another effect called charge injection is in operation. This is caused by the mobile charge in the MOS's inversion layer, which is forced to leave the channel when the gate voltage changes. Any inversion charge that escapes to the data node causes an additional error in the stored charge. This section is concerned with the computation of errors due to *clock feedthrough* and *charge injection*.

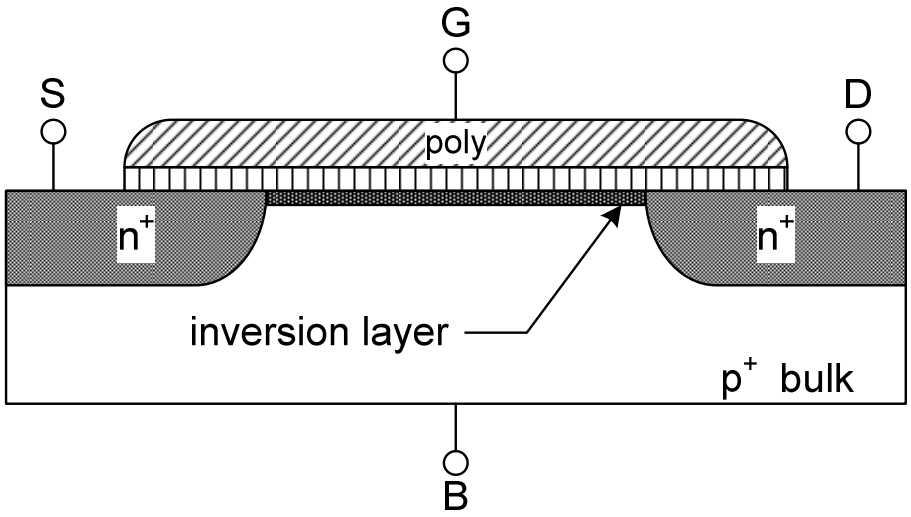

Fig. 3.8: Cross Section of NMOS transistor.

These effects are much more difficult to model than noise. The main difficulty is trying to keep an accurate accounting of where the charge goes during turn-off. The MOSFET is still conducting to some extent until the gate voltage goes well below threshold. Thus, charge is able to redistribute itself from source to drain in a complicated fashion. There is also the possibility of driving some charge into the substrate (see below). To consider these possibilities in more detail, refer to the cross section of an NMOS transistor in Fig 3.8. For gate voltages above threshold, an inversion layer (consisting of mobile electrons) will established beneath the thin oxide in order to mirror the positive charge on the gate. If the gate voltage begins to drop, then fewer electrons will be needed to mirror the reduced gate charge; the resulting electrostatic imbalance impels excess electrons to leave the inversion layer. During normal operation the source and drain voltages are greater than or equal to the substrate potential, and so excess electrons are preferentially attracted toward these terminals. In fact any electrons leaving through the source and drain will result in charge injection errors. However, the source and drain have only a limited capability for removing excess charge. The limitation stems from the resistive nature of the channel. The flow of electrons from the center of the channel toward the drain and source constitutes a current, which causes an ohmic potential drop from the ends of the channel to the center. If this potential drop becomes large enough, the potential at the middle of the channel may actually go below the substrate potential. If this occurs, electrons will be injected from the inversion layer directly into the substrate, instead of to the source or drain. This effect is called charge pumping. From the point of view of the analog circuit designer, charge pumping may be a benevolent effect since it reduces the charge injected to the data node.

2. The second considered block is the subtraction node. The main purpose of this block is to generate the perfect difference between the analog input signal and the output of the DAC. Some typical solution include the use of an operational amplifier (see Fig. 3.9) which has the main purpose to elaborate analogically the difference between them.

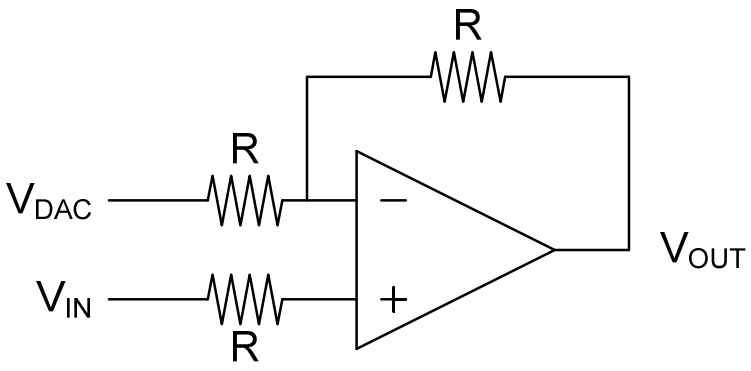

Fig. 3.9: Simple schematic of active subtraction block ($V_{OUT} = V_{IN} - V_{DAC}$).

In this family of solution the good choice of the analog amplifier is at the base of a good operation of the system. Usually, at the input point of an analog to digital converter, as known, the input signal is sampled by the use of a capacitance and also the output of the DAC is regularly commanded from the timing of the clock. In this way, a possible solution to implement a low-power subtraction node is to use a switch capacitor architecture (Fig. 3.10).

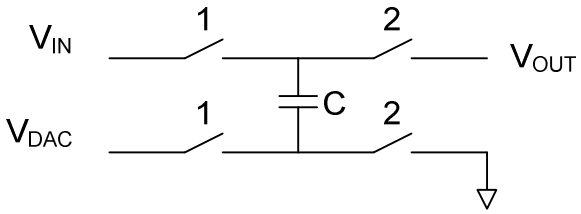

Fig. 3.9: Simple schematic of Switch-Cap subtraction block ($V_{OUT} = V_{IN} - V_{DAC}$).

The main problems about introduced errors in the latter structure are very similar in consistence like the errors introduced in the S&H structure, both about the capacitance and about the switches.

3. The next basic building block token in consideration is the DAC. The accuracy of a DAC is stated in terms of the maximum allowable error in the analog output level. The output error is the difference between the measured and the predicted output level, and is normally expressed as a percentage of the full scale output voltage $V_{REF} = V_{REF+} - V_{REF-}$. As discussed previously, accuracy is not the same of resolution. However, a convert circuit with high accuracy but poor resolution, or vice versa, offers very limited appeal to the system designer. Therefore, from practical design considerations, both the accuracy and the resolution specifications are normally chosen to be comparable. Typical accuracy requirement from a DAC circuit is of the order of ±LSB. This implies that the total allowable output error voltage V_ε for an N-bit converter with a full scale output swing of V_{REF} is

$$\Delta V_\varepsilon = \pm\frac{1}{2}LSB = \pm\frac{V_{REF}}{2^{N+1}} \tag{3.6}$$

Thus, the total percentage error, $V_{\varepsilon\%}$, allowable at the output is

$$V_{\varepsilon\%} = \pm\frac{100}{2^{N+1}}\% \tag{3.7}$$

for ½ LSB accuracy. Thus, the accuracy requirement increases very rapidly as the bit count is increased. For example, a 4-bit converter with ± ½ LSB accuracy can allow a total error of ± 3.12%

at the output; but for 6- and 8-bit converters, the allowable error decreases to ± 0.78% and ± 0.195% respectively. In literature are present a lot of structure which realizes the Digital to Analog Conversion, but in this short introduction about DAC is introduced only a typical low power passive structure, based on switch capacitor architecture. Usually it contains three basic sections: binary switches, voltage references, capacitive network. In the following Fig. 3.10 is shown a typical schematic of a DAC realized with capacitive network. From that picture is possible to observe that each capacitance is initially discharged by turning on the switches called "0". After this initial step are used the switches called "1" or "2" to second that the correspondence bit is equal to level high or low respectively.

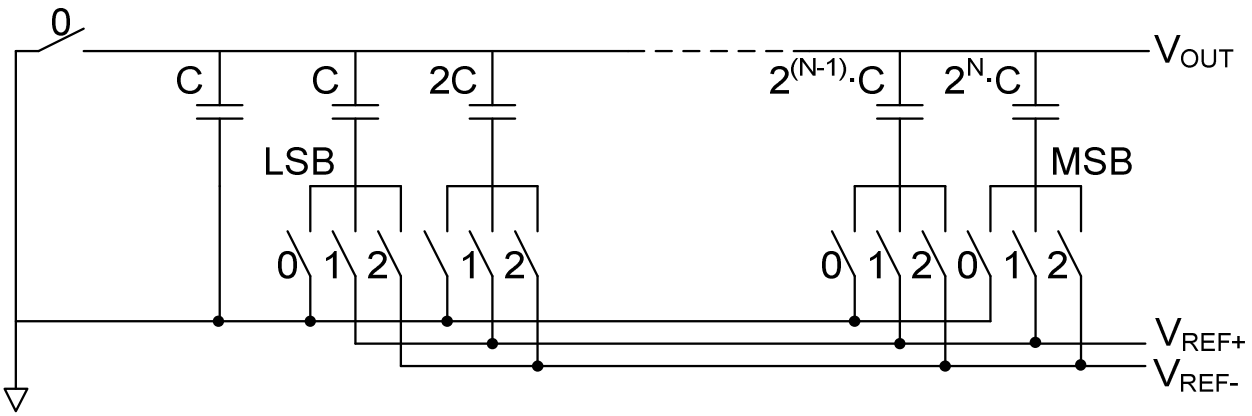

Fig. 3.10: Simple schematic of Switch-Cap DAC.

In this way the output voltage is like a capacitive divider of the voltage $V_{REF} = V_{REF+} - V_{REF-}$. The main errors introduced in this structure are the related to the use of a capacitance and the ones related to the switches realized with MOS transistor (already discussed in S&H block). Another important error can became from the noise introduced by the reference voltages. In fact, as seen before, the proposed DAC can be seen as a capacitive divider of that voltages. Naturally the effects of the noise on that voltages will be reduced to the output but is present in the measure of

$$V_n = \frac{V_{n+} + V_{n-}}{2} \tag{3.8}$$

in the worst case and then the right consideration to do.

Additional error from capacitance is represented by the real obtained value of capacitance in CMOS technology. In fact, as proposed in the schematic of Fig. 3.10, there are more than one capacitance and their value exponentially increases with the bit, therefore to obtain the right value for each capacitance is most important for the DAC operation. The realization in CMOS technology

of a capacitance is done by overlapping two different floor of metal or poly-silicon and separated by a dielectric as oxide of silicon, as shown in Fig. 3.11. The capacitive value of the obtained instance is done by the nominal value (C_0) summed to the relative error (C_ε). The errors are caused by some typical problems in CMOS process which can corrupt the thickness of the dielectric or by the presence of border effects which increase the value of the capacitance linearly to its perimeter. To limit the effects of the ladder errors is possible to implement the system using two identical unitary capacitance for obtaining a capacitance with double value.

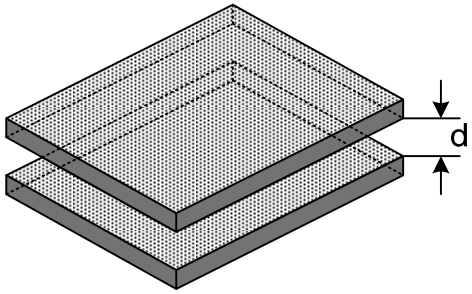

Fig. 3.11: Simple realization of a capacitance.

In this way also the perimeter is double respect to the unitary one, and then the relative effects are negligible. In the other hand, a variation of the thickness is dangerous for the absolute value of the capacitance. These errors can corrupt the right operation of the DAC. In fact the analog output of the DAC is done by the ratio

$$V_{OUT,DAC} = \frac{\sum_{i=1}^{N} C_i \cdot V_i}{\sum_{i=1}^{N} C_i} \tag{3.9}$$

where the value of V_i is done by

$$V_i = \begin{cases} V_{REF+} & if\ b_i = 1 \\ V_{REF-} & if\ b_i = 0. \end{cases}$$

Considering each capacitance can be written as a multiple of the unitary capacitance, is possible to observe that the output voltage of the DAC, done in (3.9), becomes:

$$V_{OUT,DAC} = \frac{\sum_{i=1}^{N} 2^{i-1} \cdot V_i}{2^N - 1} \tag{3.10}$$

and then in the adopted solution the most important thing is to impose the correct ratio between capacitance and not to ensure the absolute value of each one. Therefore the mismatch between the capacitance is the real parameter to keep in account to ensure a correct output to the DAC. The mismatch can be introduced between capacitance by little variation in the process or in the realization of the right capacitance with the right dimensions. The variation in process are avoidably by using opportune layout structure of capacitance, but the random errors introduced in the dimensions are to keep in account. Usually that errors are not depending by the total area of the capacitance, but by the used grid in CMOS process, in fact to use big capacitances can help to reduce the effects of random mismatch between capacitances.

4. The next basic building block token in consideration is the comparator. The main function of a comparator is to deliver an output voltage which represents the results of a comparison between two voltages at its input. Comparators are therefore used in data converters to find the level of an input voltage that can be assigned to one out of 2^N quantization level. In fact, the number of comparators in a certain converter setup is a direct measure of its complexity and cost. The circuit symbol of a voltage comparator is shown in Fig. 3.12.

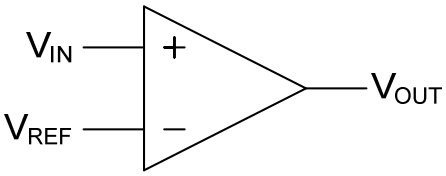

Fig. 3.12: Symbol of a comparator.

The range of comparison of a voltage comparator $V_{min} \leq V_{IN} \leq V_{max}$ is shown on its input/output relationship in Fig. 3.13.

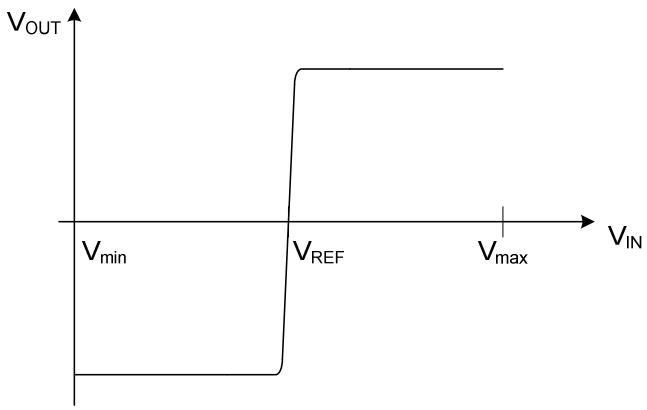

Fig. 3.13: I/O Characteristic of a comparator.

Usually $|V_{max}| = |V_{min}|$ or one of them is equal to zero. The reference voltage V_{REF} (threshold voltage) can assume any value within this range. The output voltage V_{OUT} takes only two levels (logic states). If $V_1 < V_{REF}$, then

$$V_{OUT} = V_{OUT,low} \equiv \text{"0"}.$$

While if $V_1 > V_{REF}$, then

$$V_{OUT} = V_{OUT,high} \equiv \text{"1"}.$$

The transition from logical “0” to logical “1” is not precise in practical comparators, but rather it has a finite width ΔV_{IN} of uncertainty due to the finite gain of the circuit (gain error). This width puts a limit on the number of admissible comparison levels (resolution) within the range $V_{max} - V_{min}$. Therefore it should be made as small as possible. Consider, for example, a 12-bit A/D converter. The required amplification can be determined if the type of logic circuits is known which the comparator has to drive. This determines the difference in level between “1” and “0” from which the necessary amplification is calculated. Besides high amplification, a large bandwidth is also necessary in order to keep the transition time (response time) from one state to the other as small as possible. A measure of these two characteristics is the gain-bandwidth product Gain · Bandwidth. For those reasons, comparators have a structure similar to that of an operational amplifier. However, in contrast to wideband amplifier, comparators are mostly operated in two extreme states, high-level or low-level output, i.e. they are operated in their cut-off region and hence they are overdriven most of the time. Therefore the circuit should be designed to avoid adverse consequences of overdrive, mainly saturation of the transistors. Since comparators operate between these two extremes, the response time is more meaningful than the bandwidth. Also, in an analogy to amplifier terminology, the term “input slew rate” (SR), which gives the maximum rate of change at which the input stage can follow without slew rate deterioration, is a useful specification. In addition, high common mode range is more important than for amplifiers, even if it is obtained at the expense of larger drift, smaller input resistance, and even instabilities within the linear region.

The structure of a comparator is similar to that of an operational amplifier. On the other hand, the response time or delay is more important than the bandwidth. Accuracy is further determined by offset voltage and voltage drift, as well as by offset current, adding to the error budget. Common mode voltage range should be large as well as bandwidth and stability in the tracking mode. MOS technology, while being suitable for high-density low-cost digital circuit functions, has a

number of drawbacks for analog circuits. The absolute values of device parameters, such as threshold voltage which is important in differential amplifier configurations. Therefore MOS comparators are based on *a.c.* coupled amplifiers that are fed by a difference signal obtained by switching the signal and reference voltages to a flip-flop circuit that has been previously pulsed to its unstable operating point. This type of latching circuit is extensively used in dynamic memories as a sense amplifier.

5. The next basic building block token in consideration is the Successive Approximation Register. This register has two main purposes, the first one is to furnish to the output the right digital word at the end of conversion (and eventually the signal End Of Conversion – EOC), the second purpose is to command correctly the DAC in feedback path following the Successive Approximation Algorithm, as already seen at the start of this chapter. To design the digital logic, in every system, is possible to use some CAD designer tools which allows to obtain the right implementation of the functions with opportune digital calculation. Usually the resolution of these tools are not optimized in order of speed and power consumption. The custom design of a simple Successive Approximation Register is possible without to spend a lot of resource for ensure the correct results. The choice to use the way of custom design allows us to obtain a low power circuitry which ensure the right time response.

3.3 State of the art

The actual state of the art, about the realization of A/D data converter has been looked for in the data-sheets of some silicon industry and articles presented in some of the most important conferences or write on some of the most important journals in the world.

The purpose of this work is to realize an optimal A/D converter for very low power application with a medium-high resolution and speed. Other A/D converter has been evaluated with difference bit of resolution with the purpose to keep in mind the optimal goals of our work.

The commercial devices available in market are usually based on solid configuration strategies, which allows to realize devices with high level of accuracy and yield. This considerations are most important for the factories which must keep in consideration also the quality of the product and the economic point of view. There was analyzed the product offered by some factories and the

devices with analogue characteristics are proposed in the table 3.1. To obtain a good comparison between different typology of converters we use the parameter Figure of Merit (FOM) to compare all the considered converters.

Ref.	Device Name	Factory Name	Power Consumption [mW]	SINAD [dB]	F_C [kHz]	FOM [pJ/conv.step]
[5]	AD7466	Analog Device	0.3	69	100	1.3
[6]	ADC101S021	National Semiconductor	2.34	61.5	100	24
[7]	TLC1551	Texas Instrument	40	60.5	7800	6.3
[8]	TSA1005	STMicroelectronics	100	60	20000	6.1

Tab. 3.1: Characteristics of some commercial devices

From the previous table it is apparent that the device proposed by analog device is the one with the best FOM. That device is an A/D converter based on Successive Approximation Algorithm, and then confirm that the best architecture for medium speed and 10-bit resolution, which correspond to a SINAD of 62dB, is the proposed one. The characteristic of that device, and then the purpose for our work, are the power consumption less than 300µW and a figure of merit better than 1.3 $^{pJ}/_{conv.step}$.

There are other consideration to keep in account, in particular the system proposed in some important conference or paper in journal, where in general the best performances are presented. In this optical we consider the A/D converter proposed in the last years.

The graph in Fig. 3.14 shows the FOM of each A/D converter presented on the JSSC or ISSCC, in particular are separated the relative proposal converter by typology of source and also some older systems are reported in the same graph.

From the graph of Fig. 3.14 is apparent that for a resolution of about 10 bit the FOM of the actual state of the art is about 200 $^{fJ}/_{conv.step}$. realized by Jeon [9] with a pipeline structure, but it is justified by the High sample rate at 20MS/s.

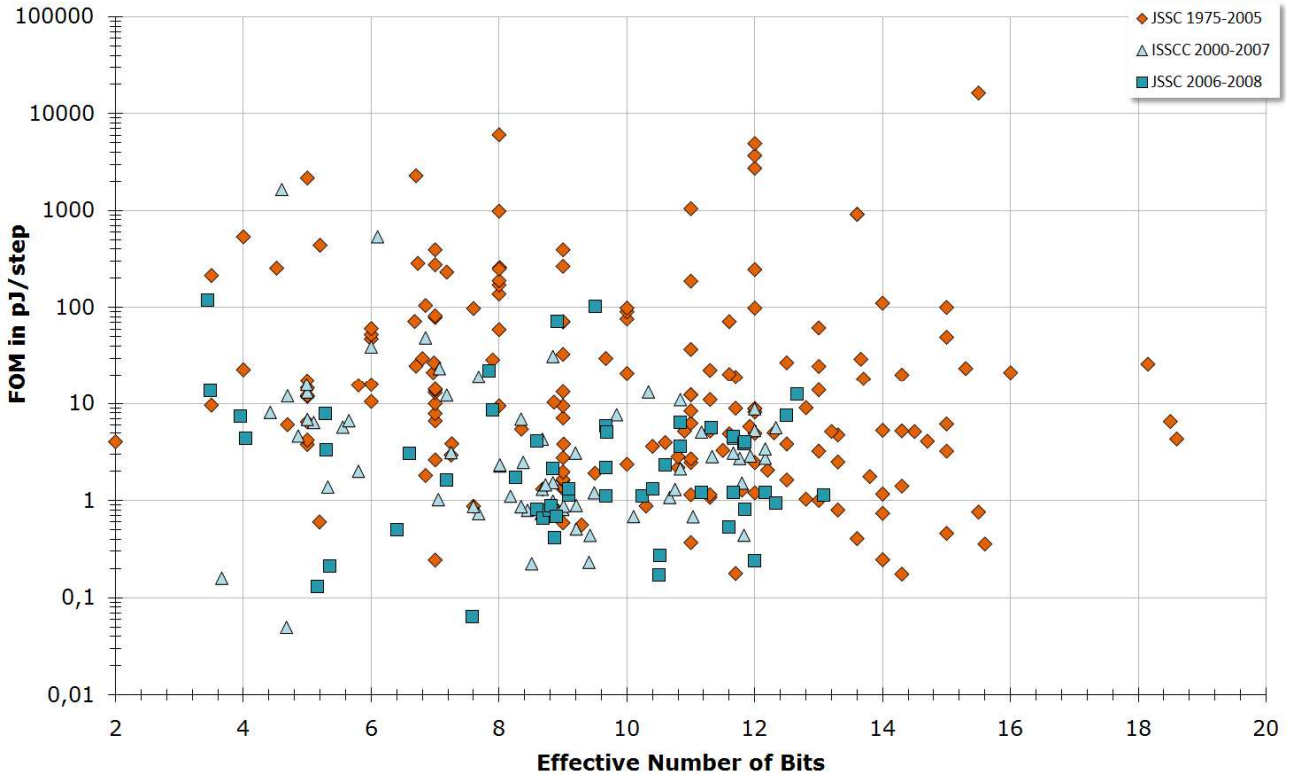

Fig. 3.14: FOM vs ENoB in the last years. (Source: http://www.wulff.no)

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[5] Data Sheets of AD7466 from www.analog.com
[6] Data Sheets of ADC101S021 from www.national.com
[7] Data Sheets of TLC1551 from www.ti.com
[8] Data Sheets of TSA1005 from www.st.com
[9] Young-Deuk Jeon; Seung-Chul Lee; Kwi-Dong Kim; Jong-Kee Kwon; Jongdae Kim; “A 4.7mW 0.32mm2 10b 30MS/s Pipelined ADC Without a Front-End S/H in 90nm CMOS”, ISSCC 2007, pp 456-457.

4

Design of each basic building block

- Principle of Design
- Building Blocks Design
- Prototype Implementation Details

4.1 Principle of Design

The purpose of this work is to design an analog to digital converter with medium-high resolution and speed, but the most important thing is the very low power of the entire system because of application. Therefore the design of each basic building block will be oriented to the reduction in power, in particular will be used the low power architecture for all the design, will be proposed a new way to think the comparator and will be full custom designed the digital logic of the S.A. A/D Converter. These particulars allows to obtain an A/D converter better than the actual state of the art which can be used in the goal applications because of its resolution and very low power consumption.

Design Issues

As with any design involving analog components, there are a number of circuit limitations and trade-offs in S.A. A/D converter design. The design considerations discussed in this section include the kT/C noise, sampling non linearity, comparator offset and mismatch among DAC elements.

1. In switched capacitor based modulators, one fundamental non-ideality associated with using a MOS device to sample a voltage on a capacitor is the presence of a random variation of the sampled voltage after the MOS switch opens. This random component has a Gaussian distribution with a variance of $\frac{kT}{C}$, where k is Boltzmann's constant, C is the capacitance and T is the absolute temperature expressed in Kelvin degree. The variation stems from a thermal noise in the resistance of the MOS channel as it is opening. The noise voltage has a power spectral density of $4 \cdot kT \cdot R$ where R is the channel resistance. This noise is low-pass filtered by its characteristic resistance and the sampling capacitor to an equivalent noise bandwidth of $\frac{1}{4 \cdot RC}$. The total integrated variance will thus be $\frac{kT}{C}$, independent of the resistance of the switch. This first stage sampling capacitors must be sized so as to limit the noise contribution to an acceptable level. From this starting point the used capacitor sizes may be determined.

2. The linearity of the sampling process at the very first input sampling capacitors will be the upper bound of the linearity for the whole converter. Care must be taken to ensure the switches are sufficiently large so that the sampled voltage will be completely settled through their non-linear resistance, but not so large so that any residual signal dependent clock feed-through is

significant. To improve linearity can be used bootstrap switches, but the medium resolution don't require this particular solution.

3. The comparison done by the comparator can be corrupted by a constant error because of the offset of the comparator. The offset is present in a comparator because of the non symmetrical design (systematic offset) or by the mismatch between the elements which are included in the design (random offset). The systematic offset can be negligible with a good design, while the mismatch between transistor is done by the technology, and the most important thing is to taken in account the effects of this errors and keep them under the ½ LSB level.

4. The standard deviation of an integrated capacitor is given by:

$$\frac{\Delta C}{C} = \frac{k}{\sqrt{C}} \tag{4.1}$$

where k is a constant depending on technology.

The larger it becomes the number of DAC levels, the smaller it becomes the unit size element size and the bigger its variance. Mismatch power results in harmonic distortion and in a higher noise floor.

Effects on Resolution

Due to the previous considerations, the noise due to three main non idealities (thermal noise of sampling switch, linearity in S&H block and mismatch among DAC elements) depends exclusively on the chosen capacitor size. Besides these errors have the same transfer function of the input signal, therefore the introduced error has to be less then ½ LSB.

Instead the errors introduced by the offset of the comparator depends by the mismatch between the elements which are include in the comparator design. The purpose is to reduce the offset less then ½ LSB to make negligible its effects on output. To obtain this goal is possible to design keeping in account the mismatch on each elements or to include a possible auto-zero algorithm for reduce its value.

Choices of Design

The goals of this work are depends by the required application. The main purpose, as already seen, is the low power in the comparison. To obtain this goal is possible to use a technology which allows to use a low voltage power supply, as 1V or 1.2V. In this way the input range of the A/D converter will be reduced to 0.8V to ensure a correct linearity. As seen in the previous chapter the

state of the art has a FOM of about 200fJ/conv. step, then our goal is to improve this value at least a factor 2. Besides the resolution has a goal of then 10 bit or little more.

In the table 4.1 are resumed the value of goals of design and some important choices as the power supply and FOM.

Characteristic	Value
Supply Voltage	$1.0 \div 1.2\ V$
Sample Rate	$100\ \frac{kS}{s}$
Figure Of Merit	$< 100\ \frac{fJ}{conv.step}$
Power Consumption	$< 5\mu W$
Input Range	$0.8\ V$
Resolution Bit	$10 \div 11\ Bit$
LSB	$780 \div 390\ \mu V$

Tab. 4.1: Summary of main goal of this project.

4.2 Building Blocks Design

In this paragraph are explored the followed design way to realize each basic building block of the Successive Approximation A/D converter. As seen in the previous chapter, and is apparent from the Fig. 3.2, the main block which are at the base of a S.A. ADC are: comparator, S&H, subtraction node, DAC and, SAR with digital logic. The first analyzed block is the comparator.

Comparator

Usually, the conventional scheme used to realize a low power comparator is done in Fig. 4.1.

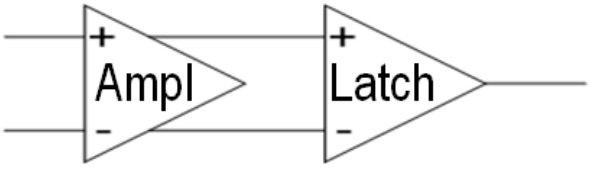


Fig. 4.1: Typical realization of a comparator.

The latch has the purpose to saturate its output voltage to V_{DD} or V_{SS} according to its inputs. In general a latch has the main purpose of the comparator, but it can response correctly only if its input differential voltage is enough large (typically > 20mV) to ensure the right accuracy in its operation. To overcome this limit is usually used to apply a preamplifier before the latch which has the purpose to amplifier the input signal. In our case it is necessary to use because the LSB is 390μV and then the required gain of the preamplifier must be at least 52 which means 34dB.

To consider the power consumption required by the preamplifier we consider the usual adopted scheme proposed in Fig. 4.2

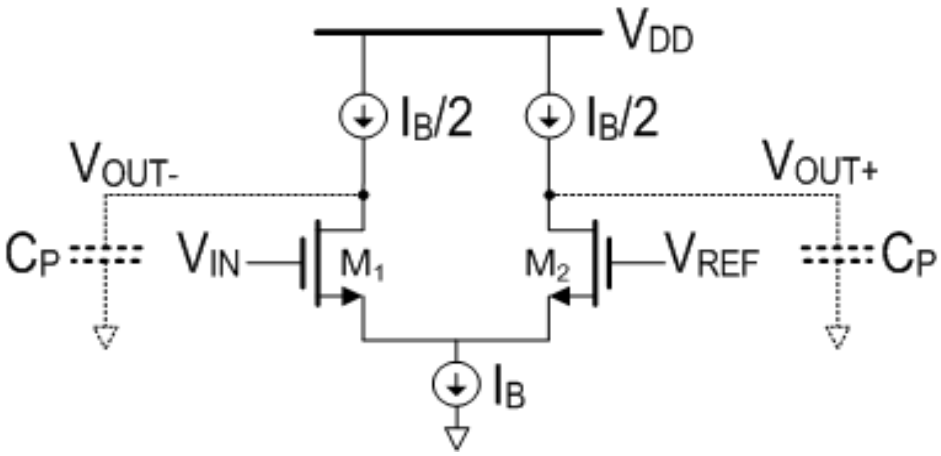


Fig. 4.2: Typical realization of a pre-amplifier.

In that realization of amplifier the dynamic gain is done by:

$$V_{OUT} = V_{IN} \cdot \frac{g_m \cdot T_P}{C_P} \tag{4.2}$$

where T_P is the pre-amplifier time.

Under the hypothesis of input pair in sub-threshold operation the 4.2 becomes:

$$V_{OUT} = V_{IN} \cdot \frac{I_B/_2 \cdot T_P}{m \cdot V_T \cdot C_P}. \tag{4.3}$$

Assuming m = 2.75, T_P=357ns, C_P=40fF and imposing a gain of 43dB, which allows a margin because of eventual technology errors, the required I_B is equal to 2.2µA. Then a power supply of 1V allows to consume only 2.2µW for the pre-amplifier.

The second step to obtain a comparator is the design of the latch. The usual structure used for low power latch id done in Fig. 4.3.

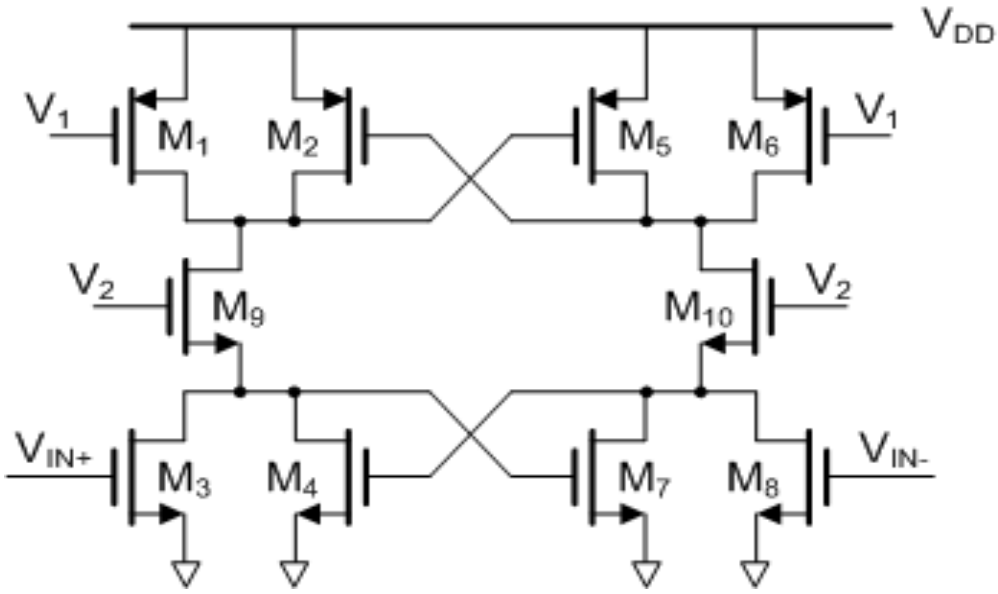


Fig. 4.3: Typical realization of a latch.

The power consumption of the schematic proposed as latch, under the power supply of 1V allows to consume only 2.5µW. This value is obtained with random changing of the output value by simulation in the required technology.

Then the realization of a comparator should be 4.7µW if the realization of the comparator uses the usual low power structure.

The purpose of our work is then to obtain a comparator with very low power and to obtain this goal we will use a non conventional way to realize the solution. In particular the proposed solution, proposed in Fig. 4.4, includes the use of two voltage to time comparator and a logic which

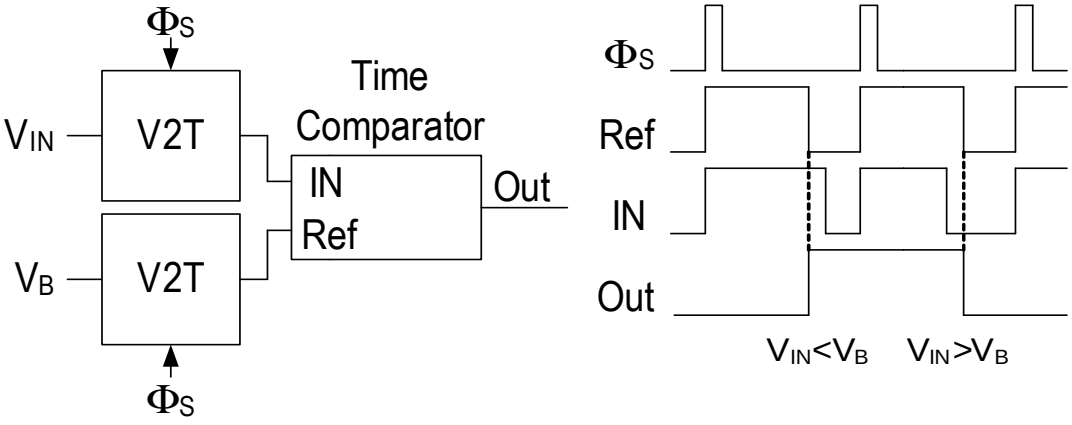


Fig. 4.4: Block diagram of the proposed solution for comparator.

compares the time delays.

The time diagram shows the behavior of the Φ_S signal and the reference voltage V_B and shows also how the digital output changes depending on the input signal. The function of the block called "V2T" is to convert the amplitude of the input voltage into delay time from the raise edge of the clock. The next block, in cascade with the two V2T has the purpose to compare the delay times and choice if the V2T referred to input voltage is faster or slower than the V2T taken as reference. Then the output of the comparator (Out) is equal to logic level "1" or "0" according with the amplitude of V_{IN} is less or more than reference voltage V_B respectively.

To use this schematic block requires to design the voltage-to-time converter with low power philosophy. To obtain that result it is proposed the schematic in Fig. 4.5.

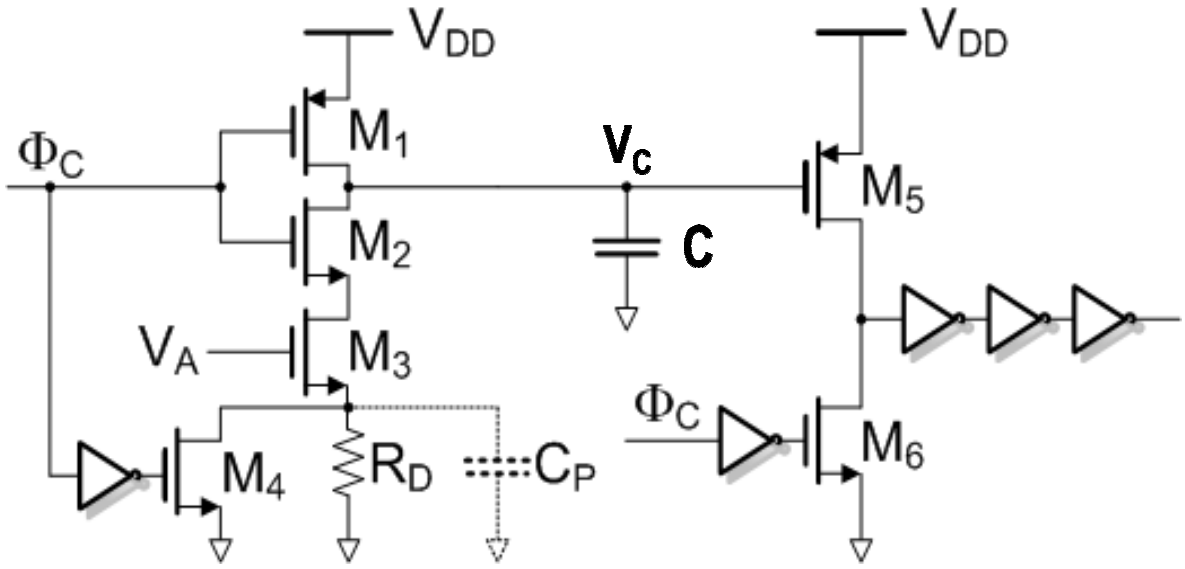


Fig. 4.5: Schematic of the proposed solution for V2T.

The supply voltage is V_{DD}=1V to ground. When the phase Φ_C is low, the transistors M1, M4 and M6 are ON while the transistors M2, M3 and M5 are OFF. Therefore the initial conditions include that the capacitance C is charged to V_{DD} and the parasitic capacitance C_P is completely discharged. The input voltage V_A, applied on gate of transistor M3, is a constant voltage during each single conversion. The conversion starts when Φ_C raises and the initial step is the V to I conversion by transistors M1, M2, M3 and the resistance R_D, which work as a constant current generator. This current is used to discharge the capacitor C, and then it has a constant discharge. When the voltage V_C, across the capacitor, falls below the threshold of transistor M5, the output of entire V2T raises. The presence of some inverter at the output has the only purpose to obtain a square wave with good edge in transitions.

The issues of this configuration are the $\frac{kT}{C}$ of the capacitance C and the thermal noise on the threshold of transistor M5. In fact as is possible to observe in Fig. 4.6, the first contribution, done by capacitance, influences the right starting value to discharge the capacitance, while the thermal noise on transistor M5 change the level of its threshold. Both components have the consequence to modify the value of delay. Both ones can be considered has an input offset, in fact to compensate the $\frac{kT}{C}$ noise is possible applying the voltage $V_{in,n1}$, and the thermal noise can be compensated by the voltage $V_{in,n2}$ at the input, as proposed in Fig. 4.6.

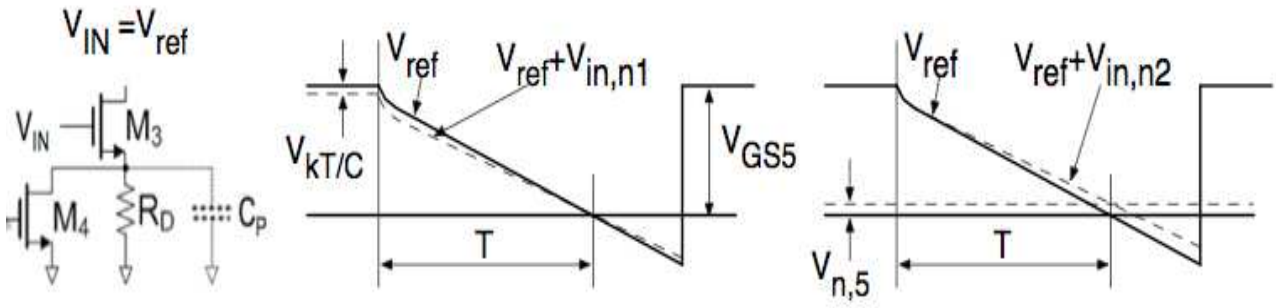


Fig. 4.6: Time diagram of some issues in V2T converter.

The two considered contribution have the same effects, then is possible to calculate the equivalent input noise as:

$$V_{in,n} = \sqrt{V_{in,n1}^2 + V_{in,n2}^2} = \sqrt{V_{\frac{kT}{C}}^2 + V_{n,5}^2} \cdot \frac{V_{ref} - V_{GS3}}{V_{GS5}} \tag{4.4}$$

Considering the LSB equal to 390µV and the limitation to impose $V_{in,n}$ < ½ LSB, and assuming that the voltage across the resistance R_D is nominally equal to 0.15V and the threshold of PMOS is equal to 0.4V, a possible trade off between size of transistor and capacitance bring us to choose a capacitance of 0.8pF and a thermal noise on transistor equal to 50nV. With these parameters is possible to calculate the equivalent noise referred to the input is equal to

$$V_{in,n} = \sqrt{V_{in,n1}^2 + V_{in,n2}^2} = \sqrt{101^2 + 150^2} = 180\mu V. \quad (4.5)$$

The next step is the design of the block which realizes the time comparator. The operation principle of this block is to determine which signal is the first to raise. A simple method to implement this algorithm is the use of a Delay Flip Flop (DFF). In fact if we connect the output of the V2T correspondent to the input signal to the input called “D” of the flip flop and the output of the other V2T to the input called “Clock” of the flip flop then we will obtain a right time comparison.

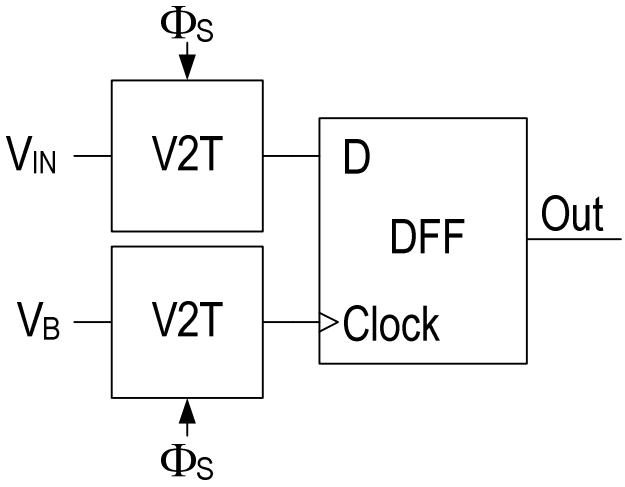


Fig. 4.7: Realization of the converter.

The operation of the DFF is to copy to its output the assumed value of the D input in the same instant of time when the Clock signal raises. In this configuration, naturally, the value of reference voltage V_B ensures the edge at the output of its V2T, while the output of the V2T correspondent to the input signal can raise before or it is able not raise. This way doing, when the Clock signal raises “read” the value of the D signal, and then if D signal raised before the output becomes “1”, while if D signal still has to raise the output becomes “0”. The implementation of this block whit a simple DFF introduces only the errors referred to the respect the hold or the setup time to ensure the correct

operation of the flip flop. Really these time will not respected, but our considerations will be on the noise in time on transition level. Some simulation on library DFF bring us to consider an equivalent input noise voltage, on V_B, of about 73µV. This result, united to the other noise contributions, have a total equivalent input noise of

$$V_{in,tot} = \sqrt{180^2 + 73^2} = 194\mu V,$$

which corresponds to a little bit less than ½ LSB.

The power consumption of the full comparator is done by the power consumption of each V2T and the power consumption of the DFF. The V2T requires the charge to V_{DD} of the capacitance, and after there is its slow discharge. The V2T connected to V_B is opportunely designed to obtain the transition at about the end of comparison and then the capacitance will be discharged only part of it one. While the power consumption of the other V2T depends to the value of V_{IN}, in fact an high input voltage can discharge completely the capacitance, while a little input voltage should not discharge the capacitance. Whit these hypothesis, it is possible to suppose that the energy of each V2T for one conversion step is about the half of the energy spent on a capacitance which discharges itself completely from supply voltage. This one is a reasonable hypothesis because the input voltage can discharge completely the capacitor or cannot discharge the capacitor with the same probability. The power consumption of the DFF is very low, in fact with a clock of 1.4MHz (14 clock period allows to obtain the required sample rate of 100kS/s) it consumes only 50nW. Therefore results

$$P_{CS} \cong f_S \cdot N_{BIT} \cdot 2 \cdot \frac{1}{2} \cdot \left(\frac{1}{2} \cdot C \cdot V_{DD}^2\right) + P_{TimeComparator} \cong 1\mu W \tag{4.6}$$

To adopt this solution, proposed completely in Fig. 4.8, for the comparator allows to reduce the power consumption of the comparator from the estimated 4.7µW of typical solution to about 1µW.

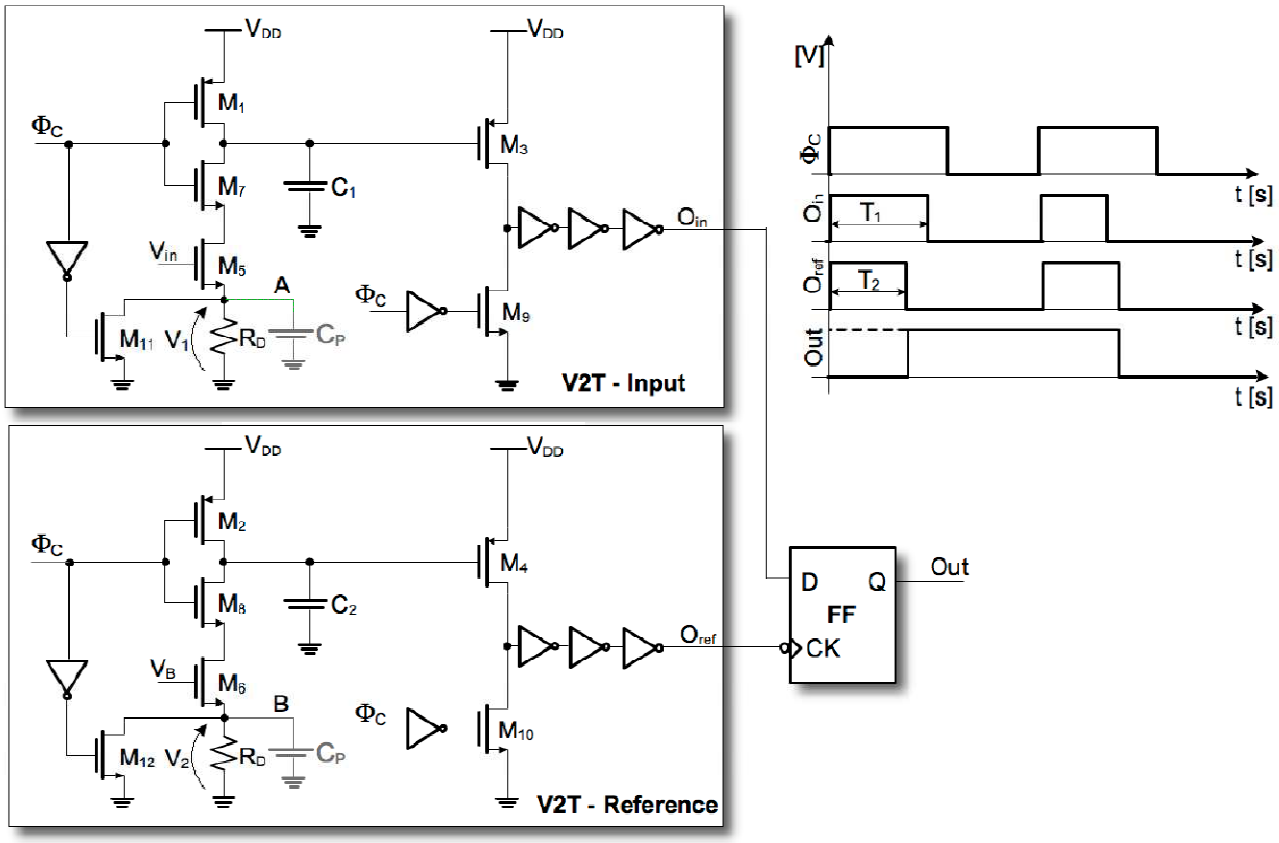


Fig. 4.8: Complete scheme of a used low power comparator.

As seen in the previous chapter, the high precision of the comparator is very important because the offset error is reported to each done comparison. Therefore is much important that the offset value is kept less than ½ LSB. In this type of comparator the offset is done by the mismatch between each single element: the resistance, the capacitance, the transistors M5 and M3. In fact they determine the real value of the sampled voltage in the capacitance, the current which flows with reference voltage, the value of the threshold to compare. In this way is very difficult that each component will be designed so big for respecting the mismatch specification, then it is mandatory to include a circuit for offset cancelation, after chip fabrication. The adopted solution can include the variation of only one element, which will change its value to compensate all the mismatch errors introduced also by the other elements. The simplest way to obtain this calibration is to use a trimmed resistance. Obviously it is not possible to implement a trimmer on silicon, but it is possible to implement the resistance a series of high number of resistance and then to choose the right "point of input" by an opportune array of switches, as shown in Fig. 4.9. The implementation of this solution is possible by using transistors as switches and manually choosing the right combination of switches by an opportune binary code from external.

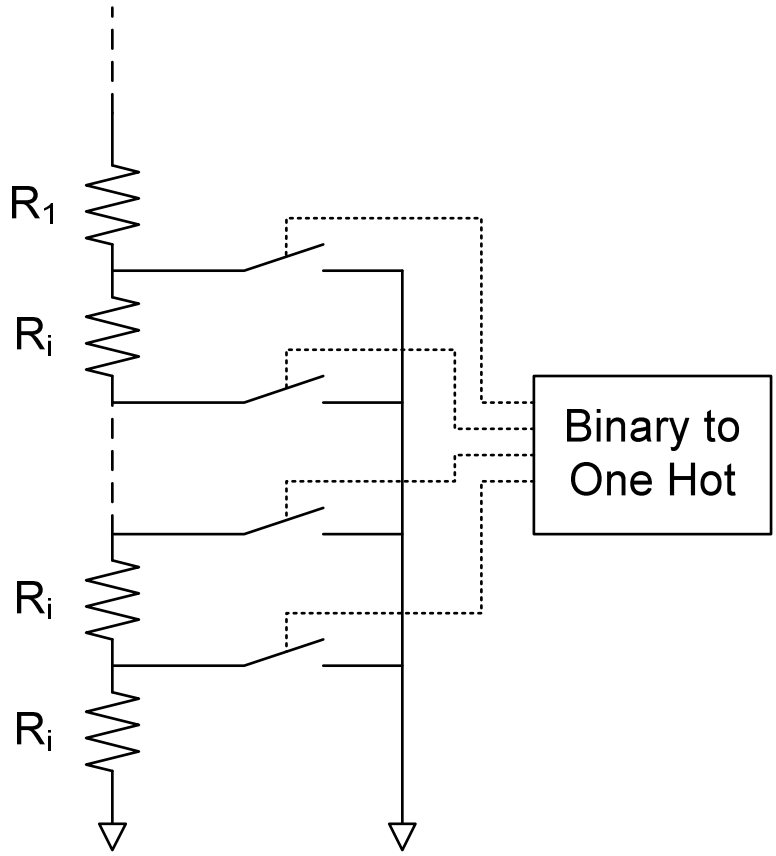


Fig. 4.9: Realization of the resistance for compensating the offset.

S&H – Subtraction node – DAC

To design a low power DAC is possible by avoiding the amplifiers. A possible way can be the use of switched capacitors structure which allows to obtain the right analog value at the output by switching some capacitances. A typical switched capacitors structure in Fig. 4.10 is given.

The main characteristics of this structure are that it:

- has no static power consumption;
- has a dynamic power proportional to the total capacitance used;
- has a total capacitance equal to 2^N times the unitary capacitance C_u;

therefore is possible to reduce the value of the unitary capacitance for reducing the power consumption. The entire structure of capacitance can be used also as S&H block simply sampling the value of the input signal on all the capacitance, in this way the capacitance continues to divide opportunely the reference voltages to obtain the correct value of the DAC output, but the charge accumulated on the capacitance subtract the sampled input signal from the ideal DAC output.

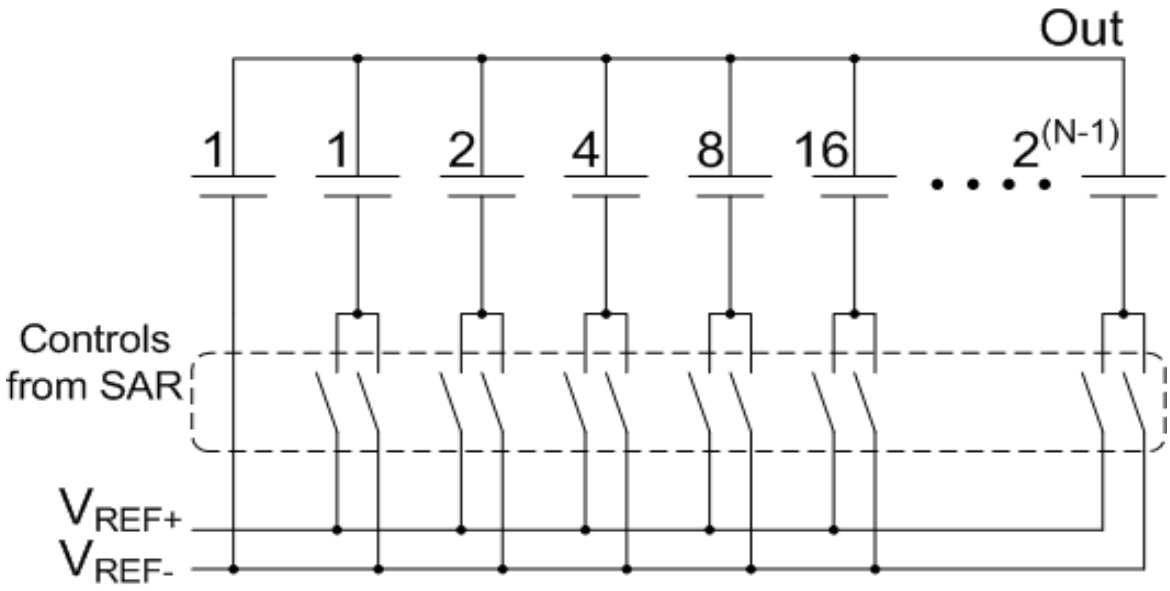


Fig. 4.10: Typical structure of low power DAC.

To use this solution, proposed entirely in Fig. 4.11, allows to reduce the errors in charge transfer between different stages of signal elaboration. The sample phase in this structure includes a differential sample because of the comparator. In fact the comparator does the comparison respect to a reference voltage V_B opportunely designed for obtaining a good performances in the operation of the same comparator. Therefore is opportune that the sample phase include the subtraction of the voltage V_B from the obtained sample, and this operation is obtained by connecting on plate of all the capacitances to the input voltage and the other plate to the voltage V_B. Ended the initial sample phase, the structure starts the continuous change of the value of the bit following the successive approximation algorithm. The correct value of the output is ensured because of the open circuit in one side of the capacitances, then it is not possible to have change of charge with external point of the circuit, but only between capacitances.

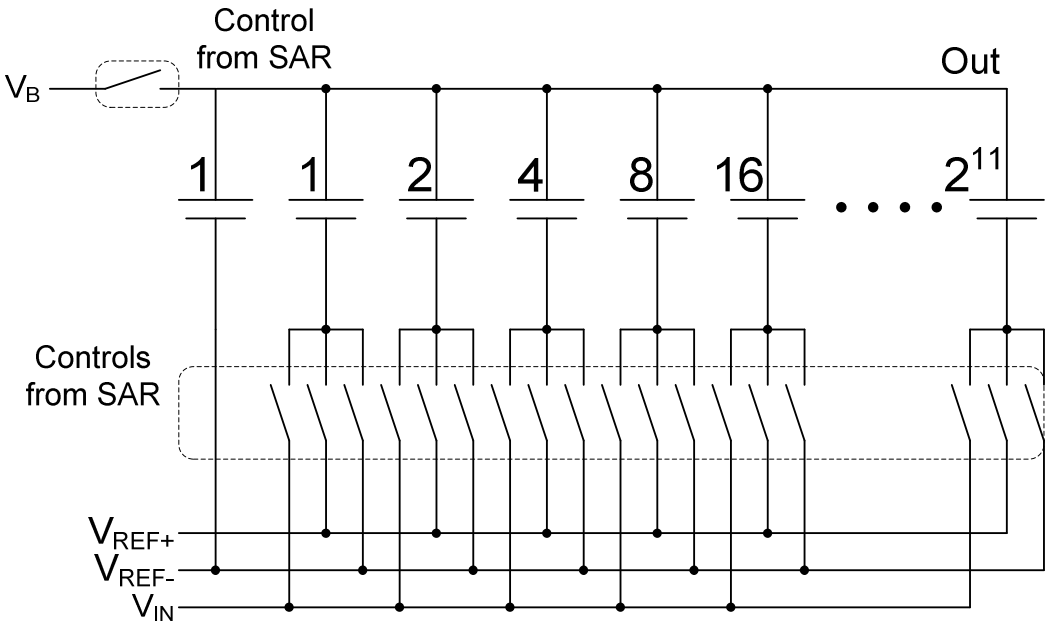


Fig. 4.11: Structure of low power DAC used also as S&H and subtraction node.

The design of this structure include to keep in account the usual errors introduced by capacitances. The first considered noise is the $\frac{kT}{C}$. Naturally all the capacitances have the purpose to sample the input and then the $\frac{kT}{C}$ limit impose the minimum value of the sum of all the capacitances. In particular it is necessary impose that the power of the introduced noise must be less than the power of the quantization noise, then results

$$\frac{kT}{C_{TOT}} < \frac{\Delta^2}{12}; \frac{kT}{C_{TOT}} < \frac{1}{12} \cdot \left(\frac{V_{Range}}{2^N}\right)^2; C_{TOT} > 0.83pF \tag{4.7}$$

This value of total capacitance means that the required value of the unitary capacitance C_u must be at least 0.4fF, but this value is very low, therefore this limit doesn't represent a very limit because of other technology factor. But the design of the capacitance relatives this block must also take in account the mismatch among the capacitances, in fact the correct operation of the DAC depends from it one. Then it is required that

$$2 \cdot \frac{\Delta C_{MAX}}{C_u} \cdot \sqrt{2^{N-1}} = \frac{2 \cdot k_C}{\sqrt{w \cdot l}} \cdot \sqrt{2^{N-1}} < \frac{1}{2} \tag{4.8}$$

Where the k_C of the our technology is equal to 0.003 and a correct design at 3σ for 11bit requires an unitary capacitance of at least 8.2fF. But also this value doesn't represent a real limit, in fact the parasitic effects on capacitances and other limits imposed by the used technology impose us

to use capacitance of at least 30fF, value which allows us to satisfy all the limits in noise and mismatch.

The power consumption of the capacitive structure which realizes the DAC, S&H and subtraction node is determined by the value of the total capacitance. Therefore 11bit structure has a total capacitance equal to $2^{11} \cdot C_u = 2^{11} \cdot 30fF \cong 61pF$. To estimate the power consumption of this structure is possible to calculate as

$$P_{11bit} = f_S \cdot \sum_{i=1}^{11} E_i \cong f_S \cdot \frac{1}{2} \cdot C_{TOT} \cdot V_{ref}^2 \tag{4.9}$$

because the capacitor are charged only one time per each sample. There is also the power consumption of the initial step of sampling, which can be calculate, in average, as

$$P_{Sample} = f_S \cdot \frac{1}{2} \cdot C_{TOT} \cdot \left(\frac{V_{Range}}{2}\right)^2 \tag{4.10}$$

because the real power consumption is a function of the input voltage, and then we consider a charge/discharge of about half range. Then the total power consumption include, at 100kS/s, the power of 2µW for the DAC and about 0.5µW for the initial sampling, therefore a total power consumption of about 2.5µW.

In order to reduce the power consumption of the DAC structure is possible to taken in account some different structure which allow to reduce, with alternative scheme, the value of the total capacitance and then the total power consumption. The possible solution should be the “bridge solution”, as presented in Fig. 4.12. This solution allows to reduce the capacitors count by dividing the capacitive array into two parts separated by an attenuation capacitance, C_x. The maximum switched element in the array of the right side is $2^{N/2-1}C_u$ while the lowest one is C_u. Thanks to an attenuation factor equal to $2^{N/2}$ the biggest element of the left array is $2^{N/2-1}C_u$ instead of $½C_u$ allowing to convert N/2 bits and having C_u to represent the LSB.

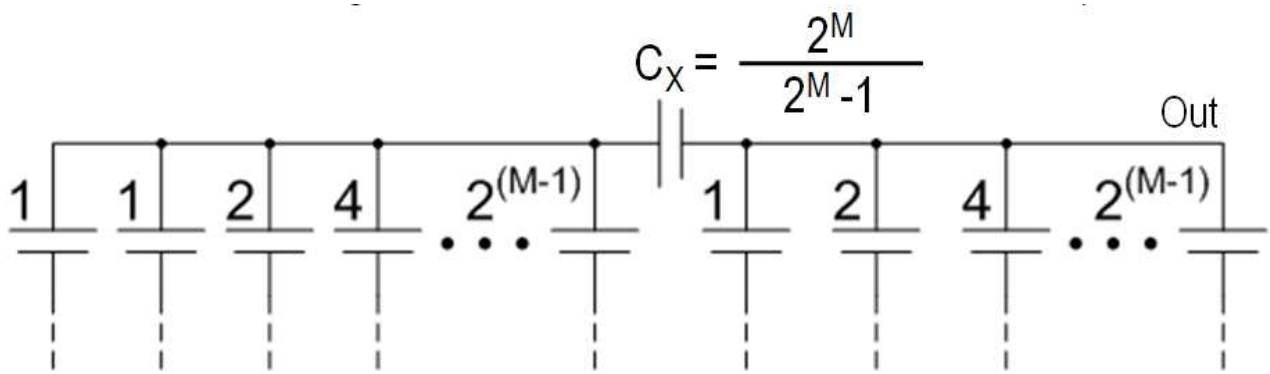


Fig. 4.12: Structure of low power bridge solution DAC.

Summing up, the capacitances count goes from 2^N down to $2 \cdot 2^{N/2} - 1$. The series of attenuation capacitance and the entire right array must equal the C_u

$$\frac{C_x \cdot 2^{N/2} \cdot C_u}{C_x + 2^{N/2} \cdot C_u} = C_u \tag{4.11}$$

which yields the value of C_x

$$C_x = \frac{2^{N/2}}{2^{N/2} - 1} \cdot C_u \tag{4.12}$$

Unfortunately the value of C_x is a fraction of C_u: obtaining the necessary accuracy requires care in the layout. Another little disadvantage of this structure is that it requires an even number of bit, but usually the advantage of capacitance reduction is so high that it is possible increment eventually the number of bit to ensure the correct operation of the circuit. While the main advantage of this solution is the reduction of the total used capacitance and then the occupation of less area on silicon, in fact the required capacitance for 12bit structure is equal to

$$C_{TOT} = \left[2^{N/2} + \left(2^{N/2} - 1\right)\right] \cdot Cu = 127 \cdot Cu \tag{4.13}$$

The result is very good for our converter, but the realization of the attenuation capacitance C_x is really difficult, in particular if we want to ensure a correct operation of the circuit with small value of unitary capacitance C_u. In this way an alternative solution has been adopted which includes the use of two arrays of capacitance but using an attenuation capacitance equal to unitary

capacitance. To change this value of attenuation capacitance requires to modify the first array of capacitance as shown in Fig. 4.13.

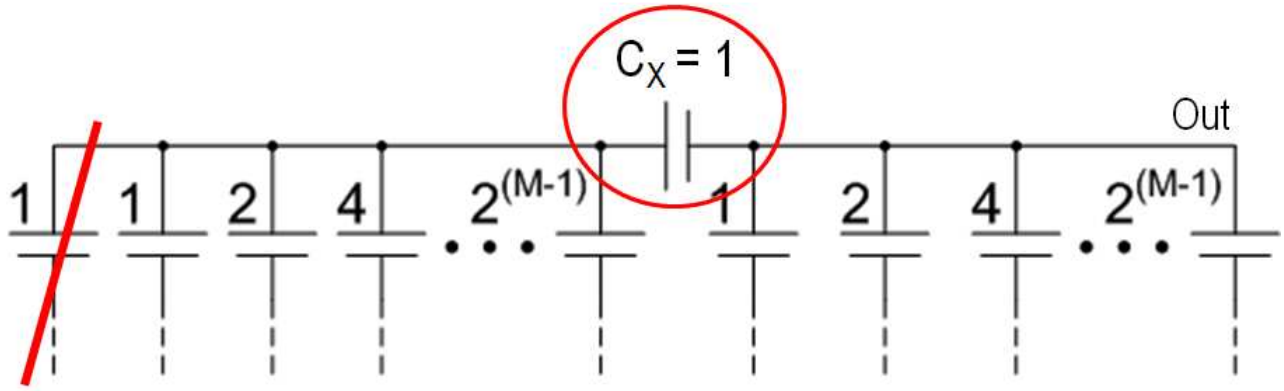


Fig. 4.13: Structure of low power modified bridge solution DAC.

The proposed solution with modified bridge architecture has the main advantage of to reduce the problem in ratio between capacitances because also the attenuation capacitance is equal to unitary capacitance. But this solution doesn't realize the perfect DAC characteristic, in fact it introduces some errors. To analyze the introduced errors by the use of a 12bit structure we simplify the study by calling in different way the main part of the system, as shown in Fig. 4.14.

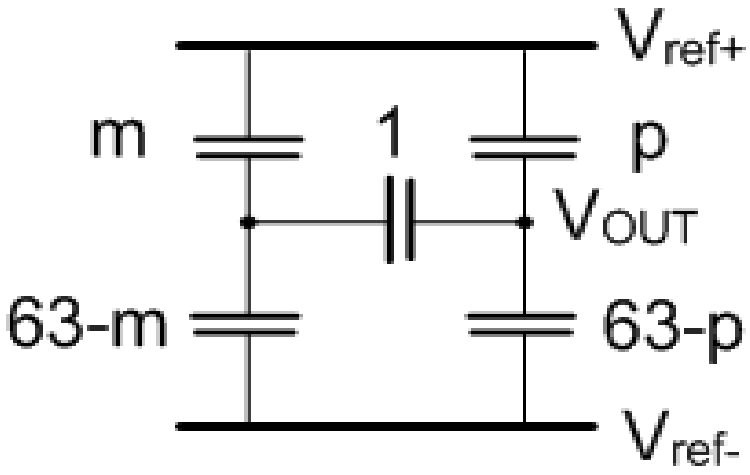


Fig. 4.14: Simplified structure of the DAC for studying introduced errors.

With this simplified scheme is possible to calculate the value of the output voltage as a function of the digital word in input, in particular it is equal to m+64·p. Under this hypothesis, and supposing that all the capacitance are completely discharge, the output voltage is equal to:

$$V_{OUT} = \frac{4096}{4095} \cdot \frac{m+64 \cdot p}{4096} \cdot \left(V_{ref+} - V_{ref-}\right). \quad (4.14)$$

Therefore it is apparent that the introduced error is only a gain error with a maximum of 1 LSB at the end of the dynamic range. Besides it is possible to consider that a possible offset between the voltages V_{ref+} and V_{ref-} can be useful to compensate this gain error. Then the choice of the DAC reverts on this solution with matched capacitances.

The total capacitance of the proposed solution is equal to

$$C_{TOT} = [2 \cdot (2^{N/2}-1)] \cdot C_u \quad (4.15)$$

which is equal to $126 \cdot C_u$ for a 12bit (6+6) solution.

The used of two arrays of 6 bit each one is obligated, in fact this configuration is only possible with the inclusion of two identical arrays. As seen before the limits calculated for the previous structure are kept also in this one, therefore it is mandatory to impose a total capacitance at least 0.83pF because of $\frac{kT}{C}$ noise which imposes, in this structure, a unitary capacitance of at least 6.58fF. The mismatch, instead, must be particularly precise because the attenuation capacitance realizes a factor of multiplication of the error. In particular the factor is equal to $2^{N/2}$, which implicates to require a unitary capacitance equal at least 65.6fF. In this way, because of safety margin, the unitary capacitance will be realized of 120fF and then the total capacitance is equal to 15.12pF, well low then 61pF required from the previous configuration.

Under the same simplifier hypothesis of the previous case for the calculation of the power consumption, and to taken in account that the number of bit is equal to 12, the new formulas to calculate the power consumption are

$$P_{DAC} = f_S \cdot \sum_{i=1}^{12} E_i \cong f_S \cdot \frac{1}{2} \cdot C_{TOT} \cdot V_{ref}^2 \quad (4.16)$$

for DAC and

$$P_{Sample} = f_S \cdot E_S = f_S \cdot \frac{1}{2} \cdot C_{TOT} \cdot \left(\frac{V_{ref}}{2}\right)^2 \tag{4.17}$$

for initial sampling step.

Then the adopted solution, completely proposed in Fig. 4.15, allows to reduce the consumption from 2.5µW to 605nW.

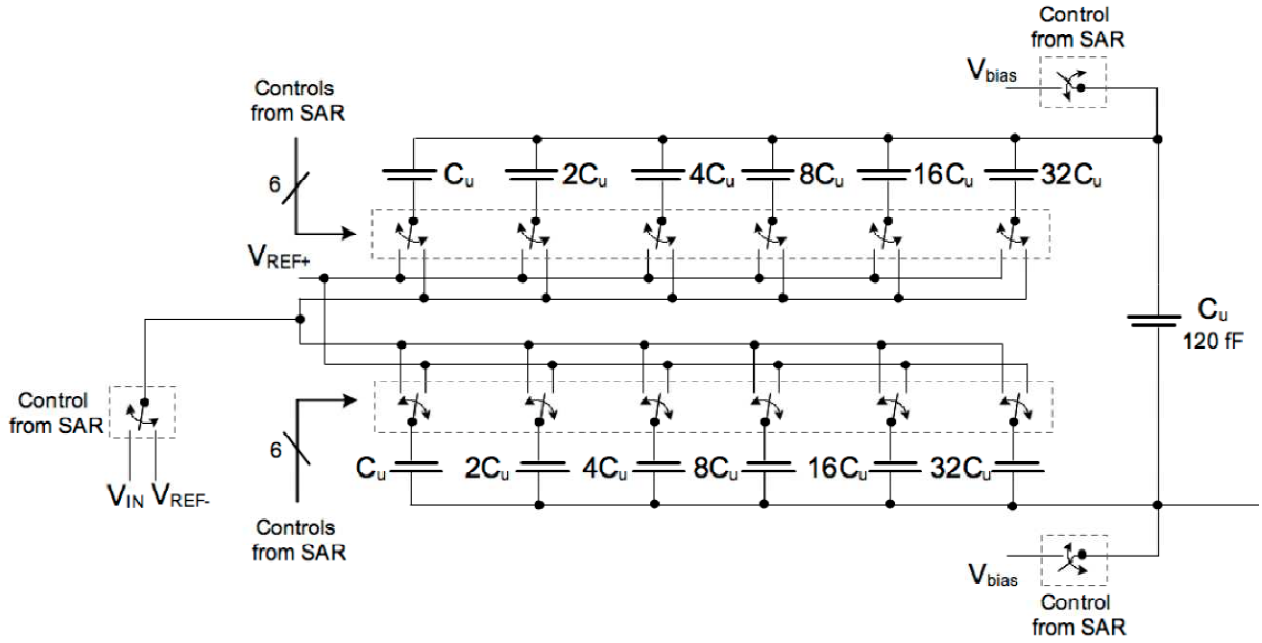


Fig. 4.15: Proposed solution for S&H, subtraction node and DAC.

Digital Logic (S.A.R.)

The last main block to design for obtaining the entire system of converter is the digital logic. As seen in the Chapter 3, the main functions of digital logic are to memorize the sequence of bit in output from comparator and realize the successive approximation algorithm for proponing the right sequence of data to DAC. In order to realize these function, the digital logic is divided in same functional blocks as shown in Fig. 4.16. The block called “Phase Generator” has the purpose to indicate to the “logic” on which bit the comparator is working, the “logic”, instead, is the mind of successive approximation algorithm, ending there is the “PIPO Register” which has the function to sample the digital word at the end of conversion and hold it for all time required by the successive conversion steps.

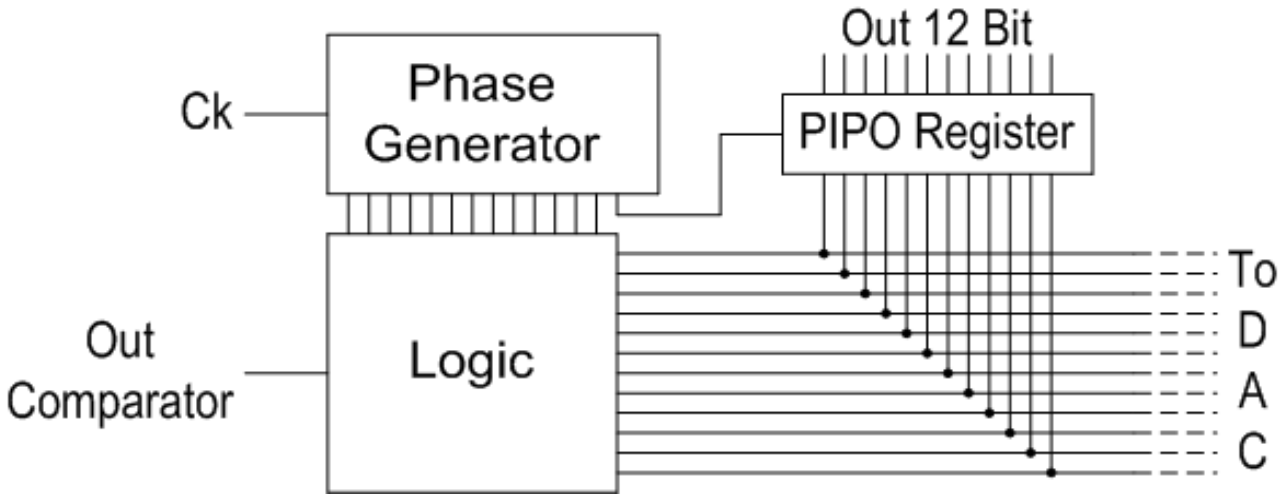


Fig. 4.16: Main functional blocks in digital logic.

The realization of each block has been done by full custom design. In particular the “Phase Generator” is designed with a cascade of DFF in series, as shown in Fig. 4.17. This structure has the purpose to indicate on which bit the converter is working.

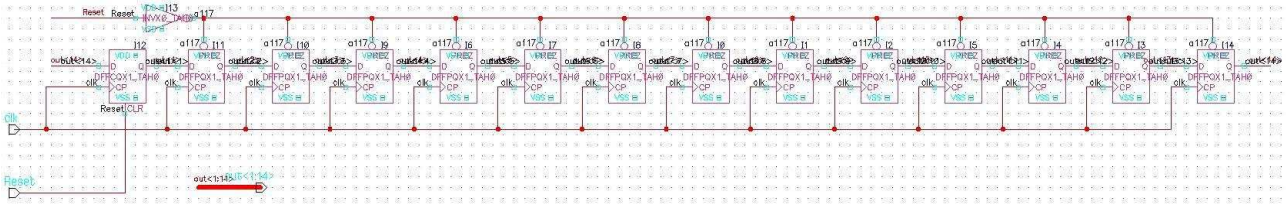


Fig. 4.17: Chain of DFF for generating a cyclic counter one hot.

To obtain this goal there is an initial phase of reset during which all the DFF except the first one are set to logic level “1”, while the first one is set to “0”. During next steps the DFF continues to ‘transfer’ the “0” from 1st to 2nd, and then from 2nd to 3rd, and then from 3rd to 4th, and so on. When the 14th is “0” then the transfer is done means that the first sample is ready and then it is possible to transfer from 14th to 1st for restarting the transfer from the 1st to the other and obtaining another sample of the input. This principle of operation is like to have a counter with 14 bit and continually to count from 1 to 14 with one hot system.

The “Logic” block can be realized with twelve identical cells which have two main purpose: 1. to set respectively bit to logic level “1” when start its phase, 2. to copy the output of the comparator as soon as it have finished its comparison. The realization of a simple cell of these ones is based on the Set-Reset Flip Flop (SRFF), as shown in Fig. 4.18. The correspondent output of the “Phase Generator” enters in the pin called “NOT_Phi”, and then, as soon as that pin becomes “0” the SRFF set to “1” its output. The signals “Comp” and “Comp_ready” are the signal which

indicate when the comparator is working and when the output of the comparator is ready respectively. In this way, if the all the signal confirm that the bit is the right one, the comparator is ready and its output is right, then the signal reset of the SRFF follows the value of the output of the comparator, which enters in the cell by pin called “Sampl”. This way doing, if “Sampl” is “1” the Reset should not operate and the output is kept to “1”, while if “Sampl” is “0” the Reset should operate and the output is resettled to “0”.

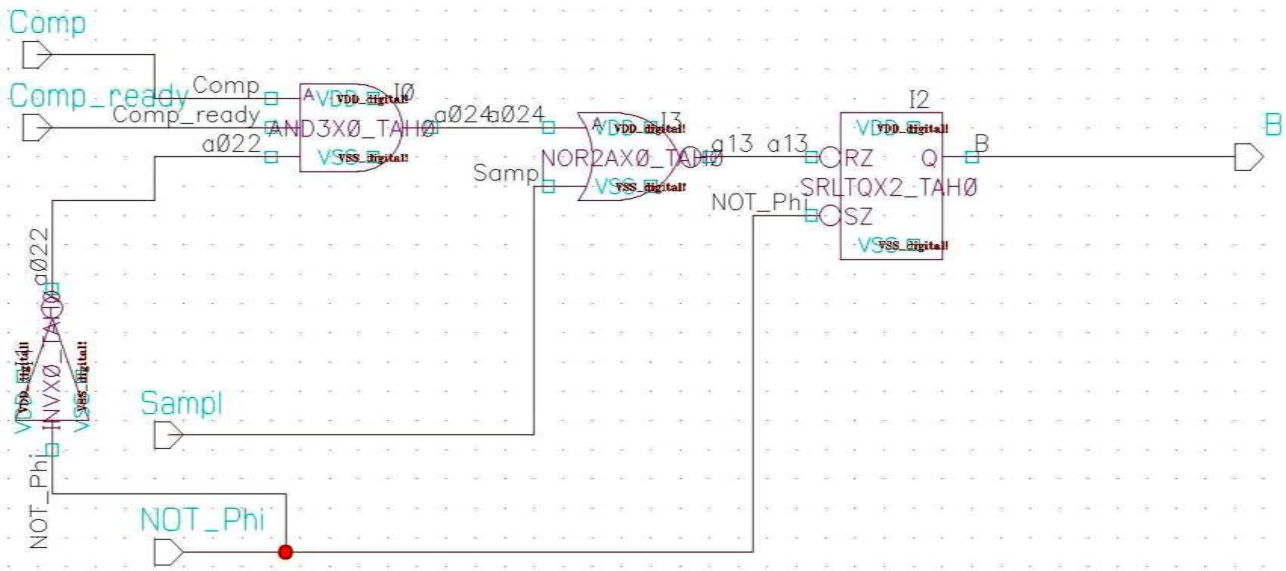


Fig. 4.18: Schematic of one of twelve a cell of block “Logic”.

The last cell to design is the PIPO register, but it is realized with basic technique with 12 DFF which work in parallel, as shown in Fig. 4.19.

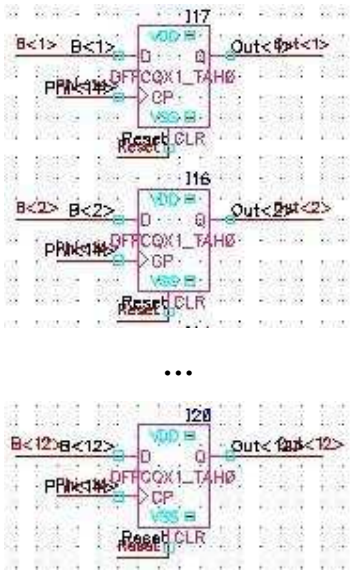


Fig. 4.19: PIPO register realized with DFF.

4.3 Prototype Implementation details

The test chip has been realized with technology of National Semiconductor® fabrication. It is a CMOS process with minimum channel size of 0.18µm.

The die photo is reported in Fig. 4.20, where is possible to see also the layout floor plan. Since all features are hidden by the presence of metal-5 dummies, so the layout has been overlapped in transparence on the photo. Attention has been used to separate as well as possible the digital logic from analog region where there are the critical arrays of capacitance of the DAC, the supply filter for reference voltages, and part of comparator. The symmetry has been used only for DAC because is much important the matching among the capacitance of it one. While the capacitances used for additional filter for reference voltages can be unmatched between them.

In Fig. 4.21 is represented the layout of the entire system without the presence of dummies, so it is possible to observe all pads, all connections from pads to core and it is possible to know the supply path because have a larger width.

In Fig. 4.22 the layout of the entire comparator is done. It is apparent the symmetry of the layout, in fact the two V2T converter included in the comparator are speculated between them. In the middle there is the DFF which has the purpose to compare the delays.

In Fig. 4.23 is given the layout of DAC. Also this layout appears as two big blocks. Each of them is one array of capacitances. Each capacitance of the array has the same center. The bridge capacitance is situated in the center of one array.

In Fig. 4.24 is reported the layout the layout of the digital logic. The construction of this layout is made with the purpose to have short connection, in particular for critical signal as the clock which can influence the analog part of the circuit.

The core area is $0.24mm^2$ and the entire die is $0.7mm^2$.

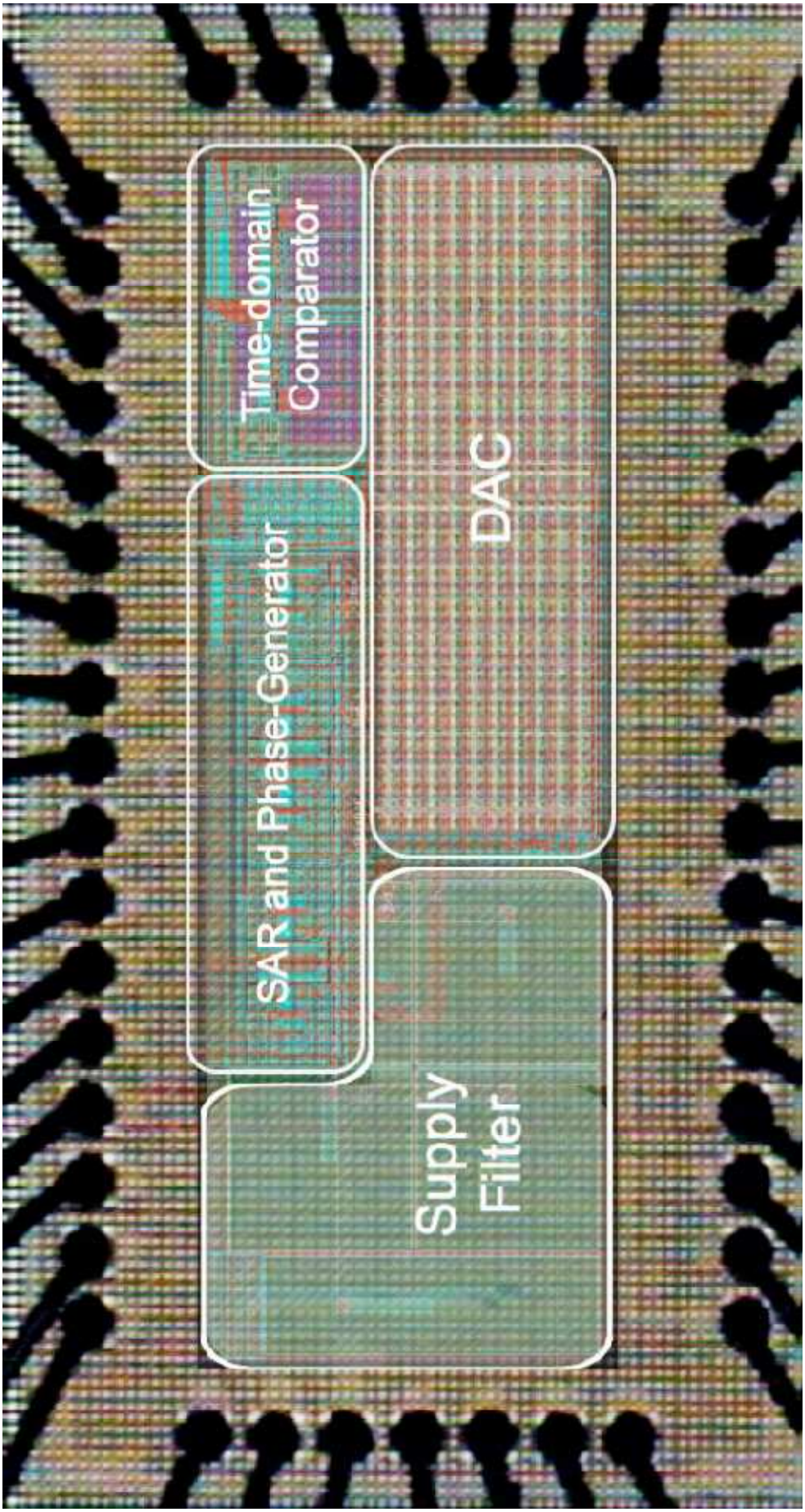


Fig. 4.20: Photo of the chip with layout in transparency because of dummies.

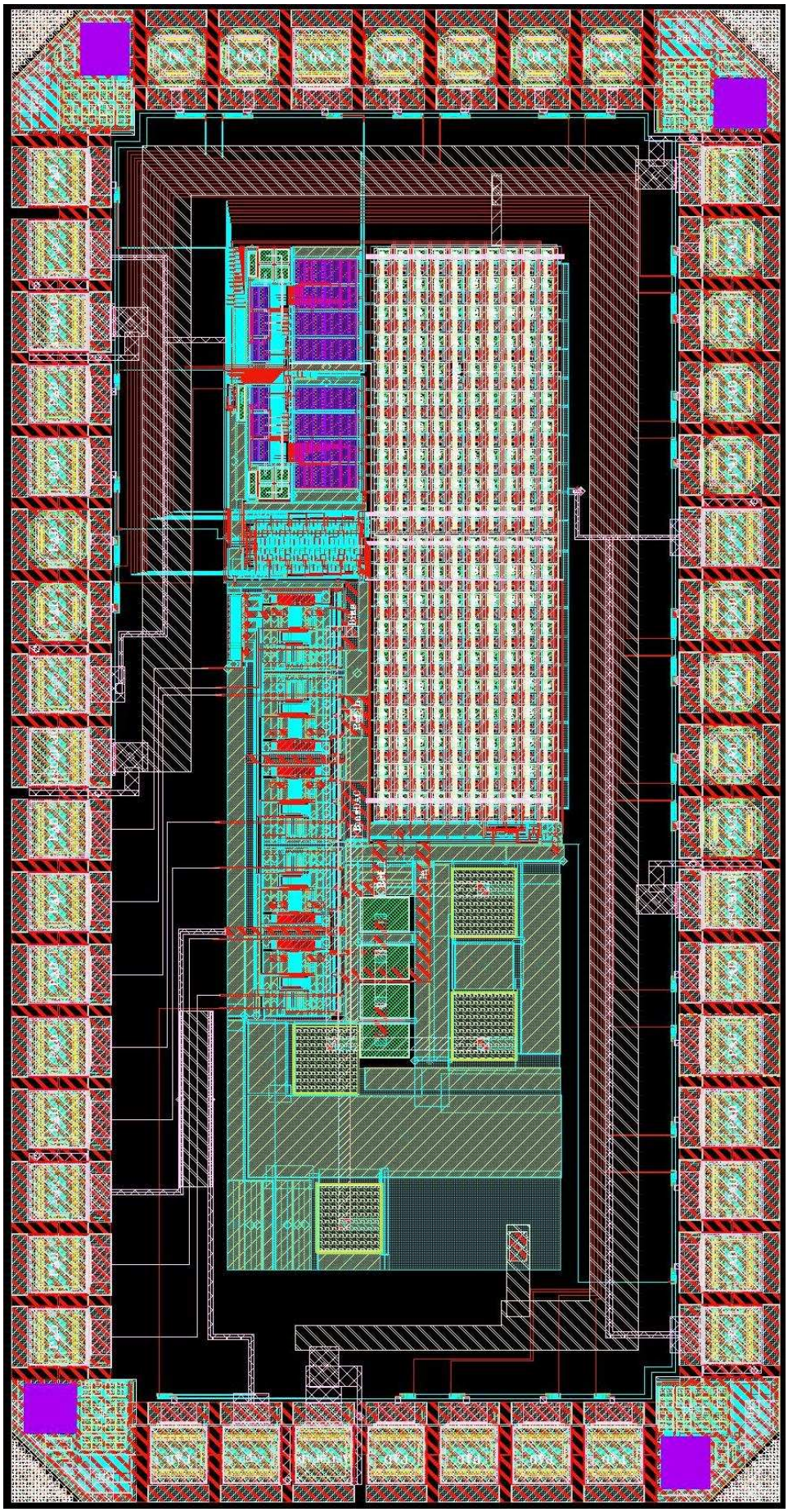


Fig. 4.21: Layout of the A/D comparator without dummies.

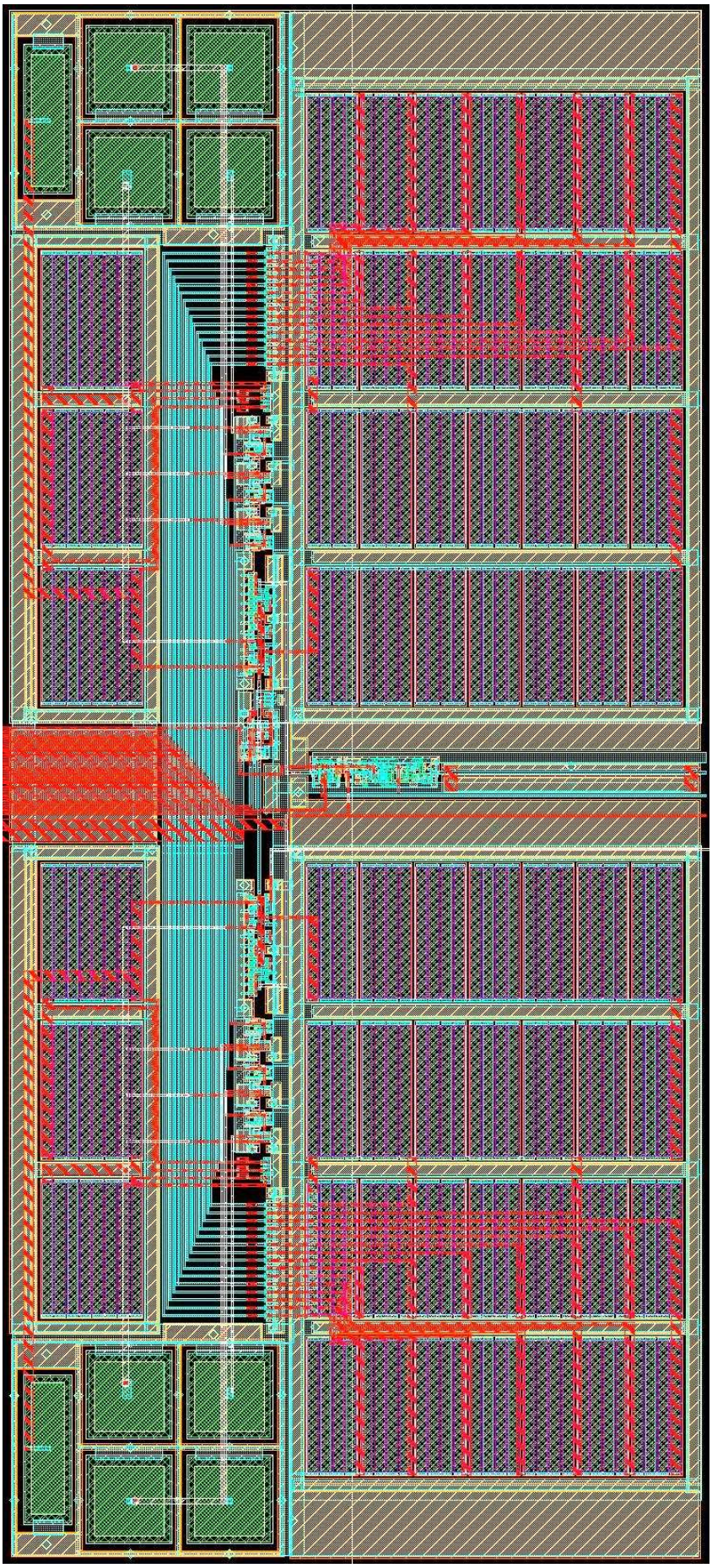


Fig. 4.22: Layout of the entire comparator.

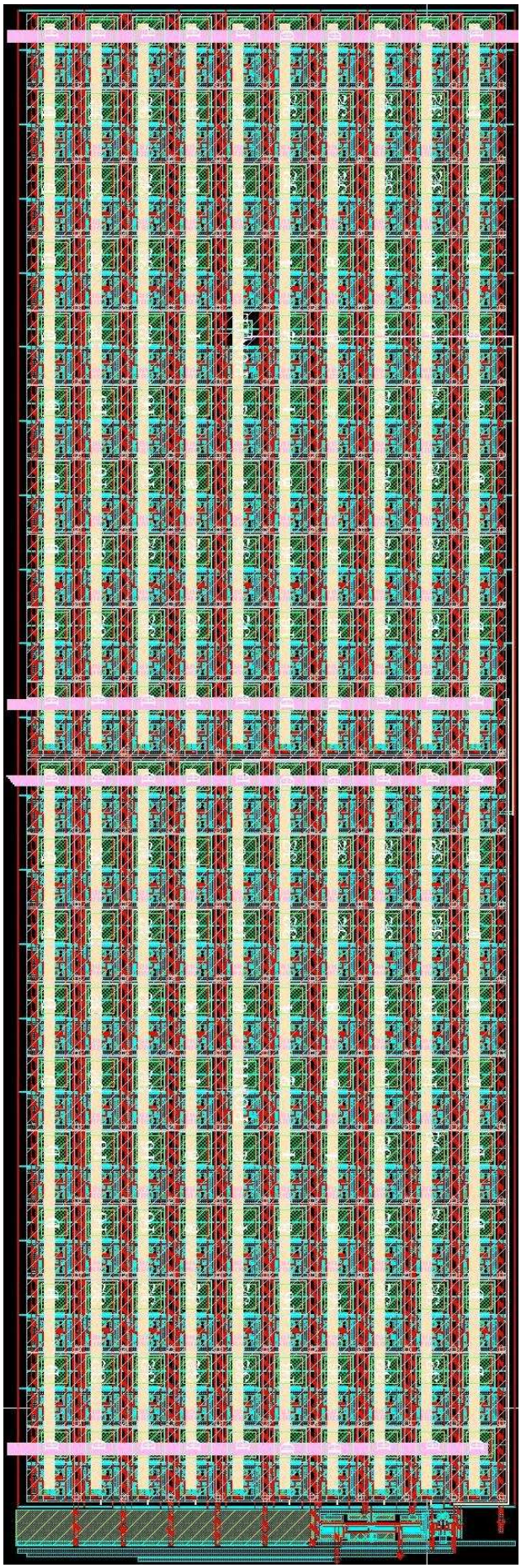


Fig. 4.23: Layout of the DAC.

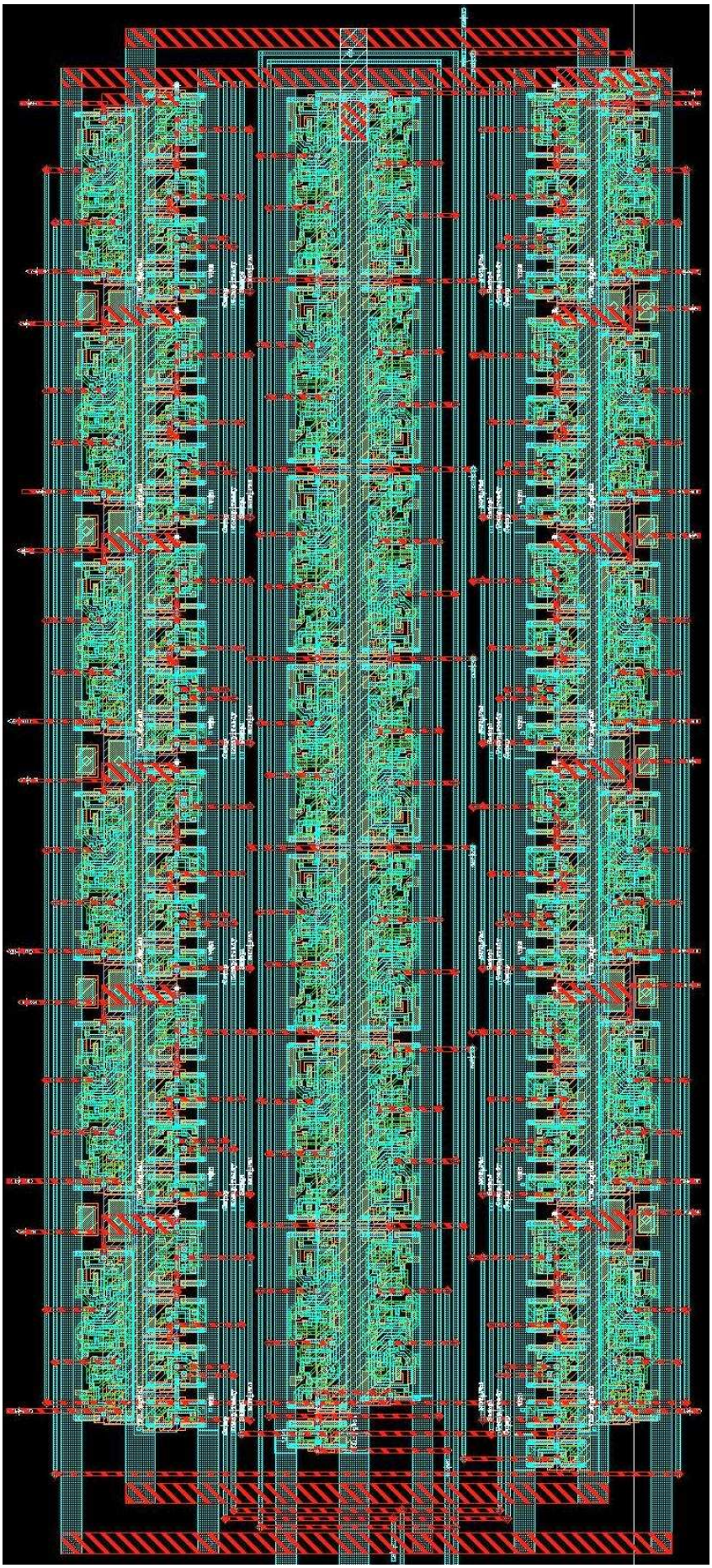


Fig. 4.24: Layout of the Digital Logic.

5

Experimental Results

- Measures
- Setup
- Results

5.1 Measures

The measurement to do on the test chip must suggest us the main characteristic of the converter. Some of the static and dynamic performance are given by the characteristic and by application to which this A/D converter has been designed. Therefore is possible to resume the main basic characteristic of the test chip (see Tab. 5.1) so for designing the circuit and the testing board for measuring all the other specs.

Characteristics		**Value**
Static	Voltage Supply	$1V$
	Input range	$0.8V$
	Analog Resolution	$12bit$
	Monotonicity	$Ensured$
Dynamic	Sampling Rate	$100\frac{kS}{s}$
	Input Bandwidth	$50kHz$
	Power Dissipation (simulated)	$3\mu W$

Fig. 5.1: Example of an output histogram of an ADC with dc input signal.

As is possible to observe in Tab. 5.1, the monotonicity is ensured, this result is known because the operation of the successive approximation algorithm.

The other static specifications (offset, gain error, …) can be taken by the DNL and INL characteristic. Therefore the our main purpose is to determine that curves. To obtain these characteristics is possible to change continually the value of the input signal injected to the test chip whit steps equal to ¼ LSB, and keeping constant the input for some sample of conversion. In this way is possible to be sure of the stability of the test chip. Then it is required to memorize all the digital words at the output for each sample of conversion, and then to evaluate the input-output characteristic for tracing the DNL and INL of the converter, by MATLAB®.

While the other dynamic characteristics (harmonic distortion, SNDR, …) are evaluated by putting some full range sinusoidal signal with different frequencies, to the input (up to input bandwidth) of the converter and to evaluate the spectra of the digital output.

These method for obtaining the performances of the converter are the simplest, cheapest, and more useful way to test a medium resolution converters.

5.2 Setup

All the foresee tests have the main purpose to put a particular signal to the input of the converter and to memorize a big piece of information for successive elaboration by software. Therefore the design of the test board for chip must be a simple connection for input signal and output digital signals, but must create high precision reference voltages and filters all the power supply voltages and reference voltages from undesired noise.

A photo of the testing board used to do the measurement is given in Fig. 5.1.

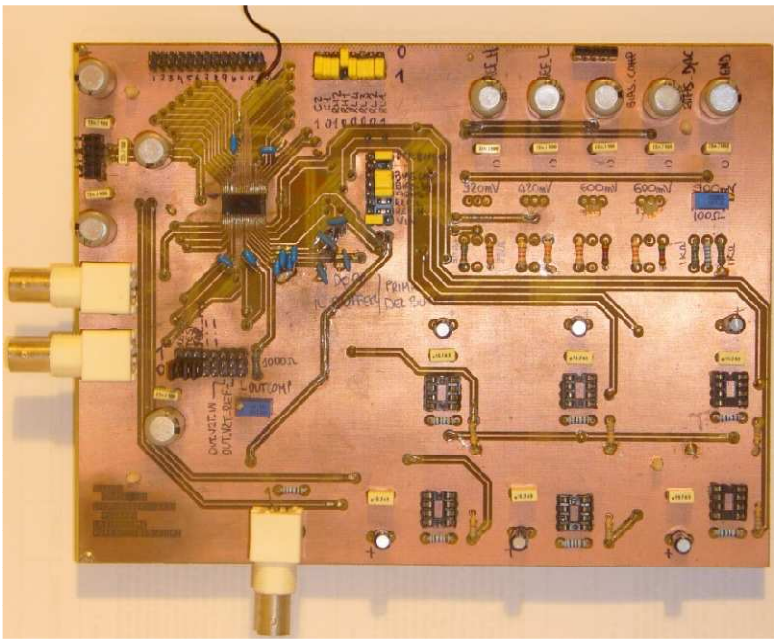


Fig. 5.1: Photo of the testing board.

To realize the input signal needed for obtaining the DNL and INL curves is equal a long ladder with 2^{12} steps. To obtain that signal is used an high precision National Instrument® analog board commanded by a computer with LabView® which allows to implement this type of process. In practice that board is a high performance DAC with 18bit of ENOB, therefore it can be used to characterize a 12bit A/D converter. The used software allows besides to read the output by a reading board and to memorize all the obtained digital word and the correspondent analog input done.

While the sinusoidal signal is given by a high precision signal generator with the possibility to introduce the desired offset and to modulate the amplitude of the signal. To read the output digital word is used a Logic Analyzer of Agilent®, which allows to transfer the read data to computer.

5.3 Results

Besides the output of the chip is a bus of 12 bit because the symmetry of the DAC, the successive performance are calculated on 10 bit, as the goal of the A/D converter required. Fig. 5.2 shows the low-frequency DNL and INL for 10b output obtained by the histogram of 65536 points (VDD=1V).

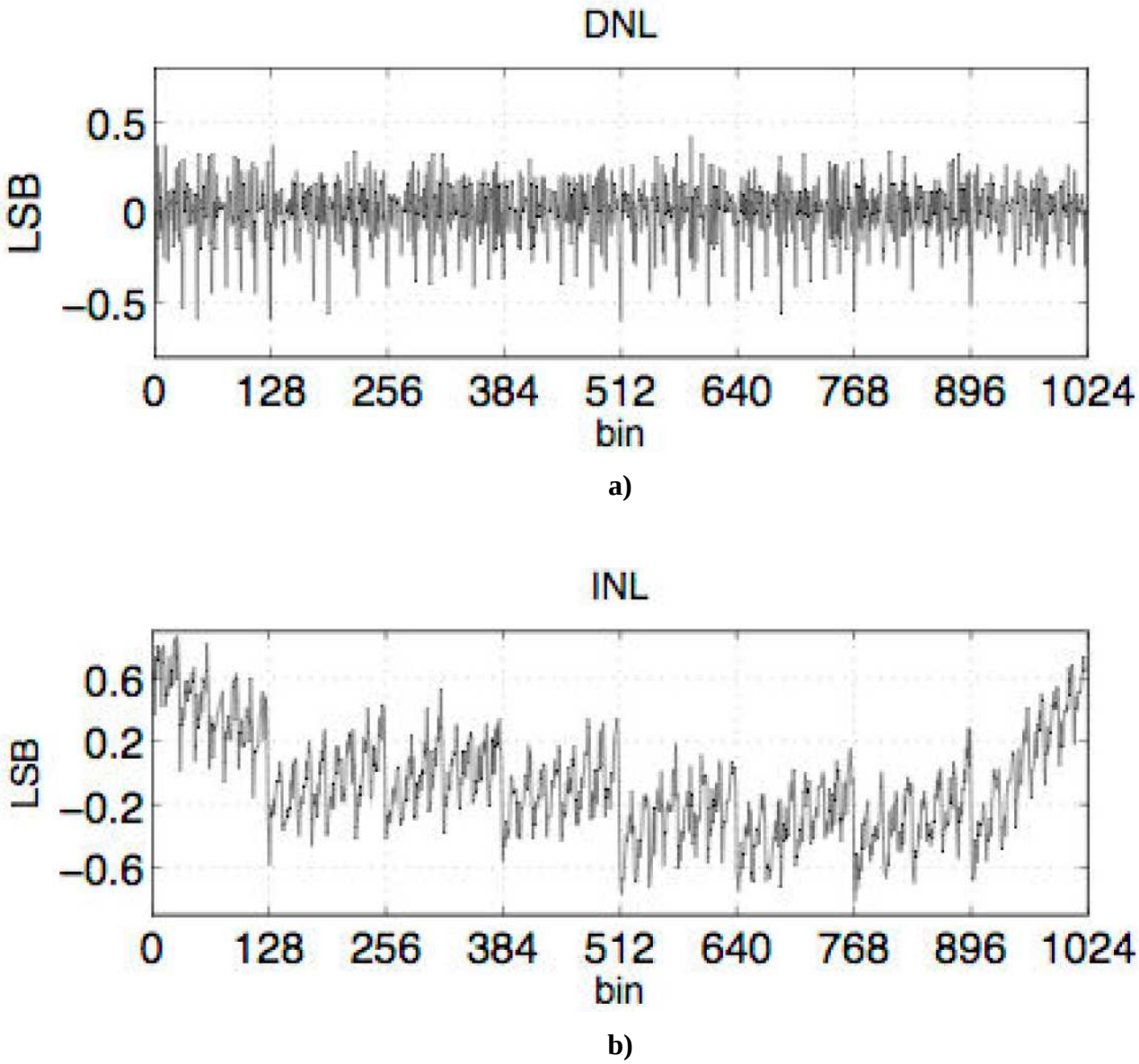
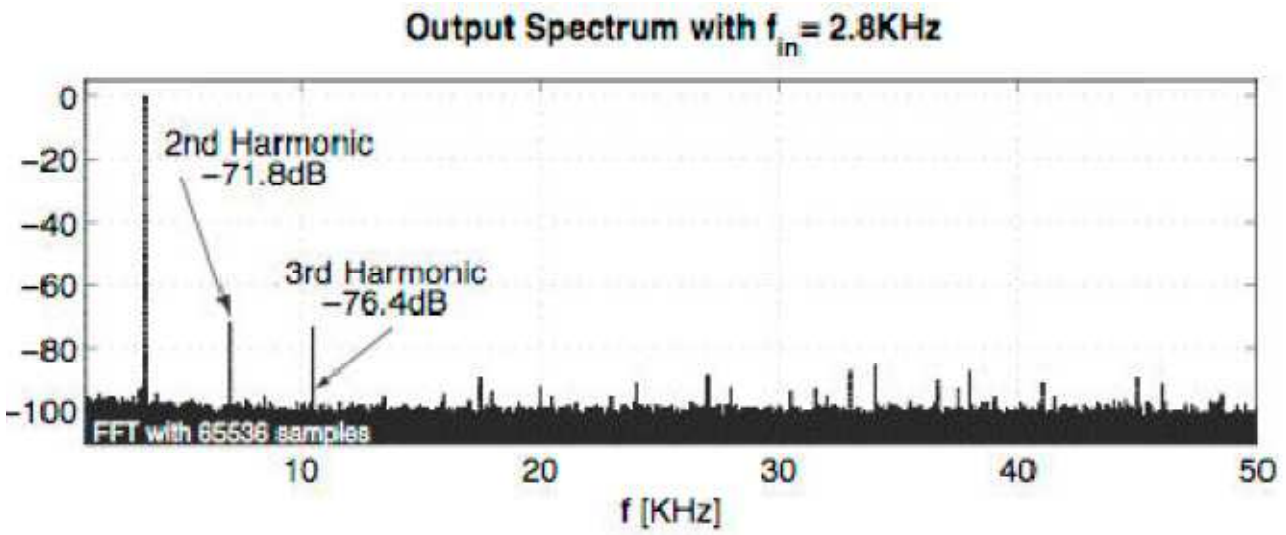


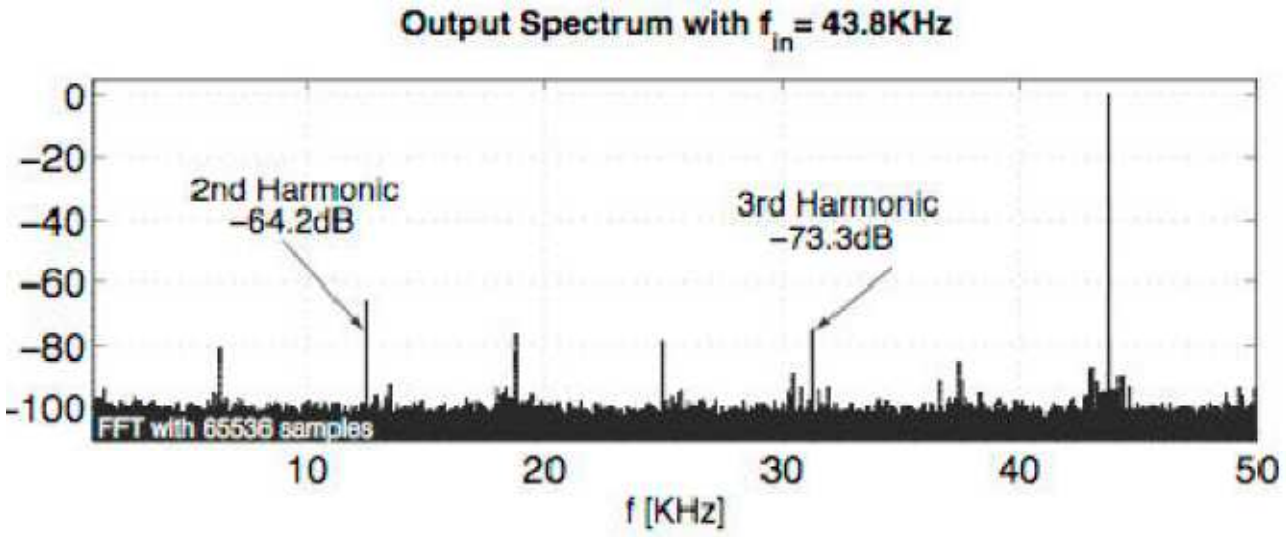
Fig. 5.2: DNL (a) and INL (b) of the converter.

From the characteristics is possible to observe that DNL is always less than 0.55 LSB and INL is always less than 0.7 LSB. It is also apparent the effects of the bridge DAC, in fact there are continually and periodic spike in both characteristics, they are done by the mismatch in attenuation capacitance in the DAC.

As dynamic characteristics are given the spectra of two sinusoidal tests, so it is possible to compare the effects at low frequency and at frequency near the Nyquist limit. In particular, the Fig. 5.3 shows the spectra of the digital output with input frequency equal to 2.8kHz and 43.8kHz respectively.



a)



b)

Fig. 5.3: Spectra of the output with input frequency equal to 2.8kHz (a) and 43.8kHz (b).

In the spectra are also indicated the distortion on the 2nd and 3rd harmonics, respectively equal to -71.8dB and -76.4dB for low frequency and these values degrade to -64.2dB and -73.3dB for high frequency.

These test are done for 11 different input frequencies and the distortion on the 2nd and 3rd harmonics are given in Fig. 5.4.

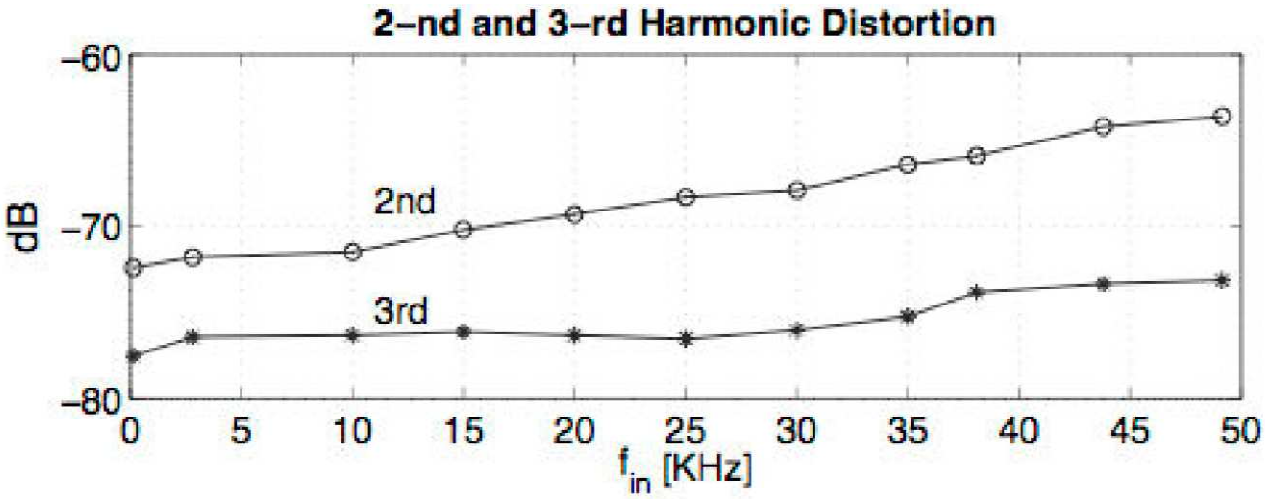


Fig. 5.4: 2nd and 3rd harmonics distortion *vs* frequency.

Knowing the floor noise and these distortion effects is possible knowing the SNDR, which is done in Fig. 5.5 at the same frequencies.

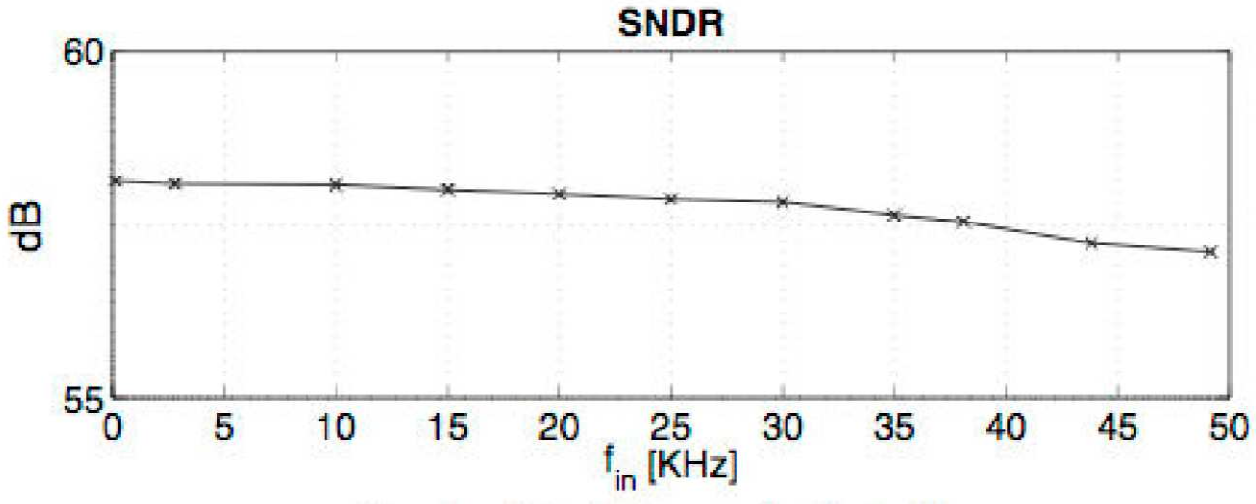


Fig. 5.4: SNDR *vs* frequency.

Experimental measurements show that the circuit works with a 0.8V to 1.8V supply, VDD, and reference voltages at 0.1VDD and 0.9VDD. The power consumption is 3.8µW at 1V and

11.5µW at 1.8V. The increasing supply voltage improves the SNDR (at VDD=1.8V is 4.8dB more), but the FOM worsens. The FOM, is 56fJ/conversion-step, at VDD=1V. The 3.2mV mismatch in the comparator is corrected by an external trimming of VB (with V_{bias} at 0.54V. The single ended configuration is the source of the second-harmonic distortion that dominates the SFDR: -71.8dB at low frequency and near the Nyquist frequency equal to -64.2dB, as shown in Fig. 5.3. The SNDR at Nyquist drops by 1.7dB with a loss of 0.3b. Higher distortion at higher frequency is due to a relatively high non-linear on-resistance of the switches connecting the capacitive arrays to V_{bias}.

Then is possible to resume the obtained performance in Tab. 5.2

Process	0.18-µm CMOS
Area	$0.7mm^2$
Voltage Supply	0.8 to 1.8V
Clock Frequency	Max 1.4MHz
Sampling Rate	Max 100kS/s
Power Consumption	3.8µW @ 1V
SNDR	58
ENOB	9.4 Bit
FOM	56 fJ/conv. step

Tab. 5.2: Resume of performance.

The obtained work is at limit the state of the art, in fact updating the Fig. 3.14 to 2008, is possible to observe the good position of our work.

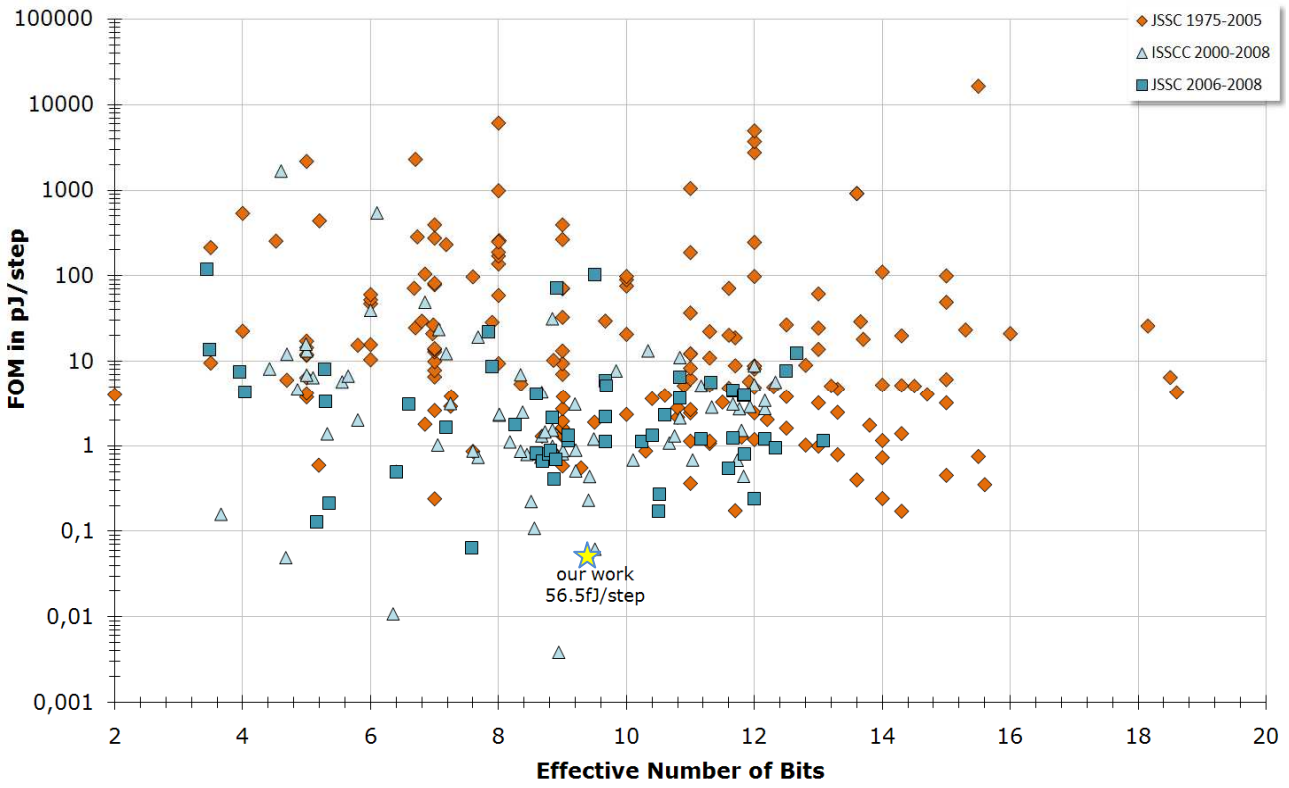


Fig. 5.5: FOM vs ENoB in the last years. (Source: http://www.wulff.no)

6

Conclusions

- Conclusions
- Research products
- Acknowledgements

6.1 Conclusions

The increasing requests of low power consumption, in particular in medical applications, has bring to design the successive approximation analog to digital converter which has been presented. To improve the power consumption it has been introduced a novel very low power time domain comparator which has the main purpose to convert both the input voltages into time delays and then a simple time comparator can decide the output of the comparator. This way allows to obtain a power consumption of about 1uW.

In this work, always in order to reduce the power consumption, has been introduced also a modified bridge capacitance solution DAC. It allows to use a 12bit capacitive array with only 15 pF by a two arrays structure and a unitary attenuation capacitance which allows to obtain a good mismatch and to ensure a correct attenuation factor.

Finally the digital part and SAR included in the system has been realized with a full custom design in order to reduce the power consumption then the automatic tools. The total measured power consumption in the test chip is equal to 3.8µW, the ENOB is equal to 9.4bit which lead to obtain a FOM of 56fJ per conversion step.

The main goal of the work is the power reduction and the purpose has been centered by the introduction of one novel way to think the comparator. The author has demonstrated the efficacy of this novel way by an attention design of this part of the system and after to obtain confirmation first by using behavioral simulations and after by the measurements of the realized test chip.

The results reached with the prototype are satisfying, considering that they were obtained at the first runs, with the first prototype of this type of comparator and that the obtained performance are good choices if compared with the actual state of the art of the similar 10 bit A/D converter.

A possible and interesting continuation of this work would be an improving of the comparator design, maybe to find an opportune method to reduce the power consumption in the discharge of capacitance or improving the resolution time of the time comparator respect than a simple library DFF as used in this first test chip. In this way is possible to obtain a further decreasing in power and a possible increasing in resolution.

6.2 Research products

[1] A. Agnes, F. Maloberti: "Multi-bit High-order Incremental Converters with Digital Calibration"; IEEE European Conference on Circuit Theory and Design, ECCTD ’09, August 2009, pp. 739-742.

[2] F. Geusa, A. Agnes, F. Maloberti: "Use of Chopper-Notch Modulator in Chopper Amplifiers for Replica Images Cancellation"; IEEE Int. Conference on Electronics, Circuits, and Systems, ICECS '08, August 2008.

[3] F. Erario, A. Agnes, E. Bonizzoni, F. Maloberti: "Design of an Ultra-Low Power Time Interleaved SAR Converter"; IEEE Ph.D. Research in Microelectronics and Electronics, PRIME '08, June 2008, pp. 245-248.

[4] A. Agnes, E. Bonizzoni, F. Maloberti: "Design of an Ultra-Low Power SA-ADC with Medium/High Resolution and Speed"; IEEE International Symposium on Circuits and Systems, ISCAS '08, May 2008, pp. 1-4.

[5] A. Agnes, E. Bonizzoni, P. Malcovati, F. Maloberti: "A 9.4-ENOB 1V 3.8W 100kS/s SAR ADC with Time-Domain Comparator"; IEEE Int. Solid-State Circuits Conf., ISSCC '08, February 2008, pp. 246-247.

[6] A. Agnes, A. Cabrini, F. Maloberti, G. Martini: "Cancellation of Amplifier Offset and 1/f Noise: An Improved Chopper Stabilized Technique"; IEEE Transactions on Circuits and Systems II, TCAS II, June 2007, pp. 469-473.

[7] A. Agnes, F. Maloberti, G. Martini: "Improved Chopper Stabilized Amplifier for Offset and 1/f Noise Cancellation"; IEEE Int. Conference on Electronics, Circuits, and Systems, ICECS '06, December 2006, pp. 529-532.

6.3 Acknowledgements

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7

Other activities

- Chopper OpAmp
- Time Interleaved SAR
- Incremental Sigma-Delta
- Conclusions

The PhD activity was mainly focused on the previously described project. In addition other studies have been performed. They are:

- Study of a new architecture for chopper stabilized op-amp. The study was the basis of another research project for low offset and low power amplifier.
- Time interleaved SAR for extending the main project of this PhD work to higher frequency band.
- Incremental ΣΔ A/D converter with multibit feedback has been studied and realized on silicon. In particular has been studied some technique for reducing the effects of the errors introduced by DAC.

7.1 Chopper OpAmp

Many instrumentation applications require using amplifiers with ultra high-gain and virtually zero offset and *1/f* noise for processing the signal that sensors produce at very low level. The use of nested architectures obtains high gain and, at the same time, enables compensation. The offset is faced by the auto-zero or the chopper stabilized approach. Both methods are also effective against the *1/f* noise. The auto-zero technique is more performant than the chopper approach but, unfortunately, it requires to use large auto-zero capacitances to obtain a low *kT/C* contribution. On another hand, the chopper stabilization method generates images of offset and *1/f* noise at the chopping frequency and its multiples. These spurs are unwanted and must be filtered out by on-chip low pass or notch filters. A possible architecture with three stages is the nested scheme shown in Fig. 1. The low frequency gain is $A_0 = A_3+A_2 \cdot A_3+A_1 \cdot A_2 \cdot A_3$. The feedthrough path through A_3 sustain the gain at high frequency. The offset and the *1/f* noise of the first amplifier, A_1, can be reduced by the auto-zero or the chopper method [1]. The offset and the *1/f* noise of A_2 and A_3 are referred to the input attenuated by a factor A_1 and $A_1 \cdot A_2$ respectively, therefore these contributions are negligible.

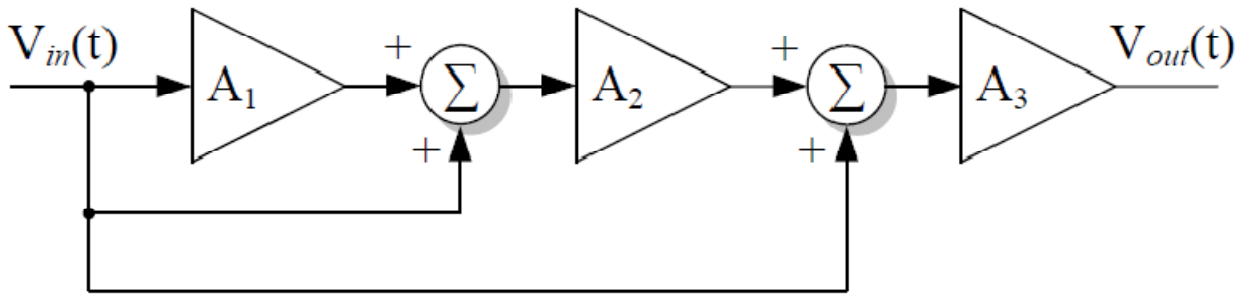

Fig. 7.1: Conventional scheme of a nested amplifier.

One of the solutions used to cancel the offset is the autozero [4] method. It requires a time-slot during which the amplifier is not used. The inputs are shorted and an auxiliary gain stage is suitably driven to zero the output. The auto-zero signal is stored on a capacitor for the successive amplification phase. The method can also use the solution of Fig. 7.2(b) that stores the offset on C_1 placed in series with the input. The value of the capacitor and the auto-zero rate determine the noise floor limit that is $\_kT/(C_1 \cdot f_{az})$. For obtaining a noise floor of $50\frac{nV}{\sqrt{Hz}}$ with f_{az} = 10 *kHz* it is necessary to use 164 *pF*, an area consuming value for on-chip implementation.

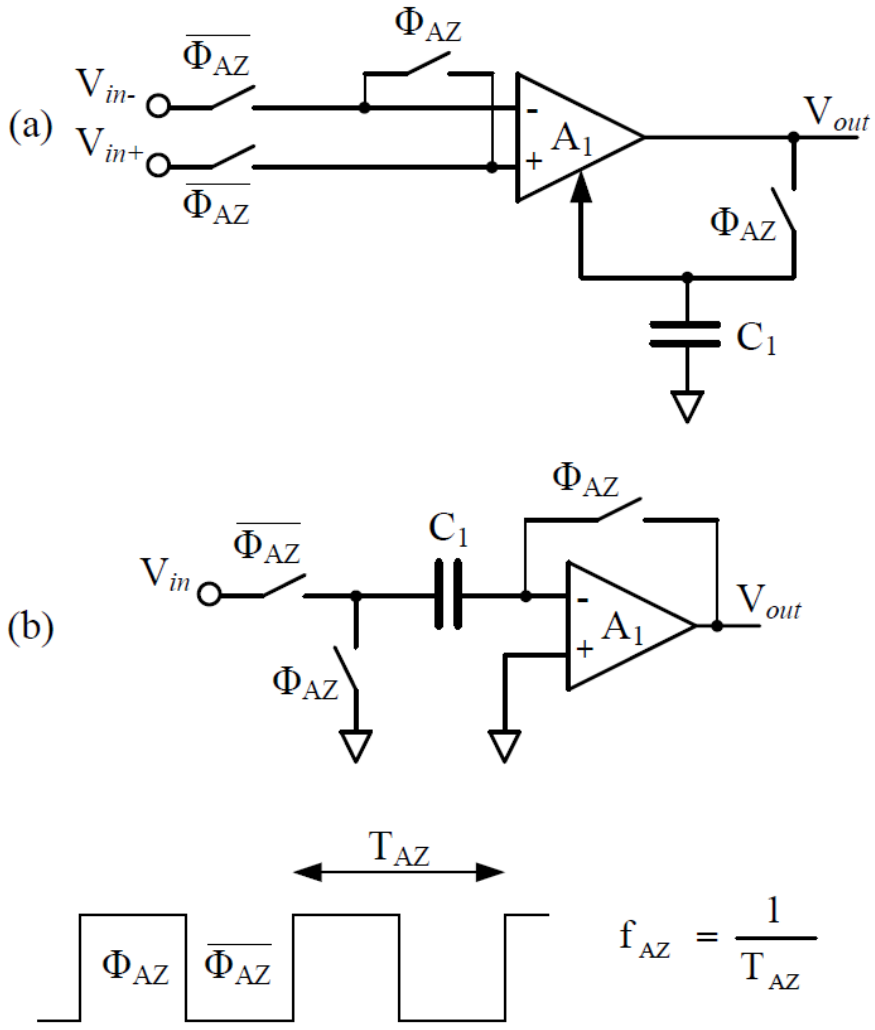

Fig. 7.2: Schemes for auto-zero.

The above motivates the use of the chopper stabilization method and to study possible solutions that resolve the problem of the spur images. The method described in this paper is an hybrid solution that uses the chopper method before the amplifier and exploits an auto-zero like approach to reconstruct the signal in the base-band. The analysis and simulations verify the benefits of the proposed method.

A chopper stabilized amplifier multiplies the input signal by a square wave for moving the band limited input spectrum around the chopping frequency and its multiples. The operation separates the signal from offset and the 1/f noise so that the spectra are like the ones shown in Fig. 7.3. The input spectrum is the one in Fig. 7.3(b). After chopping and the addition of $v_n(t)$ that includes the offset v_{os} and the 1/f noise v_f (t) we have the spectrum of Fig. 7.3(c). After the second modulator the spectrum becomes the one of Fig. 7.3(d). It results that spurs at f_{ch} and its multiples deteriorate the result. A low-pass filter can possibly reduce the amplitude of the offset and the 1/f contributions.

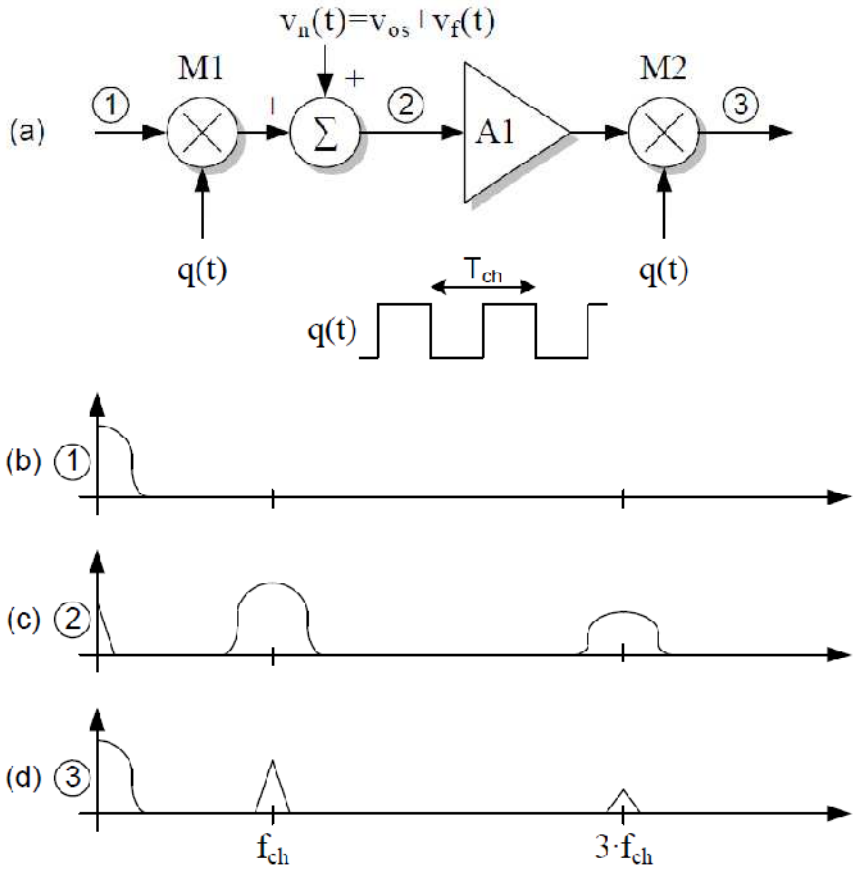

Fig. 7.3: a) Schemes of chopping solution and spectra b) of the input signal, c) of the signal after first modulation and d) of the output signal.

The method has been simulated by using a test 1/f noise whose spectrum is shown in Fig. 7.5(a). The spectrum of the output spur, after modulation, is the one in Fig. 7.5(b) and after a first order low pass filter with cut-off frequency at $f_{ch}/10$ becomes the one of Fig. 7.5(b). It is evident that the residual at f_{ch} is still high and, likely, many applications cannot admit the result. A possible remedy is use a chopping signal with, intentionally, a jitter. The effect is to blur the spur power and to spread it around f_{ch} and its multiples. As shown in [2] the method works but the level

of the noise floor increases and, therefore, there is a trade-off between level of the noise floor and the presence of spur tones.

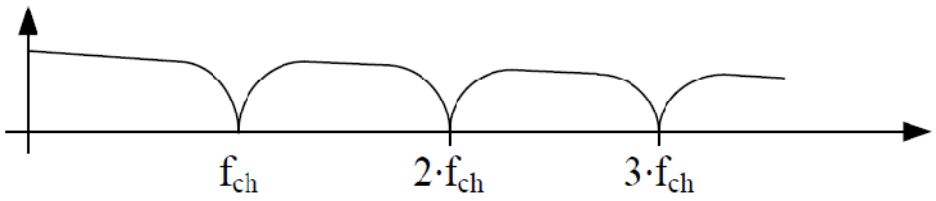

Fig. 7.4: Possible notch response.

The spur tones can also be removed by a notch filter, that replaces or is placed after the low-pass filter [6], centered at f_{ch} and multiples. The possible notch response is shown in Fig. 7.4 that must be provided by an active or a passive SC scheme.

The proposed solution is based on the following observations/assumptions:

- the chopping frequency is higher than the signal band and aliasing is not a problem;
- the chopped path takes care of the low-frequency part of the input (as it is for the auto-zero case);
- the input is transformed into a pseudo-square wave, while the offset is a *dc* term.

Therefore, the goal of the circuit is to reject the *dc* and to reveal the peak-to-peak amplitude of the square wave. It is well known that a *dc* component is rejected with a capacitive coupling and that the peak-to-peak amplitude of a square wave results from subtracting the negative value from the positive value.

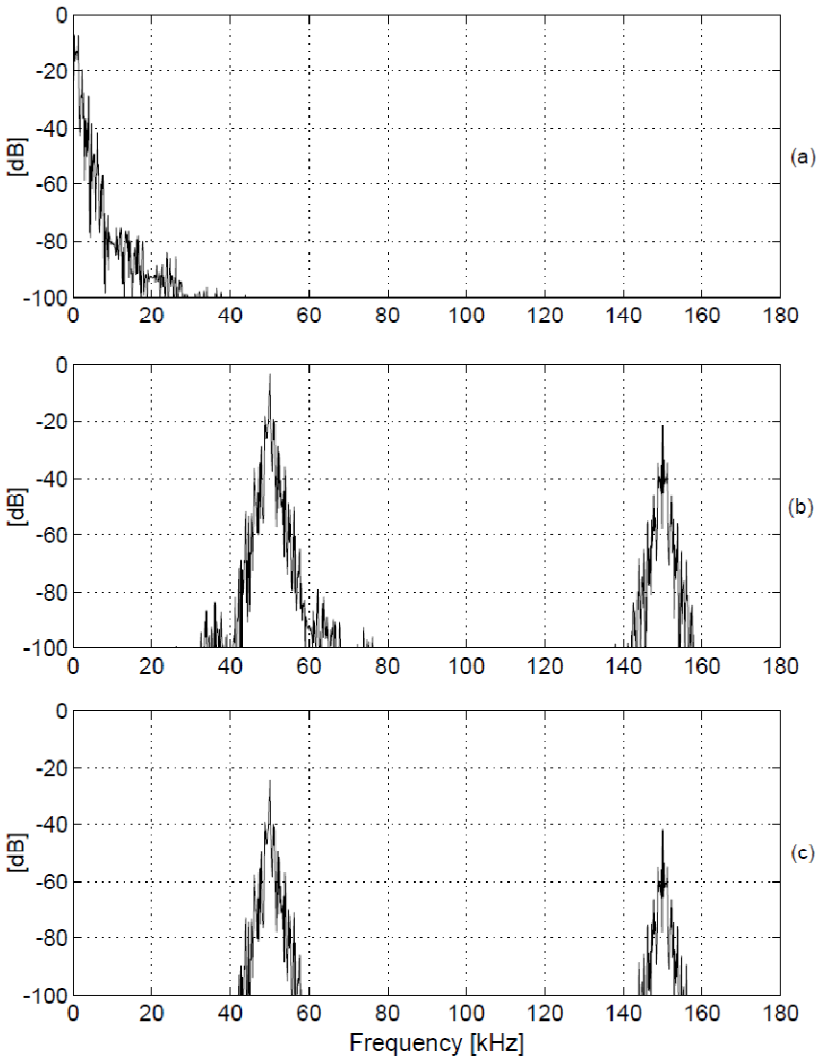

Fig. 7.5: Spectra of the a) 1/f noise used for simulations b) output of the second modulator M2 and, c) output of the low-pass filter with cut-off frequency at $f_{ch}/10$.

These functions are obtained by the simple circuit of Fig. 7.6. During the phase Φ_1, the signal equal to $A_1[-V_{in}(t1) + V_{os}]$ is sampled on the capacitor C_s, while during the phase Φ_2 the capacitor acts as a level shift giving rise to the output V_{out} at the end of Φ_2 ($t = t2$) equal to

$$V_{out}(t2) = A_1 [V_{in}(t1) + V_{in}(t2)] \tag{7.1}$$

Indeed, if in addition to the offset there is also a $1/f$ term, V_f the output voltage becomes

$$Vout(t2) = A_1 [V_{in}(t1) + V_{in}(t2) - V_f(t1) + V_f(t2)] \tag{7.2}$$

That corresponds to a $(-1+z^{-1})$ high-pass filter of $V_f(t)$ in the sampled-data domain, as it is obtained by the auto-zero method.

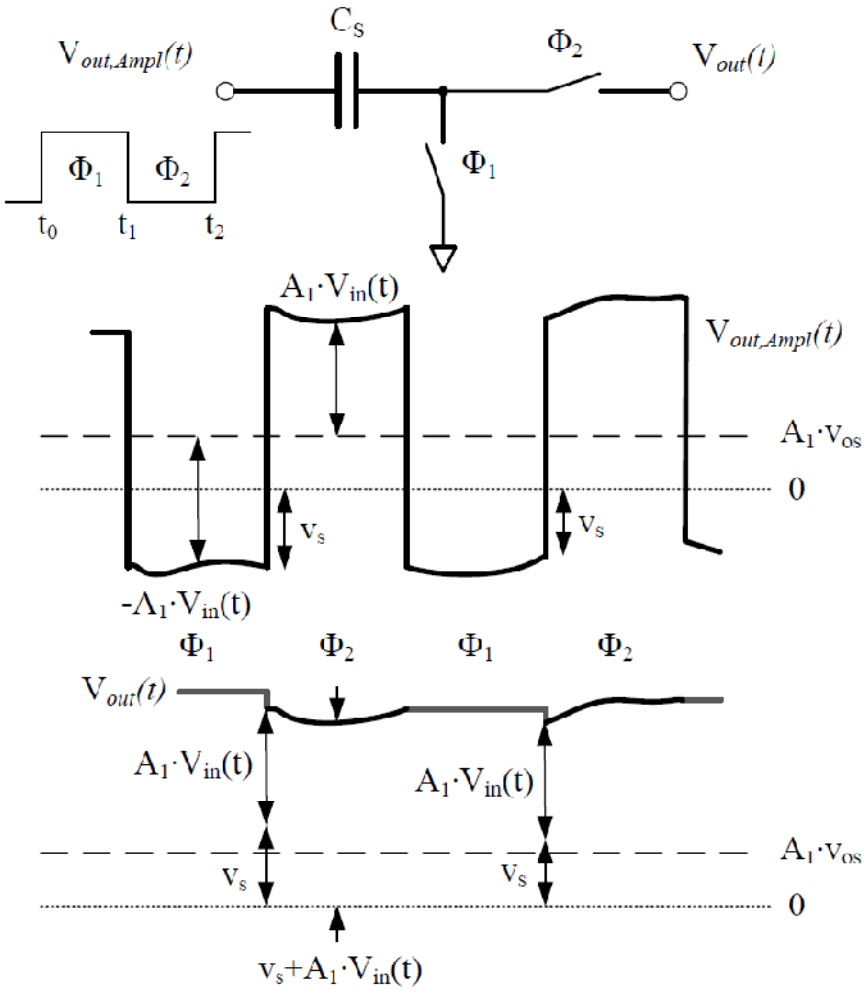

Fig. 7.6: Chopper-notch with SC structure.

The *dc* coupling established by the simple circuit of Fig. 7.7 naturally removes the offset but, if the gain A1 is large, a non negligible offset give rise to an amplified result that can saturate the output of the amplifier.

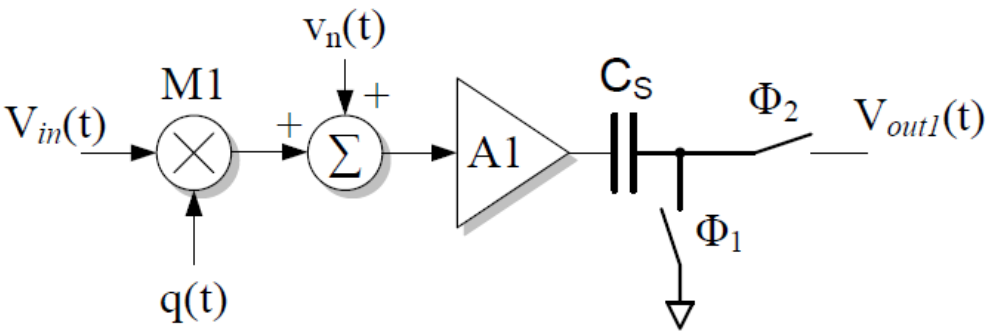

Fig. 7.7: Circuit for offset cancelation.

Therefore, it is necessary to properly control the frequency response of the amplifier. Indeed, it is not necessary to remove the dc but it is just enough to limit the gain to a level that avoids the output saturation. A possible conceptual solution is shown in Fig. 7.8. It is made by two amplifiers one with the full gain and the other with reduced gain that add their contributions to obtain the output. The low gain inputs serve for a local loop that limits the low frequency gain.

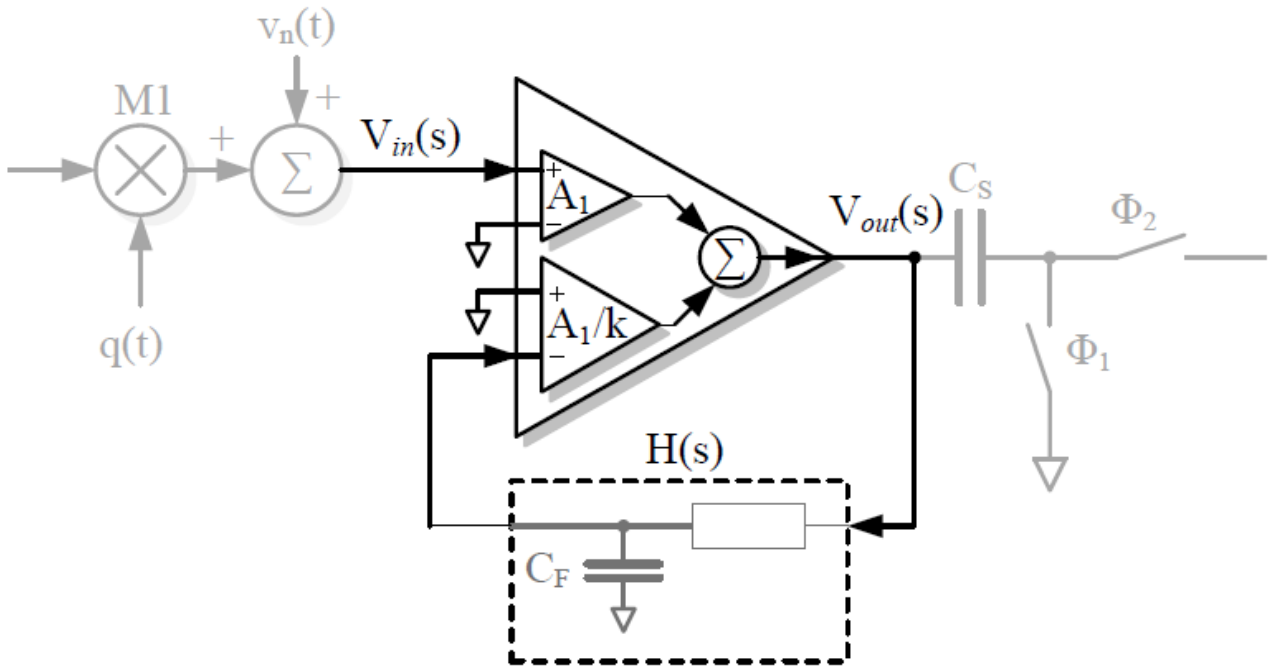

Fig. 7.8: Amplifier with local loop for offset control.

By inspection of the scheme it results:

$$V_{out}(s) = V_{in}(s)\frac{k}{\frac{k}{A_1}+H(s)} \tag{7.3}$$

and then, if H(s) is a low pass filter, H(s) = 1/(1 + $s\tau$), results

$$A(s) = \frac{V_{out(s)}}{V_{in}(s)} \cong k \cdot \frac{1+s\tau}{1+s\tau\frac{k}{A_1}} \tag{7.4}$$

denoting a gain by k at *dc* and a zero-pole pair separated by k/A_1. If the pole occurs before the dominant pole of the amplifier, then the frequency response is like the diagram of Fig. 7.9. The offset and the 1/*f* noise is amplified by k and the chopped signal by A_1.

Assuming a chopper frequency of 50 kHz, as shown in Fig. 7.9, and a signal bandwith of 20 kHz, the flat gain bandwidth has to be at least 40 kHz around of the chopper frequency. Therefore the dominant pole of the amplifier *A*1 can be set at 100 kHz and if its gain is 60 dB the $f_t = 100\ MHz$. A reasonable position of the pole of A(s) is at 10 kHz. With the zero at 100 Hz the low frequency gain of the amplifier is 20 dB that is a limited value for offset of few mV. The design strategy can lead to different positions of zero and poles; however the above figures give an indication on the design of the block H(s).

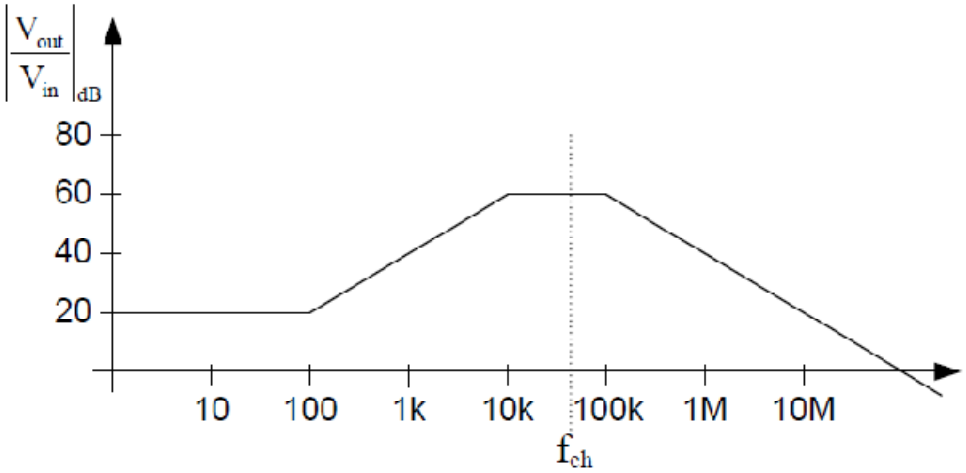

Fig. 7.9: Typical frequency response of the chopped amplifier.

Before has been shown the need of designing a low pass filter with a relatively low cut off frequency (around 100 Hz). The problem has been faced in many biomedical applications showing that the solution is not trivial but possible to achieve.

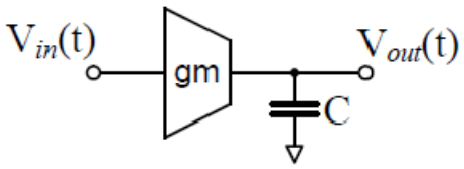

Fig. 7.10: gm-C low pass filter.

For a cut off frequency of 100 Hz the equivalent time constant is 1.4 msec. The resistance can be realized with high-resistive poly or with a transconductor and a possible value is in the few MΩ range. Assuming to obtain 5 MΩ the required capacitance is 320 pF. This value is large for an integrated implementation; however, techniques that multiply grounded capacitors can be used. Fig. 7.11 shows the transistor implementation of the scheme proposed in [7]. The current on the capacitance *Ci* is measured and amplifier by a current mirror with gain α. Therefore the optained

capacitance is $Ci \cdot (1+\alpha)$. By using $\alpha = 49$ the capacitance to be integrated is reduced to 6.4 pF, a large but affordable value.

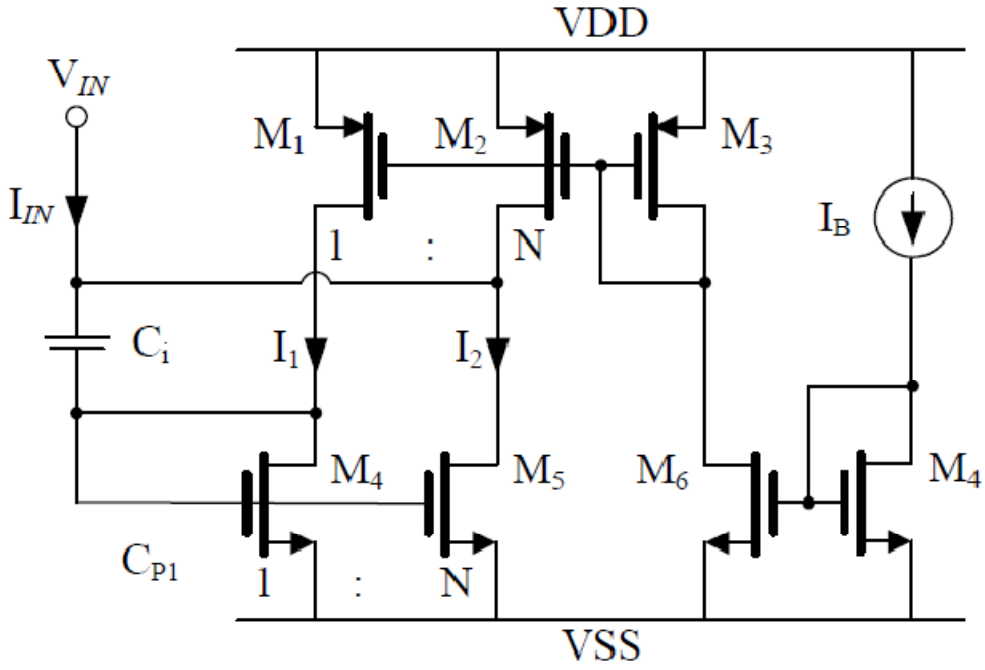

Fig. 7.11: Circuit for capacitance multiplier.

Fig. 7.12 shows the complete scheme of the nested amplifier made by two stages with gain $A1$ and $A2$. Therefore the *dc* gain becames $(A2+A1 \cdot A2)$. The amplifier $A1$ has in front the first chopper and is followed by the chopper-notch proposed circuit. Moreover a local loop obtain a limited gain of the low frequency input. The operation of the circuit has been simulated at the behavioural and transistor level to demonstrate the proposed technique.

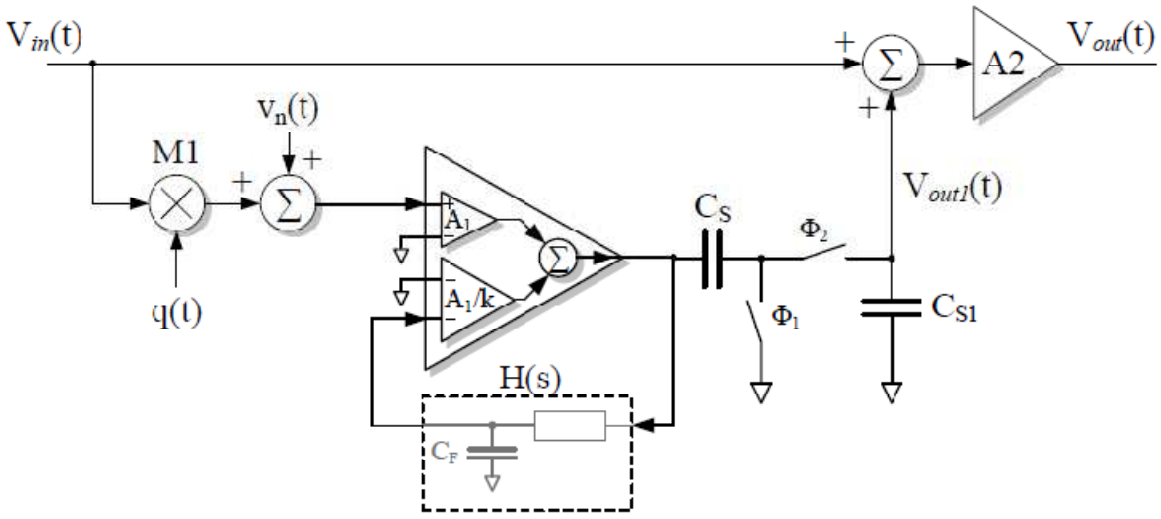

Fig. 7.12: Complete amplifier.

Fig. 7.13 shows the spectrum at the output under the same conditions used in Fig. 7.6. The offset (equal to 4.3 mV) is completely removed while the *1/f* noise is strongly attenuated by more than 60 dB. The chopping action that has a continuous time path during Φ_2 causes the replicas at multiples of the f_{ch} that are below 90 dB in the worst case.

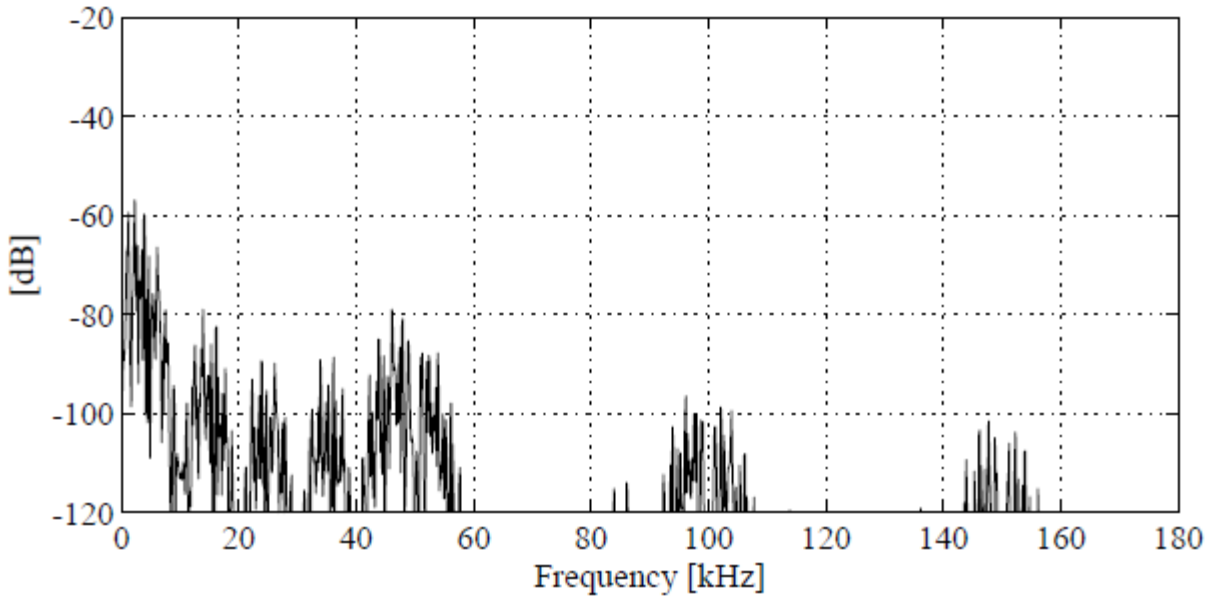

Fig. 7.13: Spectrum of the output caused by 1/f noise.

7.2 Time Interleaved SAR

The power consumption is important for micro-sensors wireless systems. After performing a first analog processing, many architectures use an A/D to move into the digital domain. The typical requirements for many sensor systems are medium resolution (~10–12 bit) and low speed (~500-700 kS/s). Therefore, the specs are not difficult but the required low power level is very challenging. Among the data converter architectures, the flash is a first generic option: it uses (2*n*-1) comparators. However, the high number of comparators makes the architecture too power hungry even for low resolutions. Also the pipeline architecture is not a good approach for ultra low-power. As known, a pipeline converter reduces the power as it divides the conversion task into several consecutive steps; however, each stage uses an active gain element whose power equals the one of many comparators. Therefore, it becomes competitive for high resolution and, in general, requires too much power. Other architectures, like the sigma-delta and the time interleaved have similar limits because despite their use of speed or multiple paths to increase resolution or throughput, they use active power hungry elements.

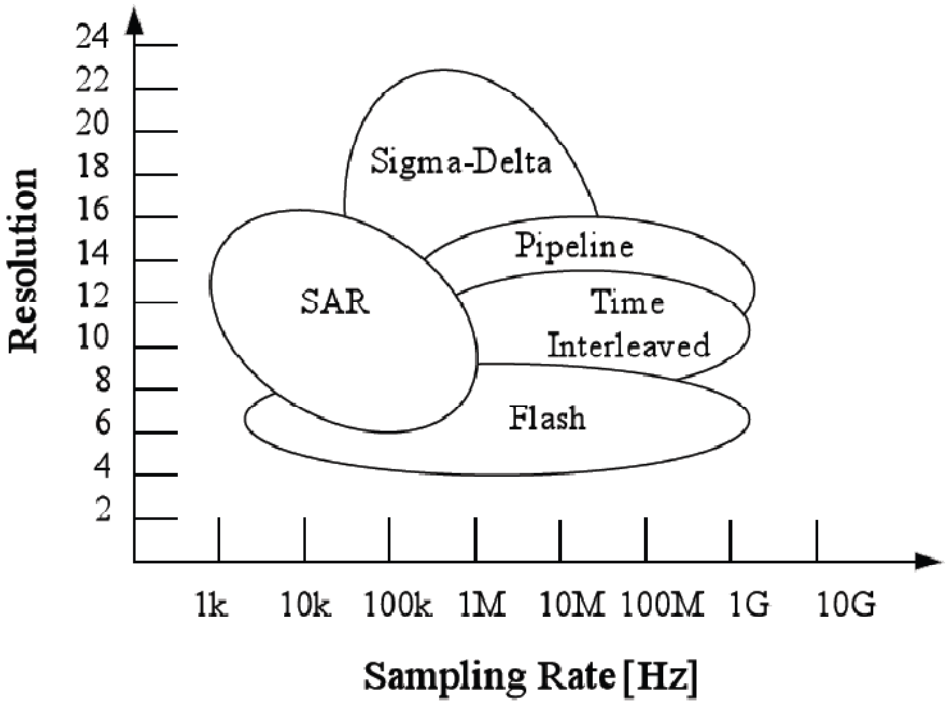

Fig. 7.14: Tipical converter topologies as a function of the sampling rate and obtained resolution.

If the speed is low the most suitable algorithm is the successive approximation that uses a successive approximation register (SAR) to control a DAC in a feedback loop with a single

comparator. The cost is that it requires n+1 comparison cycles to achieve n-bit resolution. The above considerations are summarized in Fig. 7.14, that shows the best data converter topologies as a function of the desired sampling rate and the required output bit resolution.

The diagram depends on the technology and the used supply voltage; however, the SAR algorithm is preferable for signal bands up to one, two hundred of kHz. As known, the SAR architecture has a circuit configuration like the one shown in Fig. 7.15, [8 - 11]. The comparator refers to ground after the subtraction of the sampled-and-held input and its foreseen version generated by the DAC. The given topology increases the resolution by just increasing the number of cycles of the algorithm; therefore the power has the logarithmic dependence with the number of quantization steps.

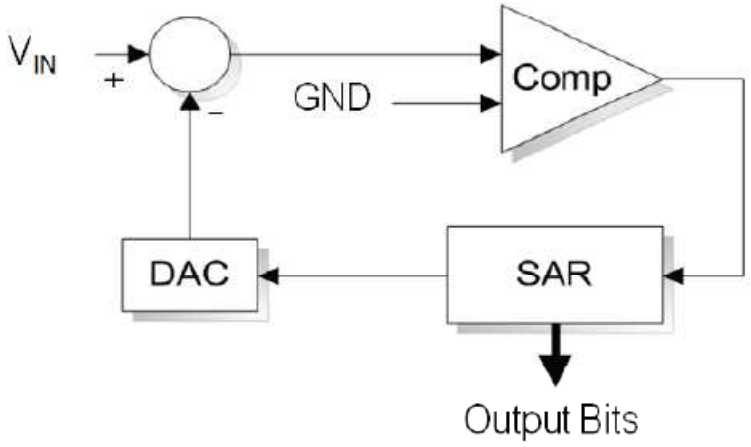

Fig. 7.15: Conventional SAR converter architecture.

Starting form this favorable algorithm, this work studies architectural strategies to optimize the power consumption of a medium-speed medium-resolution SAR ADC. Namely, a careful design of a SAR architecture, [12], and the use of the time interleaved technique achieves ultra low power. With a 0.18-µm CMOS technology and a sampling rate of 700 kS/s, the expected power consumption is 40 µW, giving rise to a FOM as low as 37 fJ/conv.-step.

The basic architecture of Fig. 7.15 has been realized with non conventional and custom designed circuits to minimize the consumed power. This Section discusses the design strategies and provides circuit details. The foreseen resolution is 12-bit (enough for many sensor systems) with a reference voltage of 1 V and supply voltage VDD= 1.2 V.

DAC

Fig. 7.16 shows the circuit schematic of the DAC, the input S&H and subtractor. It consists of two identical 6-bits sub-array binary weighed capacitors with unary attenuation capacitor. The use of two sub-arrays is a common way to reduce the capacitor spread and, consequently the power due to the charging and discharging of capacitors during the conversion cycles. However, as discussed in [8], the capacitor used to bridge the two arrays and ensure the attenuation factor of 32 should be non unity. The solution of Fig. 7.16 uses a unity capacitor but the sub-array is made by 63 elements instead of 64. This causes a global gain error that is acceptable, [13]. The value of the unity capacitance is at least 100 fF and the power consumption turns out to be about 570 nW.

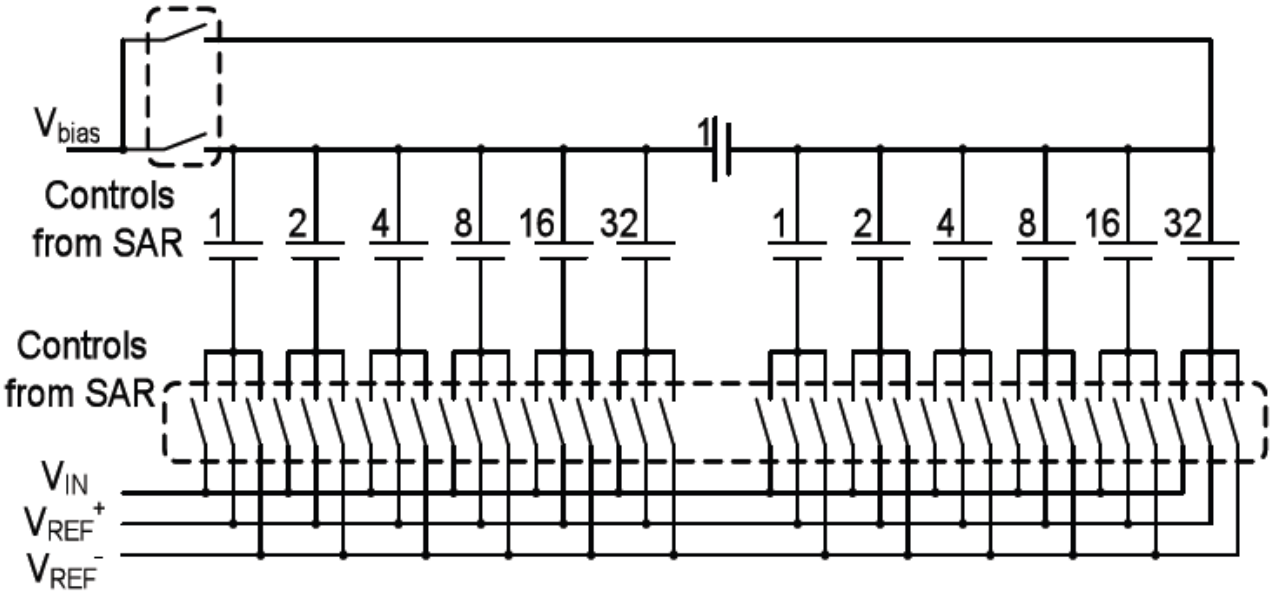

Fig. 7.16: Binary capacitors arrays with attenuation capacitor.

The solution of Fig. 7.16 is the same used in [12], but the switches used for the input sampling are driven by a clock-boost, shows in Fig. 7.17. The switch transistor is MN1 and the others allow controlling the switch transistor with the same overdrive despite the input variations. The charge and discharge of bootstrap capacitors in the switches introduce a power consumption of about 850 nW.

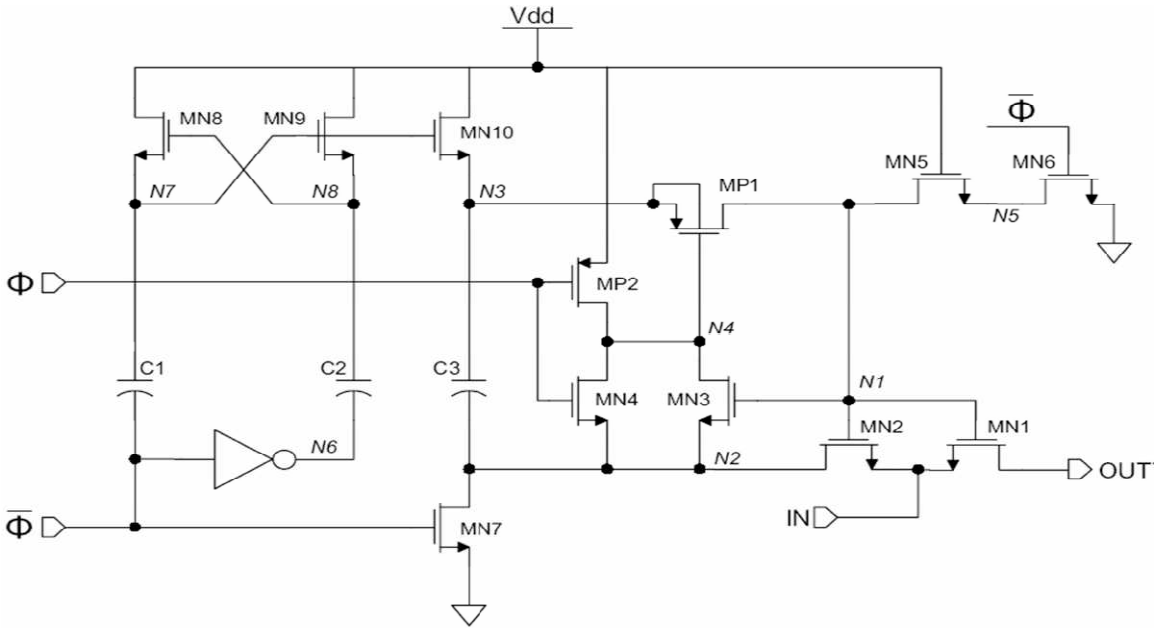

Fig. 7.17: Schematic of a bootstrapping switch.

Time Domain Comparator

Conventional SAR ADCs foresee the use of a voltage comparator, typically made of a preamplifier followed by a latch stage. Theoretical analysis and simulation results demonstrate that this approach is not the best in terms of power consumption, [13]. In order to minimize the power consumption, in this paper, a power effective time-domain comparator is used. Two identical voltage-to-time (V2T) converters make the core of the time-domain comparator, [12]. The V2T, depicted in Fig. 7.18, provides an output pulse which is delayed with respect to the reference clock, Φ_C, as a function of the input voltage, *VA*. This process is based on a voltage-to-current conversion (i.e., the input voltage into the current flowing through *RD*). This current is used to discharge capacitor *C* with a constant slope. When voltage V_C crosses the threshold of transistor *M*5, the output voltage *OutV2T* rises, driven by a tapered inverter chain. A simple flip-flop delay (DFF) identifies the faster signal between the two V2T output pulses. The digital logic connected to the gate of transistor *M*2 has the purpose to stop the discharge of the capacitor *C* after the commutation of the signal *OutV2T*, as shown in Fig. 7.19.

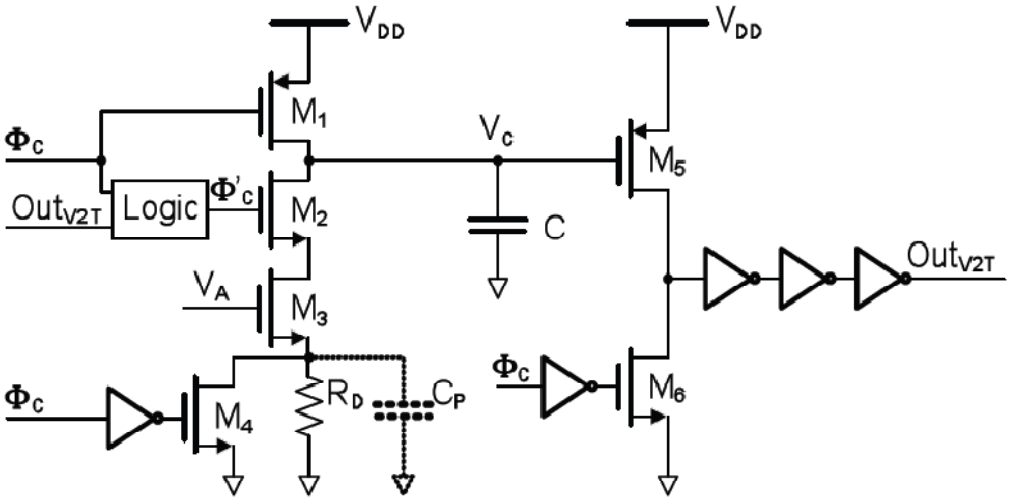

Fig. 7.18: V2T schematic diagram.

In this way the power consumption spent for a comparison step decreases of at least a factor two. The most important limit on the value of capacitance *C* is the thermal noise which imposes at least 0.8 pF. Therefore, the estimated power related to the comparator is about 880 nW. When designing a time-domain comparator, the time error, conceptually described in Fig. 7.20, introduced by the DFF has to be taken into account.

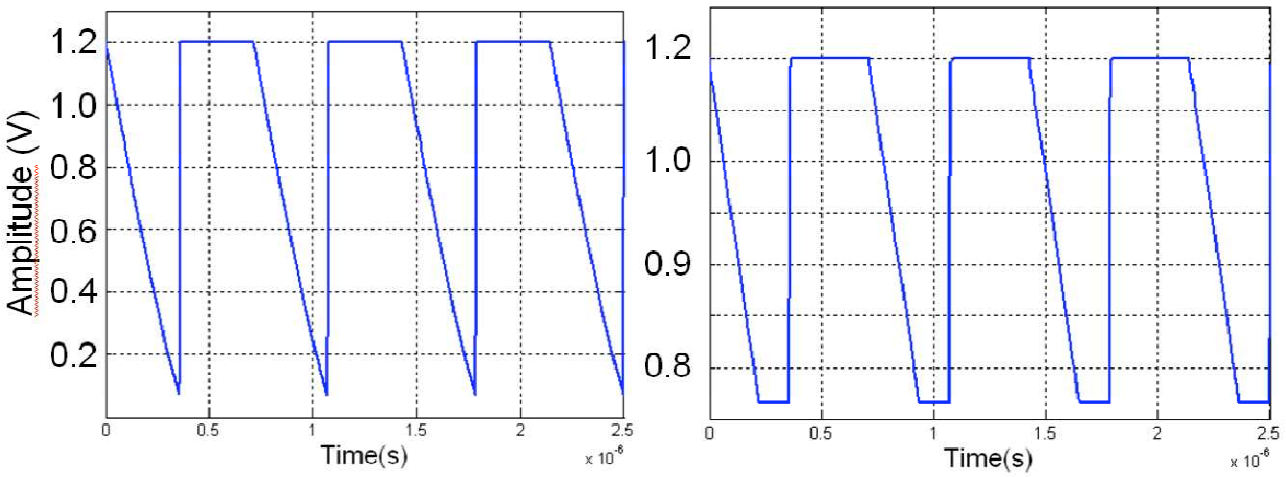

Fig. 7.19: Voltage across C without and with the digital logic on gate of M2.

This error can be considered as an equivalent input voltage of

$$V_{IN,eq.err} = \frac{t_{ji}}{T} \cdot \left(V_{ref} - V_{GS3}\right) < \frac{V_{REF}}{\sqrt{2} \cdot 2^{N+1}} \tag{7.5}$$

where the time t_{ji}, characteristic of the time comparator, is equal to 130 ps, V_{ref} is the input voltage of the V2T used as reference, and $V_{REF} = V_{REF+} - V_{REF-}$. Therefore, to obtain an equivalent input error less than a quarter of LSB, it is required a comparison time of at least 226 ns.

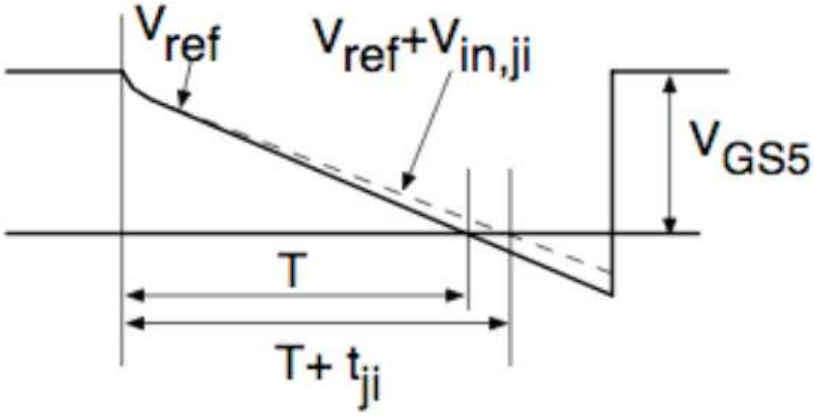

Fig. 7.20: V2T schematic diagram.

Time Domain Comparator

As mentioned above, to meet the low power requirements, the successive approximation register is full custom designed, which implicates a power consumption of about 1.8 μW. It is worth to point out that the SAR logic generates also the A/D converter control phases. The SAR logic is optimized for minimum power consumption. The conversion requires 14 clock periods of the main clock: the first for the input sampling, 12 periods are for the successive approximation cycles and the last one for end of conversion and data transfer.

Time Interleaved Solution Issues

The SAR converter requires 14 clock periods to obtain a single conversion and this limited comparison speed of the time-domain comparator motivates the choice to consider a time interleaved approach to meet the required conversion rate. The number of different paths used in this approach must to be equal to an integer divisor of the number of clock periods needed for a conversion with a simple SAR. In particular, in this paper, an architecture with 7 parallel paths is analyzed. In the single-path solution, as described above, two V2T converters are used in the time-domain comparator, one to process the input signal (signal V2T) and the other used as a reference (reference V2T). This choice ensures good matching performance between the two V2T

blocks. When considering a 7 parallel paths solution, it is possible to use only one reference V2T for all 7 signal V2Ts, as shown in Fig. 7.21. This solution, obviously, allows strongly reducing the power consumption. When approaching a time interleaved topology, issues related to gain and offset errors have to be carefully analyzed. In a time interleaved SAR ADC, the gain error of each converter depends mainly from the DAC. In this work, the DAC has been designed with analog output as a function of the reference voltages. It has to be pointed out that the reference voltages are the same for all DACs present on each path, thus leading to any gain error. The gain error depends also on DAC capacitors mismatch, but the DAC structure adopted in this design allows obtaining good matching performance, [13].

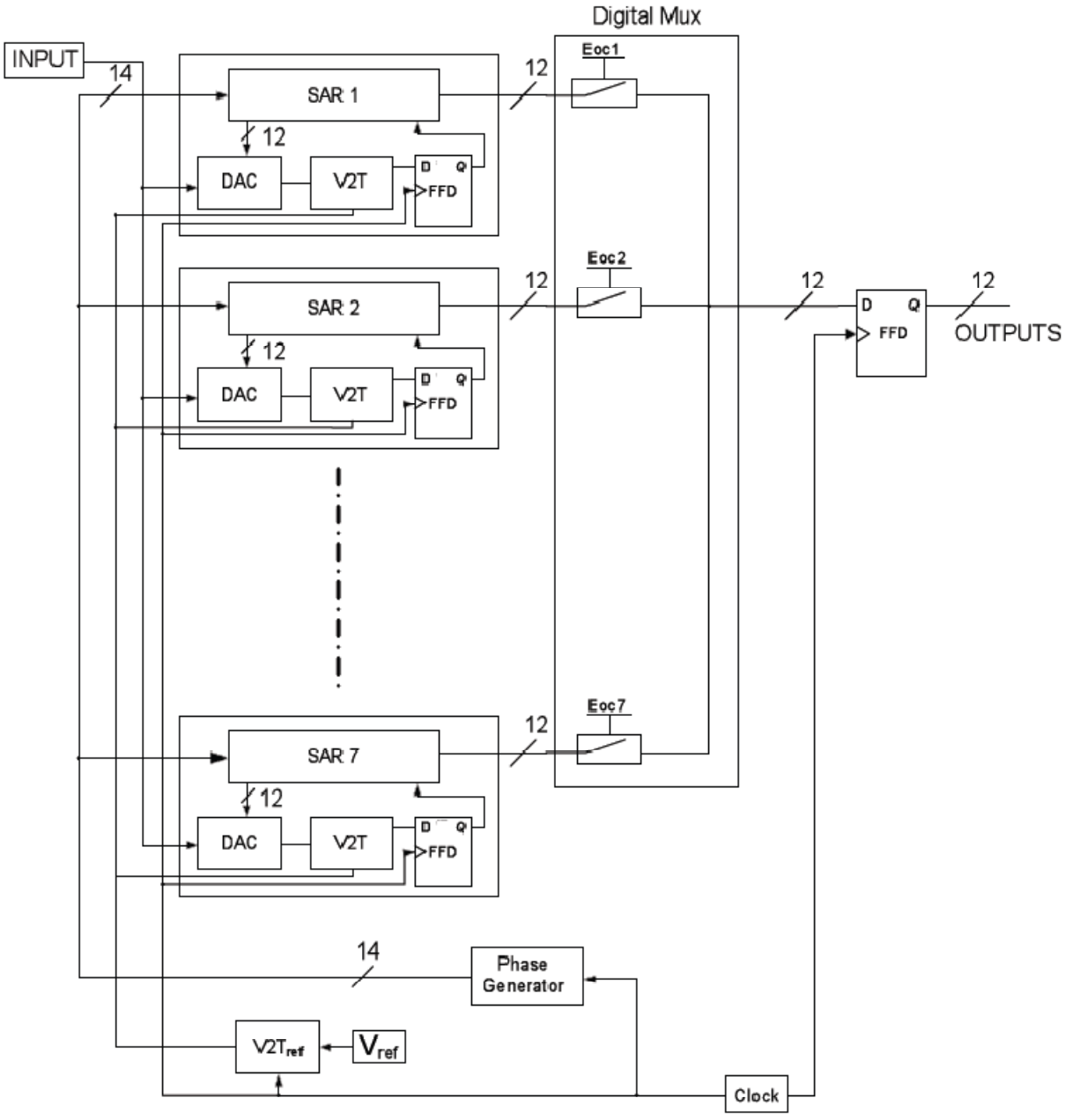

Fig. 7.21: Time interleaved solution with SAR converter based on time-domain comparator.

The second critical issue to be considered when designing a time interleaved ADC is the offset error. In the case of a time interleaved SAR converter, the block that introduces this kind of error is the comparator. In our design, different sources of V2T input offset are present: mismatch among capacitors C or resistors R_D, transistor $M5$ threshold variations, and FFD time errors. The basic idea in order to compensate for all these offset contributions is to trim the value of resistor RD by means of an adequate digital trimming circuit. This leads to reduce the equivalent input offset below half LSB. To estimate the overall equivalent input offset of a reference V2T with comparison time equal to 230 ns, several Montecarlo simulations have been performed. As a result, it has been verified that the comparison time is in the range from 200 ns to 260 ns. Translating these time values in the voltage domain, it means that the possible equivalent input offset can assume values from -43 mV to +40 mV. Considering that half LSB is equal to 122 μV, it is apparent that the digital trimming of resistor R_D is not effective. The idea is to perform first a coarse offset reduction by trimming on each DAC the bias voltage, referred to as V_{bias} in Fig. 3, and then the fine digital trimming of resistor R_D. The manual course calibration precision is typically of about 10-15 mV. With regard to the fine digital trimming design, it is worth to point out that a V2T input offset error equal to half LSB can be compensated for by a R_D variation of 330 Ω. In this way, at least 100 330-Ω resistors are required to compensate for the residual offset of 10-15 mV. This leads to a digital trimming that foresees the use of 7 bits (i.e., 128 steps). Considering the technology mismatches on resistors values, a nominal resistor of 312 Ω is used. Considering mismatch, this resistor can vary from 294 to 330 Ω so that an overall input offset of 13.9-15.6 mV, respectively, can be corrected. The power consumption of the digital logic which manages the time interleaved structure is estimated to 10 μW.

The proposed time interleaved SAR ADC has been realized at the transistor level and simulated by using a conventional 0.18-μm CMOS technology. The used power supply value is 1.2 V. Fig. 7.22 shows the simulated output spectrum (obtained with 1024 samples) of a SAR converter. The sampling rate is 100 kS/s and the sine wave input signal frequency is 29.8 kHz. It can be noted that the noise floor is almost flat. The simulated SNDR is equal to 65.6 dB.

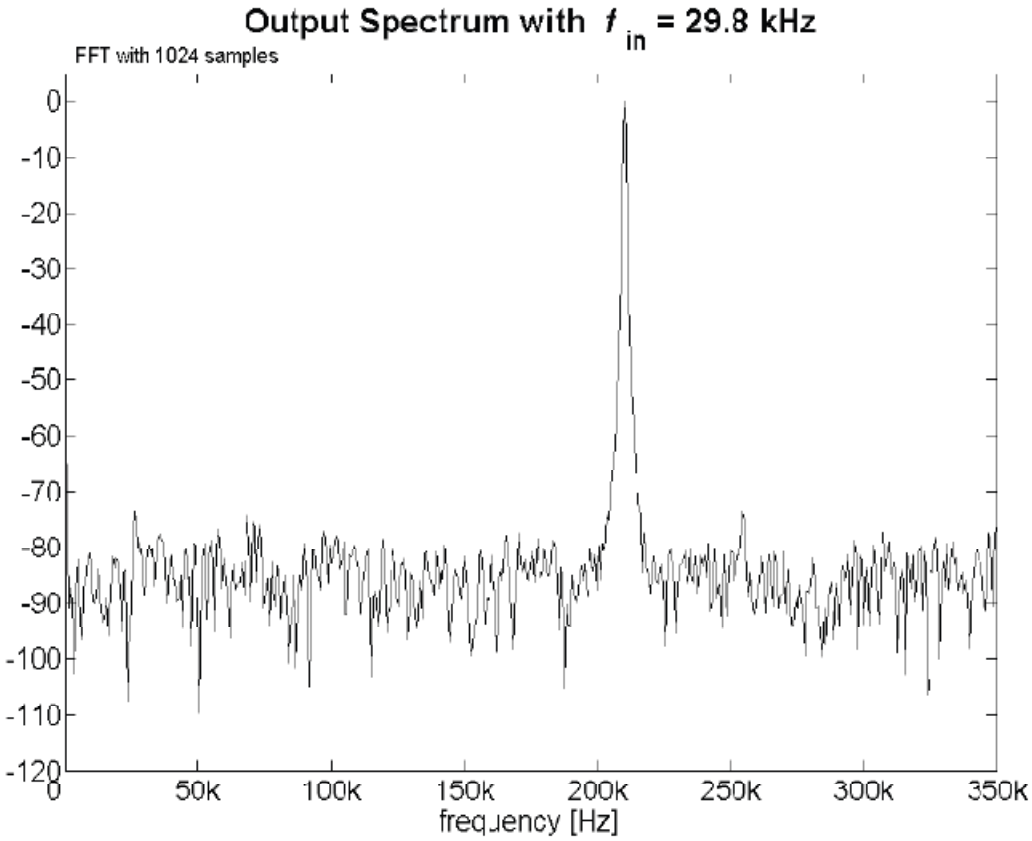

Fig. 7.22: Single path SAR ADC output spectrum.

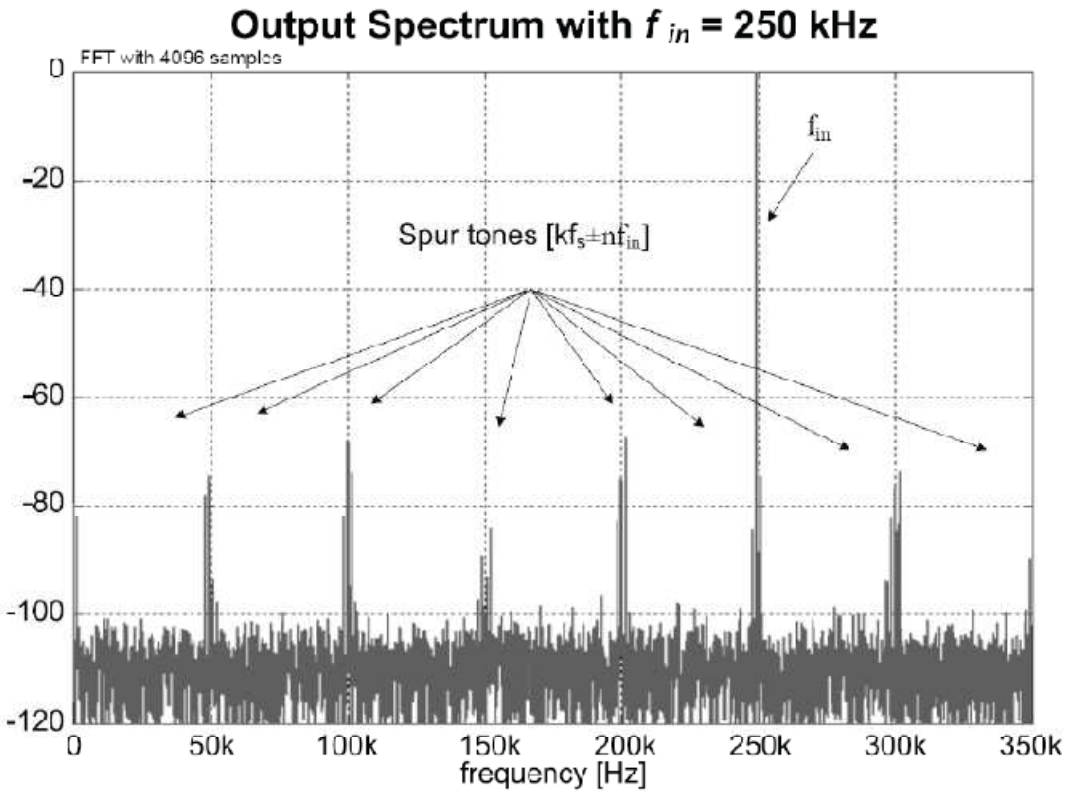

Fig. 7.23: Effects of offset on output spectrum.

Fig. 7.23 shows the output spectrum simulated at the behavioral level in order to evaluate the effect of different offset into each path of the time interleaved structure, before the relative correction. It is apparent the presence of spur tones at 1/7 of the sampling frequency and its multiples. Fig. 7.24 shows a behavioral dynamic simulation of the 7 parallel paths time interleaved SAR converter after the digital correction of the offset. The output spectrum depicted in Fig. 7.24 has been obtained including an offset error with standard deviation equal to 2 LSB. The frequency of the input sine wave is 200.9 kHz. It can be noted that the second and the third harmonics are present. The second harmonic tone, placed at about 300 kHz, is at -78 dB while the third harmonic tone, placed at about 100 kHz, is at -81 dB. The simulated power consumption of the time interleaved SAR ADC is about 40 µW. This value leads, considering a signal bandwidth of 350 kHz, to a FoM as low as about 37 fJ/conv.-step. Has been presented an ultra low-power time interleaved SAR ADC. This design uses 7 interleaved converters and achieves a conversion rate of 700 kS/s. Design considerations about time-domain comparator offset calibration have been drawn. The A/D converter has been simulated at the transistor level by using a 0.18-µm CMOS technology. The simulated power consumption is as low as 40 µW which allows obtaining a state-of-the-art FoM equal to 37 fJ/conv.-step.

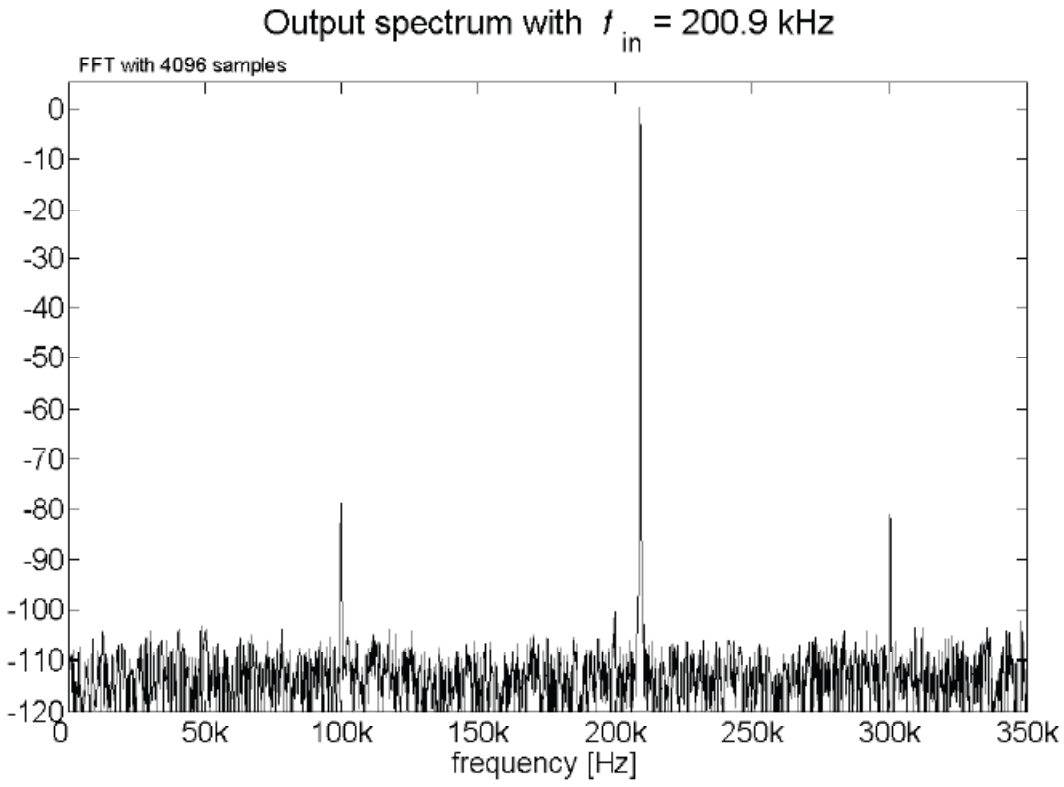

Fig. 7.24: Simulated time interleaved SAR output spectrum.

7.3 Incremental Sigma-Delta

The DAC, into an analog to digital converter, is used in the feedback path; therefore errors introduced by the DAC have the same transfer function of the input signal and then it is impossible to discriminate that errors from the signal. Fortunately the other errors, in particular the ones which are introduced by the ADC in the direct path, have a different transfer function to output and then is possible to reduce their effects on the conversion. A particular attention to this way has been given by the *Sigma-Delta* modulator, which have the purpose to implement an optimized transfer function for the errors of the ADC. In fact their solution, which is valid when the quantization noise can be represented as noise, includes a noise shaping outside the signal bandwidth, and that shaping depends from oversampling ratio [14]. They are also among the most power efficient A/D conversion architectures [15]. It is important to underline that for very slow signal, at limit *dc*, the hypothesis to consider quantization error like a noise is not valid, and then it is not possible to exploit the previous consideration. The main advantage to use a ΣΔ modulator is the effects of the noise shaping about the quantization noise introduced by the ADC [16]. This effect is apparent by the different between the transfer function of the input signal (STF) and the transfer function of the quantization noise (NTF). Another type of error, which must be considered, is the non-ideal analog value of each level at the output to the Digital to Analog Converter (DAC), used in feedback. In fact it can give critical effects, because it has the same transfer function of the input signal (STF).

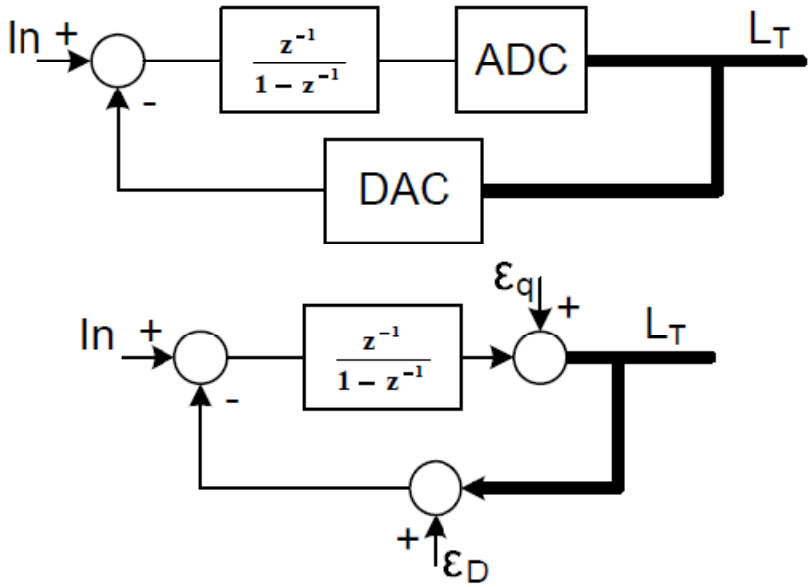

Fig. 7.25: Incremental 1st order ΣΔ modulator.

Must be taken in account that if the input bandwidth is very low, at limit *dc*, it is not possible to match the quantization error introduced by the ADC as a noise, and then the previous hypothesis, which are at the base of the used model to approximate the ΣΔ modulators, are not true; therefore the model cannot be used to represent the ΣΔ modulators for very low frequencies. Using an input signal with these characteristics, a possible solution is to realize an ADC based on an incremental ΣΔ modulator. This one keeps the advantages of typical ΣΔ modulator in noise reduction *vs* Over Sampling Ratio (OSR), but it can work at very low frequencies. The simplest solution of the incremental modulator is the first order one, represented in Fig. 7.25. From the scheme appears as a simple ΣΔ, but it works for a fixed number of steps (N) and, every conversion requires to reset the initial conditions of each component whit memory. At the end of N steps series will be done a digital word which represents the average of N samples of input signal. The digital output *LT* will be connected to a digital logic which has the purpose to elaborate the sequence of digital data to supply the right value in output.

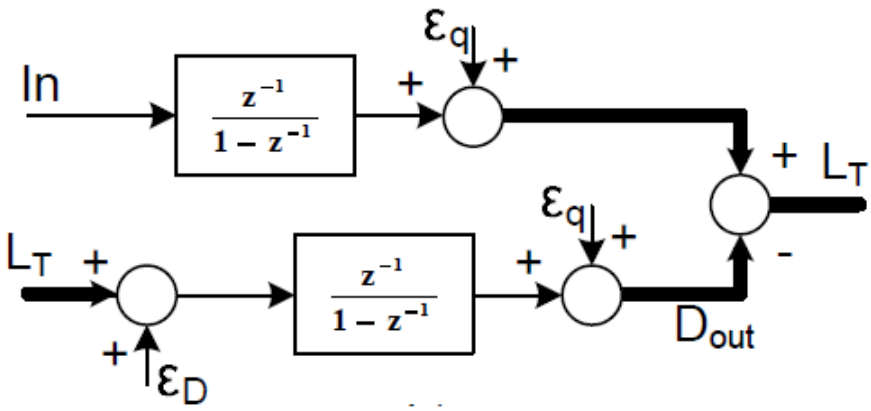

Fig. 7.26: Linear transformation on Incremental 1st order ΣΔ modulator.

The design of digital logic is based on the schema in Fig. 7.26 where the digital word D_{out} represent the best approximation of N-times integration of the analog input. To obtain the correct conversion it is required that the value of *Dout* after N clock period has to be divided by the same value obtained at the output when the input signal is equal to full range voltage (equal to N in first order modulator). In this way the architecture for a first order solution is given in Fig. 7.27, and the value of the output is done by the digital word *Out* at $(N+1)^{th}$ step. In the ladder schema is possible to observe that the quantization error (ε_q) introduced by the ADC is token in account by the digital calculation block while the DAC errors (ε_D) is considered as the input signal. In particular the output digital value, at the end of a single conversion, results:

$$Out(N+1) = \frac{\sum_{i=1}^{N} In_i}{N} - \frac{\sum_{i=1}^{N} \varepsilon_{Di}}{N} + \frac{\varepsilon_q(N)}{N} \tag{7.6}$$

Then, the obtained value represents the average of N sample of input signal but it is corrupted by the errors of ADC and DAC. In particular the error $\boldsymbol{\varepsilon_q}$, introduced by ADC is always more negligible with the increase of N, while the error $\boldsymbol{\varepsilon_D}$, introduced by DAC, is considered with the same weight of input signal and then it must be designed negligible respect to LSB.

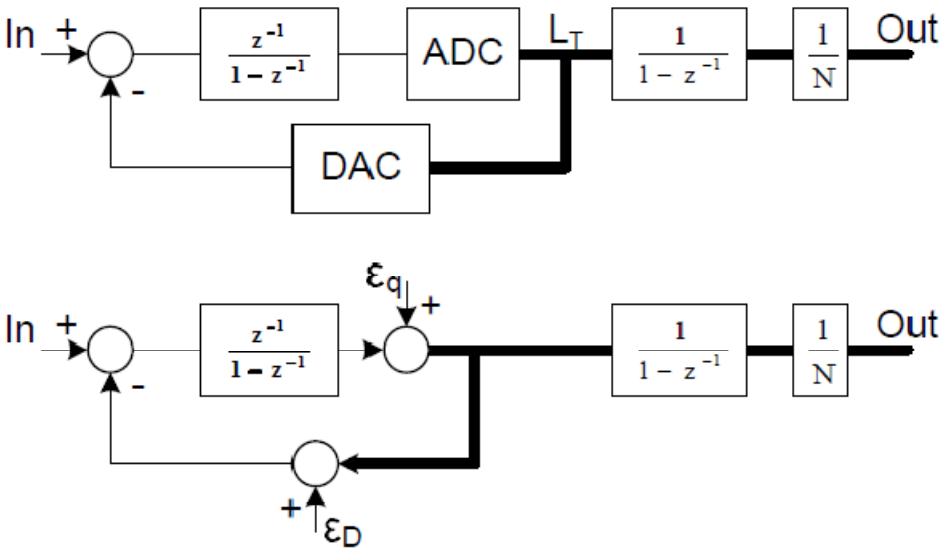

Fig. 7.27: Incremental 1st order ΣΔ Modulator with digital calculation.

The used DAC configuration is a typical switched capacitor structure shown in Fig.7.28. The following considerations are based on a 9 levels DAC, realized with 8 capacitances, but is possible to extend the results to any multibit DAC. The numbers 1 or 2 on each switch represent which Phase controls the relative switch. The left switches are controlled in timing from Phase 1, while the choice of the voltage to connect is determined by the value of the digital word written in thermometric scale (LT). Using that solution is possible to determine the 9 levels: 0, V_{ref} ·1/8, V_{ref} ·2/8, … , V_{ref} ·7/8, V_{ref}. Because of the mismatch between capacitances, really, the levels are not so good determined, and it is possible to obtain some errors on each analog level. Naturally the level 0 and level 9 are not corrupted to the mismatch because they require the connection of all the capacitance to the same voltage. For ensuring M bit with a G capacitances structure, it is mandatory that the mismatch must be better than $\sqrt{\frac{G}{2} \cdot 2^M}$ between capacitances. Suppose to use a technology that ensure matching accuracy with $\sigma = \frac{0.3\%}{\mu m^2}$ which improves as $\frac{1}{\sqrt{A}}$, where A is the area of the plate,

1ppm requires 9˙000˙000 µm^2 which corresponds at about 45nF of capacitance, much more than the value required by the $\frac{kT}{C}$ limit, and too large for ensuring a low power consumption.

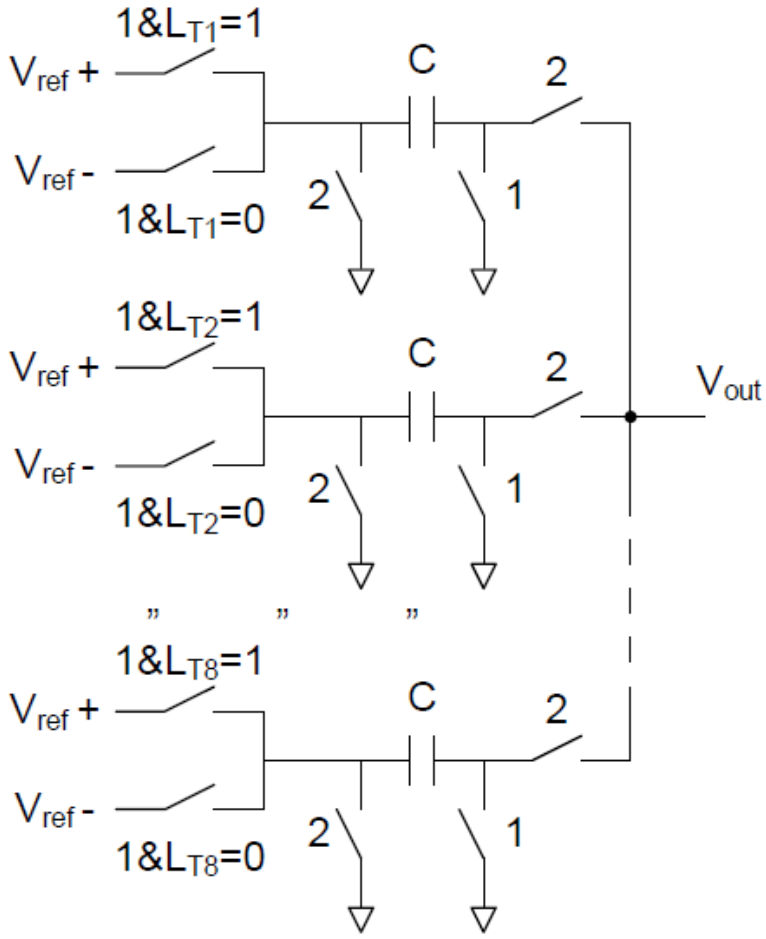

Fig. 7.28: 9 levels DAC.

Typical solutions applied to ΣΔ modulator are to use anyway small capacitance and adopt some scrambling algorithms for choosing capacitances in the DAC. In this way, the same level has not determined by the same capacitances, then the result is to use different analog level, in different steps, to the output of the DAC with the same digital word. A possible implementation chosen among these solutions can include, for example on first level DAC (Input word equal to 0001), to use the capacitance C1 the first time, the capacitance C2 the second time etc. When the capacitance C8 has used for first level than will be used newly C1 and so on. The idea is to cancel the effects at the output of the integrator after 8 time the first level has used. Similarly to the first level is possible to follow the same way for the other levels. But, while for the first level there are 8 different combinations, for the second level (0010) there are 28 different analog levels and 56 for the third one (0011), 70 for the fourth one (0100), 56 for the fifth one (0101), 28 for the sixth one (0110), and

8 for the seventh one (0111). For minimizing the residual effects at the output is required to ensure that each combination for every considered level will be used the same number of time. This consideration is not so easy to ensure but, is possible to consider negligible the output effects if the number of step in the incremental modulator is very high respect to 70 possible different combination of capacitance in the fourth level.

Proposed solution with digital correction

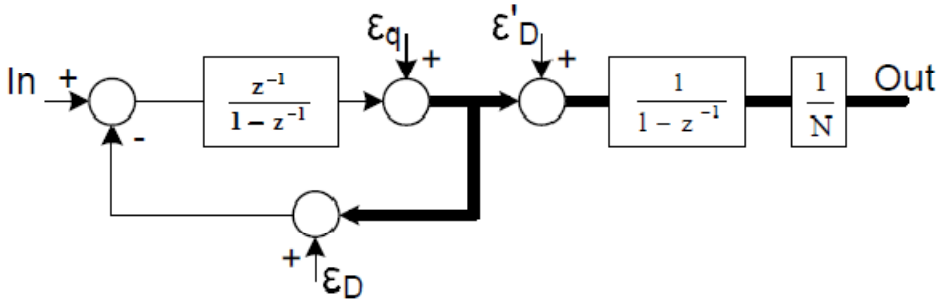

Fig. 7.29: Proposed Solution applied to an Incremental 1st order ΣΔ Modulator.

The first proposed solution, applied to first order incremental ΣΔ modulator, can be represented by the Fig.7.29. In this figure is apparent that the purpose of the introduced sum block which keeps in account the DAC errors also in the digital path. This change allows to reduce the real effects of DAC errors. In fact, how it is shown in Fig. 7.30, the introduction of the sum block in that position is equivalent to reduce the errors introduced in the feedback path to the difference of DAC errors and its estimated value. Therefore it is needed realize an opportune calibration to define ε'_D with the required resolution.

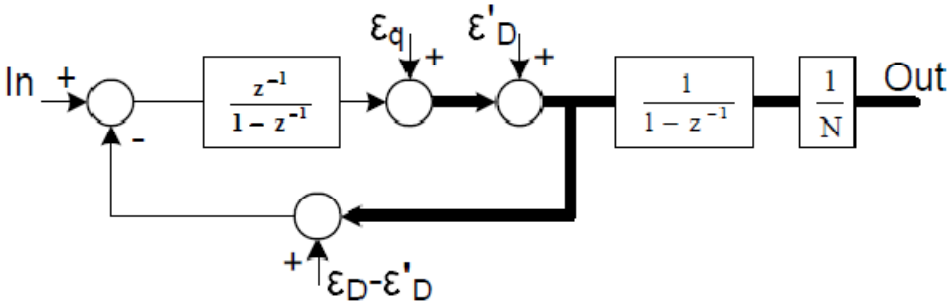

Fig. 7.30: Equivalent Scheme of Proposed Solution.

In the adopted solution, with zero initial conditions, we obtain:

$$Out(N+1) = \frac{\sum_{i=1}^{N} [In_i - (\epsilon_{Di} - \epsilon'_{Di})]}{N} + \frac{(\epsilon_q(N) + \epsilon'_D(N))}{N} \tag{7.7}$$

where ε_{Di} is equal to ε_1, ε_2, …, ε_7 depending if at the step *i-th* is used the 1*st*, 2*nd*, …, 7*th* level of the DAC. The values of the ε_1, ε_2, …, ε_7 are the relative errors introduced by the mismatch of the capacitance on the own level. If the 0-*th* or 8-*th* levels are applied, the correspondent error is equal to zero. The errors are definite as:

$$\begin{aligned} \epsilon_1 &= \frac{C_1}{\sum_{i=1}^{8} C_i} - \frac{1}{8} \\ \epsilon_2 &= \frac{C_1 + C_2}{\sum_{i=1}^{8} C_i} - \frac{2}{8} \\ &\dots \\ \epsilon_7 &= \frac{\sum_{i=1}^{7} C_i}{\sum_{i=1}^{8} C_i} - \frac{7}{8} \end{aligned} \tag{7.8}$$

The first step to evaluate the values of ε_1, ε_2, …, ε_7 is to determine the relative value of each capacitance respect to one of them, and to obtain that digital value is used the schemes in Fig.7.31. The configurations shown here has based on the idea to use an integrator which integrate the difference in charge injected by the reference capacitance (C_{ref}) and the unknown capacitance (C_x), both charged to V_{ref}. The number of needed steps (N_{StepX}) to the output of the integrator to reach the V_{ref} represent the searched information, in fact we can assume that:

$$\begin{aligned} C_1 &= C_{ref} = 1; \\ C_2 &= C_1 + \epsilon_{C2} = C_1 \pm \frac{1}{N_{Step2}} \\ &\dots \\ C_8 &= C_1 + \epsilon_{C8} = C_1 \pm \frac{1}{N_{Step8}} \end{aligned} \tag{7.9}$$

where ε_{C1} is equal to zero, and the sign plus or minus depends by the sign of the accumulated voltage on the integrator. To reduce the effects of the OpAmp and comparator offset to the measure

of capacitance are used two different measure based on the use of chopper technique in the OpAmp and change the environment conditions to the comparator. So the first measure (Fig.7.31 a)) is corrupted by the offset of the Opamp and the comparator, but second one (Fig.7.31 b)) is corrupted by the opposite value. In this way the effective *NStepX* is equal to the average of the two measure done. Obtained the values of the capacitances is possible to calculate the relative errors, for each level, at the output of the DAC.

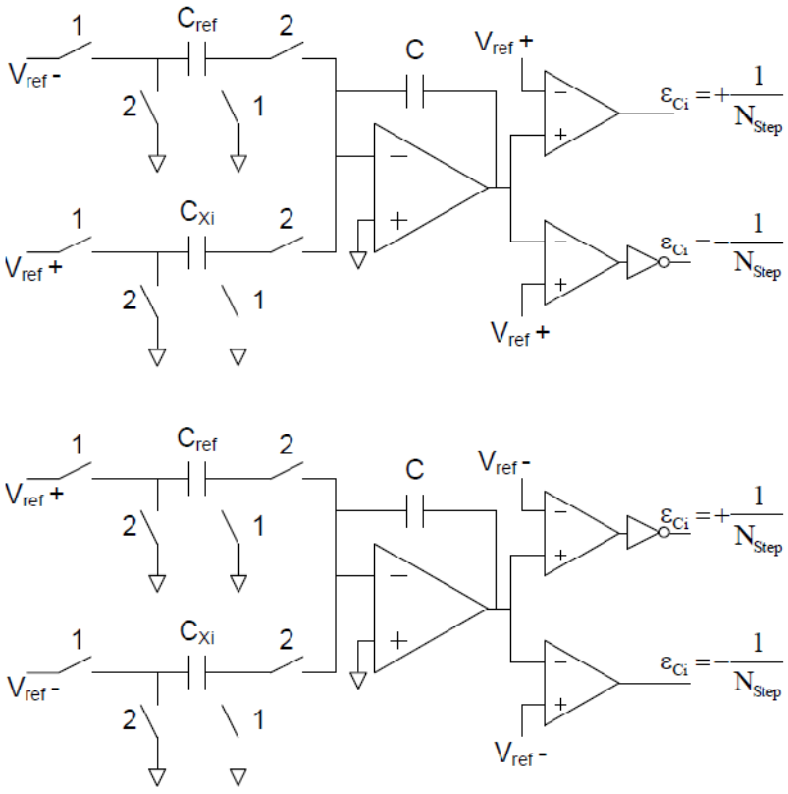

Fig. 7.31: Schema used for measuring the coefficients ε_{Cx}.

These values can be evaluated by (7.8), but it is not so comfortable to do those operations in digital logic, so is possible to approximate the formulas with:

$$\begin{aligned}
\epsilon_1 &= \frac{C_1}{\sum_{i=1}^{8} C_i} - \frac{1}{8} = \frac{C_1}{8 + \sum_{i=1}^{8} \epsilon_{Ci}} - \frac{1}{8} = \\
&= \frac{C_1 \cdot \left(8 - \sum_{i=2}^{8} \epsilon_{Ci}\right)}{8^2 - \left(\sum_{i=2}^{8} \epsilon_{Ci}\right)^2} - \frac{1}{8} \cong -\frac{\sum_{i=2}^{8} \epsilon_{Ci}}{8^2}; \\
\epsilon_2 &= \frac{(2 \cdot C_1 + \epsilon_{C2}) \cdot \left(8 - \sum_{i=2}^{8} \epsilon_{Ci}\right)}{8^2 - \left(\sum_{i=2}^{8} \epsilon_{Ci}\right)^2} - \frac{2}{8} = \\
&= \cong \frac{8 \cdot \epsilon_{C2} - \sum_{i=2}^{8} \epsilon_{Ci}}{8^2}; \\
&\cdots \\
\epsilon_7 &\cong \frac{8 \cdot \sum_{i=2}^{7} \epsilon_{Ci} - \sum_{i=2}^{8} \epsilon_{Ci}}{8^2}.
\end{aligned} \tag{7.10}$$

The precision used to write these values must respect the LSB of the desired resolution of the ADC, as already seen in (7.7).

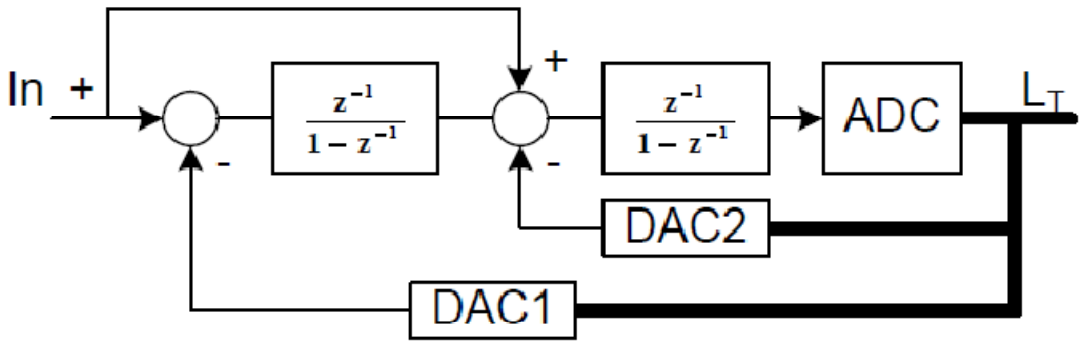

Fig. 7.32: Incremental 2nd order incremental modulator.

A second order incremental ΣΔ modulator is used to study the benefits of the proposed solution. The scheme used for simulations is given in the Fig. 7.32. The purpose of that circuit is to ensure a converter with an Effective Number of Bits (ENoB) greater than 19 bit. 1024 steps of incremental and multilevel DACs with 9 output levels are used for simulations. In this schema it is apparent that there are two different DAC, one for each integrator. In this simulations the DAC1 includes correction, while DAC2 is used ideal because its errors have negligible contributions [4]. For designing the digital correction we assume a mismatch between the capacitance equal to 1.8‰. The maximum ratio is about 1.0036 and can be approximated with the sum of 2^{-9} … 2^{-12} bits. In the other hand the required precision must be better than 2^{-19}, therefore are required at least 10 bits to indicate the error of each capacitance.

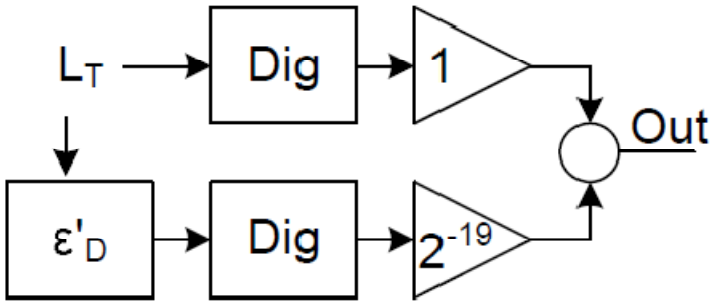

Fig. 7.33: Digital part used to calculate output in simulations.

The output of the calculations in (7.10) determines the error for each level of the DAC, and they can have a precision of 2^{-22} for ensuring a high precision digital correction at the output. The maximum error is done at the fourth DAC level when the relative capacitance has a different sign of error and this value is equal to 2^{-14}. Therefore are required at least 9 bit to write the values of $\varepsilon_1, \varepsilon_2, \ldots, \varepsilon_7$. Final applied digital circuit is given in Fig. 7.33 where the ε'_D block has the purpose to supply the right value between $\varepsilon_0, \varepsilon_1, \ldots, \varepsilon_8$ depends from L_T. Behavioral simulations have done. The main performances of the ADC full system was investigated. The simulation consist of inject a dc voltage to the input of the converter and read the difference between input and output. That value represent the error introduced by the converter and then it is possible to obtain the ENoB The Fig.7.34 shown two plots, the light one represent the ENoB of the converter without correction, while the dark one represent the ENoB after proposed digital correction.

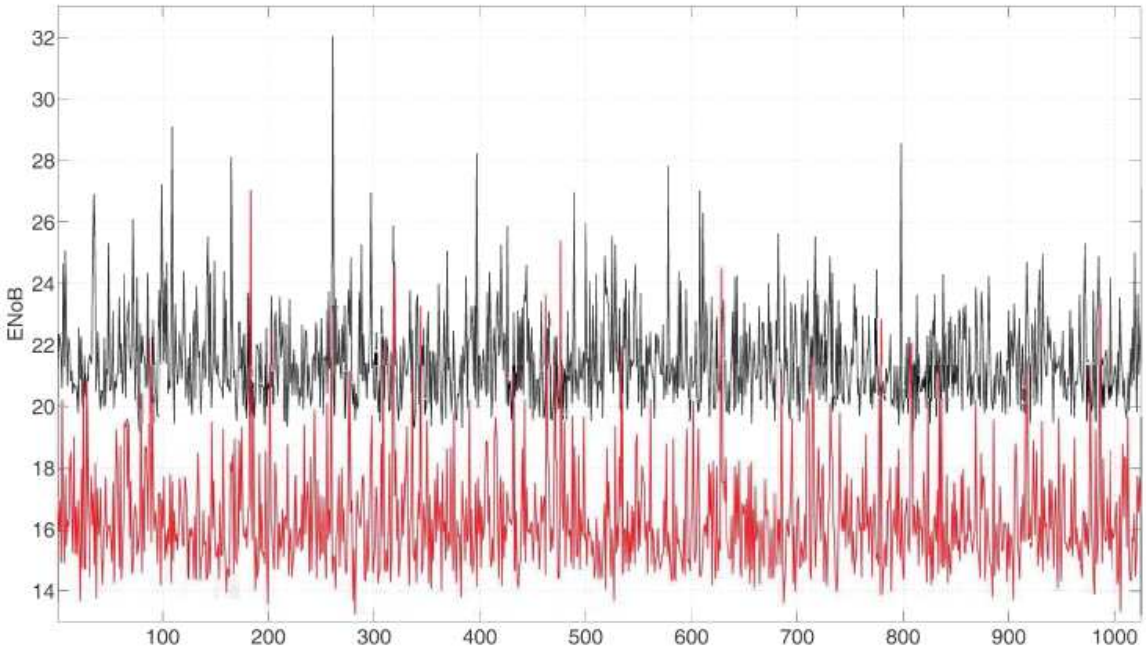

Fig. 7.34: ENoB before (red line) and after (black line) digital correction *vs* different cases.

On the independent axes is done the number of the case. The value of each capacitance is changed every case, keeping in account the mismatch. The number of bits in an incremental ADC is also a function of the input voltage, therefore the input voltage is changed every case too. It is apparent the increasing of the performances, in fact the minimum of the value obtained on 1024 cases without correction is equal to 13.3 bit, while the value of ENoB obtained with digital correction is equal to 19.08 bit. It was demonstrated that it is possible to increase the signal to noise ratio in an ADC based on incremental ΣΔ modulator by introducing a digital correction. This correction requires a initial step where all the capacitance must be measure by the same modulator used for conversion. The final digital filter must keep in account the calculated value of each output level of the DAC putted in feedback to the modulator. This approach allows to introduce multi-bit DAC in the converter loop with all the benefit introduced by the use of multi-bit solution. A second order incremental ΣΔ modulator is studied in this paper and the proposed solution increases the effective number of bit from 13.3 to 19 bit.

Proposed solution with fast DAC

Considering a second order ΣΔ modulator, as seen before the most critical DAC is the one connected to the input because it has the same transfer function of the input. In order to obtain a good mismatch between elements has been searched a solution which allows to obtain a good trade-off in speed and resolution. The second proposed solution, represented in Fig.7.35, where have been simplified the integration blocks, which are represented by a simple digital representation. In particular it is possible to observe that the DAC1 and DAC2 are not identical, in fact the DAC2 has been realized by the simple configuration because of the little influence on output of its introduced errors. The most particular solution is applied to DAC1 which is realized by the use of just one capacitance, so it is possible to avoid any mismatch errors. This solution has the main characteristic to require an high speed solution for DAC1. In this way the first integrator has the purpose to integrate the same quantity of charge of traditional solution, but it is injected by 8 different step by the same capacitance and then each step is equal to the other ones.

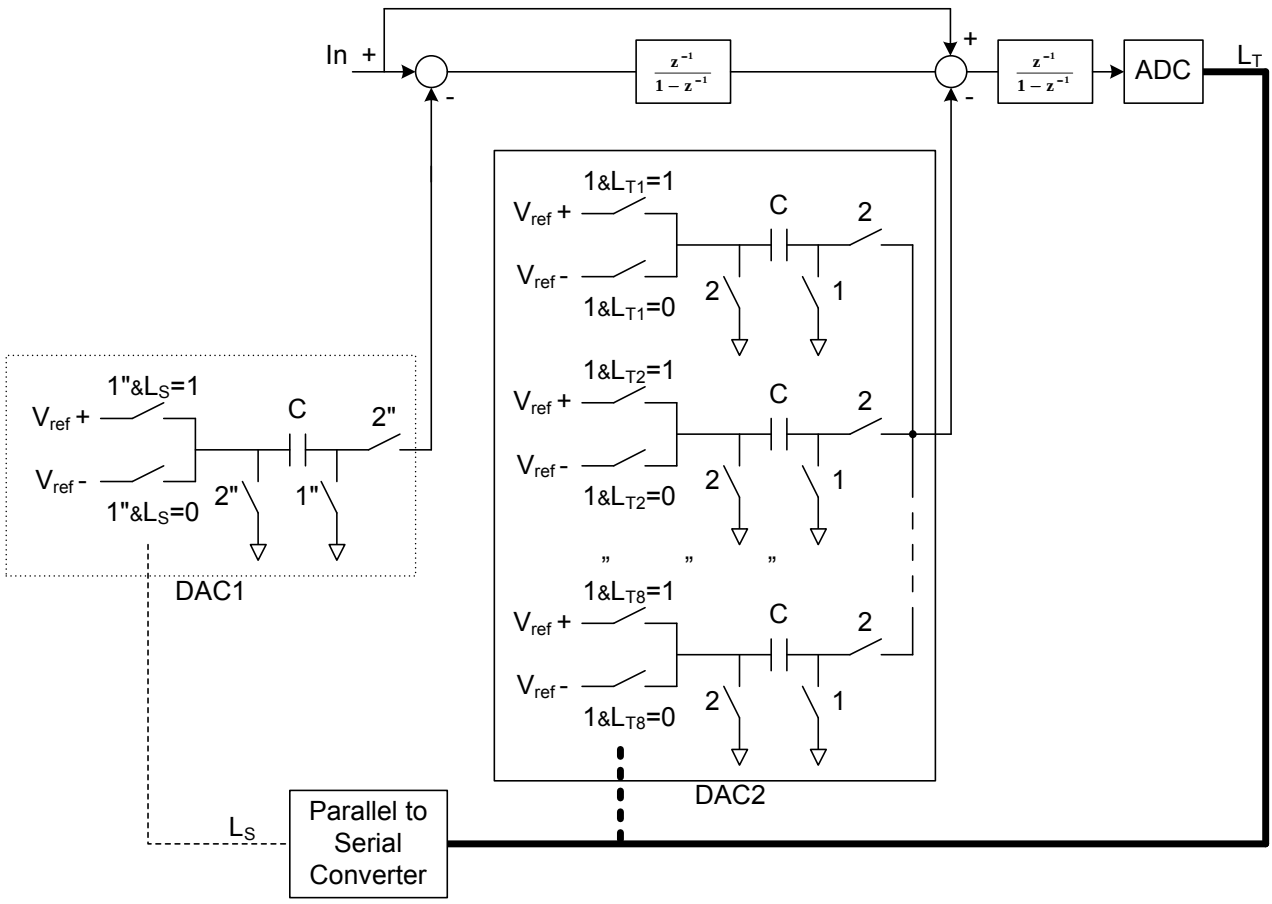

Fig. 7.35: Schema of the fast DAC solution.

Then the used phases to command the full system are shown in Fig. 7.36.

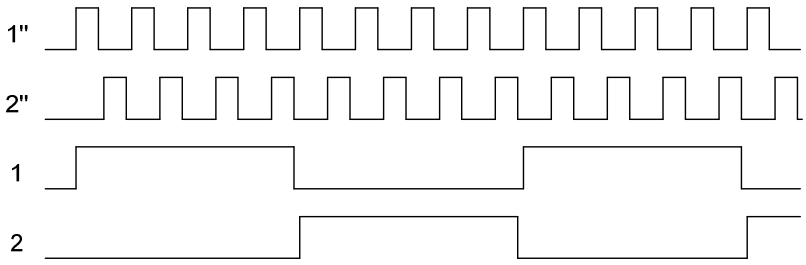

Fig. 7.36: Phases used in the proposed solution.

Offset issues

Another issues which must be taken in account in these structures are the offset introduced by each operational amplifier used in the ΣΔ modulator. In fact they are the purpose to realize an integrator and their offset can corrupt the output by integrating also it one. To cancel the effects of the offset in an integrator is possible by using a chopper technique where the chopper signal must keep in account the number of step of integration. In fact the purpose in designing the optimal chopper signal is to obtain zero contribution from offset. In order to obtain that goal is possible to evaluate the effects of the offset at the output of each integrator.

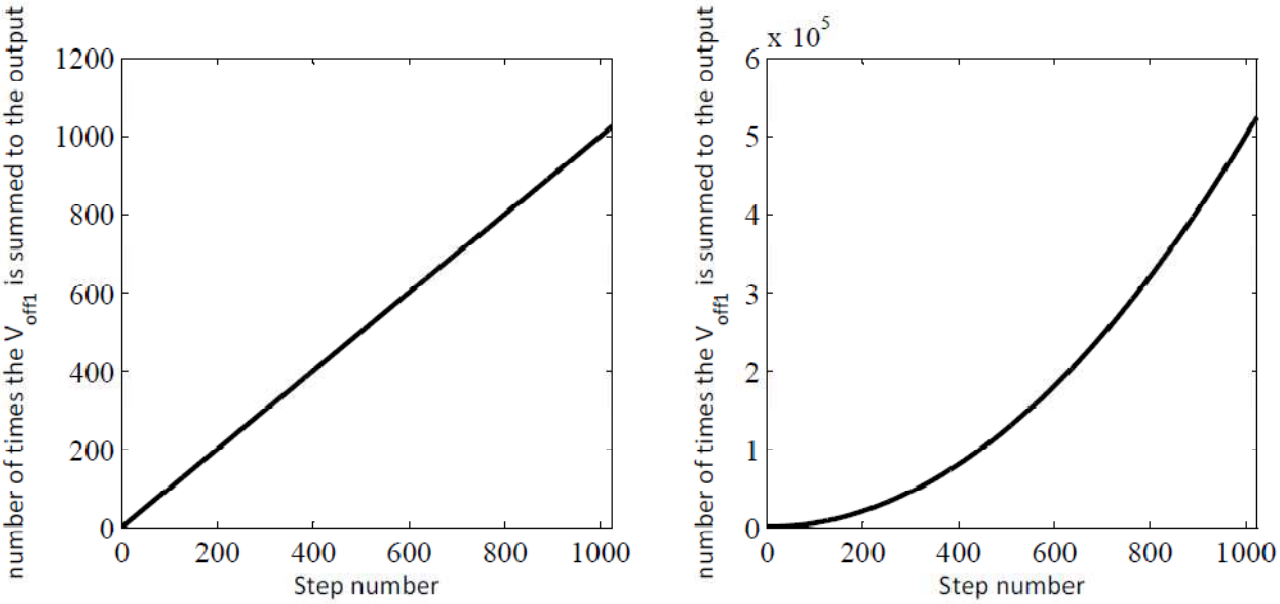

Fig. 7.37: Effects of the 1st opamp offset to the output of the 1st and 2nd integrator w/o chopper.

In Fig. 7.37 are shown the output of each integrator with input signal equal to zero, and all ideal objects except the offset of the first integrator amplifier, which has been putted to 1 for simplicity the equations. With the purpose to get a zero contribution from offset, and to use a chopper technique for obtaining that goal, has been found the possibilities to use a chopper signal with just two edge at 256th and 768th step. In this way the respectively output become the signal shown in the Fig. 7.38.

The offset contribution of the second integrator amplifier can be considered negligible with a particular and attention design of the amplifier. In the other way is possible to introduce the chopper technique also to the second integrator amplifier commanded from the same chopper signal, in fact the output of the second integrator, considering all ideal things except the offset of the second

integrator amplifier is correspondent to the Fig. 7.37 (a) without chopper and Fig. 7.38 (a) after the chopper technique applied.

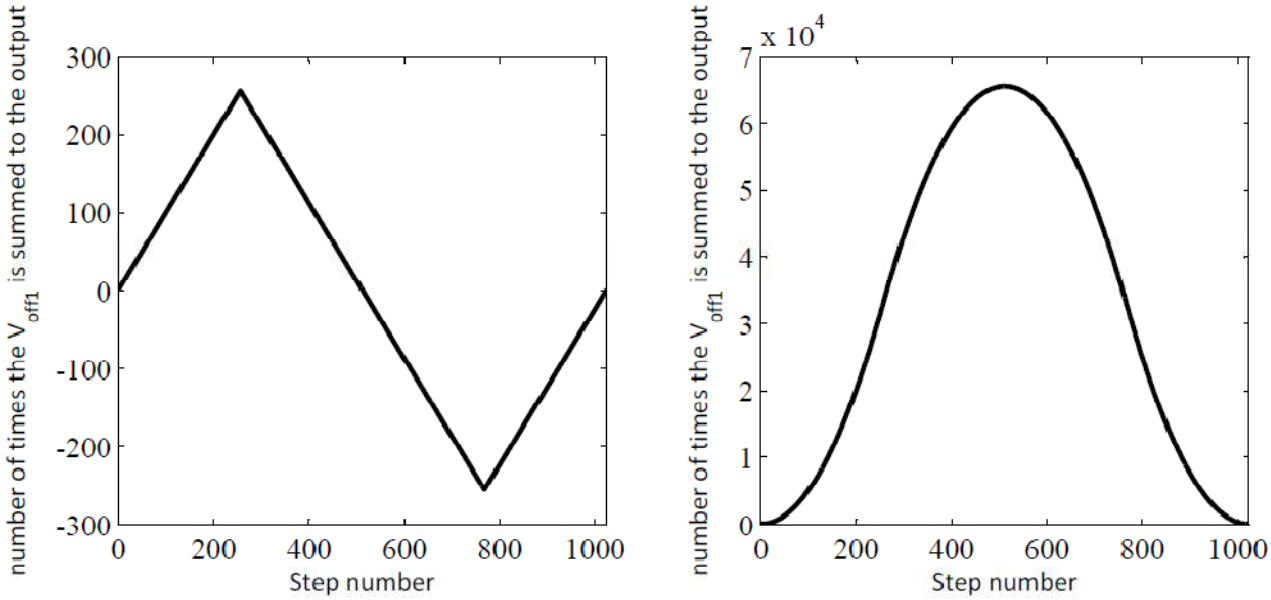

Fig. 7.38: Effects of the 1st opamp offset to the output of the 1st and 2nd integrator with chopper at 256th and 768th step.

Conclusions

In conclusion these project about incremental Sigma-Delta are studied with the purpose to increase the efficient of the use of a multibit DAC into a ΣΔ modulator. The architecture with fast DAC has been implemented on silicon but, because some problem about process delay, the experimental results are not suitable on the test chip yet.

7.4 Conclusions

The PhD activity was mainly focused on the project about the SAR converter described in the previous chapter. In addition other studies have been performed. They are:

- Study of a new architecture for chopper stabilized op-amp. The study has allowed to understand the possibility to change the classic solution with square wave signal to a random signal for obtaining the whitening of the noise.
- Time interleaved SAR converter has the purpose to increase the performance in frequency input of the main project.
- Incremental ΣΔ A/D converter allowed the studied of some technique for reducing the effects of the errors introduced by multibit DAC.

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